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A high gain Z-source boost DC–DC converter with common ground for solar PV applications

Meghraj Morey [a,*], Manikanta Golla [b], Man Mohan Garg [a], Nitin Gupta [a], Ajay Kumar [c]

[a] Department of Electrical Engineering, Malaviya National Institute of Technology, Jaipur, Rajasthan, 302017, India
[b] Department of Electrical Engineering, Indian Institute of Science, Bangalore, India
[c] Department of Electrical Engineering, Punjab Engineering College, Chandigarh, 160012, India

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ABSTRACT

This paper proposes a high-gain dc–dc converter with common ground utilizing a Z-source network for low voltage solar photovoltaic (PV) applications. This converter features a common ground and a high output–input voltage conversion factor at a low duty cycle. These converters find their most common application in grid-tied or stand-alone solar photovoltaic systems, particularly those with low output voltages that must be increased to the required level. The presented converter operating duty ratio is within 0–0.5 and maintains similar voltage stress on Z-network components since it employs the conventional Z-source configuration. The presented converter provides a common ground between source and load, unlike conventional Z-network converter. A type-2 closed-loop voltage controller and state–space average model evaluate the converter's dynamic behavior for reliable and steady performance. A laboratory hardware prototype of 250 Watts is built and low gate signals are generated by using a ARM cortex M4 Microcontroller (STM32F407VGT6). The experimental results confirm that the proposed converter, with a gain of 10.46 and a power of 250 Watts, has a maximum efficiency of around 93%. The experimental results validates the effectiveness of the proposed converter under both constant and shifts in amounts of solar irradiation.

1. Introduction

The power generation from renewable energy sources (RESs) like wind power, fuel cells, and solar photovoltaic (PV) is becoming more popular due to rising energy demand and environmental concerns associated with fossil fuel-generated electricity [1,2]. In 2021, solar photovoltaic (PV) generation reached to an all-time high of 179 TWh (up by 21.75%) to surpass 1000 TWh. In terms of absolute increase, solar PV output in 2021 was second only to wind among various renewable energy sources. Solar PV has emerged as the most cost-effective alternative for new electricity generation in almost every part of the world. However, in order to achieve the Net Zero Emissions scenario by 2050, annual solar generation must increase by an average of 25% between the years 2023 and 2030. Solar PV generation are rapidly emerging as the most economically viable option for new forms of worldwide electricity production.

High voltage conversion ratio is frequently required for a variety of applications, involving solar PV systems, uninterruptible power systems, electric vehicles, and many others [3]. Solar PV panels due to low voltage at their output terminal, are linked to the interfaced inverter's dc rail through a high gain boost dc–dc converter [4,5]. In order to interface low voltage solar PV panels to the electrical grid, supplying dc loads or charging energy storing units, high-voltage gain dc–dc converters are needed.

These high gain converters are useful in microgrids (both alternating current and direct current) as well as in standalone systems [6]. The general architecture of a high gain dc–dc converter that bridges a low voltage solar PV system with a 3/1-phase grid and standalone system is presented in Fig. 1. Stepping up low dc voltages from 12 to 125 V to 350–400 V is required to get voltages equal to 230 V in 1-Phase and to 690–710 V to obtain voltages of 415 V in case of 3-Phase supplied voltage source inverters (VSI) [7].

In the literature, many different topologies for dc–dc converters have been presented, categorized as galvanically isolated (transformer based) and non-isolated (coupled inductor) converters that can boost voltage significantly [8]. High gain voltage is attained by regulating transformer/coupled inductor turns ratio [8] which suffers from the demerit of large volume, and reduction in the efficiency due to the

* Corresponding author.
E-mail addresses: 2021ree9065@mnit.ac.in (M. Morey), manikanta.golla18@gmail.com (M. Golla), mmgarg.ee@mnit.ac.in (M.M. Garg), nitingupta.ee@mnit.ac.in (N. Gupta), ajaykumar@pec.edu.in (A. Kumar).

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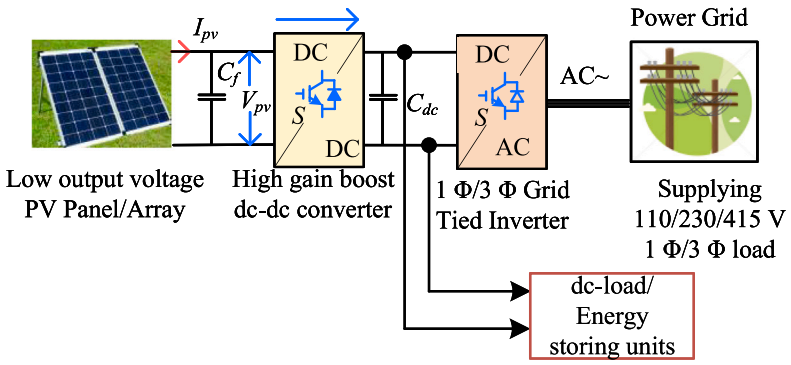


Fig. 1. Two-stage solar PV system with a high gain boost dc–dc converter.

presence of leakage inductance. Additionally, isolated dc–dc converters based on coupling inductors have considerable voltage stress across the switches, demands the high voltage switches (*i.e.* large on-state resistance), increases on-state switches losses. Due to lower cost, smaller size, and enhanced conversion efficiency, a nonisolated boost dc–dc converter has become more prevalent. These high gain dc–dc converters are made to interface energy storage (batteries) or PV panels with low dc voltage output into the distributed generation system's common dc link, which has a significantly higher operational voltage. The most commonly used non-isolated converter uses one switch yields a high gain near-unity duty cycle. High voltage gain with converters have been achieved by voltage multiplier technique in [9], coupled inductors [10, 11], switched capacitors [10], and switched inductors [12], combined switched inductor–capacitors [13], and voltage lift techniques [14]. However, these techniques suffers from the hardware complexity and low efficiency. A new soft switching multiphase interleaved boost converter for high voltage batteries in EV applications and low voltage sources as PV and fuel cell systems requiring high-voltage conversion capability presented in [15]. [16] introduces an interleaved buck–boost converter with reduced power electronics devices count in comparison with the conventional topology. Combining several methods of increasing voltage has led to the development of high step-up converters in recent years, such as Z-source (ZS) and quasi-Z-source (qZS) configurations. ZS and qZS topologies were developed to solve shoot-through problem in conventional inverters and to produce a buck–boost mode [17–19]. Here, an X-shaped Z-source network is formed by connecting two inductors and two capacitors. The Z-configuration is applied to conventional boost converter in [19]. In this boost converter, high gain is obtained at a low duty ratio ($D < 0.5$); however, the input power source and load side do not have a common ground. The author in [20] has modified the Z-source dc–dc converter by replacing the inductor with a diode; however, the voltage gain achieved with this is smaller than that in [21], also does not have the common ground. In [22] a commonly grounded high gain Z-source based converter is presented. In [23], a hybrid switched capacitors–inductor method has low efficiency and lacks in common ground.

A bidirectional dc–dc converter in [24] for use in microgrid, nanogrid, and PV applications is proposed. The author in [25] presented a high gain Z-network converter where only the mathematical modeling of the converter is presented. A new architecture with a high step-up ratio and continuous source current is provided to meet the demand for renewable energy sources is presented in [26]. The converter presented in [27] employed a cascaded boost converters utilizes four semiconductor power switches along with their diodes further increases the hardware complexity. To attain the high voltage, the converter in [28] uses a coupled inductor with equal turns that operates at a high duty cycle. Therefore, this paper presents a Z-source dc–dc converter that uses one power switch and an inductor integrated with conventional Z-network converter for low voltage solar PV applications.

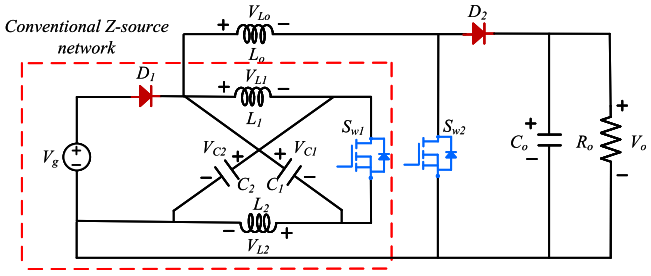


Fig. 2. Proposed high gain Z-source dc–dc converter schematic.

The significant features of the proposed high gain Z-source dc–dc converter for solar PV applications are listed below:

1. The presented converter provides the high gain factor ($G \geq 5$) over wide duty cycle region ($0 < D < 0.5$) as compared to other state-of-the art dc–dc converters.
2. It provides the high dc gain even at low duty ratio ($0.05 < D < 0.1$) and facilitates the commonly grounded source and load, which is crucial from the view of safe maintenance, especially in solar PV-fed systems.
3. The high voltage gain capability is accomplished without exposing the Z-network components to more severe voltage-current stresses supported by the experimental results.
4. An effective converter for increasing the solar PV panel's low voltage has been presented and validated by developing a laboratory prototype.

For the closed loop functioning of the system, the mathematical modeling of the presented converter is provided. The closed loop voltage controller is designed with the type-2 controller to obtain the predetermined output voltage. The small signal modeling is used to analyze the dynamic performance of the converter. The following sections will discuss the presented converter's dynamic and steady state functioning.

2. Working operation of the proposed converter

This part presents a brief description of the stated model's working principle and dynamical equations. The converter schematic shown in Fig. 2, is a 6^{th} order, involving inductors and capacitors energy storage elements. The following assumptions are made while analyzing the working principle of the presented high gain converter:

1. All the constituent elements of the proposed dc–dc converter being examined possess ideal characteristics.
2. Inductor currents and capacitor voltages varies linearly.

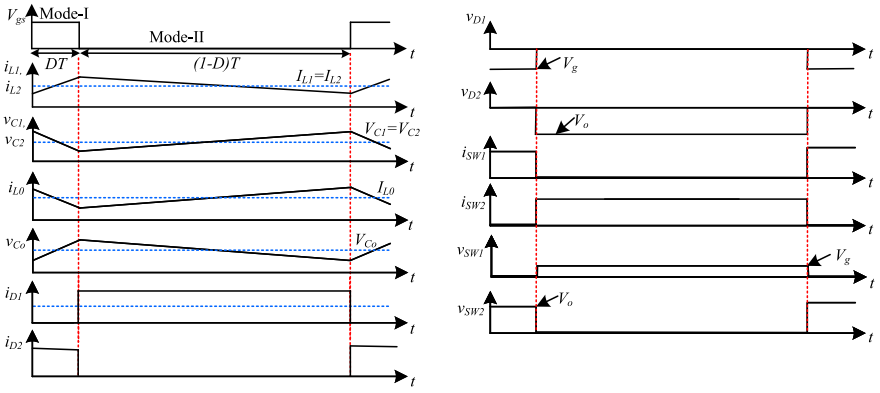
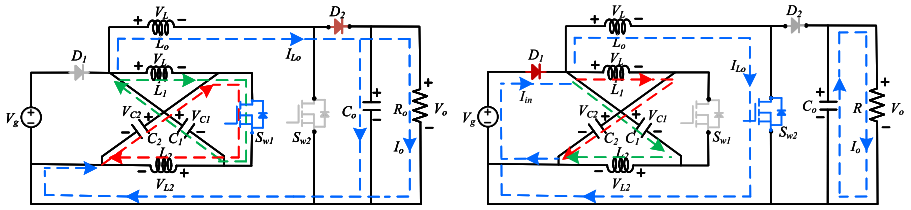


Fig. 3. Fundamental waveforms of the converter over a switching period.



(a) (b)

Fig. 4. Operating switching states of the converter (a) Mode-I, and (b) Mode-II.

Table 1
Switching modes of the converter.

Semiconductor components	S_{W1}	D_1	S_{W2}	D_2
Mode-I 0 ≤ t ≤ DT	1	0	0	1
Mode-II DT ≤ t ≤ T	0	1	1	0

3. The converter's Z-network has identically sized inductors and capacitors.
4. The inductor parasitic resistance and capacitor ESR are omitted.

For designed inductor values L_1 and L_2, presented converter functions in continuous conduction mode (CCM) are selected larger than their critical values. The switching state of the proposed converter, Mode-I and Mode-II are listed in Table 1. The variable D is the duty cycle of the semiconductor switches S_{W1} and S_{W2}, lies within a 0%–*50%* range and T is total switching period represents the interval when the switch remains ON and OFF.

The operating steady-state waveform of the presented high gain dc–dc converter over period of a switching cycle, in Mode-I and Mode-II, as presented in Fig. 3.

2.1. Operating Mode-I (0≤T≤DT)

The waveform and equivalent circuit of the presented converter during the Mode-I, over a switching cycle as depicted in Fig. 3 and Fig. 4(a), respectively. In this, Mode-I of operation, switch S_{W_1}, diode D_2 are ON and switch S_{W2}, diode D_1 are OFF. The voltage of the inductors L_1 and L_2 are same *i.e.* $V_{L1} = V_{L2}$ and voltage across the Z-source network capacitor C_1 and C_2 are equal *i.e.* $V_{C1} = V_{C2}$. In this converter, the output inductor (L_o) charges the capacitor(C_o), providing power to 'R' load as well. The energy is being discharged from the capacitor '*C*' into the inductor'*L*'. Let *DT* is the interval of operating Mode-I in a switching cycle of T, where D> 0 is the duty cycle of semiconductor switch S_{W_1}. During this mode of switching operation there are two loops: (1) The first loop consists of L_1, C_1, L_2, C_2), and S_{W_1}. The Z-network capacitors C_1 release energy to L_1 and C_2 to L_2; (2) Second loop made up of $S_{W1}, C_1, C_2, D_2, C_o$, and R_o. C_1 and C_2 release the energy to inductor L_o and R_o. The dynamical equations are obtained from the circuit depicted in Fig. 4(a),

$$L_1 \frac{di_{L1}}{dt} = V_{L1} = V_{C1}, \qquad L_2 \frac{di_{L2}}{dt} = V_{L2} = V_{C2} \tag{1}$$

and output capacitor voltage and inductor voltages are,

$$V_{Co} = V_o, \text{and} \qquad L_1 \frac{di_{L1}}{dt} = 2V_C - V_{Co} \tag{2}$$

Now, applying Kirchhoff's current law capacitor currents are expressed as,

$$C_o \frac{dV_{Co}}{dt} = I_{Co} = I_{Lo} - Io, \qquad C_1 \frac{dV_{C1}}{dt} = I_{C1} = -I_{L1} - I_{Lo} \tag{3}$$

$$C_2 \frac{dV_{C2}}{dt} = I_{C2} = -I_{L2} - I_{Lo} \tag{4}$$

2.2. Operating Mode-II (DT≤t≤T)

As illustrated in the equivalent circuit Fig. 4(b), switch S_{W2} and diode D_1 are active here, whereas switches S_{W1} and D_2 are off. During this switching mode, S_{W2} remains ON for the $(1 - D)T$ interval of the switching cycle T. In this mode, (1) One loop is formed by L_1, C_2, D_1 and V_g. (2) Another loop formed by L_2, C_1, D_1 and V_g. (3) In third loop, output inductor L_o receives its energy from the input source V_g and completes the path through S_{W2}. The input source V_g and the inductor L_1 discharge its energy to C_2 and L_2 to C_1. The load 'R' receives power from the capacitors at the output. Here, the energy is supplied by the inductors L_1 and L_2 and stored by the capacitors C_1 and C_2, the output inductor L_o charging. The equations during switching Mode-II can be obtained from Fig. 4(b), and are extracted by applying fundamental law to the circuit as below,

$$L_1 \frac{di_{L1}}{dt} = V_{L1} = V_g - V_{C2}, \qquad L_2 \frac{di_{L2}}{dt} = V_{L2} = V_g - V_{C1} \tag{5}$$

$$L_o \frac{di_{Lo}}{dt} = V_{Lo} = V_g, \qquad V_{Co} = V_o \tag{6}$$

$$C_1 \frac{dV_{C1}}{dt} = I_{C1} = I_{L2}, \qquad C_2 \frac{dV_{C2}}{dt} = I_{C2} = I_{L1} \tag{7}$$

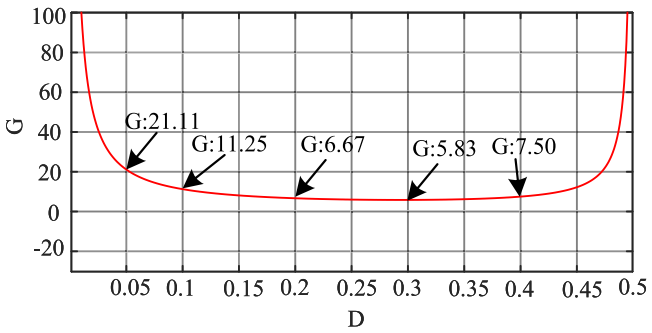


Fig. 5. Voltage gain against duty ratio curve of the proposed converter.

$$C_o \frac{dV_{Co}}{dt} = I_{Co} = -I_{Lo} \tag{8}$$

$$I_{in} = I_{Lo} + I_{L1} + I_{L2} \tag{9}$$

The performance behavior of the stated system is analyzed using the dynamical Eqs. (1) to (4) and (5) to (9), to develop state–space model, and to design the elements. Now, in CCM, using the volt-second balancing equation, with assumption $V_{C1} = V_{C2} = V_C$,

$$V_{C1} = V_{C2} = V_C = \frac{V_g(1-D)}{(1-2D)} \tag{10}$$

Again, by applying voltage-second principle for the inductor L_o,

$$DV_{Co} = V_g(1-D) + 2V_C D \tag{11}$$

By using above expressions, the voltage at the output capacitor C_o may be expressed as,

$$V_{Co} = \frac{V_g(1-D)}{D(1-2D)} \tag{12}$$

Therefore, the proposed dc–dc converter's voltage dc gain can be calculated as,

$$G = \frac{(1-D)}{D(1-2D)} \tag{13}$$

where, 0≤D≤0.5. Similarly, by applying ampere-second balance theory to the capacitors C_1 and C_2, and assuming, $I_{L1} = I_{L_2} = I_L$, we can write,

$$I_L = \frac{DI_{Lo}}{(1-2D)} \tag{14}$$

Similarly, for capacitor C_o, by ampere-second balance principle,

$$I_o = DI_{Lo}, \qquad I_{L1} = I_{L2} = \frac{I_o}{(1-2D)} \tag{15}$$

Also, the average input current is computed as,

$$I_{in}D + I_{in}(1-D) = (I_{Lo} + I_{L1} + I_{L2})(1-D) \tag{16}$$

Using above obtained equations, we can have,

$$I_{in} = I_o \frac{(1-D)}{D(1-2D)} \tag{17}$$

Fig. 5, displays the relationship between the duty ratio and the dc gain of the converter proposed. Figure clearly demonstrates that high gain values at low duty cycles are possible with the presented Z-source converter. As the figure illustrates, for $D = 0.05$, gain of $G = 21.11$ is achieved. Also, converter accomplishes a significant dc voltage gain of G≥5 across the wide duty range of 0≤ D≤0.5.

3. Dynamic modeling and control design

The steady state analysis of the converter is developed in the previous section. To analyze the behavior of the proposed high gain Z-network under dynamic scenario, the equivalent circuit is transformed into a mathematical model. The state space representation of the proposed converter is an effective method for analysis of the converter over a switching cycle. The inductor currents (I_{L1}, I_{L2}, I_{Lo}), capacitor voltages (V_{C1}, V_{C2}, V_{Co}) chosen as state variables for the formation of state–space modeling. State vectors are stated in (18) as,

$$x(t) = \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & i_{Lo}(t) & v_{C1}(t) & v_{C2}(t) & v_{Co}(t) \end{bmatrix}^{\mathrm{T}} \tag{18}$$

The output vector is described as,

$$y(t) = \begin{bmatrix} v_o(t) \end{bmatrix}. \tag{19}$$

In this case, the converter is fed by a single dc voltage source, and the input vector expressed as:

$$y(t) = \begin{bmatrix} v_g(t) & i_g(t) \end{bmatrix}. \tag{20}$$

3.1. State–space model of the proposed converter

The presented converter state–space model is developed and presented as,

$$\frac{dx(t)}{dt} = Ax(t) + Bu(t), \qquad y(t) = Cx(t) \tag{21}$$

where,

$$\begin{cases} A = & A_1 D + A_2(1-D), \\ B = & B_1 D + B_2(1-D), \\ C = & C_1 D + C_2(1-D) \end{cases} \tag{22}$$

$$A = \begin{bmatrix} 0 & 0 & 0 & & \frac{(1-D)}{L_1} & 0 \\ 0 & 0 & 0 & \frac{(1-D)}{L_2} & \frac{D}{L_2} & 0 \\ 0 & 0 & 0 & \frac{D}{L_O} & \frac{D}{L_O} & \frac{D}{L_O} \\ \frac{D}{C_1} & \frac{(1-D)}{C_1} & \frac{D}{C_1} & 0 & 0 & 0 \\ \frac{(1-D)}{C_2} & \frac{D}{C_2} & \frac{D}{C_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{D}{C_O} & 0 & 0 & \frac{1}{RC_O} \end{bmatrix}; \quad B = \begin{bmatrix} \frac{(1-D)}{L_1} & 0 \\ \frac{(1-D)}{L_2} & 0 \\ \frac{(1-D)}{L_o} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{23}$$

The state–space averaged matrices (A and B) of the converter can be estimated, by utilizing the state–space matrices A_1, B_1, and A_2, B_2, derived from the Mode-I and Mode-II operating conditions, respectively. In order to approximate the non-linear converter as a continuous linear system, the state–space averaging method is used. This technique establishes a link between the mathematical models that characterize the converter at each conduction mode, whether linear or time-invariant. The average model is expressed as (21) by using the averaging method for a single switching cycle. One switching cycle is the total of the on and off times for a given switch, denoted by (DT) and $[(1-D)T]$, respectively, where T is the duration of a single switching cycle and $\frac{1}{T} = f_{sw}$ is the switching frequency of the semiconductor switch.

3.2. Model linearization

The state–space averaging method yields a non-linear and time varying mathematical model of the proposed converter. By linearizing the developed model around a dc or steady-state equilibrium point, the non-linear equation (22) can be made linear by applying a small-signal perturbation at the operating point. State variable, output voltage, duty cycle, and input voltage small-signal perturbation are $\hat{x}(t)$, $\hat{y}(t)$, $\hat{u}(t)$, and $\hat{d}(t)$, whereas X, Y, U, and D presents the steady-state parameters.

$$\begin{cases} x(t) & = X + \hat{x}(t), \qquad y(t) = Y + \hat{y}(t), \\ d(t) & = D + \hat{d}(t), \qquad u(t) = U + \hat{u}(t). \end{cases} \tag{24}$$

Table 2
Specifications of the converter used in MATLAB SIMULINK®.

Components	Parameters and values
Input source	10–15 V
Z-Source inductors	$L_1 = L_2 = 911.25$ μH
Z-Source capacitors	$C_1 = C_2 = 50$ μF
Output capacitor	$C_o = 50$ μF
Output inductor	$L_o = 607$ μH
Switching frequency	$f_s = 25$ kHz

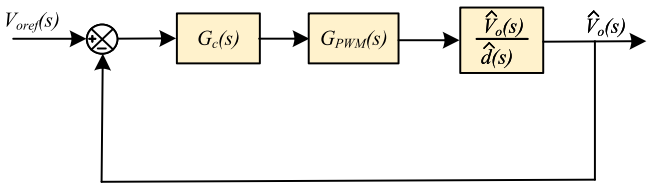


Fig. 6. The proposed converter closed-loop voltage controller.

The small-signal state–space model of the converter can be represented by (25) as,

$$\begin{aligned}\hat{X} + \dot{\hat{x}}(t) =& (A_1(D + \hat{d}(t)) + A_2(1 - D - \hat{d}(t)))(X + \dot{\hat{x}}(t)) \\ &+ (B_1(D + \hat{d}(t)) + B_2(1 - D - \hat{d}(t)))(U + \dot{\hat{u}}(t)) \\ Y + \hat{y}(t) =& C_1(D + \hat{d}(t)) + C_2(1 - D - \hat{d}(t))(X + \hat{x}(t))\end{aligned} \tag{25}$$

Above equation can be rearranged in matrix form (26) as,

$$\begin{cases} \hat{X} + \dot{\hat{x}}(t) = \begin{bmatrix} A & B \end{bmatrix} \begin{bmatrix} X + \hat{x}(t) \\ U + \hat{u}(t) \end{bmatrix} + (A_{net}X + B_{net})U\hat{d}(t) \\ Y + \hat{y}(t) = \left(CX + C\hat{x}(t) + C_{net}X\hat{d}(t) \right) \end{cases} \tag{26}$$

Also, from (26) the steady-state model is expressed as (27), where the dc component is set to zero:

$$\begin{aligned}\dot{\hat{x}}(t) =& A\hat{x}(t) + B\hat{u}(t) + B_{net}\hat{d}(t) \\ \hat{y}(t) =& C\hat{x}(t)\end{aligned} \tag{27}$$

where, the parameter is calculated by,

$$B_{net} = (A_1 - A_2)X + (B_1 - B_2)U \tag{28}$$

Most dc–dc converters are employed for the purpose of keeping the output voltage constant regardless of changes in either the input or the load. The output voltage of a dc–dc converter may be easily controlled by modifying the duty ratio. Control-output voltage transfer function in open loop for the converter can be derived by using the obtained state space matrices,

$$\frac{\hat{v_o}(t)}{\hat{d}(t)} = C[SI - A]^{-1} + B_{net}. \tag{29}$$

where, system matrices are calculated using the parameters shown in Table 2. The small-signal control to output voltage transfer function is expressed by (30). The coefficients of the transfer function are $z_5 = 7.11 \times 10^5$, $z_4 = -3.292 \times 10^8$, $z_3 = 2.548 \times 10^{13}$, $z_2 = -1.171 \times 10^{16}$, $z_1 = 2.167 \times 10^{20}$, $z_0 = -9.832 \times 10^{22}$, $p_6 = 1$, $b_5 = 632.1 \times 10^5$, $p_4 = 3.698 \times 10^7$, $p_3 = 2.317 \times 10^{10}$, $p_2 = 3.34 \times 10^{14}$, $p_1 = 2.04 \times 10^{17}$, $p_0 = 1.015 \times 10^{20}$.

$$\frac{\hat{v_o}(s)}{\hat{d}(s)} = \frac{z_5 s^5 + z_4 s^4 + z_3 s^3 + z_2 s^2 + z_1 s + z_0}{p_6 s^6 + p_5 s^5 + p_4 s^4 + p_3 s^3 + p_2 s^2 + p_1 s + p_0} \tag{30}$$

The proposed converter controller is designed based on output voltage control loop. The control block diagram of the proposed converter to obtain the desired voltage is shown in Fig. 6.

It consist of the voltage controller transfer function, switching pulse width modulator $G_{PWM}(s)$ and the system control to output voltage and feedback transfer function with unity feedback. The derived small signal open loop model of the proposed converter is important for studying the dynamics behavior of the converter. In addition, it can be used to develop a more efficient controller. A small-signal model of the converter is provided by (30), exhibiting that the system is in a non-minimum phase (first undershoot), wherein the right hand plane (RHP) contains four complex zeros and one real zero. The proposed high gain dc–dc converter is of higher order 6, as the derived transfer function has 6 poles. Proportional plus integral controllers with only two parameters, can be simply developed. However, this tuning works best for simple second-order systems. But for high-order converters to achieve the robust and stable performance with the conventional controller is a complex task. The need for closed-loop stability and power regulation at the specified output voltage necessitates the development of an appropriate controller. A type-2 based controller (31) with two poles and two zeros is used, provides a degree of freedom in adjusting the gain near the crossover frequency where the gain is equal to unity. The controller transfer function is expressed as,

$$G_c(s) = \frac{k(s + \alpha_1)(s + \alpha_2)}{s(s + \alpha_3)} \tag{31}$$

Substituting the parameter values,

$$G_c(s) = \frac{0.09105(s + 13300)(s + 4310)}{s(s + 90.59e4)} \tag{32}$$

The bode plot of the proposed converter control to output voltage transfer function with a type-2 controller in feedforward path is shown in Fig. 7. In a type-2 controller based on a two-poles ($s = 0$, α_3), and two-zeros ($s = \alpha_1$, α_2) structure, the stable operation and satisfactory performance of the closed-loop converter depends on the proper selection of the controller's gain, *i.e.* position of the two zeros, and the simple pole. By establishing the position of one pole at the origin, this controller provides a maximum of 90° of phase enhancement with no steady-state inaccuracy. In addition, using a cascaded type-2 controller improves the presented converter's closed-loop performance, despite the fact that it suffers from a non-minimum phase problem. The fast transient response, low overshoot, and zero steady-state error of the closed-loop can be achieved with a well-tuned controller. To ensure sufficient phase margin with increased bandwidth, a controller is developed. The controller for the proposed dc–dc converter is designed to maintain a phase margin between 50° and 70°, and a gain margin of at least 15 dB considered satisfactory. Higher the gain margin, more will be the robustness. This guarantees better closed-loop performance and stability. In point of view of robust performance and stable operation the type-2 controller is indicated in (32) is employed to design the closed-loop control system. Type-2 controller compensation in the feedforward path ensures better-closed loop stability and robust performance. It can be observed from the bode diagram when the proposed converter operated to achieve the desired voltage, the magnitude margin, and the phase margin both are positive. The phase margin of 56° ensures the robust performance of the converter.

4. Design of proposed converter parameters

4.1. Design of inductor

The design of inductors for the proposed converter mainly depends on the switching frequency (f_{sw}) of the semiconductor devices at which it is operating, and the current ripple ΔI_L. The inductances of the converter are designed to limit their current ripple relatively to their average current. From Fig. 4(a), Fig. 4(b), using inductor current (15), and ensuring converter operates in the continuous conduction mode, the value of inductors are calculated. To ensure the converter operates

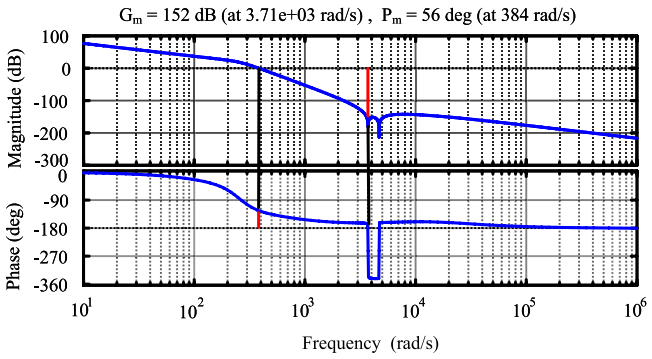


Fig. 7. Frequency response of the control to output transfer function with compensation.

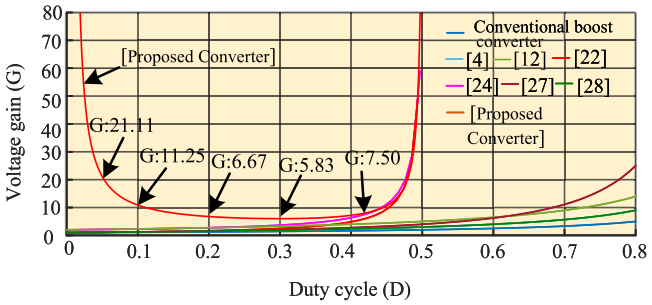


Fig. 8. G Vs D curve: comparison of various dc–dc converters.

in CCM and ripples in the inductor current are limited to 25%. the inductors' value are selected slightly higher than their theoretical value, as expressed by (33),

$$L \geq \frac{DV_C}{\Delta I_L f_{sw}}, \qquad L_o \geq \frac{(2V_C - V_o)D}{\Delta I_{Lo} f_{sw}} \tag{33}$$

4.2. Design of capacitor

The voltage ripple limiting rule was adopted as the basis for designing capacitors. The capacitors of the proposed converter are designed to allow small enough voltage ripples relatively to their average voltages. Ripples in the capacitor voltage are limited to 5%. By using equations from Fig. 1 and using (34), the inequalities in the capacitor's math equations are derived. To reduce the converter's voltage ripples, the capacitor's value should be higher than its actual value.

$$C \geq \frac{I_L(1-D)}{\Delta V_C f_{sw}}, \qquad C_o \geq \frac{I_o(1-D)}{\Delta V_{Co} f_{sw}}. \tag{34}$$

5. Comparative analysis with state-of-the-art converters

Despite Z-network-based topologies and conventional boost topologies can both provide higher boosting, Z-network-based topologies require a lower duty ratio. Due to the fact that conventional boost converter's gain is a function of $[G = 1/(1-D)]$ and needs to be operated at higher duty ratio to achieve high boost voltage output and yield a relatively small voltage gain. Since the gain $[G = 1/(1-2D)]$ of Z-network-based dc–dc converters functional dependence differs from that of conventional boosting gain, converters exhibit high voltage gain.

The high gain Z-source converter under consideration is compared to similar state-of-the-art topologies in order to evaluate its advantages and drawbacks. Fig. 8 depicts the proposed dc–dc converter's dc voltage gain against duty cycle to that of other comparable competitive converters. Compared to conventional dc–dc converters operating at the same duty cycle, the presented Z-source converter exhibits a much higher dc voltage gain, which can be observed from the figure. The converters in [4,12,22,24,27,28] and the proposed converter are compared on the basic of gain-duty ratio curve. The proposed converter yields the high gain over wide duty cycle range *i.e.* $0.05 \leq D \leq 0.47$. Additionally, Fig. 9 provides a quick overview of various state-of-the-art dc–dc converters schematics, duty cycle range, dc gain factor, along with merits and demerits.

This demonstrates that the proposed converter is particularly suitable for the PV panels having unregulated low output dc voltage whether supplying a dc load or interfacing with the grid. Also, high gain at low duty cycle guarantees the low switching conduction losses. Conventional boost converter with the gain of $G = 1/1-D$, theoretically has value of infinity at high duty cycle (near one). Due to practical limitations of the converter, it produces medium dc gain values at duty cycle range of $0.7 \leq D < 1$. This converter suffers from the high conduction losses and low efficiency. The converter in [20] belongs to the conventional Z-source family network with gain of $G = 1/(1-2D)$ and [19] novel dc–dc Z-source converter having gain of $G = (1-D)/(1-2D)$. Both, the converters gives the high gain value for the D in the range of $0 < D < 0.5$. Further, the gain of greater than 5 can be attained for the value of $D > 0.4$. The converter in [4] generates a high gain $G = (1+D)/(1-D)$ across a large duty cycle range *i.e.* $0 < D < 1$ and also, provides the commonly grounded input–output. However, high gain of G>5, can be obtained for the duty cycle $0.6 < D < 1$ only. Additionally, this converter employs three power semiconductor switches and three capacitors. This increases gate driver circuits, controller hardware complexity and cost. The converter presented in [10] uses a coupled inductor to achieve the high dc gain in the range of $0 < D < 1$. Also, converter provides the continuous input current and common ground, makes it suitable for low voltage alternative energy sources applications. The voltage-gain curve is similar and just above that of [4] and [28]. In addition, the high gain is accomplished with the help of two semiconductor power switches, four diodes, and four capacitors in this converter increasing the circuit cost. Also, neither converter provides a common ground between the source input side and the output load side.

The analytical comparison with the competitive converters in terms of number of components used, voltage gain achieved, duty cycle range, voltage stress across the semiconductor devices, cost, and efficiency is presented in Table 3. Higher power components count, reduces the efficiency and increases the circuit cost. Also, large number of capacitors means high energy storage, and thus lowering the power density. The proposed converter, on the contrary together, needs only two power switches making it cheaper circuit. The same number of capacitors count as of conventional Z-source dc–dc converters [19,20] and provides absolute common ground. The converter in [27] with high gain $G = 1/(1-D)^2$ has the voltage gain-duty curve just above that of the conventional boost and Z-network converters presented in [4,28]. However, in order for the converter to attain the high gain, it must operate with a high duty cycle. In addition, this converter employs a total of eight semiconductor power devices (4 switches + 4 diodes) against 2 switches and 2 diodes in the presented converter. In contrast to the conventional Z-source network, the converter proposed in this article has a single power switch and a single inductor, considerably reducing the number of components and achieving high gain compared to the existing high-gain converters described above. Furthermore, input and output share a single ground for added safety during maintenance and diminished EMI interference. Also, the proposed converter dc gain is relatively high compared to other competitive converters over the low range of the duty cycle, $0.05 < D < 0.47$.

Also, the proposed converter's Z-source components and semiconductor devices have moderate voltage stress when the high voltage gain is obtained at a low-duty cycle. As the duty cycle increases, the voltage stress across the proposed converter diodes and switches becomes low, which has been verified experimentally. Also, the number

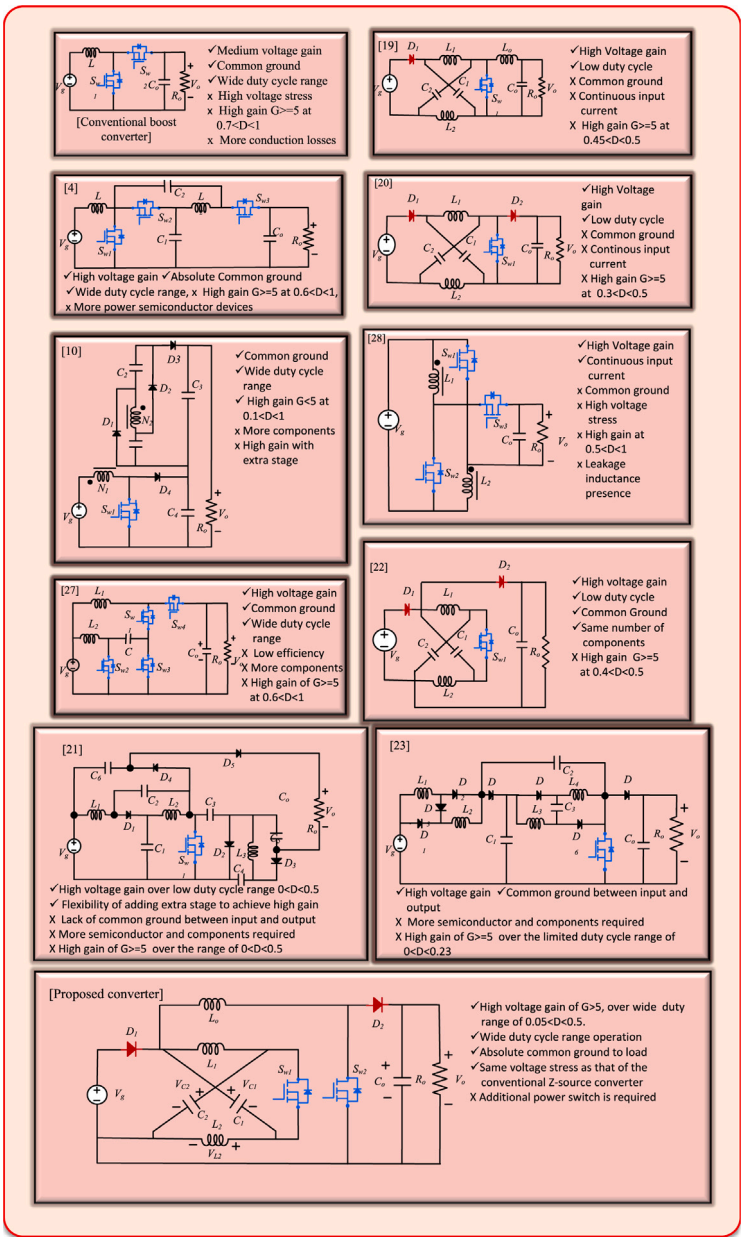


Fig. 9. Comparison of the proposed converter with the state-of-art converters.

of components required for the proposed modified Z-source converter is less and achieves a high voltage gain of more than 10 compared to the available DC–DC converters in the literature. Also, as compared to other converters the proposed converter has good efficiency of 93% with moderate numbers of components. The problem of low output voltage and the adverse effects of atmospheric conditions cause the PV panel's output to be unfit for supplying the load. The presented converter is suitable for low output and non-regulated voltage PV panel applications with slight modification in the primary Z-source network.

The drawback of the proposed converter is high voltage appears across the output capacitor and a switch S_{W2} at high duty cycle, increasing the power loss and affecting the overall efficiency. The low drain–source resistance (R_{ds}) plays a key role in reducing the magnitude of conduction losses to a great extent. Losses from the switches can be minimized to a larger extent by replacing silicon (S_i) based with silicon carbide (S_iC) devices operating at higher frequency.

6. Power loss analysis of the proposed dc–dc converter

The power loss of the proposed high gain common grounded dc–dc converter includes the losses of the power semiconductor switches S_{W1}, S_{W2}, diodes D_1, D_2, Z-network inductors L_1, L_2, output inductor L_o, and capacitors C_1, C_2, C_o. The parasitic elements of the components used for the proposed dc–dc converter, the losses of the components are calculated as:

The power losses due to the switches consist of the conduction loss and switching loss, which is calculated by

$$P_{SW} = P_{SWcond} + P_{SWloss} = I^2_{SW,\mathrm{rms}} R_{\mathrm{DS}} + V^2_{SW} C_{\mathrm{oss}} f_{\mathrm{sw}} \tag{35}$$

The root-mean-square (rms) currents and voltage stress of the switches are as follows:

$$I_{SW1,\mathrm{rms}} = \frac{2I_o\sqrt{D}}{(1-2D)} \tag{36}$$

Table 3
Comparison of proposed dc–dc converter with the state-of-the-art dc–dc converters.

Ref.	N_S	N_D	N_L	N_C	Gain (G)	Duty cycle (D)	Maximum voltage stress across diodes	Maximum voltage stress across switches	Cost	Efficiency (%)
[4]	3	–	2	4	$\frac{1+D}{1-D}$	0< D <1	–	$\frac{1}{2+D}V_o$	L	96.9%
[10]	1	4	1	4	$\frac{1+(1+D)N}{1-D}$	0< D <1	$\frac{1}{2+D}V_o$	$\frac{2-D}{3}V_o$	L	95%
[13]	1	3	4	4	$\frac{2-D}{1-3D}$	0< D <0.33	$\frac{1}{1-D}V_o$	V_o	M	93%
[19]	1	1	3	3	$\frac{(1-D)}{(1-2D)}$	0< D <0.5	$(1-D)V_o$	$(1+D)V_o$	L	94%
[20]	1	2	2	3	$\frac{1}{1-2D}$	0< D <0.5	V_o	V_o	L	93%
[21]	1	5	3	7	$\frac{2+D}{1-2D}$	0< D <0.5	$\frac{1}{2+D}V_o$	$\frac{1}{2+D}V_o$	H	90.1%
[22]	1	2	2	3	$\frac{2(1-D)}{1-2D}$	0< D <0.5	V_o	V_o	L	85%
[23]	1	7	4	4	$\frac{2(1+D)}{1-4D+D^2}$	0< D <0.23	V_o	V_o	H	91%
[26]	1	1	3	3	$\frac{(1+D)N}{1-2D}$	0< D <0.5	$\frac{1}{1-2D}V_g$	$\frac{1}{1-2D}V_g$	L	91.6%
[27]	4	4	2	2	$\frac{1}{(1-D)^2}$	0< D <1	V_o	V_o	M	97%
[28]	3	3	2	1	$\frac{(1+D)}{(1-D)}$	0< D <1	V_o+V_g	V_o	L	93.5%
Proposed converter	2	2	3	2	$\frac{(1-D)}{D(1-2D)}$	0< D <0.5	$\frac{(1-D)}{(1-2D)}V_g$	$\frac{(1-D)}{D(1-2D)}V_g$	L	93%

V_g: Input voltage, V_o: Output voltage, N_S: Number of switches, N_D: Number of diodes, N_L: Number of inductors, N_C: Number of capacitors, L: Low, M: Medium, H: High.

$$I_{SW2,\mathrm{rms}} = \frac{I_o\sqrt{1-D}}{D} \tag{37}$$

$$V_{SW1} = \frac{V_g(1-D)}{(1-2D)} \tag{38}$$

$$V_{SW2} = \frac{V_g(1-D)}{D(1-2D)} \tag{39}$$

Substituting (36)–(39) in (35), the loss occurring in the switches are written as,

$$P_{SW} = \frac{2{I_o}^2}{(1-2D)^2}R_{\mathrm{DS1}} + \frac{{I_o}^2(1-D)}{D^2}R_{\mathrm{DS2}} + \frac{{V_g}^2(1-D)^2}{D(1-2D)^2}C_{\mathrm{oss}}f_{\mathrm{sw}} \tag{40}$$

The power losses in diodes are contributed by diode forward resistance (R_{DF}) and forward voltage drop (V_{DF}). The loss of the diodes is presented as

$$\begin{aligned} P_D &= P_{D_1} + P_{D_2} \\ &= V_{DF}\left(I_{D_1,\mathrm{avg}} + I_{D_2,\mathrm{avg}}\right) + R_{DF}\left(I^2_{D_1,\mathrm{rms}} + I^2_{D_2,\mathrm{rms}}\right) \end{aligned} \tag{41}$$

The rms and average (avg) currents of the diodes are expressed as,

$$I_{D_1,\mathrm{rms}} = \frac{2I_o\sqrt{D}}{(1-2D)} + \frac{I_o\sqrt{1-D}}{D} \tag{42}$$

$$I_{D_1,\mathrm{avg}} = \frac{2I_o(1-D)}{(1-2D)} + \frac{I_o(1-D)}{D} \tag{43}$$

$$I_{D_2,\mathrm{rms}} = \frac{I_o\sqrt{D}}{D} \tag{44}$$

$$I_{D_2,\mathrm{avg}} = I_o \tag{45}$$

The conduction loss of the inductors calculated by considering the dc-resistance of the coil (DCR) used for inductors L_1, L_2, and L_o given by,

$$\begin{aligned} P_L &= P_{L1} + P_{L2} + P_{Lo} \\ &= I_{L1,\mathrm{rms}} \times \mathrm{L_{1DCR}} + I_{L2,\mathrm{rms}} \times \mathrm{L_{2DCR}} + I_{Lo,\mathrm{rms}} \times \mathrm{L_{oDCR}} \end{aligned} \tag{46}$$

The rms currents of the inductor are written as,

$$I_{L_1,\mathrm{rms}} = I_{L_2,\mathrm{rms}} = \frac{I_o}{(1-2D)} \tag{47}$$

$$I_{L_o,\mathrm{rms}} = \frac{I_o}{D} \tag{48}$$

Equivalent series resistance (ESR), internal resistance exists within the capacitor has the most significant impact on converter efficiency and working temperature. Total capacitor losses are calculated accounting the power dissipation in ESR as:

The rms currents of the capacitors are written as:

$$I_{C_1,\mathrm{rms}} = I_{C_2,\mathrm{rms}} = I_o\sqrt{(1-2D)}\left(\frac{\sqrt{(1-2D)D}}{D} + 1\right) \tag{49}$$

$$I_{C_o,\mathrm{rms}} = \left(\frac{\sqrt{(1-D)}}{1-2D}\right)I_o\left(\frac{\sqrt{(1-D)D}}{D} + 1\right) \tag{50}$$

The total loss of the proposed high gain dc–dc converter is given by:

$$P_{Loss} = P_{SW} + P_D + P_L + P_C \tag{51}$$

The efficiency of the proposed converter is calculated analytically by using:

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{Loss}}}. \tag{52}$$

where, P_{out} is load power at the output of converter.

7. Simulation and experimental results

In this section, simulation and experimental results are presented to validate the small-signal modeling and controller design using state–space average technique. The converter operating switching frequency is of 25 kHz. The detailed parameters used in simulink are mentioned in Table 2.

7.1. Simulation results

The proposed dc–dc converter high gain capability has been verified at different duty cycles (a) $D = 0.1$, (b) $D = 0.2$, and (c) $D = 0.3$. Fig. 10 depicts the simulation results based on an open loop configuration. Figure presents the proposed converter key waveforms, from top to bottom gate signal for power switch S_{W1} as G_1, (gate signal for S_{W2} as G_2 which is complement of G_1 not shown here), voltage across diode D_1 and D_2 as V_{D1} and V_{D2}, V_{s1} and V_{s2} presents voltage across power switches S_{W1} and S_{W2}, Z-network inductor currents as $I_{L1} = I_{L2}$,

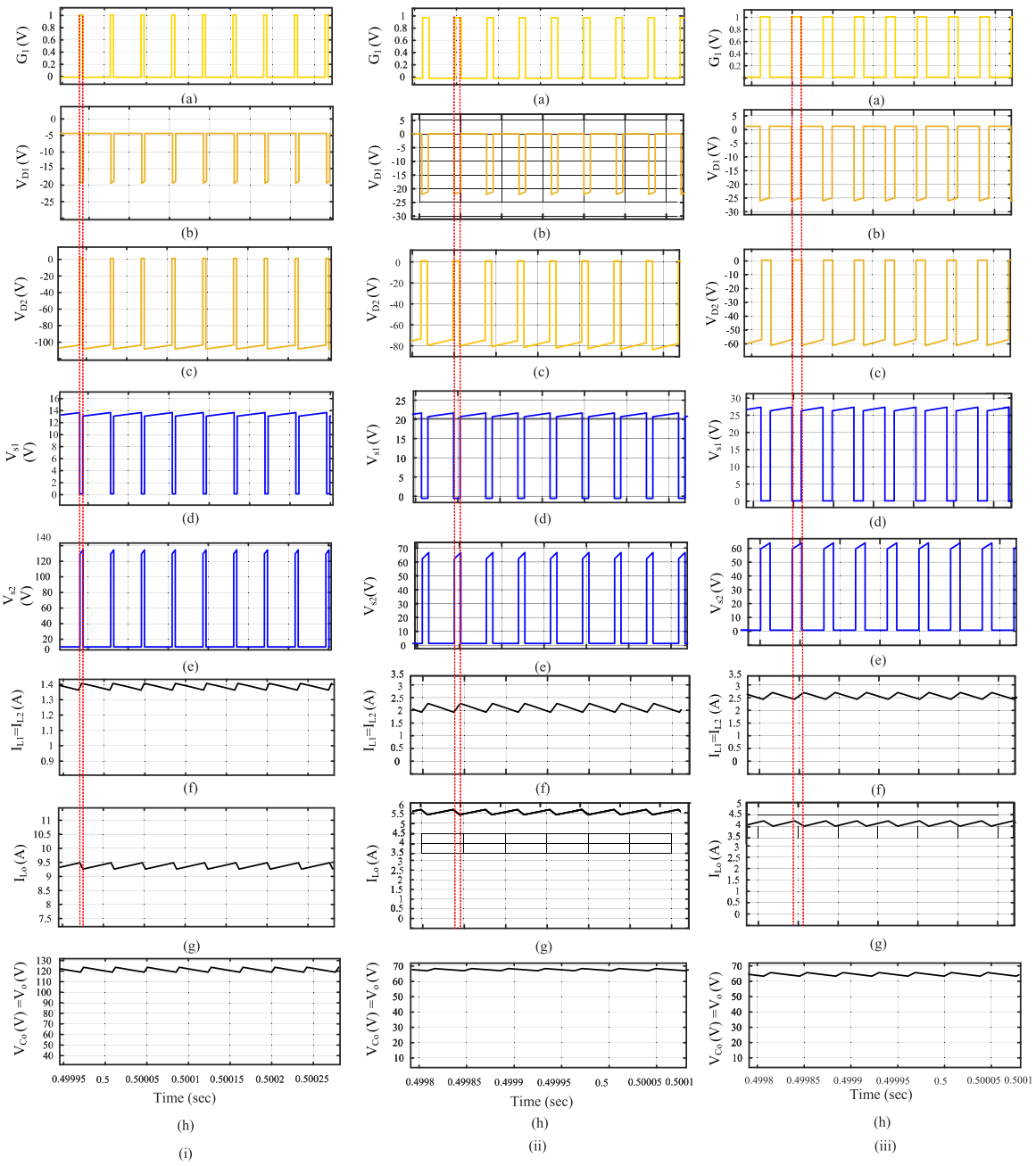


Fig. 10. Simulation results of the proposed converter at (i) D = 0.1 (ii) D = 0.2, and (iii) D = 0.3 where, (a) Gate signal for power switch S_{W1}, (b)–(c) Voltage across diode D_1 and D_2 (V_{D1} and V_{D2}), (d)–(e) Voltage across power switches S_{W1} and S_{W2} (V_{s1} and V_{s2}), (f) Inductor currents ($I_{L1} = I_{L2}$), (g) Output inductor current (I_{Lo}), and (h) Output capacitor and output voltage ($V_{Co} = V_o$).

output inductor current I_{Lo}, and output capacitor is equal to output voltage shown by $V_{Co} = V_o$. The input voltage for all duty cycle operation is fixed at 12 V. Fig. 10(i) represents the results when V_g = 12 V and D = 0.1. The output voltage obtained is V_g = 127 and dc gain value of the proposed converter is G = 10.58 which is lower than the theoretical gain value of 11.25. Fig. 10(ii) represents the results when V_g = 12 V, D = 0.2, and V_g = 67.92. The dc gain value of the proposed converter is G = 5.66. However, input diode voltage V_{D1} has low voltage across it and output diode voltage V_{D2} is equal to the output voltage for short duration can be observed from the waveform. The difference between theoretical and simulation results are mainly due to semiconductor devices (power switches + diodes) voltage drop during the conduction state. However, the boosting factor is quite large as compared to competitive convectional boost and Z-source based converters discussed in Section 5. It can be observed from Fig. 10(iii), when D = 0.3, output voltage boosts to 63 V having dc gain of G = 5.25. The dc gain value decreases with increase in duty cycle.

Also, any further increase in the duty ratio beyond D = 0.4, the proposed dc–dc converter gain starts increasing. Thus, the presented converter dc gain is large for $0 \leq D \leq 0.1$ and $0.4 \leq D \leq 0.5$. However, it is important to note that compared to other high gain converters, efficiency of the presented converter is significantly greater in the range $0.1 \leq D \leq 0.4$. The Z-network inductor and capacitors voltages are similar to that of the conventional Z-source network converter. Here, from the circuit diagram it is clear that the voltage across the output capacitor is identical as that of the output voltage. Therefore, in order to achieve the same voltage gain as conventional converters, the proposed converter has to run at a low value of duty cycle. In addition, high voltage gain

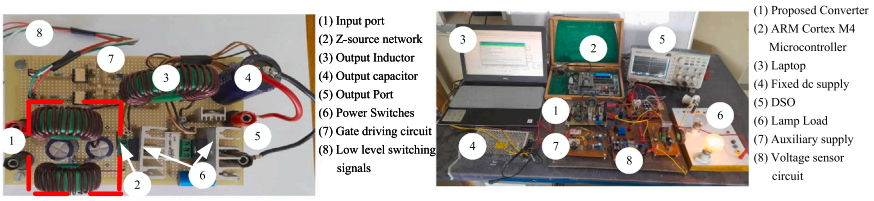


Fig. 11. Experimental prototype (a) Proposed Z-source high gain converter prototype, and (b) Experimental setup.

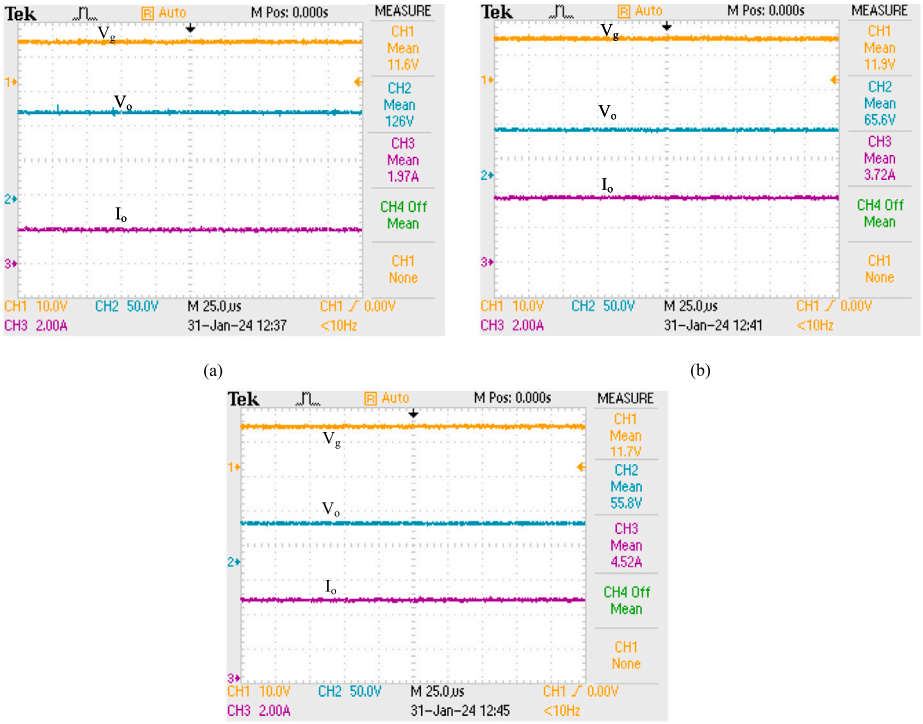


Fig. 12. Experimental results showing converter's input voltage, output voltage and output current at different duty cycle (a) $D = 0.1$, (b) $D = 0.2$, and (c) $D = 0.3$.

Table 4
Experimental specifications of the proposed converter.

Components	Values	Components	Values
Input source	15–21 V	Rated Power	250 W
Z-Source inductors ($L_1 = L_2 = L$)	L = 1.53 mH L_{DCR} = 0.01 Ω	Z-Source capacitors ($C_1 = C_2 = C$)	C = 70 µF, 100 V C_{ESR} = 4 mΩ
Output capacitor	C_o = 50 µF, 250 V C_{oESR} = 3.5 mΩ	Output inductor	L_o = 2.72 mH L_{oDCR} = 0.0285 Ω
Switching frequency	f_{sw} = 25 kHz	MOSFET	IRFP250N R_{DS} = 0.075 Ω
Diodes (D_1, D_1)	HFA25PB60 V_{DF} = 1.7 V, R_D = 0.07 Ω	Controller	ARM Cortex M4 Microcontroller

($G \geq 5$) is possible at a wide range of duty cycles with the proposed converter.

7.2. Experimental results

A 250-W prototype of the proposed high gain dc–dc converter has been developed in the laboratory. Fig. 11 depicts the complete hardware experimental set up to validate the efficacy of the proposed topology. The components and their values used in developed model of the proposed dc–dc converter is shown in Table 4. Signals for the power switches S_{W1} and S_{W2} are generated by the low-cost, fast STM32F407VGT6 Microcontroller, which is member of the Arm Cortex M4 family. The proposed high gain dc–dc converter is employed for boosting the low voltage output of the solar panel given at the input dc-link of the three-phase inverter that interfaces solar PV system with the grid. Specifications of grid-tied solar PV system used for experimentation purpose are: Grid voltage (L-L) = 60 V, Grid Interfacing inductor = 3 mH, IGBT switches FGA25N120ANTD, 3-phase Inverter switching frequency= 5 kHz, LEM-LV25 voltage sensors and LEM-LA-55 current sensors, Solar peak voltage (V_{mp}) = 18.76 V, peak current (I_{mp}) = 13 A, and solar peak power (W_p) = 250 W. All results are recorded by using Tektronix make DSO in the laboratory.

7.2.1. Performance of the converter at different duty ratio

A regulated dc input voltage of 12 V is applied to the proposed converter, and a constant output voltage of 125 V is obtained at D = 0.1 as illustrated in Fig. 12(a). The experimental dc gain value obtained is 10.41 as compared to the theoretical estimated value of 11.25. Similarly, the converter when operated with a duty cycle of D = 0.2 and D = 0.3, the output voltage obtained is 65.6 V and 55.8 V,

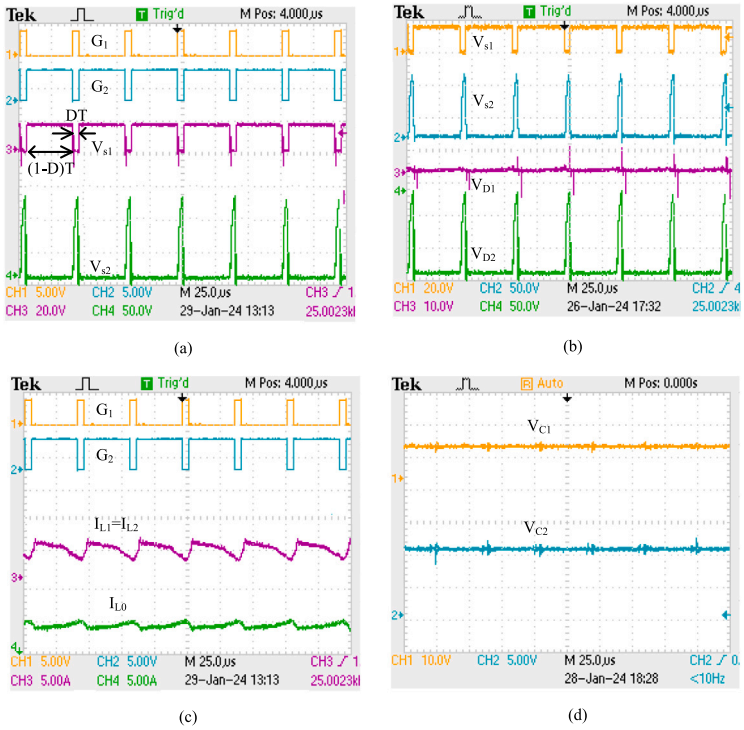


Fig. 13. Experimental waveforms of the converter operated at $D = 0.1$ (a) Gate signals G_1, G_2, voltages V_{s1} and V_{s2}, (b) V_{s1}, V_{s2}, V_{D1} and V_{D2}, (c)–(d) V_{s1} and V_{s2}, $I_{L1} = I_{L2}$ and I_{Lo}, and (d) Z-network capacitor voltages V_{C1} and V_{C2}.

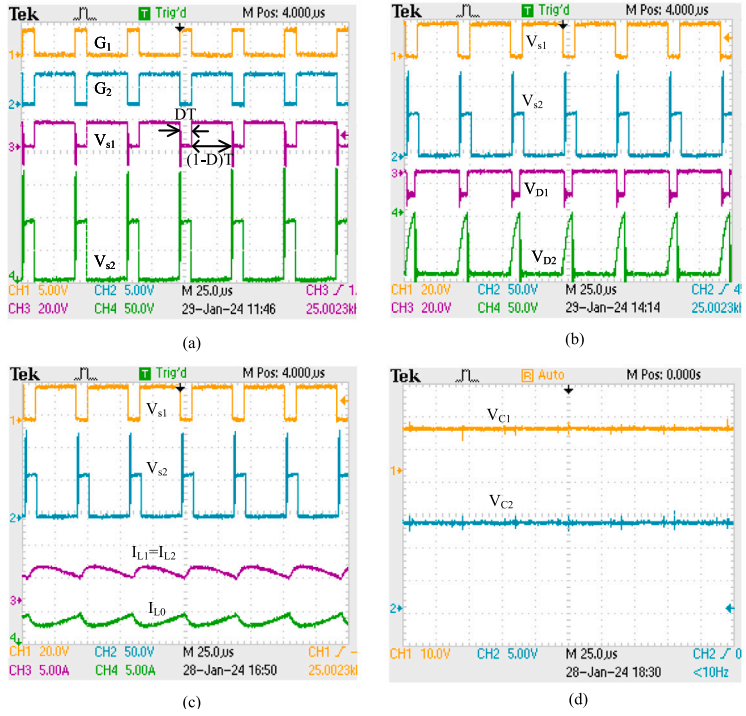


Fig. 14. Experimental waveforms of the converter operated at $D = 0.2$ (a) Gate signals G_1–G_2, V_{s1} and V_{s2}, (b) V_{s1}, V_{s2}, V_{D1} and V_{D2}, (c) V_{s1} and V_{s2}, $I_{L1} = I_{L2}$ and I_{Lo}, and (d) Z-network capacitor voltages V_{C1} and V_{C2}.

depicted in Fig. 12(b) and (c), respectively. Also, the output current has low ripples (<20%) which is required for the dc output current. As the value of D increases, the gain achieved decreases due to increase in conduction losses of the converter. Experimental and theoretical results differ primarily due to the voltage drop of semiconductor devices and the ESR of each element of the converter.

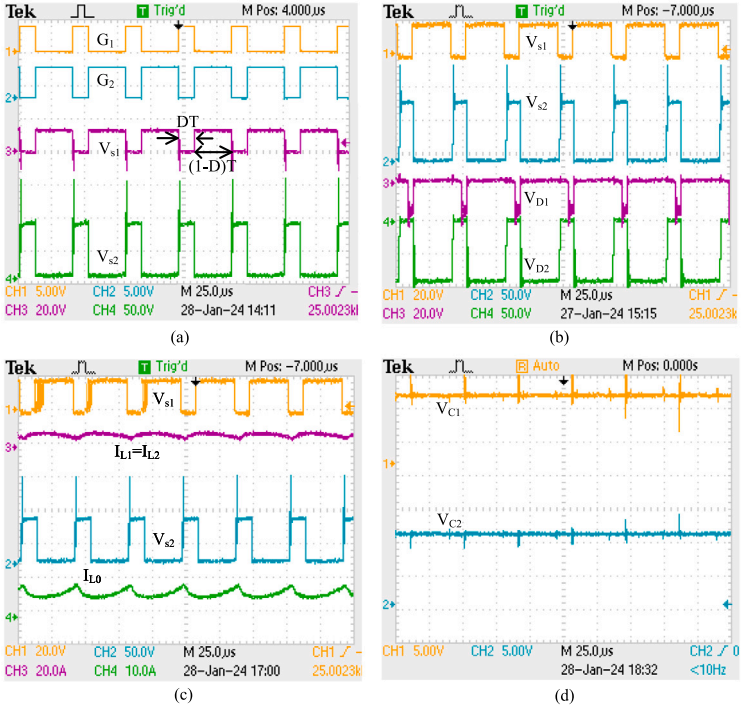


Fig. 15. Experimental waveforms of the converter operated at $D = 0.3$ (a) Gate signals G_1–G_2, V_{s1} and V_{s2}, (b) V_{s1}, V_{s2}, V_{D1} and V_{D2}, (c) V_{s1} and V_{s2}, $I_{L1} = I_{L2}$ and I_{Lo}, and (d) Z-network capacitor voltages V_{C1} and V_{C2}.

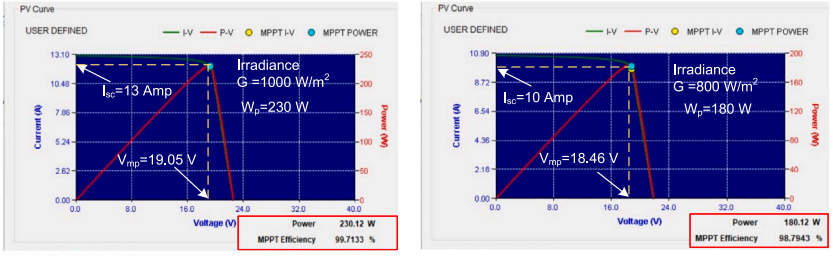


Fig. 16. $I - V$ and $P - V$ characteristics of solar PV panel with MPPT controller operating at constant irradiance of (a) 1000 W/m^2, and (b) 800 W/m^2.

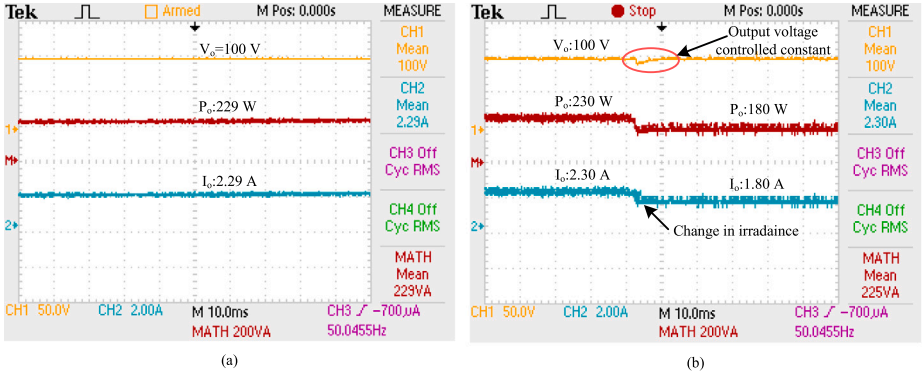


Fig. 17. Proposed converter experimental results when supplied from solar PV panel (a) at constant irradiance of 1000 W/m^2, and (b) change in irradiance from 1000 to 800 W/m^2.

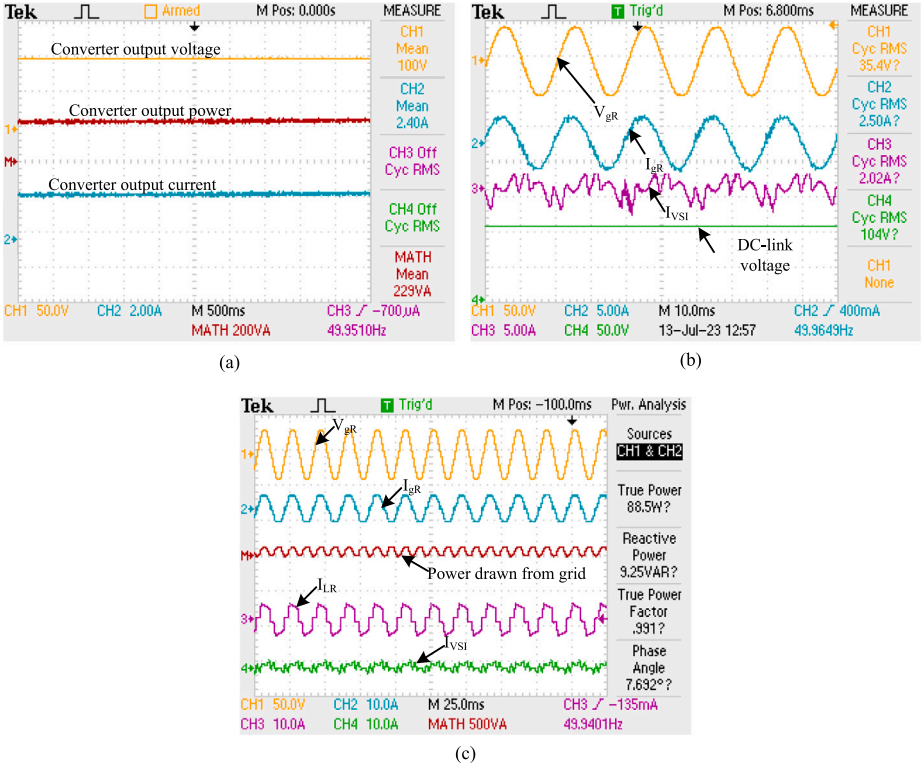


Fig. 18. Solar PV integrated with grid through proposed dc–dc converter (a) proposed Z-source dc–dc converter output voltage current, and power, (b) R-phase grid voltage (V_{gR}), current (I_{gR}), inverter output current (I_{VSI}), and dc-link voltage (V_{dc}), and (c) Grid power waveform.

7.2.2. The experimental key waveforms

Experimental waveforms of the converter at different duty ratio are obtained at $D = 0.1$, $D = 0.2$, and $D = 0.3$. The results shows gate signals G_1 and G_2 for power switches S_{W1} and S_{W2}, voltage across power semiconductor switches S_{W1} and S_{W2} as V_{s1} and V_{s2}, diode voltages V_{D1} and V_{D2}, Z-network inductor currents $I_{L1} = I_{L2}$ and output inductor current I_{Lo}. The experimental results of the proposed dc–dc converter when input is fixed at $V_g = 12$ V and output voltage obtained as $V_o = 126$ V, $V_o = 65.6$ V and $V_o = 55.8$ V at different duty cycle value are shown in Fig. 12. The experimental key waveforms of the proposed converters are obtained and presented in Figs. 13, 14, and 15 for duty cycles $D = 0.1, D = 0.2$, and $D = 0.3$ respectively. The waveform of the gate signals shows that semiconductor switches are operated complementary, as illustrated in Fig. (a) and (b). The diodes D_1 and D_1 operate in the manner as discussed in the operating principle of the converter, and their voltages are presented in Fig.(b). The charging and discharging of Z-network inductors as per the switching operation can be seen in Fig.(c) and Z-network capacitor voltages in Fig.(d). The waveforms also present the output inductor current (I_{Lo}) behavior following the switching operations presented in the proposed converter's switching Mode I and II operation.

Fig. 13(a) shows the voltage stress across the power switches S_{W1} and S_{W2} are 18 V and 130 V matches with simulation and theoretical values, respectively. Therefore, the proposed converter achieves the high voltage gain with low voltage stress on the power switches. The current in Z-network and output inductor are depicted in Fig. 13(c) and inductor current ripple are well within the specified values. The voltage of the capacitors C_1, and C_2 are shown in Fig. 13(d) as 12 V and 13 V, respectively. Thus, voltage across Z-network capacitors are maintained at low values. The voltage ripples are also small ($\leq 5\%$) and validates correctness of the selected values of the capacitors. In similar way, Figs. 14 and 15 validates the operation of switches, voltage stress across converter components, and inductor current matches with simulation results when operated at duty cycle of $D = 0.2$ and $D = 0.3$.

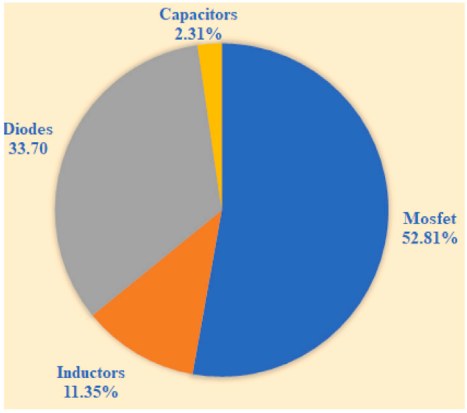


Fig. 19. Power loss distribution of the proposed converter.

All the experimental results are in agreement with the theoretical and simulation results. The features of the proposed dc–dc converters are, hence, verified.

7.2.3. Performance of the converter when fed from low output solar PV under fixed and varying solar irradiance

To extract the maximum power from the solar PV panel maximum power point tracking (MPPT) algorithm is implemented in conjunction with the proposed dc–dc converter. The performance of the suggested converter's MPPT is examined utilizing the conventional perturb and observe (P&O) method. Fig. 16(a) and (b) depicts the $I - V$ curve and $P - V$ curve of the solar panel for varying solar irradiance and MPPT operating point. In Fig. 16(a) at irradiance of 1000 W/m^2 the solar panel delivers the peak power of 230 W with $V_{mp} = 19.05$ V and $I_{mp} = 13$ A. Whereas, at irradiance level of 800 W/m^2, $V_{mp} = 18.46$ V and

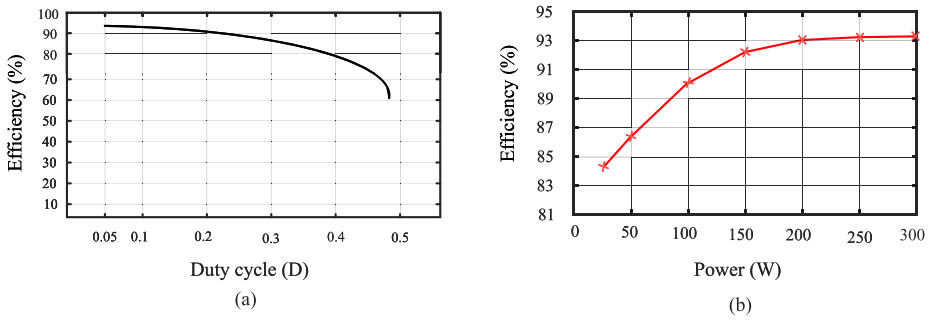


Fig. 20. Proposed converter experimental measured efficiency plots (a) Efficiency-versus-duty cycle, and (b) Efficiency-versus-output power.

I_{mp} = 10 A are obtained, delivering the peak power of 180 W which is presented in Fig. 16(b). Implemented MPPT efficiency is observed to be more than 95% for varying irradiation levels.

To maintain the desirable output voltage at specific value, designed closed loop controller is realized in the laboratory. Here, proposed converter first is fed from low output solar PV panel operating under 1000 W/m^2 irradiance producing the output voltage of 100 V and 229 W of power is presented in Fig. 17(a). Also, the proposed converter operation is verified under sudden change of the solar irradiance from 1000 to 800 W/m^2 as depicted in Fig. 17(b). The output dc current also decreased due to change of irradiance and reaches the steady-state value. The converter output voltage is maintained at 100 V and the converter output power reduces to 180 W as the solar PV power lowers with solar irradiance. Thus, the proposed converter operates effectively in standalone solar PV fed mode under steady state and dynamic condition.

7.2.4. Performance of the converter in grid integrated solar PV fed mode

A grid-connected PV system for supplying the non-linear load is developed in the laboratory and the proposed converter is connected between the solar PV panel and the grid-tied inverter. The solar PV simulator (Itech Make) is used to mimic the PV panel characteristics. A detailed explanation of the setup is not given here. The designed voltage-controlled closed-loop and MPPT algorithm are realized using ARM Cortex Microcontroller. The grid voltage is 60 V (L-L) and dc-link voltage is selected to be at 100 V for satisfactory operation of the inverter. A three phase non controlled diode bridge rectifier is used as non linear load. Fig. 18(a)–(c) depicts the experimental substantiation of the performance of the proposed converter when the load demand is supplied by the grid and solar PV system generated power.

Fig. 18(a) illustrates, the maximum power of 230 W is extracted from the solar PV and the 19 V solar output voltage, is stepped up to 100 V using the proposed high gain converter. Throughout the operation, the solar irradiance was maintained constant at 1000 W/m^2. It can be seen from Fig. 18(b), the output voltage of the converter produced is 100 V and remains constant at 100 V set value, grid voltage, grid current for the phase-R, and inverter output current in grid integrated solar PV mode. From Fig. 18(c) it can be observed that the power of 230 W (76 W/ph) is supplied from the PV and remaining load demand of 88.5 W/ph is fed from the grid. The grid current profile is maintained sinusoidal during the entire operation of the system. This shows that the proposed converter can be utilized effectively for supplying the load in low voltage output solar PV applications when interfaced with the grid.

8. Power loss and efficiency analysis of the proposed converter

The loss distribution profile among semiconductor switches and other components of the proposed converter is given in Fig. 19. Among the total losses, around 52.81% constitute the losses due to MOSFET switches. The diodes are responsible for approximately 33.70% of the total losses due to their uncontrolled conduction. Other losses include gate driver losses, capacitor ESR losses etc. The majority of the losses are caused by MOSFETs, diodes, and inductors. Employing 'S_iC' devices instead of 'S_i' based devices can reduce MOSFET losses substantially.

The efficiency of the presented converter plotted against the duty cycle is shown in Fig. 20(a). The maximum and minimum efficiency of the proposed converter is found to be 93.5% and 63.5%, respectively. The presented converter has a high efficiency of 93.5% when operated at a duty cycle of $D = 0.1$. Due to the low conduction period of the main power switch, voltage and current stress across Z-network components is low. As the duty cycle further increases, the conduction period of the power switch and Z-network components increases, increasing the conduction losses and resulting in reduced efficiency. The proposed converter yields an efficiency of more than 90% and a high gain of $G \geq 10$ for the duty cycle range of $D \leq 0.2$.

The efficiency-versus-output power plot of the developed experimental prototype-250 W is presented in Fig. 20(b). These measurements are recorded, keeping the input voltage constant at 12 V, and load is increased in steps on the converter. The maximum efficiency achieved is 93.34% at 250 W of load, as shown in the figure. The converter was operated at a duty cycle of 0.1 during the experimentation, achieving a gain of 10.41. At low power ratings, losses in the diodes and switches have a substantial effect on efficiency. However, the converter achieves more than 90% efficiency over a wide range of loads. The proposed converter has been developed for use in low-voltage solar PV applications. The converter transfers the power of 200 W with an efficiency more than 90%, which proves its suitable operation for high voltage gain (during the experiment, the voltage gain was 10.41). The dynamic response of the proposed converter under step load variation between light load (25 W) and full load (300 W) is shown in Fig. 20(b) validates the effectiveness of the proposed converter. Owing to the high gain ability of the proposed converter with common ground between input and output side, it is observed that the proposed converter is more suitable for solar PV system interfacing with grid.

9. Conclusion

A novel high-voltage-gain common-grounded Z-source based dc–dc converter is presented for solar PV applications in this paper. Operation principles, detailed analysis, voltage and current waveforms and performance evaluation have been investigated through simulation and experimental results. The salient features of the proposed converter are a simple configuration, low components, smooth output current, low voltage stress on Z-network capacitors, common ground, wider duty ratio range (0≤D≤0.5) with high voltage gain at a low duty cycle. A 250-Watt laboratory setup was implemented to confirm the effectiveness of the proposed converter and controller. The maximum efficiency of around 93% is achieved in the proposed converter (with a gain of 10.46 and power of 250 Watts) verified through experimental results. Thus, proposed topology provides a better combination of high voltage gain and efficiency. Also, the proposed converter performance

is promising when fed by low voltage solar PV panel, even under varying solar irradiance in standalone and grid connected PV mode. As a result, the proposed converter is well suited for grid-connected or stand-alone solar PV power-producing systems, where a high voltage boost is often demanded. Designing a high-gain, high-efficiency dc–dc converter for large power levels is challenging. Additional investigation and experiment in this domain offer the potential for converter designs that are even more efficient and effective in the context of renewable energy applications.

CRediT authorship contribution statement

Meghraj Morey: Writing – original draft, Validation, Software, Conceptualization. **Manikanta Golla:** Software, Investigation. **Man Mohan Garg:** Writing – review & editing, Formal analysis. **Nitin Gupta:** Supervision, Resources, Formal analysis. **Ajay Kumar:** Writing – review & editing, Formal analysis, Data curation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

References

[1] P.K. Pardhi, S.K. Sharma, A. Chandra, Grid-integrated single phase solar PV system employed with single switch high gain boost converter, Electr. Power Syst. Res. 213 (2022) 108231, http://dx.doi.org/10.1016/j.epsr.2022.108231.

[2] L. Senapati, M.M. Garg, A.K. Panda, R.K. Lenka, Topology synthesis and control of integrated three-port converter for renewable energy system, Comp. and Elect. Eng. 101 (2022) 107996, http://dx.doi.org/10.1016/j.compeleceng.2022.107996.

[3] A. Rajabi, F.M. Shahir, R. Sedaghati, New unidirectional step-up DC-DC converter for fuel-cell vehicle: Design and implementation, Electr. Power Syst. Res. 212 (2022) 108653, http://dx.doi.org/10.1016/j.epsr.2022.108653.

[4] Y. Zhang, Q. Liu, J. Li, M. Sumner, A common ground switched-Quasi-Z-Source bidirectional DC–DC converter with wide-voltage-gain range for EVs with hybrid energy sources, IEEE Trans. Ind. Electron. 65 (6) (2018) 5188–5200, http://dx.doi.org/10.1109/TIE.2017.2756603.

[5] S. Danyali, A. Moradkhani, R. Aazami, M.T. Mejbel, New dual-source high-gain ZVS DC-DC converter for integrating renewable power source and battery storage, Electr. Power Syst. Res. 213 (2022) 108740, http://dx.doi.org/10.1016/j.epsr.2022.108740.

[6] V. Gali, P.K. Jamwal, N. Gupta, A. Kumar, An adaptive dynamic power management approach for enhancing operation of microgrid with grid ancillary services, Renew. Ener. 219 (1) (2023) 119413, http://dx.doi.org/10.1016/j.renene.2023.119413.

[7] M. Das, M. Pal, V. Agarwal, Novel high gain, high efficiency DC–DC converter suitable for solar PV module integration with three-phase grid-tied inverters, IEEE J. of Photovolt. 9 (2) (2019) 528–537, http://dx.doi.org/10.1109/JPHOTOV.2018.2877006.

[8] T.J. Liang, J.H. Lee, S.M. Chen, J.F. Chen, L.S. Yang, Novel isolated high-step-up DC–DC converter with voltage lift, IEEE Trans. Ind. Electron. 60 (4) (2013) 1483–1491, http://dx.doi.org/10.1109/TIE.2011.2177789.

[9] J.W. Baek, M.H. Ryoo, T.J. Kim, D.W. Yoo, J.S. Kim, High boost converter using voltage multiplier, in: Proc. 31st Annu. Conf. of IEEE Ind. Electron. Soc., IECON, 2005, pp. 567–572, http://dx.doi.org/10.1109/IECON.2005.1568967.

[10] T.J. Liang, S.M. Chen, L.S. Yang, J.F. Chen, A. Ioinovici, Ultra-large gain step-up switched-capacitor DC-DC converter with coupled inductor for alternative sources of energy, IEEE Trans. Circuits and Syst. I, Reg. Papers 59 (4) (2012) 864–874, http://dx.doi.org/10.1109/TCSI.2011.2169886.

[11] B. Axelrod, Y. Berkovich, A. Ioinovici, Switched coupled-inductor cell for DC-DC converters with very large conversion ratio, in: Proc. 32nd Annu. Conf. on IEEE Ind. Electron., 2006, pp. 2366–2371, http://dx.doi.org/10.1109/IECON.2006.347593.

[12] M.A. Salvador, T.B. Lazzarin, R.F. Coelho, High step-up DC–DC converter with active switched-inductor and passive switched-capacitor networks, IEEE Trans. Ind. Electron. 65 (7) (2018) 5644–5654, http://dx.doi.org/10.1109/TIE.2017.2782239.

[13] T. Takiguchi, H. Koizumi, Quasi-Z-source dc-dc converter with voltage-lift technique, in: Proc. 39th Annu. Conf. of the IEEE Ind. Electron. Soc., 2013, pp. 1191–1196, http://dx.doi.org/10.1109/IECON.2013.6699302.

[14] D. Vinnikov, I. Roasto, Quasi-Z-source-based isolated DC/DC converters for distributed power generation, IEEE Trans. Ind. Electron. 58 (1) (2011) 192–201, http://dx.doi.org/10.1109/TIE.2009.2039460.

[15] N.A. Ahmed, B.N. Alajmi, I. Abdelsalam, M.I. Marei, Soft switching multiphase interleaved boost converter with high voltage gain for EV applications, IEEE 10 (2022) 27698–27716, http://dx.doi.org/10.1109/ACCESS.2022.3157050.

[16] B.N. Alajmi, M.I. Marei, I. Abdelsalam, N.A. Ahmed, Multiphase interleaved converter based on cascaded non-inverting buck-boost converter, IEEE Access 10 (2022) 42497–42506, http://dx.doi.org/10.1109/ACCESS.2022.3168389.

[17] Y.P. Siwakoti, G.E. Town, Performance of distributed DC power system using quasi-Z-source inverter based DC/DC converters, in: Proc. Twenty-Eighth Annu. IEEE Applied Power Electron. Conf. and Expo., APEC, 2013, pp. 1946–1953, http://dx.doi.org/10.1109/APEC.2013.6520561.

[18] D. Vinnikov, I. Roasto, R. Strzelecki, M. Adamowicz, Step-up DC/DC converters with cascaded quasi-z-source network, IEEE Trans. Ind. Electron. 59 (10) (2012) 3727–3736, http://dx.doi.org/10.1109/TIE.2011.2178211.

[19] X. Fang, A novel Z-source dc-dc converter, in: Proc. of IEEE Int. Conf. on Ind. Techn., 2008, pp. 1–4, http://dx.doi.org/10.1109/ICIT.2008.4608314.

[20] J. Zhang, J. Ge, Analysis of Z-source DC-DC converter in discontinuous current mode, in: Proc. Asia-Pacific Power and Energy Eng. Conf., 2010, pp. 1–4, http://dx.doi.org/10.1109/APPEEC.2010.5448927.

[21] M.M. Haji-Esmaeili, E. Babaei, M. Sabahi, High step-up quasi-Z-source DC–DC converter, IEEE Trans. Power Electron. 33 (12) (2018) 10563–10571, http://dx.doi.org/10.1109/TPEL.2018.2810884.

[22] H. Shen, B. Zhang, D. Qiu, L. Zhou, A common grounded Z-source DC–DC converter with high voltage gain, IEEE Trans. Ind. Electron. 63 (5) (2016) 2925–2935, http://dx.doi.org/10.1109/TIE.2016.2516505.

[23] Y. Wang, Q. Bian, X. Hu, Y. Guan, D. Xu, A high-performance impedance-source converter with switched inductor, IEEE Trans. Power Electron. 34 (4) (2019) 3384–3396, http://dx.doi.org/10.1109/TPEL.2018.2853581.

[24] N. Elsayad, H. Moradisizkoohi, O.A. Mohammed, Design and implementation of a new transformerless bidirectional DC–DC converter with wide conversion ratios, IEEE Trans. Ind. Electron. 66 (9) (2019) 7067–7077, http://dx.doi.org/10.1109/TIE.2018.2878126.

[25] M. Morey, M. Golla, N. Gupta, M.M. Garg, M. Kumawat, Mathematical modelling and experimental validation of a 6th order high gain Z-source dc-dc converter using ARM based microcontroller, in: Proc. IEEE 10th Power India Int. Conf., PIICON, Nov. 2022, pp. 1–6, http://dx.doi.org/10.1109/PIICON56320.2022.10045089.

[26] F. Evran, M.T. Aydemir, Z-source-based isolated high step-up converter, IET Power Electron. 6 (1) (2013) 117–124, http://dx.doi.org/10.1049/iet-pel.2012.0289.

[27] H. Ardi, A. Ajami, F. Kardan, S.N. Avilagh, Analysis and implementation of a nonisolated bidirectional DC–DC converter with high voltage gain, IEEE Trans. Ind. Electron. 63 (8) (2016) 4878–4888, http://dx.doi.org/10.1109/TIE.2016.2552139.

[28] L.S. Yang, T.J. Liang, Analysis and implementation of a novel bidirectional DC-DC converter, IEEE Trans. Ind. Electron. 59 (1) (2011) 422–434.