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A Multilevel Switched Capacitor Inverter with Reduced Components and Self-Balance

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Abstract: This paper presents a novel 13-level switched capacitor multilevel inverter, which uses less devices to achieve six-fold voltage gain. The proposed topology structure consists of twelve transistors, two diodes, and three capacitors. It is worth mentioning that characteristics as having five complementary switch pairs and self-balanced electric capacity voltages are conducive to simplifying the control strategy. Moreover, the above components constitute the switched capacitor unit and L-type unit. The inverter can acquire more voltage levels and a higher voltage gain by using multiple L-type units with fewer elements. Furthermore, the cost function is employed to comprehensively appraise the performance of the proposed inverter. The comparison with other existing 13-level inverters shows that the proposed multilevel inverter can effectively decrease the value of the cost function. Finally, the simulation and experimental results are presented to demonstrate the feasibility and effectiveness of the 13-level inverter.

Keywords: multilevel inverter; switched capacitor; boosting; reduced components; extension

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1. Introduction

Multilevel inverters (MLIs) have emerged as an important tool for medium-voltage high-power applications like renewable energy system, electric vehicles (EVs), and flexible AC transmission systems [1–3]. MLIs possess many excellent features in contrast with the two-level inverter, such as a better performance in terms of total harmonic distortion (THD), reduced dv/dt stresses, a lower switching frequency, etc. [4]. Generally, conventional MLIs are divided into neutral-point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters [5]. However, NPC and FC inverters use numerous components with increasing voltage levels, and it is complicated to keep control of the balance of the capacitor voltage [6]. In addition, CHB inverters have drawbacks like a strong demand for isolated DC sources and a lack of boost capacity [7]. It is noteworthy that the MLIs based on the switched capacitor (SC) technique are capable of self-balancing the capacitor voltage as well as raising the input voltage [8,9].

With these unique advantages, switched capacitor multilevel inverters (SCMLIs) have been widely studied and have produced various topologies. For instance, the inverters in [10–14] use several DC sources combined with switched capacitors to produce a multilevel output. The SCMLIs proposed in [10,11] can achieve a double voltage gain with self-charging capacitors. To obtain a greater number of voltage levels, the 17-level switched capacitor inverter in [12] was developed using two SC cells. In [13,14], the inverters achieved a higher boosting factor with a number of SC units. Nevertheless, the above topologies have a common defect, namely that of employing multiple DC sources, which results in the growth of application cost.

In order to solve the aforesaid issue, several single-source SCMLIs were proposed in [15–18]. The inverter in [15] achieved seven-level output with a single source, and more

levels were obtained in [16–18] using extended structures. However, these topologies all use the H-bridge to transform the direction of the output voltage, which can raise the total standing voltage (TSV) of switches. The H-bridge was removed in [19–22] due to the intrinsic inversion ability. The multilevel inverter based on the K-type unit in [19] has a voltage gain of 1.5, while a triple boosting factor was obtained in [20–22]. The three MLIs include a T-type which maintains the capacitor voltage at half of the input voltage to produce more output levels. Nevertheless, the above topologies could be improved if they did not require abundant devices for a higher boosting factor, an issue identical to that found in [23].

The works [24–27] developed 13-level switched capacitor inverters which achieve a voltage gain of six with fewer components. Through the regular charging–discharging of the capacitor, the inverter proposed in [24] can realize the self-balancing of capacitor voltages, but the voltage stress of the switches is high. The stress on the devices of the inverter in [25] decreased, which was restricted to half the maximum output voltage. The multilevel inverter proposed in [26] used fifteen transistors and three capacitors, and the output voltage polarity was changed with two half-bridge modules. Two switched capacitor inverters proposed in [27] only used twelve switches. The topologies contain a triple-mode SC unit and a simplified SC unit. The inverter proposed in [28] also uses a triple-mode SC, but employs four capacitors, which leads to an increase in volume. In addition, the abovementioned structures cannot be expanded and the application scenarios are restricted.

Based on the previous analysis, a new 13-level SCMLI is proposed in this paper, and it has the following excellent features:

(1) The proposed multilevel inverter can acquire six-fold voltage gain with a reduced number of components;
(2) Only twelve transistors are employed and there are five complementary switch pairs, which simplifies the control strategy;
(3) The capacitor voltage is self-balancing without the need for extra loops;
(4) The proposed SCMLI is capable of extending to acquire more voltage levels and a higher boost factor;
(5) A low-value cost function (CF) can be obtained in the topology.

The remaining sections are organized as follows: Section 2 gives the structure of the proposed 13-level switched capacitor boost inverter, and its working states at different levels are also introduced. Section 3 analyzes the power losses and gives the parameter calculation of the multilevel inverter. Section 4 introduces the topology extension and comprehensive results of comparisons with other MLIs. Section 5 presents the simulation and experimental platform to verify the validity of the 13-level inverter. In the end, conclusions are given in Section 6.

2. Design of Proposed SCMLI

2.1. Topology

The proposed 13-level switched capacitor topology is depicted in Figure 1. It is made up of four switches (S_1–S_4), a switched capacitor unit (SCU), a L-type unit (LTU), two diodes, and three capacitors. The SCU contains a single DC source, five switches (S_5–S_9), a diode D_1, as well as capacitors C_1 and C_2. Figure 2 shows the working states of the proposed switched capacitor basic unit. In Figure 2a, the capacitor voltage can be maintained at V_{dc} when it is connected in parallel with the DC source. Figure 2b,c displays the discharge of capacitors connected in parallel/series. The SCU can achieve a triple voltage gain when the two capacitors are connected in parallel with the DC source. LTU includes the capacitor C_3, three switches (S_{10}–S_{12}), and a diode D_2, whilst the capacitor voltage of C_3 can be maintained at 3 V_{dc} through the L-type circuit loop.

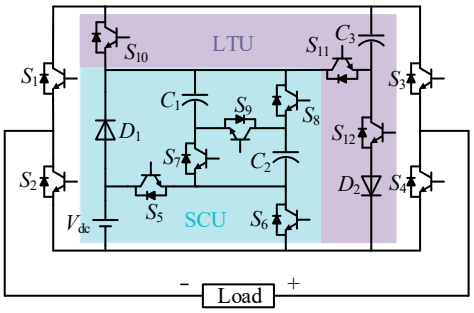

Figure 1. Proposed 13−level SC inverter.

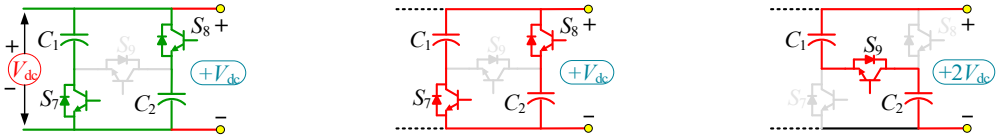

Figure 2. Working states of switched capacitors. (**a**) Charging of C_1 and C_2 in parallel. (**b**,**c**) Discharging of C_1 and C_2 in parallel/series.

2.2. Operating Mode

The proposed topology possesses a 13-level output and fourteen operating modes. The different switching modes and output levels are shown in Table 1, where "0" and "1" indicate the "off" and "on" statuses of the switches, respectively. The working conditions of capacitors are presented by "C", "D", and "–", which denote the charging, discharging, and idle states. A total of five complementary switch pairs are employed to prevent the capacitors from being short-circuited. Moreover, capacitors C_1 and C_2 have the same state and a high charging frequency, which is beneficial to diminish the capacitor voltage ripple and improve the waveform quality of the output voltage.

Table 1. Operating modes of the proposed MLI.

Modes	Output Voltage	Switches						Capacitors		
		$S_{1,2}$	$S_{3,4}$	$S_{5,6}$	$S_{7/8,9}$	$S_{10,11}$	S_{12}	C_1	C_2	C_3
1	$+6\,V_{dc}$	01	10	10	01	01	0	D	D	D
2	$+5\,V_{dc}$	01	10	10	10	01	0	D	D	D
3	$+4\,V_{dc}$	01	10	01	10	01	0	C	C	D
4	$+3\,V_{dc}$	01	10	10	01	10	1	D	D	C
5	$+2\,V_{dc}$	01	10	10	10	10	0	D	D	–
6	$+V_{dc}$	01	10	01	10	10	0	C	C	–
7	0	01	01	10	01	10	1	D	D	C
8		10	10	10	01	10	1	D	D	C
9	$-V_{dc}$	10	01	01	10	10	0	C	C	–
10	$-2\,V_{dc}$	10	01	10	10	10	0	D	D	–
11	$-3\,V_{dc}$	10	01	10	01	10	1	D	D	C
12	$-4\,V_{dc}$	10	01	01	10	01	0	C	C	D
13	$-5\,V_{dc}$	10	01	10	10	01	0	D	D	D
14	$-6\,V_{dc}$	10	01	10	01	01	0	D	D	D

Figure 3 shows the positive conducting paths in each operating state. Note that the lines highlighted in green represent the charging circuit of the capacitors, and that the lines highlighted in red represent the paths of the synthetic voltage level. In addition, the proposed 13-level topology can integrate the inductive load, because there is a reverse current path composed of capacitors and anti-parallel diodes. For the simplicity of analysis, the assumption is that all devices are ideal and that the voltages of capacitors C_1 and C_2 are

constant at V_{dc}, while the voltage of capacitor C_3 is constant at 3 V_{dc}. The positive polarity voltage is generated when switches S_2 and S_3 are turned on, and the negative polarity voltage is generated when the switches S_1 and S_4 are turned on.

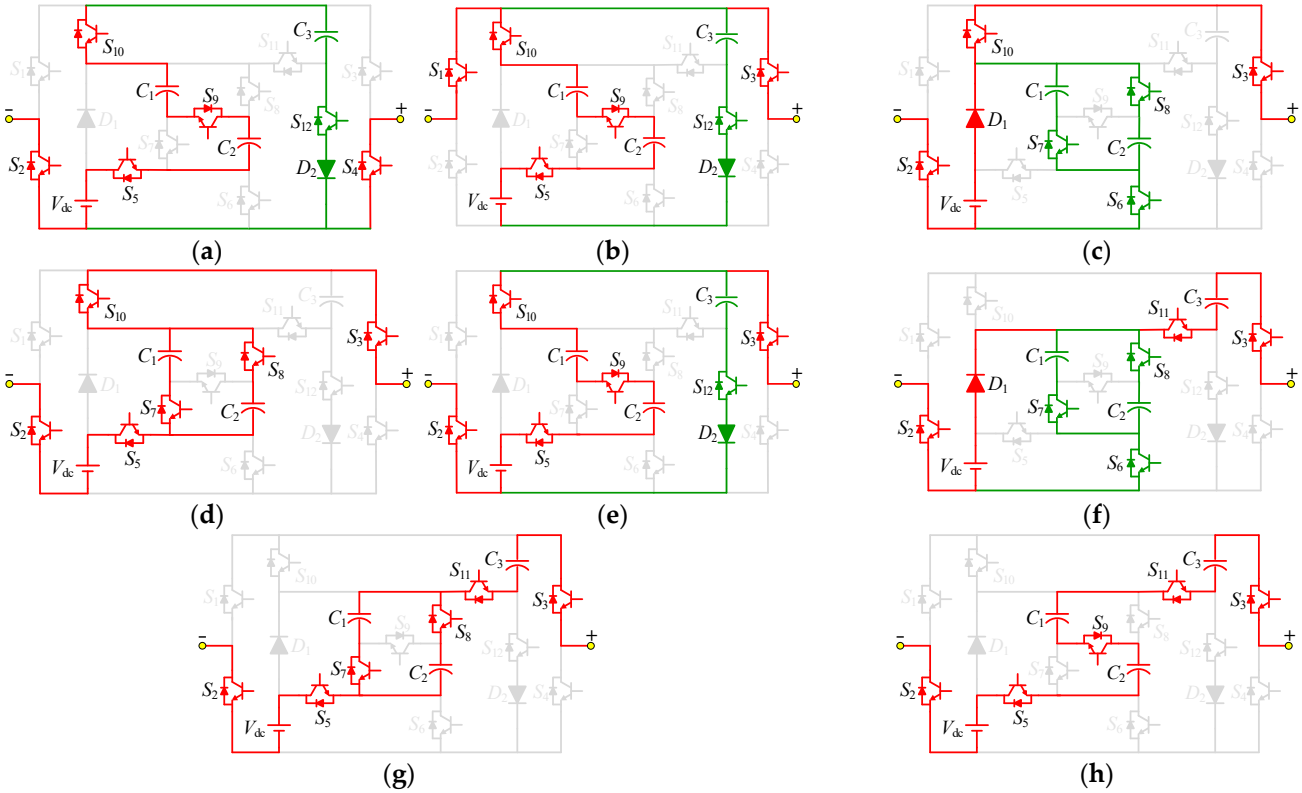

Figure 3. Operating states of the proposed 13−level inverter. (**a**,**b**) $V_o = 0$. (**c**) $V_o = +V_{dc}$. (**d**) $V_o = +2\ V_{dc}$. (**e**) $V_o = +3\ V_{dc}$. (**f**) $V_o = +4\ V_{dc}$. (**g**) $V_o = +5\ V_{dc}$. (**h**) $V_o = +6\ V_{dc}$.

2.3. Modulation Strategy

A number of modulation strategies have been put forward to control multilevel inverters, such as sinusoidal pulse width modulation (SPWM) [29], nearest level control (NLC) [30], and selective harmonic elimination (SHE) [31]. To reduce the operational complexity and the value of THD, the phase disposition pulse width modulation (PD-PWM) is used to generate the drive signal of the switches, as shown in Figure 4.

For the proposed 13-level inverter, there are twelve triangular carriers (u_1~u_{12}) with the same amplitude A_c and frequency f_c, which are compared with the sinusoidal reference wave with amplitude A_{ref} and frequency 50 Hz (f_o). The processes of the capacitor charge and discharge in one cycle are also presented. The voltage of capacitors C_1 and C_2 can be kept at V_{dc} with the same voltage ripple $\Delta V_{c1,2}$, and the voltage of capacitor C_3 can be kept at 3 V_{dc} with the voltage ripple ΔV_{c3}. The modulation logic of the 13-level inverter is presented in Figure 5. There are five complementary switch pairs and a 13-level output is obtained through logical combinations.

For the modulation strategy adopted in the proposed topology, the number of output levels is related to the modulation index, and the modulation index M can be expressed as

$$M = \frac{A\text{ref}}{6\ A\text{c}}. \tag{1}$$

Table 2 shows the output voltage levels and the corresponding range of M, which varies between 0 and 1.

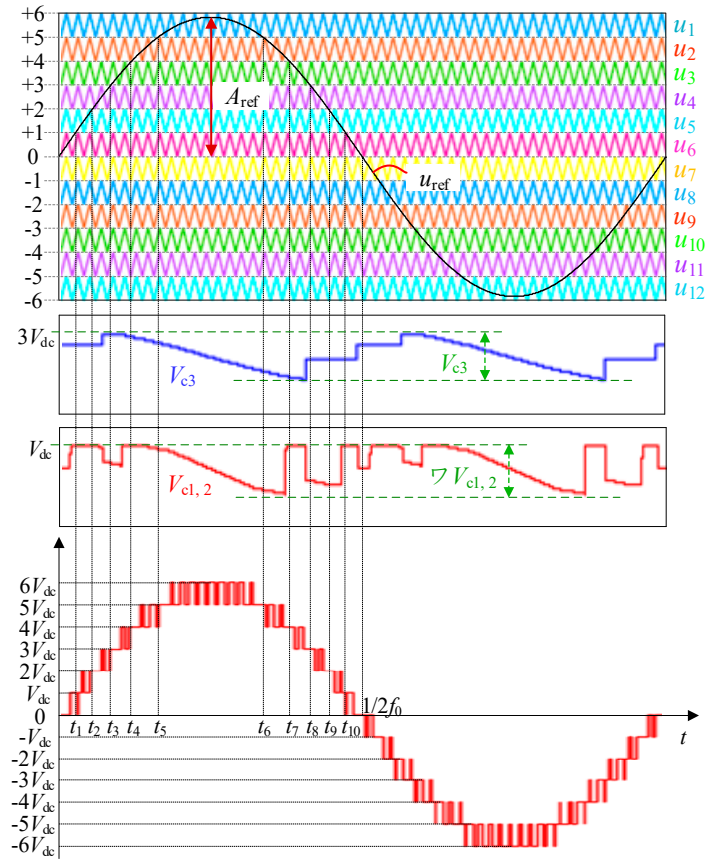

Figure 4. The PD−PWM for the 13−level inverter.

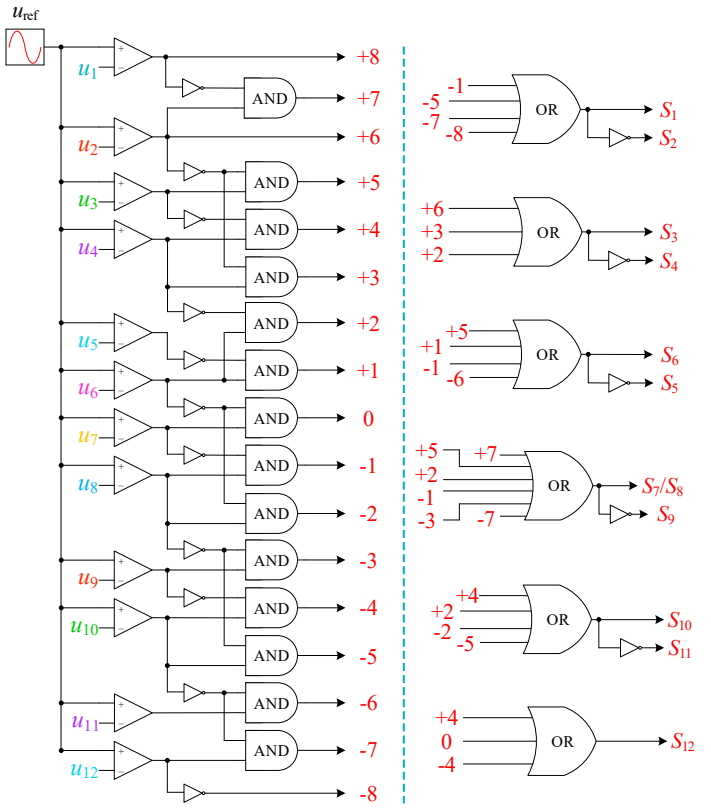

Figure 5. Modulation logic for the 13-level inverter.

Table 2. The relationship between M and the output level.

M	Number of Levels	Output Voltage Levels
$0 < M \leq 1/6$	3	$\pm V_{dc}$, 0
$1/6 < M \leq 1/3$	5	$\pm 2\ V_{dc}$, $\pm V_{dc}$, 0
$1/3 < M \leq 1/2$	7	$\pm 3\ V_{dc}$, $\pm 2\ V_{dc}$, $\pm V_{dc}$, 0
$1/2 < M \leq 2/3$	9	$\pm 4\ V_{dc}$, $\pm 3\ V_{dc}$, $\pm 2\ V_{dc}$, $\pm V_{dc}$, 0
$2/3 < M \leq 5/6$	11	$\pm 5\ V_{dc}$, $\pm 4\ V_{dc}$, $\pm 3\ V_{dc}$, $\pm 2\ V_{dc}$, $\pm V_{dc}$, 0
$5/6 < M \leq 1$	13	$\pm 6\ V_{dc}$, $\pm 5\ V_{dc}$, $\pm 4\ V_{dc}$, $\pm 3\ V_{dc}$, $\pm 2\ V_{dc}$, $\pm V_{dc}$, 0

2.4. Capacitor Analysis

The capacitor voltage of the proposed SCMLI can be balanced without the extra loops, which is crucial to generate the ideal voltage. The capacitors C_1, C_2, and C_3 can be charged through a parallel charging mechanism in each cycle, as shown in Table 1 and Figure 3.

To diminish the voltage ripple and improve the quality of the voltage waveform, the maximum voltage ripple of the capacitor is set to remain below 10% of the rated capacitor voltage. The voltage ripple is related to the continuous discharging amount of capacitor. It can be seen in Figure 4 that the points of u_{ref} intersect and that the carriers are set to t_i (i = 1, 2, 3. . ., 12), which can be calculated by

$$t_i = \frac{\arcsin\left(\frac{i}{6M}\right)}{2\pi f_o}, \tag{2}$$

where f_o is the output frequency and M is set to 0.9. As is shown in Figure 4, the maximum discharging interval of the capacitors C_1 and C_2 is [t_4–t_7], whilst the maximum discharging interval of capacitor C_3 is [t_3–t_8]. The instants t_3, t_4, t_7, and t_8 can be calculated by

$$t_3 = \frac{\arcsin\left(\frac{1}{2M}\right)}{2\pi f_o}, \tag{3}$$

$$t_4 = \frac{\arcsin\left(\frac{2}{3M}\right)}{2\pi f_o}, \tag{4}$$

$$t_7 = \frac{\pi - \arcsin\left(\frac{2}{3M}\right)}{2\pi f_o}, \tag{5}$$

$$t_8 = \frac{\pi - \arcsin\left(\frac{1}{2M}\right)}{2\pi f_o}, \tag{6}$$

The capacitors C_1 and C_2 have the same discharge cycle and rated capacitor voltage. For the simplicity of analysis, only capacitor C_1 is calculated. According to Equations (3)–(6), the maximum discharge amount of C_1 and C_3 can be obtained as

$$\Delta Q_1 = \int_{t_4}^{t_7} I_o \sin(2\pi f_o t) dt, \tag{7}$$

$$\Delta Q_3 = \int_{t_3}^{t_8} I_o \sin(2\pi f_o t) dt, \tag{8}$$

where ΔQ_1 and ΔQ_3 are the maximum discharge amounts of C_1 and C_3, respectively, whilst I_o is the output current. Supposing that the coefficient defining maximum admissible voltage ripple is 0.1, then the capacitance can be calculated by

$$C_1 = C_2 \geq \frac{\Delta Q_1}{0.1 V_{C1}}, \tag{9}$$

$$C_3 \geq \frac{\Delta Q_3}{0.1 V_{C3}}, \tag{10}$$

where V_{C1} and V_{C3} are the rated voltages of C_1 and C_3, respectively. The voltage ripple of the capacitors can be kept within an acceptable bound through a suitable capacitance.

3. Power Losses Analysis

For the proposed 13-level topology, three kinds of power loss are calculated, namely the switching losses (P_{sw}), conduction losses (P_{con}), and ripple losses of capacitors (P_{rip}).

3.1. Switching Losses

The switching losses are produced by the overlapping of the voltage and current during the switch on/off process, which includes the switch-on loss ($P_{sw,on}$) and switch-off loss ($P_{sw,off}$). For simplicity, the switching losses are calculated according to the linear approximation of the voltage and current. According to the calculation method in [16], the $P_{sw,on}$ and $P_{sw,off}$ of the i-th switch are expressed as

$$\begin{aligned} P_{sw,on,i} &= f_{sw}\int_0^{t_{on}} v_{sw,i}(t)i(t)dt \\ &= f_{sw}\int_0^{t_{on}} \left(-\frac{V_{sw,i}}{t_{on}}(t-t_{on})\right)\left(\frac{I_{on,i}}{t_{on}}t\right)dt, \\ &= \frac{f_{sw}V_{sw,i}I_{on,i}t_{on}}{6} \end{aligned} \tag{11}$$

$$\begin{aligned} P_{sw,off,i} &= f_{sw}\int_0^{t_{off}} v_{sw,i}(t)i(t)dt \\ &= f_{sw}\int_0^{t_{off}} \left(\frac{V_{sw,i}}{t_{off}}t\right)\left(-\frac{I_{off,i}}{t_{off}}(t-t_{off})\right)dt \\ &= \frac{f_{sw}V_{sw,i}I_{off,i}t_{off}}{6}, \end{aligned} \tag{12}$$

where f_{sw} is the switching frequency of the inverter, $V_{sw,i}$ represents the stress of the i-th switch, t_{on} and t_{off} are the turn-on time and turn-off time of the switch, respectively, and $I_{on,i}$ and $I_{off,i}$ represent the current through the i-th switch after turning on and before shutting off, respectively. Thus, the P_{sw} of the all switches is expressed as

$$P_{sw} = \sum_{i=1}^{12}(P_{sw,on,i} + P_{sw,off,i}). \tag{13}$$

3.2. Conduction Losses

The conduction losses can be produced by the impedance of semiconductor devices and capacitors, which include the conduction resistance R_s of switches, the internal resistance R_d of diodes, and the equivalent series resistance ESR_C of capacitors. Figure 6 provides the predigested circuits for all operating states.

Table 3 shows the equivalent parameters of each operating state. Herein, $V_{o,j}$ and $R_{eq,j}$ are the output voltage and equivalent parameters, respectively. For the interval of [0, t_1], the energy loss can be expressed as

$$E_{0\sim V_{dc}} = \int_0^{t_1} [I_o \sin(2\pi f_o t)]^2 \times [R_{eq,1}\frac{A_{ref}\sin(2\pi f_o t)}{A_c} + R_{eq,0}(1 - \frac{A_{ref}\sin(2\pi f_o t)}{A_c})]dt. \tag{14}$$

For other intervals, the energy losses can be calculated in the same way.

$$E_{V_{dc}\sim 2V_{dc}} = \int_{t_1}^{t_2} [I_o \sin(2\pi f_o t)]^2 \times [R_{eq,2}\frac{A_{ref}\sin(2\pi f_o t) - A_c}{A_c} + R_{eq,1}(1 - \frac{A_{ref}\sin(2\pi f_o t) - A_c}{A_c})]dt, \tag{15}$$

$$E_{2V_{dc}\sim 3V_{dc}} = \int_{t_2}^{t_3} [I_o \sin(2\pi f_o t)]^2 \times [R_{eq,3}\frac{A_{ref}\sin(2\pi f_o t) - 2A_c}{A_c} + R_{eq,2}(1 - \frac{A_{ref}\sin(2\pi f_o t) - 2A_c}{A_c})]dt, \tag{16}$$

$$E_{3V_{dc}\sim 4V_{dc}} = \int_{t_3}^{t_4} [I_o \sin(2\pi f_o t)]^2 \times [R_{eq,4}\frac{A_{ref}\sin(2\pi f_o t) - 3A_c}{A_c} + R_{eq,3}(1 - \frac{A_{ref}\sin(2\pi f_o t) - 3A_c}{A_c})]dt, \quad (17)$$

$$E_{4V_{dc}\sim 5V_{dc}} = \int_{t_4}^{t_5} [I_o \sin(2\pi f_o t)]^2 \times [R_{eq,5}\frac{A_{ref}\sin(2\pi f_o t) - 4A_c}{A_c} + R_{eq,4}(1 - \frac{A_{ref}\sin(2\pi f_o t) - 4A_c}{A_c})]dt, \quad (18)$$

$$E_{5V_{dc}\sim 6V_{dc}} = \int_{t_5}^{t_6} [I_o \sin(2\pi f_o t)]^2 \times [R_{eq,6}\frac{A_{ref}\sin(2\pi f_o t) - 5A_c}{A_c} + R_{eq,5}(1 - \frac{A_{ref}\sin(2\pi f_o t) - 5A_c}{A_c})]dt. \quad (19)$$

Based of the above, the P_{con} of the proposed 13-level topology can be obtained by

$$P_{con} = (4E_{0\sim V_{dc}} + 4E_{V_{dc}\sim 2V_{dc}} + 4E_{2V_{dc}\sim 3V_{dc}} + 4E_{3V_{dc}\sim 4V_{dc}} + 4E_{4V_{dc}\sim 5V_{dc}} + 2E_{5V_{dc}\sim 6V_{dc}}) \times f_{ref}. \quad (20)$$

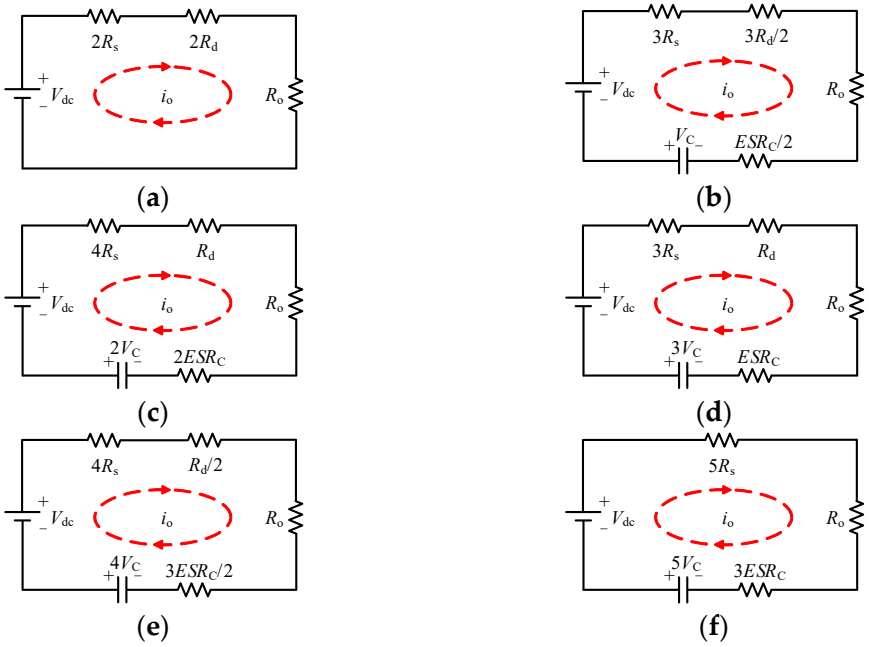

Figure 6. Equivalent circuits for each operating state. (**a**) $V_o = \pm V_{dc}$; (**b**) $V_o = \pm 2\ V_{dc}$; (**c**) $V_o = \pm 3\ V_{dc}$; (**d**) $V_o = \pm 4\ V_{dc}$; (**e**) $V_o = \pm 5\ V_{dc}$; and (**f**) $V_o = \pm 6\ V_{dc}$.

Table 3. Parameters of the equivalent circuits.

j	$V_{o,j}$	$R_{eq,j}$
0	0	$R_s + R_d$
1	$\pm V_{dc}$	$2\ R_s + 2\ R_d$
2	$\pm 2\ V_{dc}$	$3\ R_s + 3\ R_d/2 + ESR_C/2$
3	$\pm 3\ V_{dc}$	$4\ R_s + R_d + 2\ ESR_C$
4	$\pm 4\ V_{dc}$	$3\ R_s + R_d + ESR_C$
5	$\pm 5\ V_{dc}$	$4\ R_s + R_d/2 + 3\ ESR_C/2$
6	$\pm 6\ V_{dc}$	$5\ R_s + 3\ ESR_C$

3.3. Ripple Losses

The ripple losses can be produced by the voltage fluctuation of the capacitor, and the voltage ripple of capacitors C_1, C_2, and C_3 can be obtained as

$$\Delta V_{C1} = \Delta V_{C2} = \frac{\Delta Q_1}{C_1}, \quad (21)$$

$$\Delta V_{C3} = \frac{\Delta Q_3}{C_3}, \quad (22)$$

where the ΔV_{C1}, ΔV_{C2}, and ΔV_{C3} are the voltage ripples of capacitors C_1, C_2, and C_3, respectively. According to the calculation method in [28], the ripple losses of the capacitors are expressed as

$$P_{\text{rip}} = \frac{f_{\text{o}}}{2} \sum_{k=1}^{3} C_k \Delta V_{Ck}^2. \tag{23}$$

Overall, the power losses of the proposed 13-level topology are expressed as

$$P_{\text{loss}} = P_{\text{sw}} + P_{\text{con}} + P_{\text{rip}}. \tag{24}$$

Finally, the theoretical efficiency is indicated by η, which is defined by

$$\eta = \frac{P_{\text{o}}}{P_{\text{sw}} + P_{\text{con}} + P_{\text{rip}} + P_{\text{o}}}, \tag{25}$$

where P_{o} is the output power of the inverter.

4. Topology Extension and Comparison

4.1. Topology Extension

One of the main benefits of the proposed 13-level topology is that it allows for modular extensions. As illustrated in Figure 7, each L-type unit (LTU) contains a capacitor, three power switches, and a diode. It can be learned from a previous analysis that capacitor C_3 is charged in series with the capacitors C_1 and C_2 through switches S_{10} and S_{12}. Theoretically, n LTUs can be integrated into the proposed switched-capacitor multilevel inverter. For the n-th LTU, capacitor C_{n+2} can be charged to $(3 \times 2^{n-1})$ V_{dc} through series connection with the capacitors C_1~C_{n+1}, since the voltage levels and boost factor will be increased by connecting multiple L-type units.

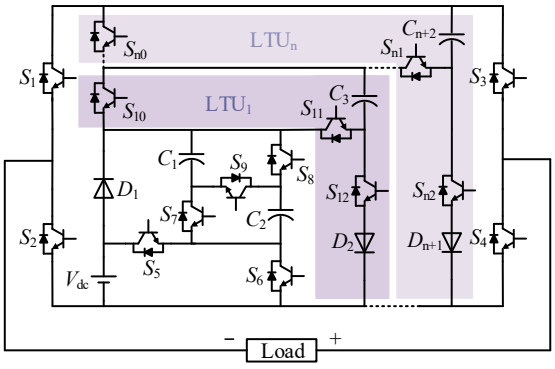

Figure 7. Extended structure with n LTUs.

The extended inverter consists of n number of LTU, the switch count N_{switch}, the diode count N_{diode}, the switched capacitor count $N_{\text{capacitor}}$, the voltage levels N_{level}, and the boost factor G can be expressed as:

$$N_{\text{switch}} = 3n + 9, \tag{26}$$

$$N_{\text{diode}} = n + 1, \tag{27}$$

$$N_{\text{capacitor}} = n + 2, \tag{28}$$

$$N_{\text{level}} = 3 \times 2^{n+1} + 1, \tag{29}$$

$$G = 3 \times 2^{n}. \tag{30}$$

The THD of the proposed inverter can be further reduced with the increase in output levels, while the control of switches will be more complex, and the demand for carriers will also increase significantly, which is twice as much as voltage gain. Therefore, reasonable output levels and voltage gain can be chosen according to application requirements.

4.2. Comparison Analysis

To assess the pros and cons of the proposed SCMLI, a comprehensive contrast with other 13-level topologies is shown in Table 4. Items which are compared include the number of power elements, the number of DC sources, the number of drivers (N_{driver}), the voltage gain, the total standing voltage (TSV), and the extensibility of SCMLIs. The cost function in [16] is defined as follows

$$\text{CF} = \left(N_{\text{switch}} + N_{\text{driver}} + N_{\text{diode}} + N_{\text{capacitor}} + \alpha \frac{\text{TSV}}{G} \right) \times \frac{N_{\text{dc}}}{13}, \tag{31}$$

where α is the "weighing factor" reflecting the proportion of TSV in the cost function, which is considered to be 0.5 or 1.5. Therefore, the multilevel inverters with a lower cost function have a better performance.

Table 4. Comparison with other 13-level SCMLIs.

Reference	N_{dc}	N_{switch}	N_{driver}	N_{diode}	$N_{\text{capacitor}}$	G	TSV	CF		Extensibility
								α = 0.5	α = 1.5	
[10]	2	11	7	1	1	2	39	4.577	7.577	No
[11]	2	14	11	0	2	2	32	5.384	7.846	No
[16]	2	14	14	2	4	3	34	6.103	7.846	Yes
[18]	1	10	8	10	5	6	43	2.814	3.365	Yes
[19]	1	12	8	2	4	1.5	15	2.385	3.154	Yes
[20]	1	12	7	4	4	3	13	2.243	2.577	No
[21]	1	14	13	2	4	3	18	2.769	3.230	Yes
[22]	1	13	11	1	3	3	17	2.372	2.808	Yes
[23]	1	29	29	5	5	6	29	5.416	5.788	Yes
[24]	1	13	9	2	3	6	39	2.327	2.827	No
[25]	1	14	10	1	3	6	33	2.365	2.788	No
[26]	1	15	12	0	3	6	35	2.532	2.981	No
[27]	1	12	6	4	3	6	36	2.154	2.615	No
[29]	1	13	9	2	3	6	32	2.282	2.692	No
Proposed	1	12	6	2	3	6	38	2.013	2.500	Yes

It can be concluded from Table 4 that the multilevel inverter in [10] can achieve 13-level output with less components, but the voltage gain is only of 2, which is the same as the inverter in [11]. The topology in [16] requires more components in the extended structure. In addition, the above three topologies use two DC sources, which also leads to a high CF value. The inverter in [18] uses a single source to achieve the high-voltage gain. However, the H-bridge will increase the voltage stress of the switches.

Compared with the above topologies, TSV is significantly reduced in [19–22], but their voltage gain is no more than 3, and the application range is limited. Due to plenty of elements being used, the inverter in [23] has a higher CF. The 13-level inverters in [24–27] and [29] can achieve a six-fold voltage gain. The inverter in [24] has a lower CF value when α = 0.5, while the inverter in [25] has a lower CF value when α = 1.5, because they have a different TSV.

Although the proposed multilevel inverter has a higher TSV, it uses fewer power devices to achieve a six-fold voltage gain. Due to the fact that the proposed inverter has five switch pairs operating in complementary states, fewer drivers are needed to control the switches, and the lowest value of N_{driver} can be achieved. Compared with the inverters in [24–27,29], the proposed topology with good extensibility can easily increase the output

levels and acquire a higher voltage gain, which is conducive to applying more scenarios. Moreover, it can be seen that the CF of the proposed 13-level switched-capacitor inverter is lowest regardless of whether α is 0.5 or 1.5, which also confirms that the proposed topology has a better overall performance.

5. Simulation and Experimental Analysis

5.1. Simulations

To validate the correctness of the proposed switched-capacitor multilevel inverter, the 13-level inverter model was built and simulated in the MATLAB/Simulink environment. The simulation parameters are listed in Table 5. In the simulation model, the input voltage V_{dc} is 25 V, the load is 80 Ω or 80 Ω + 15 mH, the output frequency is 50 Hz, and the value of M is 0.9.

Table 5. Simulation parameters.

Parameters	Values
Input voltage (V_{dc})	25 V
Output frequency (f_o)	50 Hz
Triangle carrier frequency	3 kHz
Capacitors $C_1/C_2/C_3$	2200 μF
Modulation index (M)	0.9
Load	80 Ω/80 Ω + 15 mH

Figure 8 shows the corresponding results of the proposed topology. The waves of the output voltage and current under resistive–inductive load is shown in Figure 8a. The proposed inverter outputs 13 levels and the peak voltage is close to 150 V, which also indicates a voltage gain of 6. The load current is sinusoidal, so the inverter can provide a channel for reverse current. Figure 8b presents the waves of the output voltage and current under pure resistive load. Figure 8c gives the waves of all capacitors voltage. It can be seen that the voltage of the capacitors fluctuates slightly within the allowable range during charging and discharging.

The THD of the inverter is approximately 10.37%, as shown in Figure 9, which indicates that the modulation method used can effectively reduce the harmonic content and improve the quality of the output voltage. In addition, due to the carrier frequency being 3 kHz, the 60th harmonic component is the highest compared to the others. Moreover, the low THD can be further reduced by smaller filters or optimized modulation strategies.

5.2. Experimental Result

To validate the effectiveness of the proposed topology, a 13-level switched capacitor inverter test prototype has been built, as shown in Figure 10. Table 6 gives the specific experiment parameters. The carrier frequency is set to 3 kHz and the output frequency is set to 50 Hz. The steady-state and dynamic performance of the proposed multilevel topology are experimentally analyzed.

The strain capacity of the SCMLI was tested under complicated working states by changing the experimental parameters, such as the change of the input voltage, load, modulation ratio, and frequency.

Figure 11a gives the steady-state wave of output voltage and current when the modulation ratio M = 0.9. The switched capacitor inverter can output 13-level voltage and achieve a six-fold voltage gain, which is in line with the theoretical analysis. In addition, the output current is close to the sine wave, indicating that the proposed topology has a reverse current loop to carry out the inductive load. Figure 11b shows the waves of the capacitors voltage, which slightly fluctuates within the allowable range.

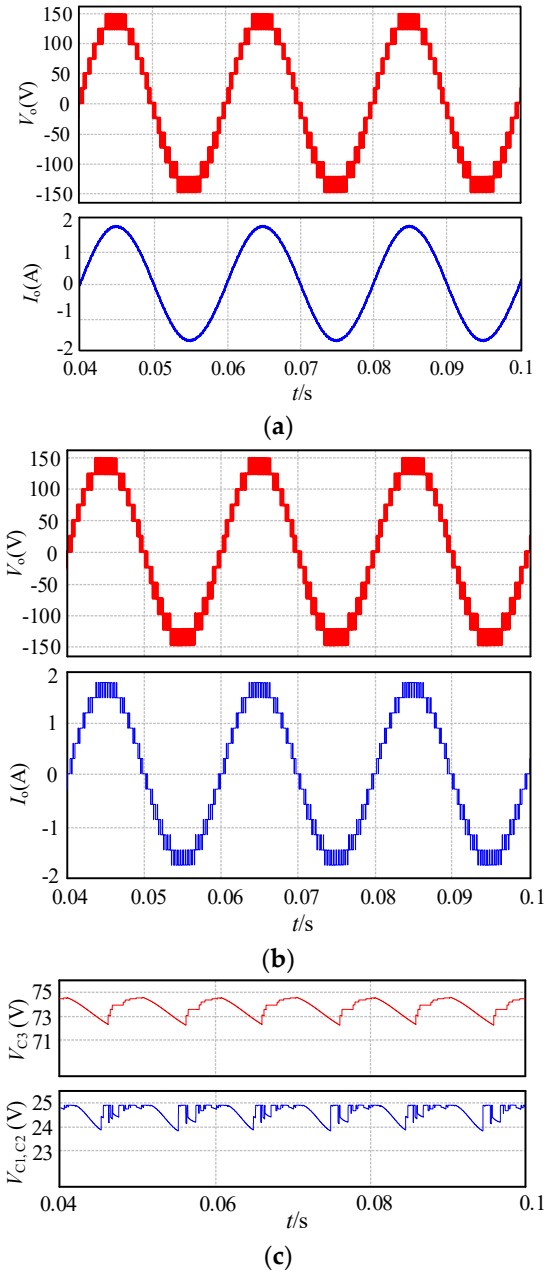

Figure 8. Simulation waveforms. (**a**) Output voltage and current under resistive−inductive load. (**b**) Output voltage and current under resistive load. (**c**) Voltage waves of C_1, C_2, and C_3.

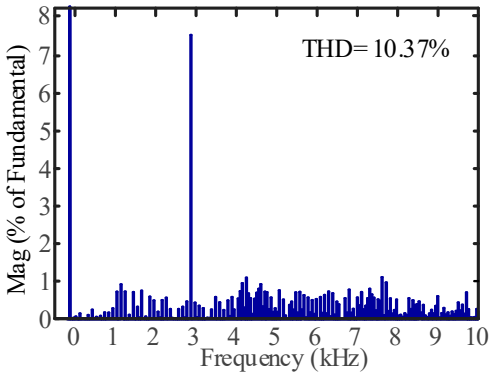

Figure 9. THD of the output voltage.

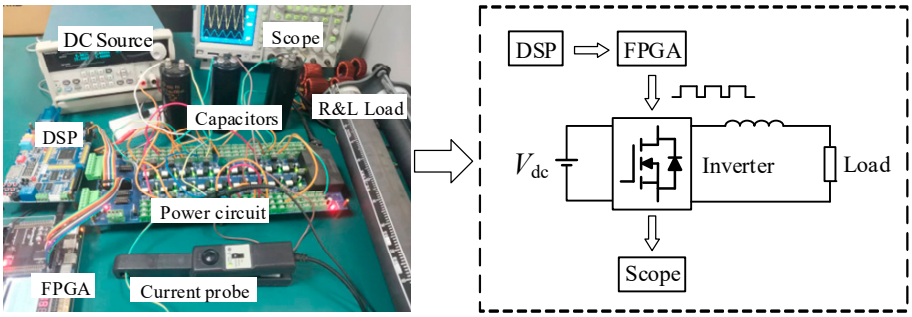

Figure 10. Experimental prototype and schematic.

Table 6. Experimental parameters.

Components	Specifications
Input voltage (V_{dc})	25 V
Output frequency (f_o)	50 Hz/25 Hz/100 Hz
Carrier frequency	3 kHz
Capacitors $C_1/C_2/C_3$	2200 μF
Resistive-inductive load	80/160 Ω + 15 mH
Switches (S_1~S_{12})	SPP20N60C3
Diode	MBR20200CTG
Optocouplers	TLP250
Current probe	Tektronix A622

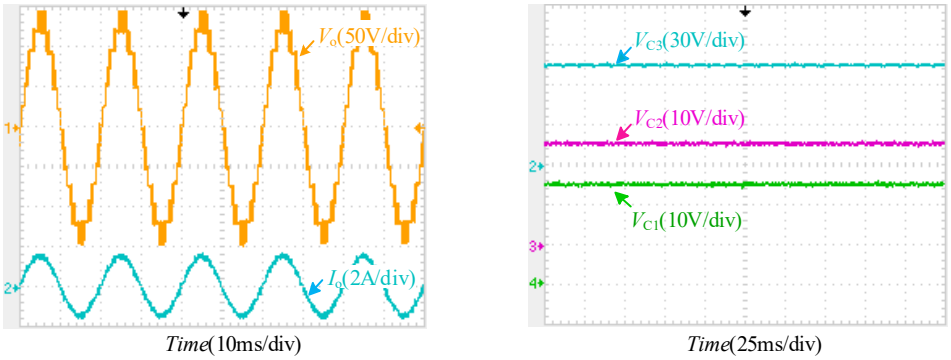

Figure 11. Experimental results at the steady-state. (**a**) Output voltage and current. (**b**) Voltages of C_1, C_2, and C_3.

Figure 12 shows the waves of the output voltage and current under input voltage changes between 25 V and 15 V. It is apparent that the voltage levels and boost factor of the inverter remain unchanged during the sudden change in input voltage, and the output voltage and load current can alter synchronously and stably with the input voltage.

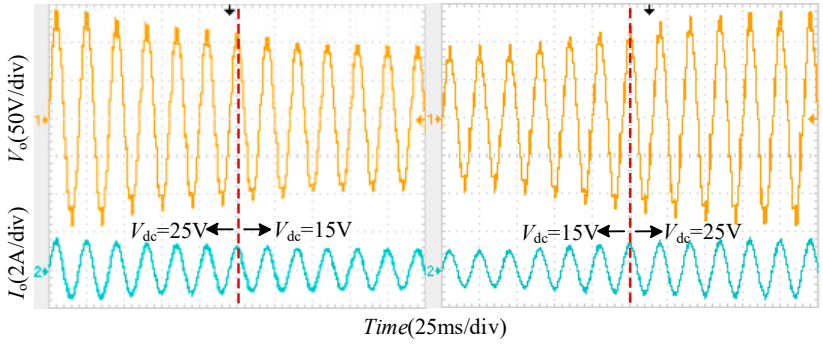

Figure 12. Waves of the output voltage and current under the mutation of input voltage changes.

Figure 13 presents waves of the capacitors' voltage under the input voltage of the topology changes between 25 V and 15 V. It is apparent that the capacitor voltage is relatively rapid and reaches the steady state after a short transition.

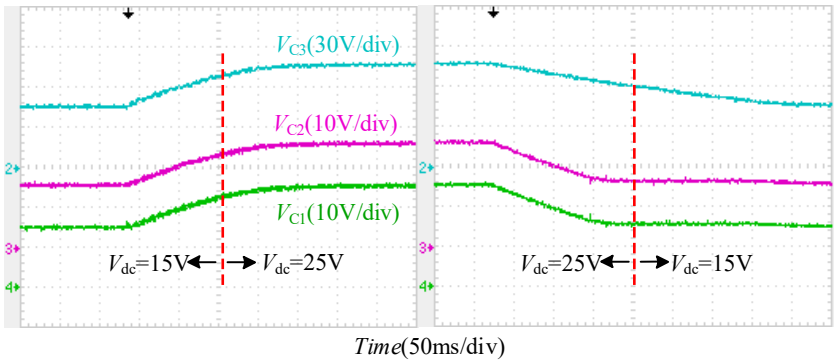

Figure 13. Waves of capacitor voltage under the mutation of the input voltage.

Figure 14 gives the output voltage and current waveform under the mutation of the load (unloaded to 80 Ω + 15 mH and 80 Ω + 15 mH to 160 Ω + 15 mH). It is apparent that the output voltage remains stable during the sudden change in load, and that the current quickly changes from 0 to the working state before decreasing as the load increases.

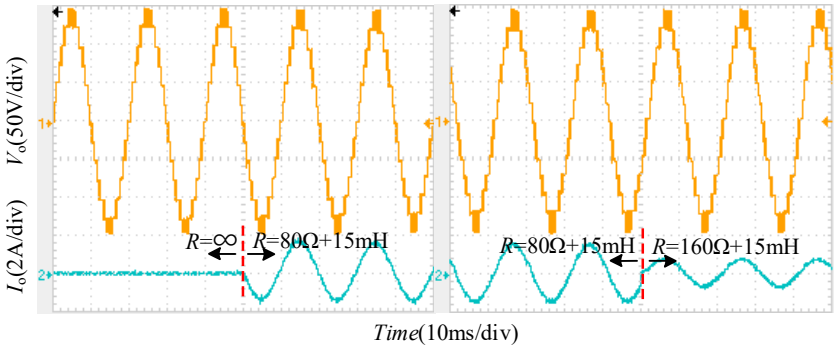

Figure 14. Waves of output voltage and current under the mutation of load.

Figure 15 presents the experimental waveforms of the proposed SCMLI under the mutation of the modulation index *M*. It is apparent that the voltage levels decrease from 13 to 9 when *M* alters from 0.9 to 0.6, and the voltage gain is reduced to 4, whilst voltage levels decrease from 9 to 7 when *M* is altered from 0.6 to 0.4, and the voltage gain is reduced to 3, which is consistent with the analysis in Table 2.

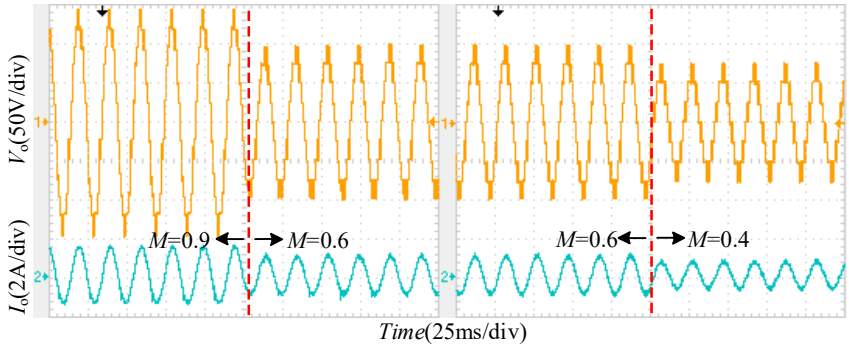

Figure 15. Waves of output voltage and current under the mutation of *M*.

Figure 16 gives the waves of the output voltage and current when the output frequency changes between 25 Hz and 100 Hz. It is apparent that, when the output frequency of the topology changes, the amplitude of the output voltage and the load current remain unchanged, and the frequency change response is rapid, which verifies that the proposed topology can work normally in a complex environment.

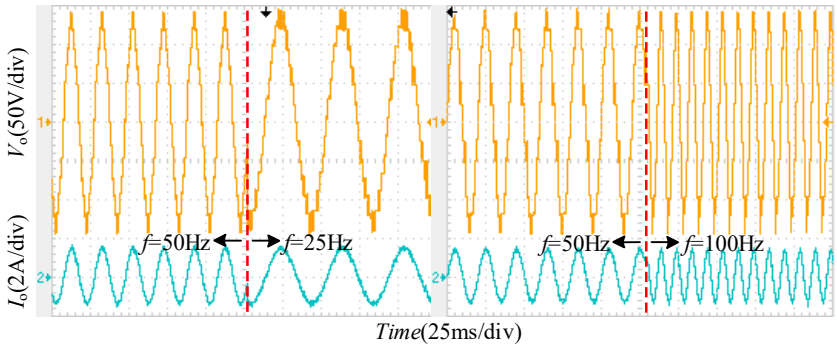

Figure 16. Waves of output voltage and current under the mutation of frequency.

6. Conclusions

This article introduces a new 13-level SCMLI, which can reduce the number of power elements and achieve voltage self-balance. Through the combination of a switched capacitor unit (SCU) and an L-type unit (LTU), the proposed inverter is capable of a six-fold voltage gain with a single DC source and twelve switches. At the same time, the modulation method and loss calculation are briefly described. In addition, the proposed topology also has the capability of modular expansion. By increasing the number of LTUs, the voltage levels and boost factor can be significantly increased. Moreover, the proposed inverter has been compared with existing 13-level switched-capacitor inverters in detail. The results show that the proposed inverter employs fewer power devices and has obvious advantages in reducing the CF value. Finally, the proposed multilevel topology is built through an experimental prototype. The static and dynamic analysis results validate the effectiveness of the proposed SCMLI, which can quickly adjust a complex working environment.

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