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Generalized one-cycle current controller for improved SAPF power quality management

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ABSTRACT

Current controllers are used in shunt active power filters to enhance the performance of electrical power systems by improving power quality and energy efficiency. Nonlinear current controllers are preferred in systems with nonlinear and dynamic loads due to their robust and rapid tracking of varying reference currents. Within this category, reference-based one-cycle current controllers feature fixed switching frequency and quasi-instantaneous reference current tracking. When compared to implementations based on classical one-cycle controllers (OCC), they enable tracking any desired reference current while maintaining cycle-by-cycle control. They are suitable for selective harmonic filtering, as well as source current balancing and reactive current compensation. However, these controllers have shown stability problems caused by the switching function alignment – even when symmetrical centred alignment is employed. To address these challenges, this work proposes a generalized reference-based one-cycle current controller. This new controller algorithm introduces two degrees of freedom in the formation of the switching signal and achieves stability, zero integral-current-error, and the selection of the final current value at the end of each switching cycle. The effectiveness of the proposed algorithm is validated through simulations and experimental results obtained from a three-leg four-wire shunt active power filter setup. A performance comparison is made between the new algorithm and previous approaches. The results demonstrate that the proposed controller achieves superior power quality indices by reducing the current harmonic distortion and approaching unity power factor.

1. Introduction

Shunt active power filters (SAPFs) generate currents to improve the power quality of electrical power systems by compensating for unbalance, reactive, and distortion phenomena [1–3]. The reduction of these power issues increases the capacity of the electrical system to deliver useful power and so produces more energy-efficient electrical power networks. SAPFs are connected at the point of common coupling (PCC) between the three-phase ac supply power network, the non-efficient installation, and the SAPF, as shown in Fig. 1 [1,4,5].

Digital signal controllers (DSC) are used to control the SAPF and generate the appropriate output currents at the PCC (i_{z_SAPF}). The main functions of DSCs include analysing the load currents, deriving the reference currents to be generated, implementing current control, and generating the switching signals for the power converter. Current controllers play a fundamental role in ensuring accurate tracking of the reference currents. As tracking precision improves, their influence on enhancing the power quality of the electrical system also increases.

Numerous linear and non-linear current controllers have been developed and used [6–37]. Non-linear controllers show excellent performance for wide operating ranges. Linear controllers enable the use of classical control theory and the segregation of controller and modulator functions, facilitating pulse-width modulation at a constant switching frequency and thereby effectively managing the main harmonics. Hysteresis current control (HCC) [11,12,18,24–26,33,35], sigma-delta control (SDC) [27,28], sliding mode control (SMC) [20–23,29,30,34,36,37], and one-cycle control (OCC) [13–17,19,31,32] are among the most employed non-linear controllers in SAPFs. While some of these controllers enable constant switching frequency, they may also experience a performance trade-off. Only OCC manages to achieve the control objective within each switching cycle and so enabling quasi-instantaneous control with a simple hardware implementation that

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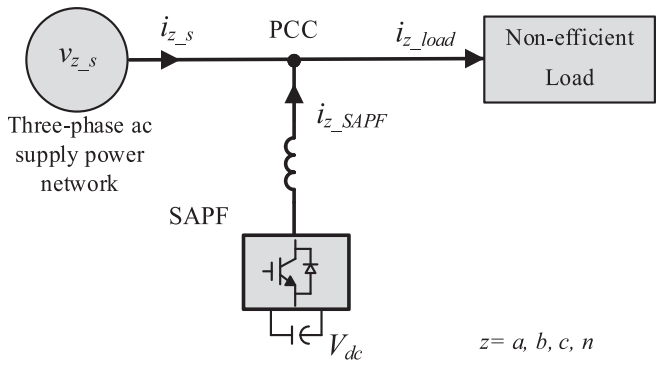


Fig. 1. Block diagram of the SAPF connection.

avoids the need of programmable digital controllers (such as DSPs or microcontrollers). In classical OCC implementations, from the perspective of the power source, the load behaves like an equivalent resistance that only demands active power. The main drawback of these approaches is that in the presence of voltage imbalance and/or voltage harmonics, source currents remain distorted and unbalanced. Furthermore, this method is unsuitable for selective harmonic filtering and so programable digital controllers are needed to solve these problems and generate the appropriate modifications for the controller.

The authors in [19] proposed a reference-based one-cycle zero-integral-error (OCZIE) current control method for SAPFs based on cycle-by-cycle tracking of a computed reference current. This controller combines the OCC one-cycle quasi-instantaneous control feature, with cycle-by-cycle switch ON-time optimisation to achieve current zero-integral-error in each switching cycle. It employed an alternating switching pattern strategy to achieve stable behaviour. However, the technological implementation proved to be complex, and problems were encountered in the transients at the zero-voltage crossovers. As a result, the authors proposed in [32] a new control approach that achieves stable zero-integral-error current control using a single symmetrical switching pattern. This innovation eliminates the need for two distinct switching patterns in the controller, so simplifying the implementation and resolving the mentioned problems. However, the control developed in [32] had the drawback of being critically stable, resulting in the failure to converge the error signal to zero. To address this issue, the authors proposed adding a proportional term to the controller which helps achieve system stability. Nevertheless, during transients, the controller is unable to zero the integral of the error in each switching cycle, thus deviating from its intended behaviour as a cycle-by-cycle zero-integral-error regulator. Furthermore, the adjustment of the proportional constant of the controller requires making a trade-off between control performance (keeping the integral of the error equal to zero) and settling time. From the previous works, it is concluded that the switching pattern influences the performance and stability of the reference-based OCZIE.

Therefore, a new reference-based one-cycle current controller that addresses the stability issues of the previous approaches is developed in this paper. The proposed algorithm enables the achievement of control objectives within a single switching cycle for all operating conditions. To achieve this, a generalization of the switching pattern using two degrees of freedom is proposed, resulting in a cycle-by-cycle controller that maintains the integral error at zero while allowing for the setting of the final value of the phase current in the switching cycle, and so ensuring stable behaviour. The ability to establish a final value for the current ($i_{(k+1)}$) in each switching cycle means that if the next reference ($i_{ref(k+1)}$) is known or can be predicted, the phase current will reach the next reference at the end of the switching cycle. This approach results in an outstanding current tracking performance, leading to improved power quality and more energy-efficient electrical power systems.

The paper is structured as follows: Section 2 introduces the optimisation problem aimed at achieving an OCC that maintains the current integral error at zero in a switching cycle, while also reaching a target phase current value at the end of that commutation cycle. In Section 3, the optimisation problem is solved and expressions for calculating the optimal times for defining the switching function in a switching period are derived. Section 4 describes the implementation of the proposed control algorithm and outlines the various scenarios for defining the phase current at the end of each switching period. Section 5 presents simulation results analysing and comparing the performance of the SAPF for each proposed scenario. Section 6 displays experimental results conducted with a laboratory SAPF prototype. Finally, conclusions are provided in Section 7.

2. Problem statement

Consider the simplified model of a three-phase SAPF depicted in Fig. 2. The power stage is formed by a three-branch four-wire grid-tied voltage source inverter (VSI). Three series inductances ($L_{a,b,c}$) must be used to connect the three phases to the ac power network. The fourth wire connects the neutral wire of the grid to the dc bus midpoint. This power stage configuration works as three independent single-phase converters sharing a unique dc bus. The VSI switches should be an IGBT-diode in anti-parallel association allowing bi-directional current flow. The switches of a branch are controlled in a complementary mode, meaning that only two states are possible for a branch at any time. The per-phase equivalent circuit is shown in Fig. 3. The control requirements are dc bus voltage regulation; dc bus midpoint voltage unbalance correction, and ac-side inductance current control.

Consider now the application of one-cycle current control with a fixed switching period T_{SW} to the circuit shown in Fig. 3. The proposal of this work is to design a stable SAPF current control with a two-degree of freedom switching pattern as shown in Fig. 4. At the beginning of the k switching period, the SAPF current has value $i_{(k)}$. The reference current is assumed to be a linear reference current $i_{ref(k)}(t) = i_{ref(k)} + m_{ref(k)}t$, where $i_{ref(k)}$ is the value of the reference current at the beginning of the switching period and $m_{ref(k)}$ is the reference slope. The period begins with the switch OFF ($S_Z = S_{off}$) during the delay time t_d, and S_Z is turned ON during time interval t_{on}. Finally, S_Z is turned OFF again if $T_{sw} - t_d - t_{on} > 0$. As a result, the control algorithm must determine not only the ON time t_{on} but also the delay time t_d.

The values of the delay time t_d and the ON time t_{on} are computed by solving the constrained optimisation problem (1)-(2) which minimizes the absolute value of the integral of the error. This is defined as the difference between the current reference $i_{ref}(t)$ and the SAPF current $i(t)$, that is $e(t) = i_{ref}(t) - i(t)$, while forcing the SAPF current value $i_{(k+1)}$ at the end of the switching period to be equal to the current reference of the next switching period $i_{ref(k+1)}$.

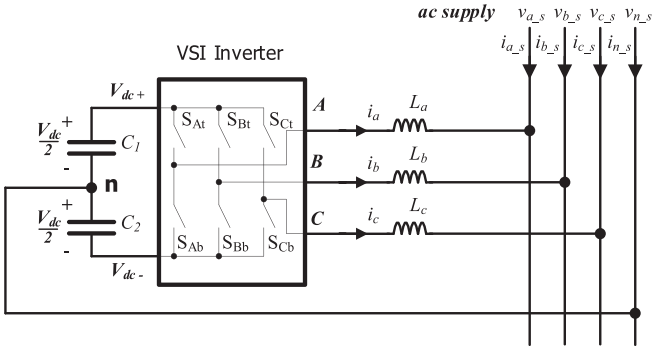


Fig. 2. Block diagram of a three-leg four-wire SAPF.

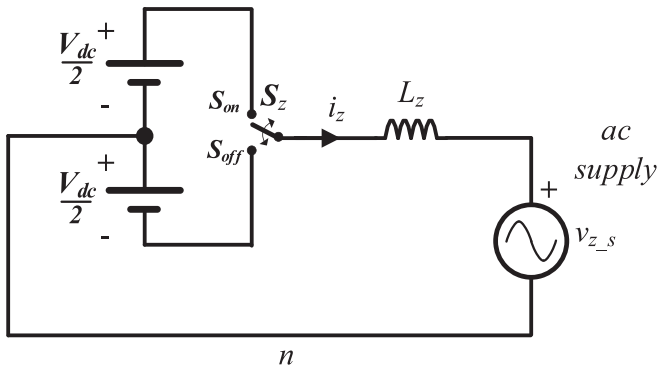


Fig. 3. Per-phase equivalent circuit of the SAPF.

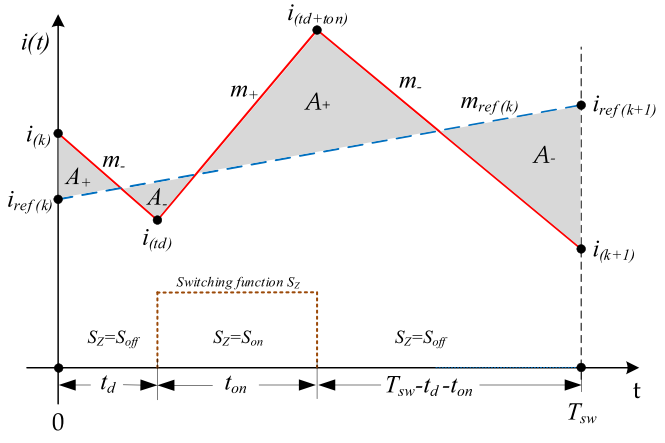


Fig. 4. Time evolution of phase current $i(t)$ with respect to t_{on} in a switching period.

$$\begin{matrix} \min \\ t_d \in [0, T_{sw}] \\ t_{on} \in [0, T_{sw} - t_d] \end{matrix} \left| \int_0^{T_{sw}} e(t)dt \right| \tag{1}$$

such that

$$i_{(k+1)} = i_{ref(k+1)} \tag{2}$$

In [32] a controller that minimized (1) was designed based on a centred switching pattern, but the resulting control was critically stable, and it was impossible to fix the value of the final current $i_{(k+1)}$ because the triggering pattern had only one-degree of freedom (the t_{on} time).

In summary, the solution to the optimisation problem defined by (1) and (2) achieves a stable control that minimizes cost function (1) and fixes the SAPF current value $i_{(k+1)}$ at the end of the switching period (2). The inclusion of constraint (2) in the optimisation problem enables including predicted values for the reference and this improves the current reference tracking.

From the power stage of Fig. 3, the current slopes are defined as follows:

- For a switching cycle *(k)*, when $S_z = S_{on}$, the phase current *i(t)* increases with slope m_+ defined as $m_{+(k)} = \frac{\frac{V_{dc}}{2} - v_{s(k)}}{L_z}$, which is always positive because $\frac{V_{dc}}{2}$ is always greater than v_s. When $S_Z = S_{off}$ the phase current decreases with slope m_- defined as $m_{-(k)} = \frac{-\frac{V_{dc}}{2} - v_{s(k)}}{L_z}$, which is always negative.
- The slopes m_+ and m_- are assumed to be constant during the switching cycle. For high switching frequencies (in the range of kHz), v_s and V_{dc} are nearly constant for a switching period. Slopes m_+ and m_- can then be considered constant for the entire switching cycle.

3. Optimal control

The optimal time delay t_d^* and ON time t_{on}^* are obtained by solving the constrained optimisation problem presented in (1) and (2). A linear reference current is assumed $i_{ref(k)}(t) = i_{ref(k)} + m_{ref(k)}t$. Furthermore, the SAPF current $i(t)$ for the two-degree of freedom switching pattern is given by (3). As a result, the current error $e(t)$ is given by (4) with $e_{(k)}$ the error at the beginning of the (k) switching period.

$$i(t) = \begin{cases} i_1(t) = i_{(k)} + m_- t & if \quad 0 \le t < t_d \\ i_2(t) = i_{(k)} + m_- t_d + m_+(t - t_d) & if \quad t_d \le t < t_d + t_{on} \\ i_3(t) = i_{(k)} + m_- t_d + m_+ t_{on} + m_-(t - t_d - t_{on}) & if \quad t_d + t_{on} \le t \le T_{sw} \end{cases} \tag{3}$$

$$e(t) = \begin{cases} e_1(t) = e_{(k)} + (m_{ref(k)} - m_-)t & if \quad 0 \le t < t_d \\ e_2(t) = e_{(k)} - m_- t_d + m_{ref(k)}t - m_+(t - t_d) & if \quad t_d \le t < t_d + t_{on} \\ e_3(t) = e_{(k)} - m_- t_d - m_+ t_{on} + m_{ref(k)}t - m_-(t - t_d - t_{on}) & if \quad t_d + t_{on} \le t \le T_{sw} \end{cases} \tag{4}$$

The optimisation problem (1) can be solved by first computing the one-cycle integral error as (5).

$$\int_0^{T_{sw}} e(t)dt = \int_0^{t_d} e_1(t)dt + \int_{t_d}^{t_d + t_{on}} e_2(t)dt + \int_{t_d + t_{on}}^{T_{sw}} e_3(t)dt \tag{5}$$

The integral of the error when $S_z = S_{off}$ during the delay time t_d is:

$$\int_0^{t_d} e_1(t)dt = e_{(k)}t_d + \frac{(m_{ref(k)} - m_-)}{2} t_d^2 \tag{6}$$

The integral of the error when $S_z = S_{on}$ is during time interval t_{on} is:

$$\int_{t_d}^{t_d + t_{on}} e_2(t)dt = e_{(k)}t_{on} + (m_{ref(k)} - m_-)t_d t_{on} + \frac{(m_{ref(k)} - m_+)}{2} t_{on}^2 \tag{7}$$

Finally, the integral of the error when the switch is again OFF.

$$\begin{aligned} \int_{t_d + t_{on}}^{T_{sw}} e_3(t)dt = {} & \frac{2e_{(k)}T_{sw} + (m_{ref(k)} - m_-)T_{sw}^2}{2} - e_{(k)}t_d + (T_{sw}(m_- - m_+) \\ & - e_{(k)})t_{on} + (m_+ \\ & - m_{ref(k)})t_d t_{on} + \frac{(m_- - m_{ref(k)})}{2} t_d^2 + \left(\frac{2m_+ - m_- - m_{ref(k)}}{2}\right) t_{on}^2 \end{aligned} \tag{8}$$

Adding the three integrals yields the final expression:

$$\begin{aligned} \int_0^{T_{sw}} e(t)dt = {} & \frac{2e_{(k)}T_{sw} + (m_{ref(k)} - m_-)T_{sw}^2}{2} + T_{sw}(m_- - m_+)t_{on} + (m_+ \\ & - m_-)t_d t_{on} + \left(\frac{m_+ - m_-}{2}\right) t_{on}^2 \end{aligned} \tag{9}$$

The minimum value of the cost function achievable in the optimisation problem (1) is zero. Hence, equating the integral of the error as given by (9) yields the equation (10) that relates the delay time t_d with the ON time t_{on}. As a result, any pair of values (t_d, t_{on}) that solve equation (10) make the integral of the error equal to zero.

$$\frac{2e_{(k)}T_{sw} + (m_{ref(k)} - m_-)T_{sw}^2}{2} + T_{sw}(m_- - m_+)t_{on} + (m_+ - m_-)t_d t_{on} + \left(\frac{m_+ - m_-}{2}\right) t_{on}^2 = 0 \tag{10}$$

Furthermore, the optimisation problem (1) and (2) constrains the value of the SAPF current at the end of the cycle to be equal to the reference of the next cycle, that is $i_{(k+1)} = i_{ref(k+1)}$. The final value of the current, $i_{(k+1)}$, is a function of t_d and t_{on} given by:

$$i_{(k+1)} = i_{(k)} + m_{-}t_d + m_{+}t_{on} + m_{-}(T_{sw} - t_d - t_{on}) \tag{11}$$

where the terms depending on the delay time t_d cancel out, hence:

$$i_{(k+1)} = i_{(k)} + m_{+}t_{on} + m_{-}(T_{sw} - t_{on}) \tag{12}$$

As a result, when equating the value of $i_{(k+1)}$ to the current reference of the $(k+1)$ switching period, that is $i_{(k+1)} = i_{ref(k+1)}$, the optimal ON time t_{on}* is given by:

$$t_{on}^{*} = \frac{i_{ref(k+1)} - i_k - m_{-}T_{sw}}{m_{+} - m_{-}} \tag{13}$$

The optimal solution of minimization problem (1)-(2) is given by t_{on}^{*} as in (13) and by t_d^{*} solved from (10), that yields:

$$t_d^{*} = \frac{(m_{-} - m_{+})t_{on}^{*\,2} + 2T_{sw}(2(m_{+} - m_{-})t_{on}^{*} - 2e_{(k)}T_{sw} + (m_{-} - m_{ref(k)})T_{sw}^{2}}{2(m_{+} - m_{-})t_{on}^{*}} \tag{14}$$

In summary, the solution of the optimal problem (1)-(2) is given by t_{on}^{*} as in (13) and t_d^{*} as (14).

4. Controller algorithm

This section summarizes the generalized reference-based one-cycle current control algorithm. At the beginning of each switching cycle the SAPF phase current $(i_{(k)})$ is measured and the reference current $(i_{ref(k)})$ is computed from the load current measurements. The current error, as well as the reference $(m_{ref(k)})$ and SAPF phase current slopes (m_{+}, m_{-}) are then computed. The algorithm also requires the current reference value to be achieved at the end of the switching cycle. There are many feasible options to set the future reference $i_{ref(k+1)}$, and some are discussed in this section. Finally, the algorithm calculates the optimal delay and ON times to generate the switching function for the current switching cycle. The control algorithm is explained in detail through the flowchart depicted in Fig. 5.

4.1. Computation of $i_{ref(k+1)}$

The proposed algorithm enables selecting the current value to be achieved at the end of the switching cycle $i_{ref(k+1)}$. Thus, different approaches for how $i_{ref(k+1)}$ is chosen can be tested. Three approaches are compared below.

4.1.1. Buffer case (known reference)

The first assumption is that the next reference, $i_{ref(k+1)}$, is known, indicating that the system is in a steady state. In this case, it is possible to precompute and store the reference current values for a fundamental cycle in a buffer. By knowing the next reference value, the proposed algorithm ensures that the phase current reaches the next real reference value at the end of the switching cycle, as shown in Fig. 6. However, when dealing with dynamic loads and during transients, the references stored in the buffers become invalid. In such cases, once a new steady state is reached, new reference currents must be calculated and stored in the buffers. It is important to note that this implementation requires significantly more memory resources than the other approaches, but it reduces the computations during steady states. Because the references are known, this case is expected to provide the best current tracking performance.

4.1.2. Full-slope prediction case

The second approach is based on predicting the next reference current $(\widehat{i}_{ref(k+1)})$ using the slope of the reference current from the last switching cycle, as shown in Fig. 7, where $m_{ref(k-1)} = \frac{i_{ref(k)} - i_{ref(k-1)}}{T_{sw}}$ and $\widehat{i}_{ref(k+1)} = i_{ref(k)} + m_{ref(k-1)}T_{sw}$. At instant (k + 1), the real value of the reference current $(i_{ref(k+1)})$ is computed and a new prediction for the

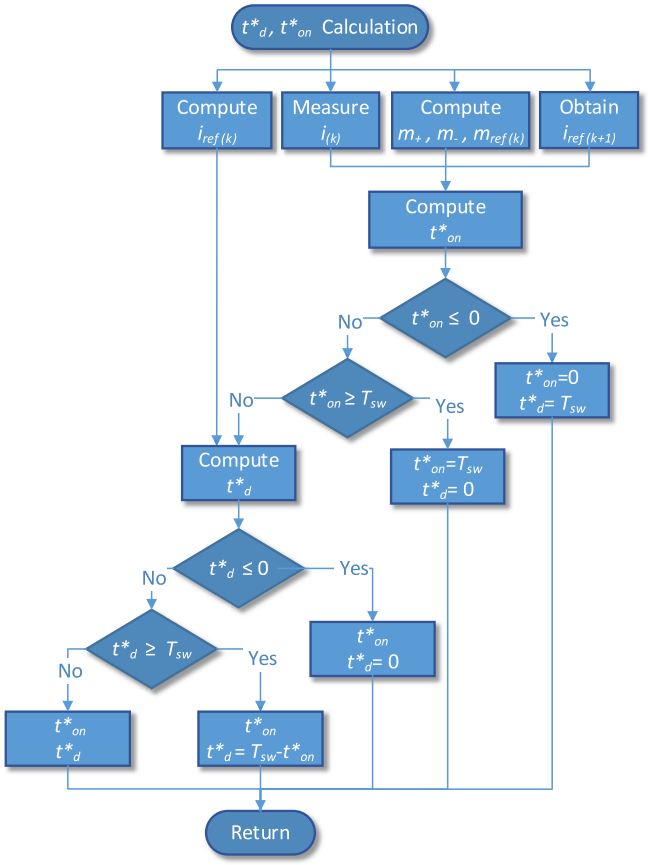


Fig. 5. GOCZIE current controller algorithm flowchart.

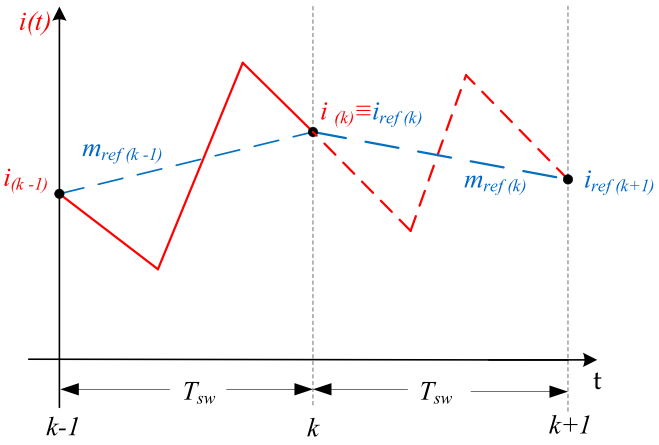


Fig. 6. Known reference value $i_{ref(k+1)}$ in steady state.

reference current is generated for the next switching cycle. In this approach, the current error at the end of the switching cycle depends on the deviation of the reference current slope from its actual value, which becomes more significant during rapid variations and even sudden changes in the slope's direction. The computational cost is higher than the buffered case; however, no buffers are needed, which saves memory resources and improves current tracking during transients.

4.1.3. Weighted-slope prediction case

Relying on the previous slope for prediction may lead to a significant tracking error, especially when dealing with fast-varying slopes or when a change in slope sign occurs. To prevent and reduce the magnitude of

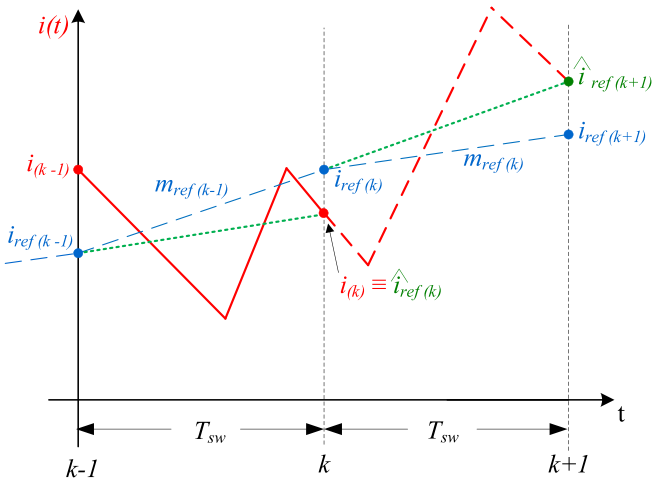


Fig. 7. Prediction of current reference value.$i_{ref(k+1)}$.

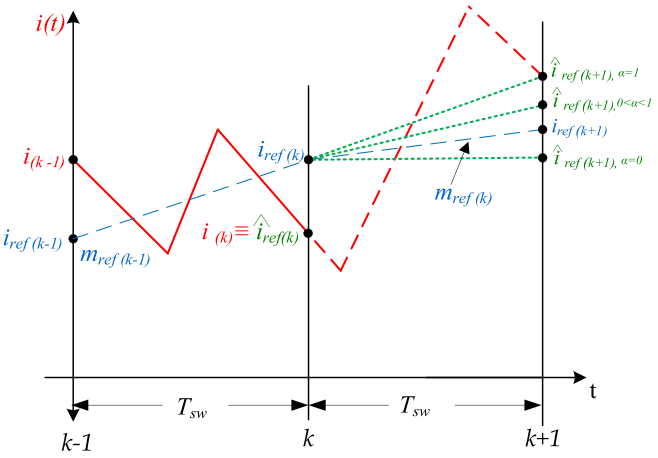


Fig. 8. Weighted-slope prediction of current reference value.$i_{ref(k+1)}$.

these errors, the slope can be weighted by a constant factor $0 \leq \alpha \leq 1$. When $\alpha = 0$, it implies a constant reference; $\alpha = 1$ corresponds to full-slope prediction, and any other value represents a conservative prediction of the next reference, as shown in Fig. 8. In this figure, the predicted values of the reference current are computed as $\hat{i}_{ref(k+1)}(\alpha) = i_{ref(k)} + \alpha m_{ref(k-1)} T_{sw}$. As the slope of the reference current changes, the optimal value of α varies for each switching cycle. In this work, the value of α will be kept constant during the experiments. In Section 5, the effect on current tracking will be analysed by comparing the results obtained for the proposed case study with different values of α. However, it is possible to recalculate α cycle by cycle, considering, for example, the slope tendency (by analysing the last switching cycles). This possibility could be considered in future research.

5. Simulation results

A simulation setup has been developed in Matlab/Simulink®. To ensure a fair comparison with previous proposals, the same power stage and load used in [32] are employed here. Fig. 9 illustrates the SAPF system under simulation where a three-phase three-leg four-wire voltage source inverter (VSI) and a three-phase inefficient load are connected to the ac supply at the PCC. The control system is represented by the block named digital controller, implementing the main control functions as detailed in Fig. 10. The major system characteristics and simulation settings are presented below:

- Three phase ac source: 120 $V_{(RMS)}$/50 Hz symmetrical supply voltages (v_{a_s}, v_{b_s}, v_{c_s}).
- VSI (dc side): 490 V (245 V + 245 V) split dc bus with central point neutral connection. $C_1 = C_2 = 4.7$ mF.
- VSI (ac side): ac output inductances $L_z = 3$ mH; with internal resistances: $r_{Lz} = 0.1\ \Omega$
- Load: diode-based three-phase rectifier with series L-R load. $L_r = 6$ mH; $R_r = 27\ \Omega$.
- VSI switching frequency $f_{sw} = 20$ kHz.
- Simulation: step-size = 0.1 μs; solver: ode15s; simulation time = 100 ms; SAPF connection at t = 55 ms.

The load currents are shown in Fig. 11 (top), while the per-phase harmonic spectrum is presented in Fig. 11 (bottom). This load requires phase-shifted and non-linear, but balanced, currents from the PCC, showing a total harmonic distortion of $THD_i = 28.6\,\%$ and a power factor of $PF = 0.958$. The power filter is assumed to have enough power to achieve a global correction of the inefficient phenomena upstream from the PCC. The reference currents ($i_{z\_ref(k)}$) calculation is presented in Fig. 10. The currents are obtained by subtracting from every load current ($i_{z\_load(k)}$) its respective positive-sequence fundamental active component ($i_{z1(k)}^{+a}$) and, adding the dc bus voltage compensating term ($i_{z1\_dc(k)}$). To obtain these components with every new sample, a fundamental positive-sequence synchronous PLL (SPLL) and a recursive discrete Fourier transform (RDFT) are used. Sampling frequency is set to 20 kHz, matching the switching frequency, therefore, a new reference

current value is obtained at the beginning of every switching cycle. The SAPF output currents for global compensation are shown in Fig. 12. By using these reference currents, the SAPF can reduce the phase shift and the current distortion upstream from the PCC to near-zero values.

As indicated previously, the proposed current controller algorithm enables achieving zero integral error in a switching cycle while also reaching a desired phase-current value at the end of that cycle. To set this final value, three approaches were proposed in Section 4.1. Several simulations have been carried out to obtain a performance comparison between them. The following are the cases under analysis:

- Buffer case: the next value of the reference current is known. Reference values through the entire fundamental cycle are stored in buffers (400 values by phase at 20 kHz sampling frequency).
- Full-slope prediction case: the next reference current is predicted cycle by cycle using the slope. Only the last reference current value must be stored to compute the slope in the next cycle.
- Weighted-slope prediction case: the next reference current is predicted cycle by cycle using a weighting factor over the slope.

Note that this last case also implies evaluating the effect of the weighting factor α.

5.1. Current tracking performance comparison

The current tracking of SAPF phase-a using the proposed controller with buffered reference currents (Buffer case) is shown in Fig. 13. The load is in steady state and so reference currents can be stored in buffers leading to the ideal control situation of knowing the future references. This case is supposed to offer the best tracking performance and it will be taken as reference for comparison. Current tracking starts at time t = 0.04 s, while reference currents for compensation are generated from t = 0.055 s. A detail of the current tracking and its corresponding phase current error are shown in Fig. 14 and Fig. 15 respectively. The zone detailed clearly reveals the tracking performance for the steepest slope in the reference current (from t = 0.0684 s to t = 0.0687 s) and after the abrupt slope sign change occurred at t = 0.0687 s. The main objectives of the proposed controller are to achieve zero-integral current error, minimum settling time, and a desired current value at the end of the switching period. Phase current error shows a ripple centered around 0 that demonstrates the excellent current tracking performed by the proposed zero-integral error controller. After the slope sign change, the algorithm enables reaching the reference in one cycle with minimum settling time and tracking error. As expected, knowing the next value of the reference current enables the proposed algorithm to perform perfect current tracking.

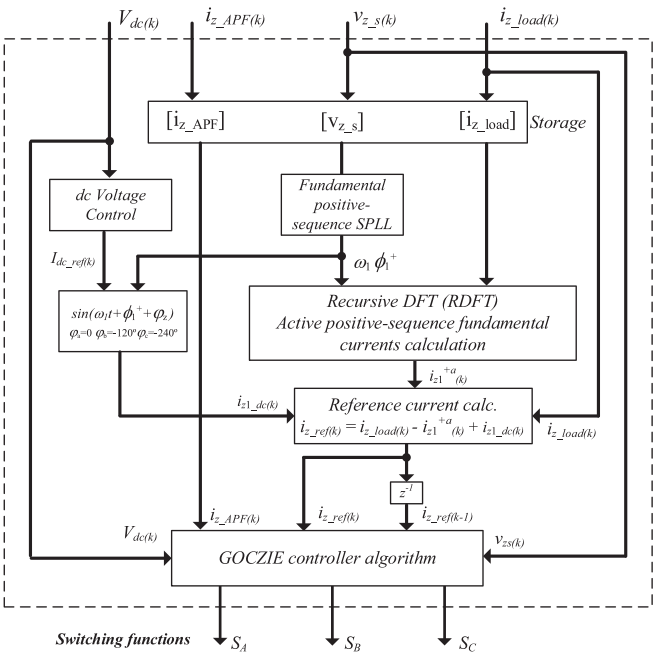


Fig. 10. Detailed block diagram of the digital controller main functions.

To compare the results obtained for the cases under analysis, Fig. 16 shows the phase-a tracking current comparison between the buffer case and the full-slope case. The phase current obtained with the full-slope prediction perfectly tracks the reference with a quite similar performance to that obtained for the buffer case, until the reference slope sign changes at t = 0.0687 s. As can be observed from the detail presented in Fig. 17, the full-slope prediction fails when the slope sign change occurs. The heavy slope in the reference before the slope sign change is the cause of the error in the first prediction. Logically, the steeper the previous slope, the greater the prediction error. As observed, the second prediction is quite accurate because the considered slope is close to the new slope of the reference current.

Weighting the slope used in the prediction will help to reduce this error. Fig. 18 shows the phase-a current error obtained for: buffered case

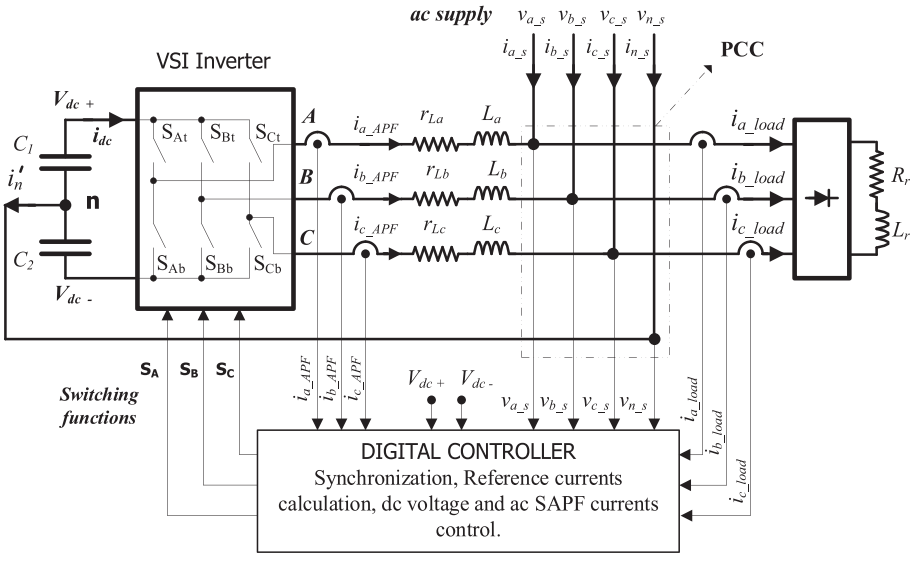


Fig. 9. Block diagram of the power system under consideration.

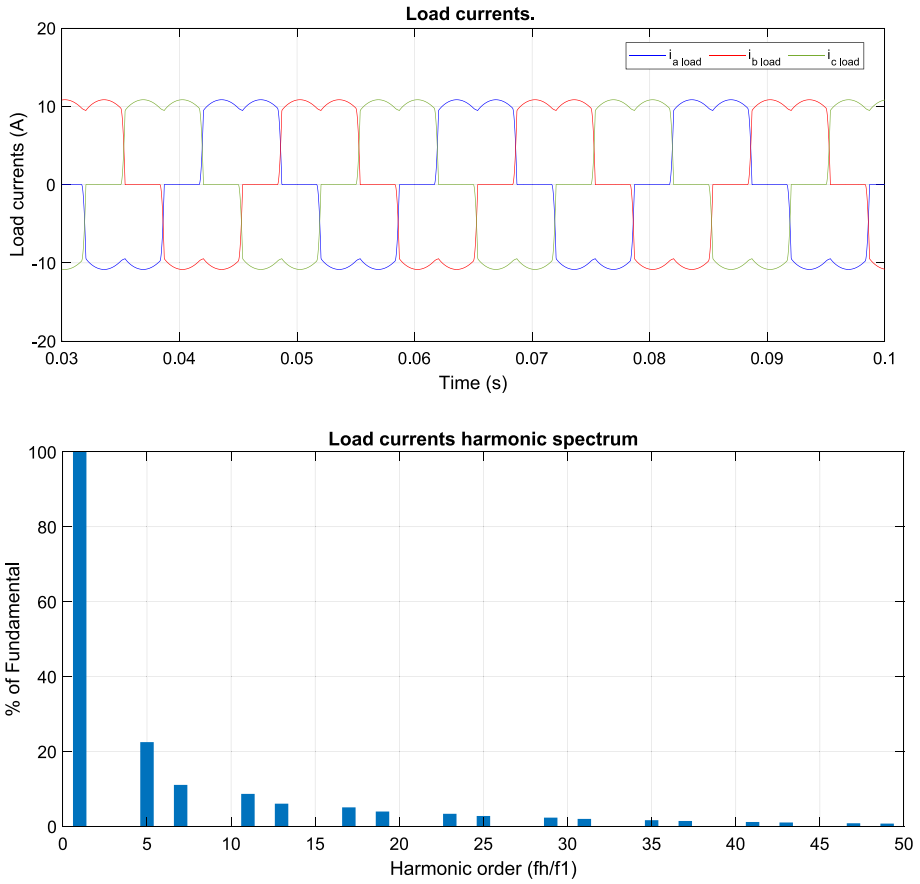


Fig. 11. Load current waveforms (top). Per-phase load currents harmonic spectrum (bottom), $THD_i = 28.6$ %.

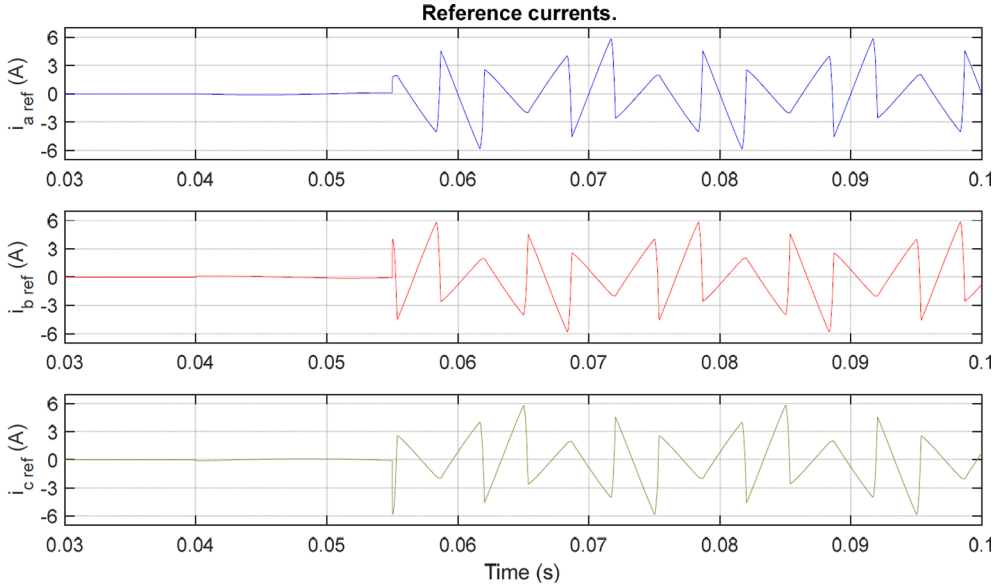


Fig. 12. SAPF compensating/reference currents waveforms. Compensation starts at t = 0.55 s.

(green); full-slope case (red); weighted-slope with $\alpha = 0.75$ (blue); weighted-slope with $\alpha = 0.5$ (magenta); and constant reference $\alpha = 0$ (orange).

It can be observed that while the reference slope is low (until t = 0.0684 s) the current tracking is quite similar in all cases and matches the performance obtained with the buffer case. However, as the reference negative slope increases during $\Delta t1$ in Fig. 16 (from t = 0.0684 s to t = 0.0687 s) the effect of reducing the slope weighting factor to predict the final current value of the switching cycle leads to an increasing error in current tracking. Comparing these errors with the ideal situation of knowing the next reference current, the use of the full-slope prediction offers the best behaviour and is very close to the ideal. In contrast, when the reference is kept constant during the switching cycle, the current tracking shows the worst behaviour for the cases analysed. As expected,

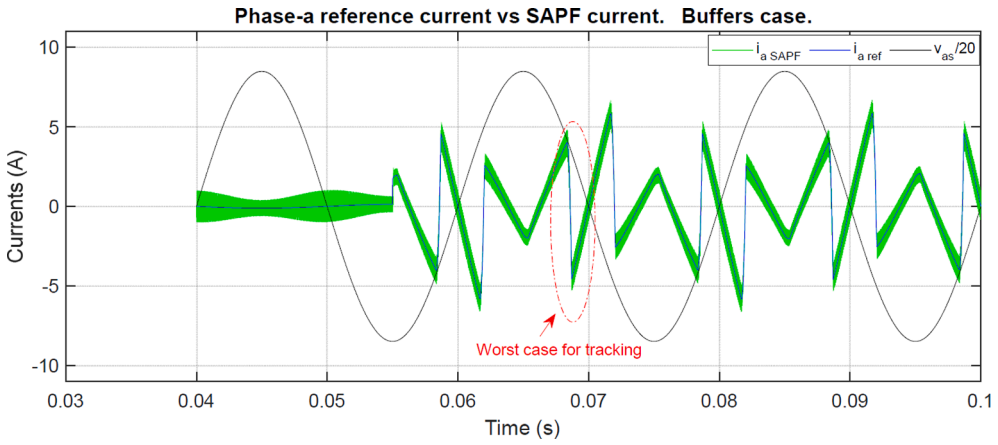


Fig. 13. Current tracking of phase-a.

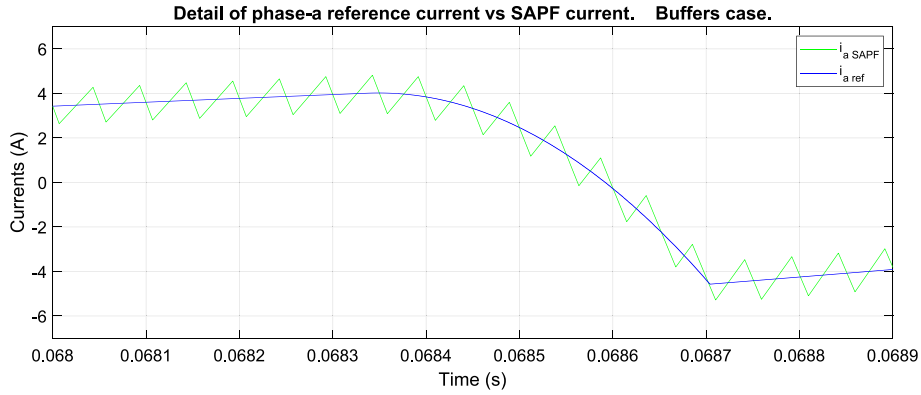


Fig. 14. Detail of the current tracking of phase-a.

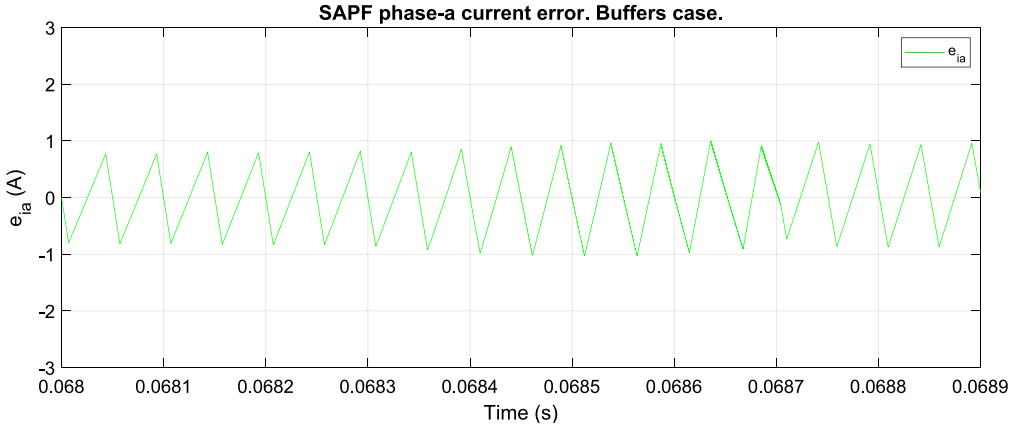


Fig. 15. Detail of the current error of phase-a.

when the slope sign changes at t = 0.0687 s, weighted-slope predictions help to reduce the absolute maximum error and enable faster settling times. However, even when the full-slope prediction is used, the proposed controller enables catching the reference in less than two switching cycles Δt2 (100 μs).

The simulated results demonstrate that the current tracking is always stable and matches the reference in a minimum time. This is a considerable improvement on previous versions of the algorithm. However, depending on the reference current shape, the optimum weighting factor may be different. To evaluate the best weighting factor value for the reference currents analysed in this work, a supply current THD_i comparison has been performed. Figs. 19, 20, and 21 show the resulting supply current waveforms obtained for global compensation when the algorithm uses buffers, full-slope prediction, and $\alpha = 0.8925$ weighted-slope prediction, respectively. Figs. 22, 23, and 24 show details of these currents where slight differences can be seen at the moments corresponding to the abrupt slope sign changes in the reference current. Table 1 summarizes the results obtained for different weighting factors, as well as for the buffer case simulation. Furthermore, the results obtained are compared with previous versions of the controller algorithm.

Firstly, it can be noted that THD_i significatively improves with the use of the proposed control compared with the previous algorithm

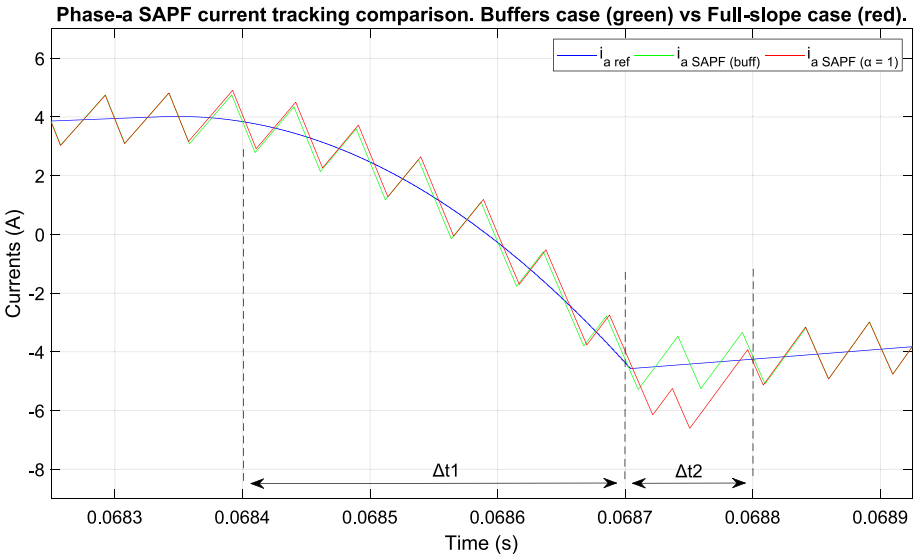


Fig. 16. Current tracking of phase-a comparison. Buffer case (green) vs. full-slope case (red). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

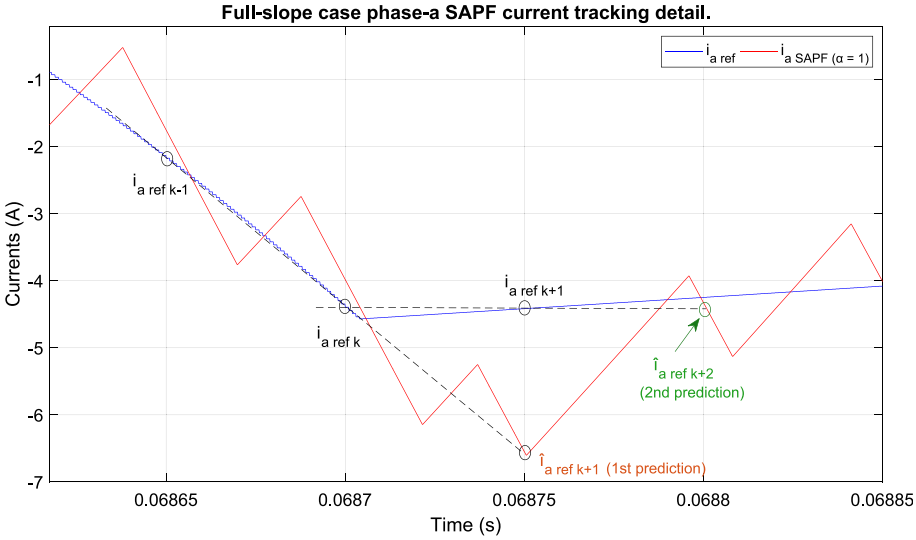


Fig. 17. Full-slope tracking when reference sign change.

proposals. Weighting factor values above $\alpha = 0.7$ lead to THD_i values under 1 %. This means an improvement of 234 % when comparing the $THD_{i(50)}$ (first 50 harmonics considered) obtained for the symmetrical commutation pattern (a = 0.9) [32] with the value obtained with the proposed algorithm using $\alpha = 0.7$ weighted slope to compute the next reference.

The best case is obtained for a weighting factor of 89.25 %, where the improvement increases to 279 %. Furthermore, if $THD_{i(25)}$ is considered, the best improvement reaches 400 % (1.86 % vs 0.466 %). As expected, the buffer case simulation obtains the best THD_i performance and achieves outstanding values of 0.34 % and 0.31 %. Nevertheless, the THD_i values obtained for supply currents are good enough when the slope-based prediction is used to obtain the final value of the current. THD_i values of under 1 % are better than those that can be obtained by most controllers. As indicated previously, the optimal value for the weighting factor is dependent on the reference current shape; however, differences are minimal when comparing values obtained for the simulated weighting factors. Obtaining the optimal weighting factor is not trivial and requires an adequate analysis of the reference currents. Furthermore, considering that load currents can vary over time, and with them, the reference currents, calculating the optimal weighting factor is not feasible for real-time compensation. Moreover, when considering that the improvement obtained in terms of THD_i and PF is insignificant, it can be concluded that applying a weighting factor to the slope is unnecessary and the full-slope prediction is the best option.

5.2. Transient analysis performance comparison

A step change in the load has been forced to test the behaviour of the proposed system in a transient situation. Load currents are presented in Fig. 25. The reference current generation uses a recursive DFT algorithm. This method has the advantage that the reference currents can be computed with every new sample of the load currents. This enables soft responses during transients. The final reference currents will be obtained after a complete cycle of the new steady state of the load currents. However, when a buffered controller is used, the stored reference currents are no longer valid and produce a complete cycle of erratic compensation as can be seen in Fig. 26. This behaviour is not desirable

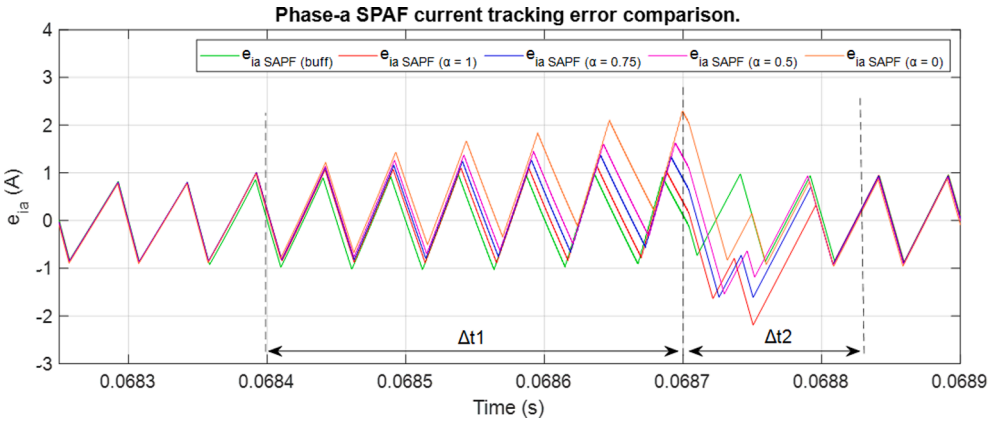


Fig. 18. Phase-a current error for: buffer case (green), full-slope case (red), weighted-slope case with $\alpha = 0.75$ (blue), weighted-slope with $\alpha = 0.5$ (magenta) and constant reference with $\alpha = 0$ (orange). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

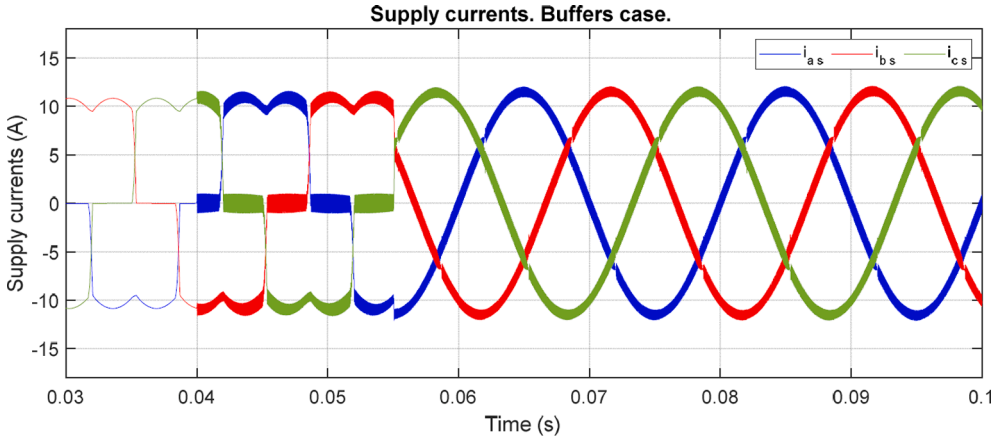


Fig. 19. Supply currents for buffer case.

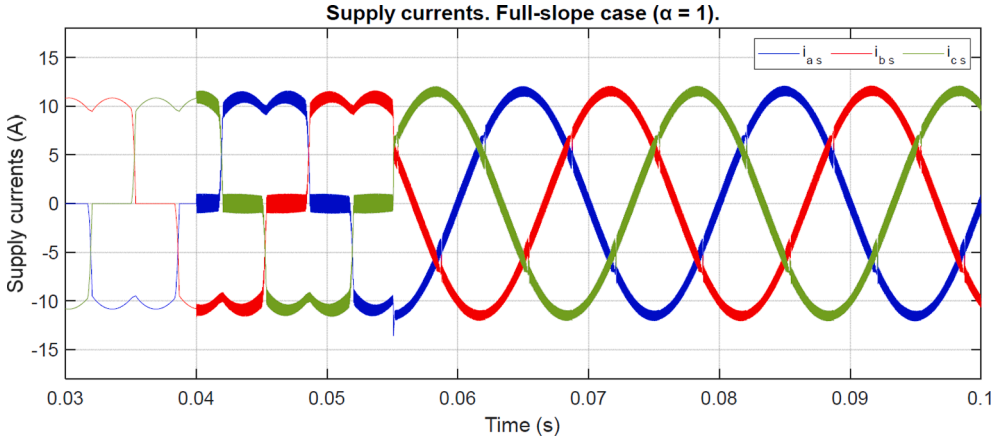


Fig. 20. Supply currents to full-slope case.

because it may cause a fault in the system. Following that cycle, a soft transition towards the new steady state is shown. These values have been computed and stored in the buffers one by one during the last cycle. The response obtained during the transient is delayed one supply cycle. Although the use of buffers provides the best results in tracking the reference current in a steady state, this method requires considerable memory and has been shown to produce problems during transients in systems with variable loads.

Fig. 27 show the results obtained for the same situation but when a slope-based prediction (non-buffered) is used (full-slope in this case). It can be observed how no erratic compensation cycle is produced. The supply current changes softly to the new steady state ones. The correct compensation is achieved just after a supply cycle in steady state. This is a great advantage of non-buffered solutions and combined with the minimum resources required and the small difference in the THD_i value, makes the full-slope solution the most suitable for implementing the algorithm.

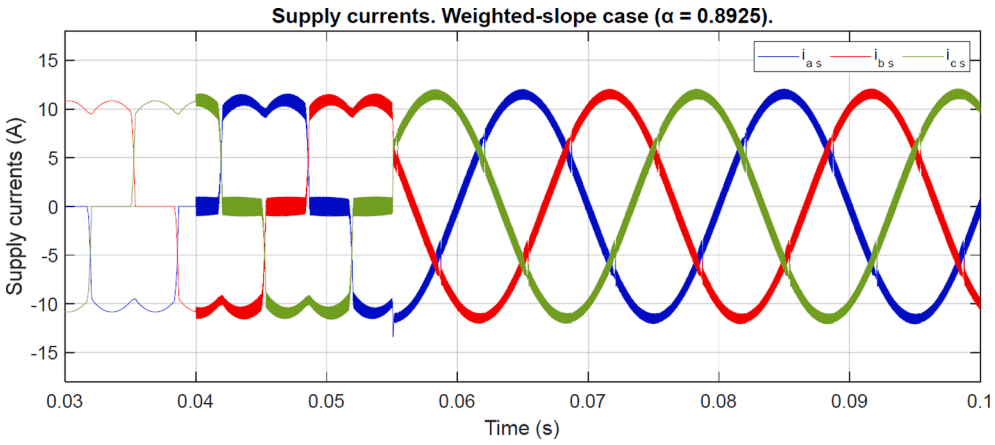


Fig. 21. Supply currents to slope weighting factor $\alpha = 0.8925$.

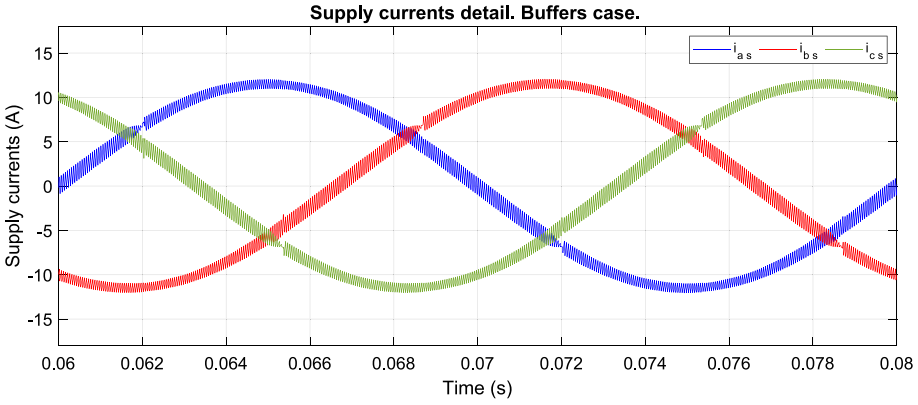


Fig. 22. Detail of supply currents to buffer case.

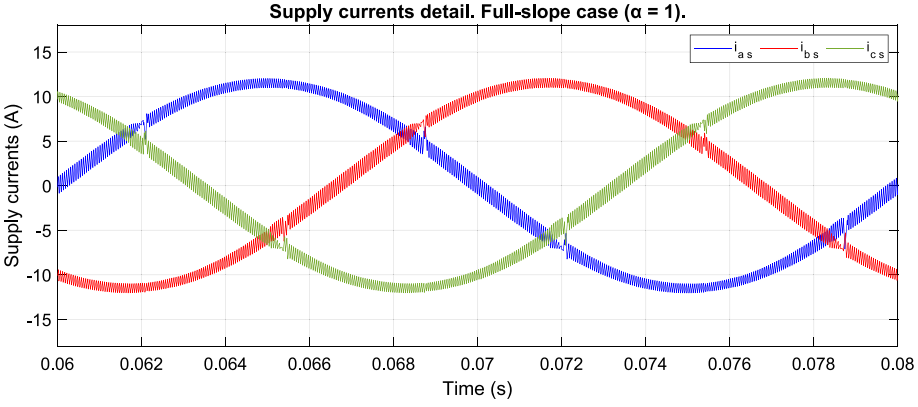


Fig. 23. Detail of supply currents to full-slope case.

6. Experimental results

The SAPF prototype shown in Fig. 28 is the same as the one used in [32]. SAPF was implemented using a Toshiba PM75CG1B120 (75 A, 1200 V) three-phase power stage switching at 20 kHz. The complete scheme of the unit is shown in the block diagram of Fig. 29. The SAPF component values (DC bus capacitors and phase inductances), as well as the load components, are the same as those presented for the simulation example in Section 5. A Pacific Power A-360MX three-phase power supply generates the 120 V RMS supply voltages. The split DC bus is controlled in two ways to provide a total voltage of $V_{dc} = 490$V and to maintain a balanced voltage distribution between the capacitors [1]. Measurements on this part, as well as the presented voltage and current waveforms, have been obtained using a LeCroy WaveJet 324 oscilloscope (200 MHz-2 GS/s).

The proposed control requires precise sampling and high-speed computing to calculate the reference currents as well as the commutation times t_d and t_{on} of the next switching period (as shown in Fig. 4). Up to six AMC1303E2520 sigma-delta modulators are used to obtain 40 high-precision samples per switching cycle. A Texas Instruments dual-core DSC model TMS320F28379D featuring 800 MIPS is used to implement the proposed control.

As demonstrated in the simulation section, the full-slope prediction is the best option for obtaining the next reference current for the proposed

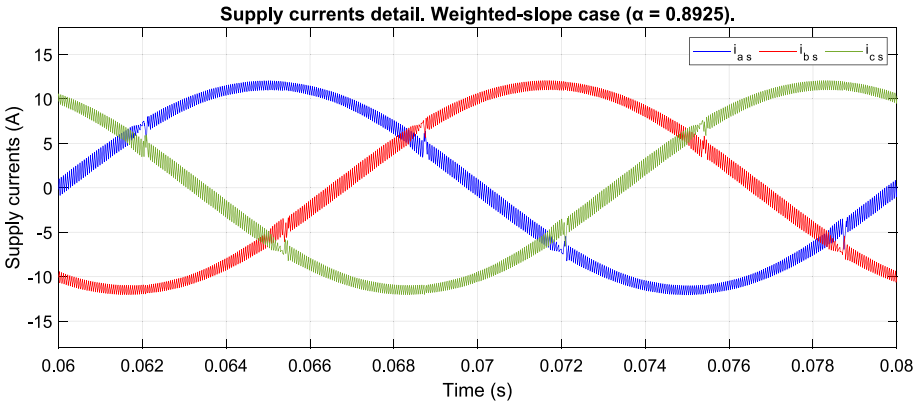


Fig. 24. Detail of supply currents to slope weighting factor α = 0.8925.

Table 1
Results obtained for different weighting factors as well as for the buffered simulation.

Pattern	Two-degrees of freedom						Symmetrical			Alternating
Next Reference	Buffered	Weighted-slope prediction					Constant			Constant
α	–	0	0.5	0.7	0.89	1	–			–
a	–	–	–	–	–	–	0.4	0.75	0.9	–
$THD_{i(50)}$ (%)	0.34	2.80	1.38	0.97	0.81	0.87	3.09	2.48	2.27	2.48
$THD_{i(25)}$ (%)	0.31	2.29	1.10	0.71	0.46	0.47	2.55	2.04	1.86	2.02
PF	0.99860	0.99807	0.99842	0.99846	0.99846	0.99845	0.99805	0.99821	0.99820	0.99820

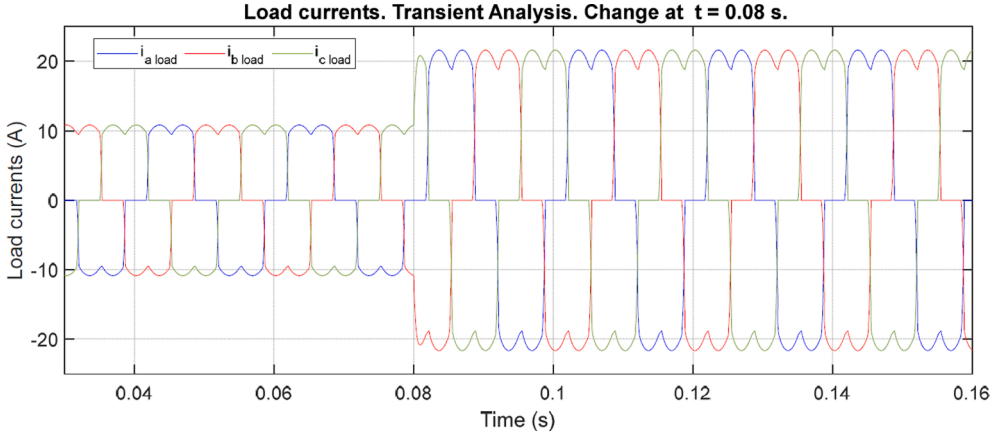


Fig. 25. Load currents to transient analysis at t = 0.08 s.

control, even more so when it is considered that the slight improvements obtained with the weighted-slope predictions will be blurred by the inaccuracies of a real implementation. For this reason, the results presented below have been obtained for the full-slope prediction case.

Supply voltages and load currents are shown in Fig. 30-a and Fig. 30-b respectively. Load current waveforms and rms values match with those presented in the simulated case (Fig. 10). The compensating currents delivered by the SAPF are presented in Fig. 31-a and details for phase-a current are presented in Fig. 31-b, Fig. 32-a, and Fig. 32-b. These detailed waveforms, especially Fig. 32-b, demonstrate excellent current tracking as the control achieves the reference in one switching cycle as expected after a reference sign change. The supply current waveforms obtained during compensation are shown in Fig. 33. Supply currents become a set of balanced sinusoidal currents. The small surges remaining in the waveforms are due to the normal error produced when tracking sudden slope changes in the reference currents. The $THD_{i(50)}$ value of the supply currents has been computed using the PTC Mathcad® software, using 65,536 samples out of the 200 k samples per cycle captured by the oscilloscope. The value obtained is 1.91 %, that is a 36.5 % better than the value obtained in [32] ($THD_{i(50)}$ = 3.01 %) and *PF* reaches a value of 0.995. A slight increment in the current THD_i value compared with the value obtained in the simulation can be observed. This is caused by the non-ideal characteristics of the semiconductors and the tolerances of the passive components used in the experimental setup.

Finally, a step change in the load currents has been introduced to evaluate the behaviour of the experimental set-up in a transient situation. Load currents are illustrated in Fig. 34-a, while Fig. 34-b depicts the smooth transition of grid currents during the time required to reach the new steady-state. As anticipated, a complete cycle of the new steady-state load currents is necessary to attain the correct new reference currents. However, a slight increase in the source currents can be observed after the end of the first fundamental cycle. During this cycle, the compensating currents of the SAPF increase, leading to an increase in the power stage losses and causing a dc voltage discharge that must be compensated. The slow dc bus voltage control loop increases the supply fundamental currents to maintain the dc voltage at its reference value. The obtained results validate the simulated ones in Fig. 27, showing the effectiveness of the proposed implementation.

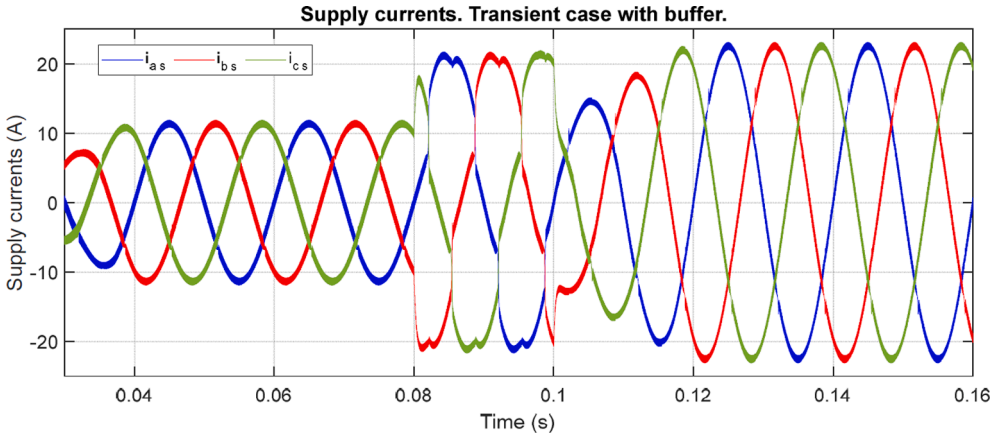


Fig. 26. Supply currents to transient analysis with buffer case.

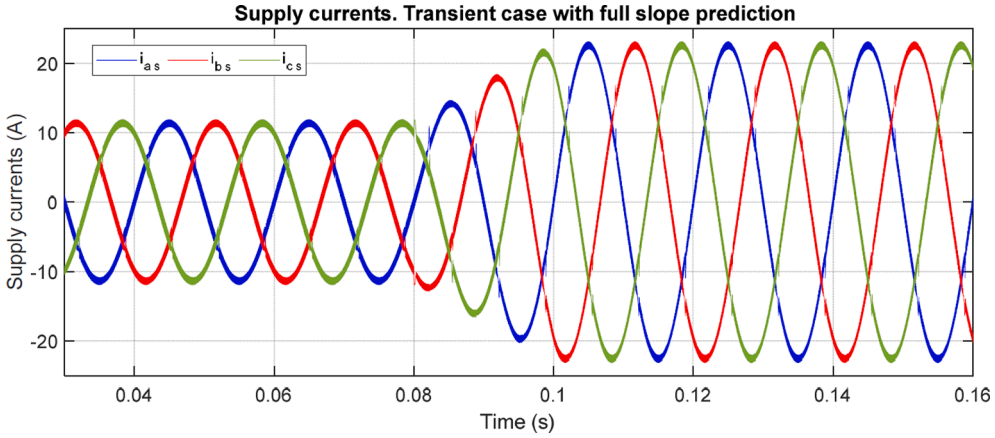


Fig. 27. Supply currents to transient with full-slope case.

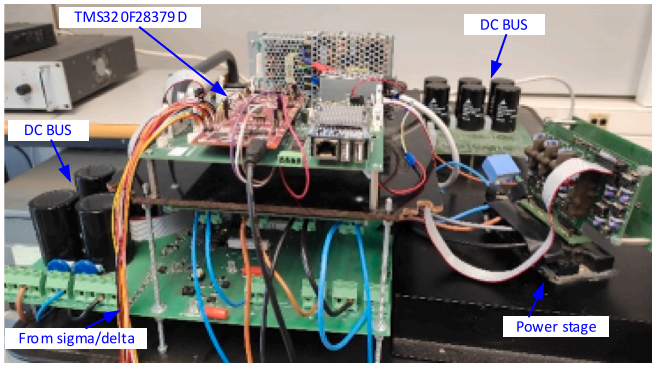


Fig. 28. Experimental setup [32].

7. Conclusions

In this work, a generalized reference-based one-cycle current controller for shunt active power filters has been proposed and analysed. A two degrees of freedom optimal control problem has been stated and solved, leading to an improved current control algorithm. The proposed controller enables different strategies to establish the final current that will be reached at the end of a switching cycle (which is also discussed). The results of the simulations with a set of three balanced reactive and distorted load currents show that the proposed controller achieves stable current tracking with minimum settling time and accurately reaches the reference in one switching cycle. The comparison between different cases, including the use of buffered reference currents and different weighted-slope predictions, shows minimal differences in terms of power quality improvement indices THD_i and *PF*. Deriving the ideal weighting factor necessitates a comprehensive analysis of reference currents. Fluctuating load currents make real-time calculation of the optimal factor unviable. While buffers work well for stable tracking, they strain memory and encounter problems during load variations. Therefore, it is concluded that full-slope prediction offers the best trade-off in terms of computational cost, memory saving, and power quality improvement. Simulations demonstrate that the total harmonic distortion of the supply current significantly improves with the proposed controller, with THD_i values under 1 % achieved for certain weighting factor values. The experimental results also demonstrate excellent tracking performance, with a high-power factor and significantly low THD_i values compared to previous algorithms. This results in a set of balanced sinusoidal currents flowing through the power network and carrying only the useful power load and thereby increasing the energy efficiency of the electrical power system.

It is possible to find in the literature recent works dealing with the current control problem in SAPFs. For the same or similar load and reference currents, some merit factors can be compared such as source currents THD_i, power factor, stability, bandwidth, and settling time after a step change in the reference. In this way, the THD_i value obtained with the proposed controller for the first 50th harmonic component is 1.9 %. This result is 36.55 % better than the previous approach in [32] and much better than most of the works found in the literature. *PF* achieves near unity value, and settling time is less than two switching cycles for fast varying reference currents (fast when compared with other

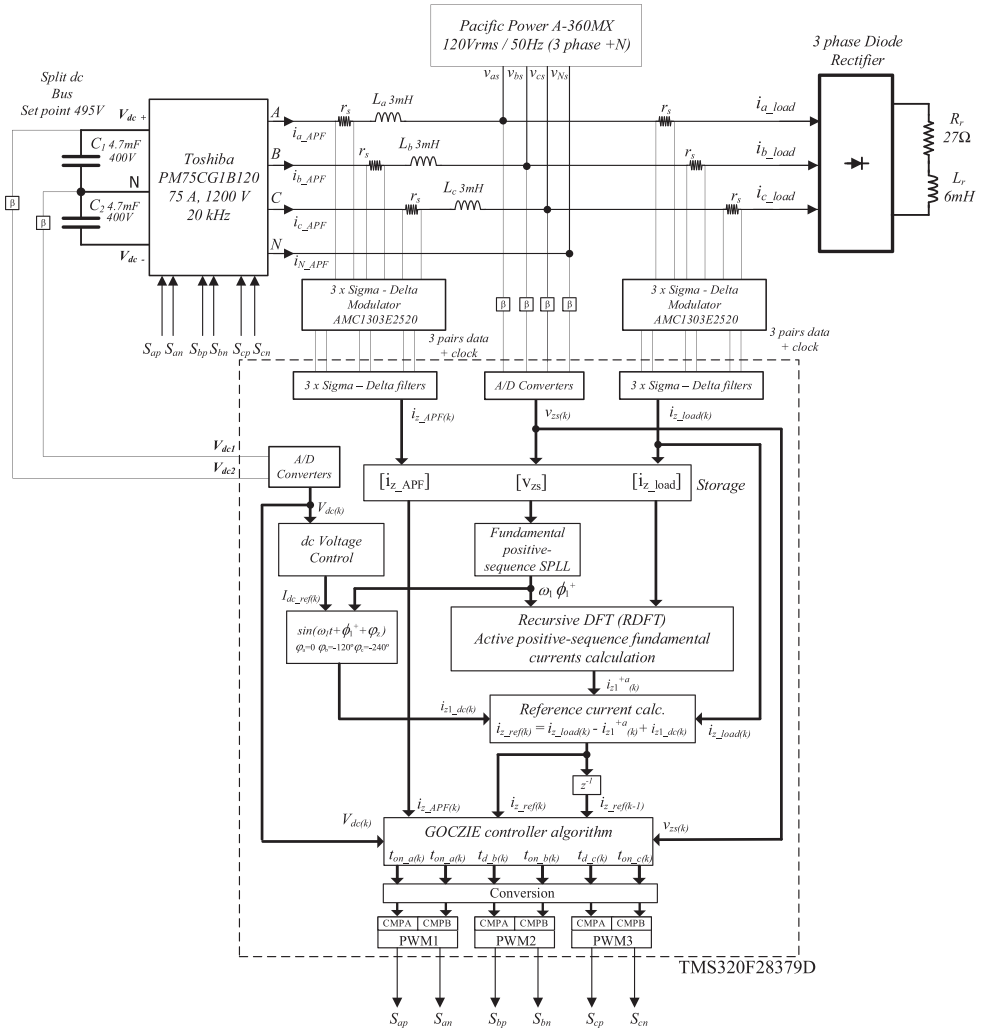
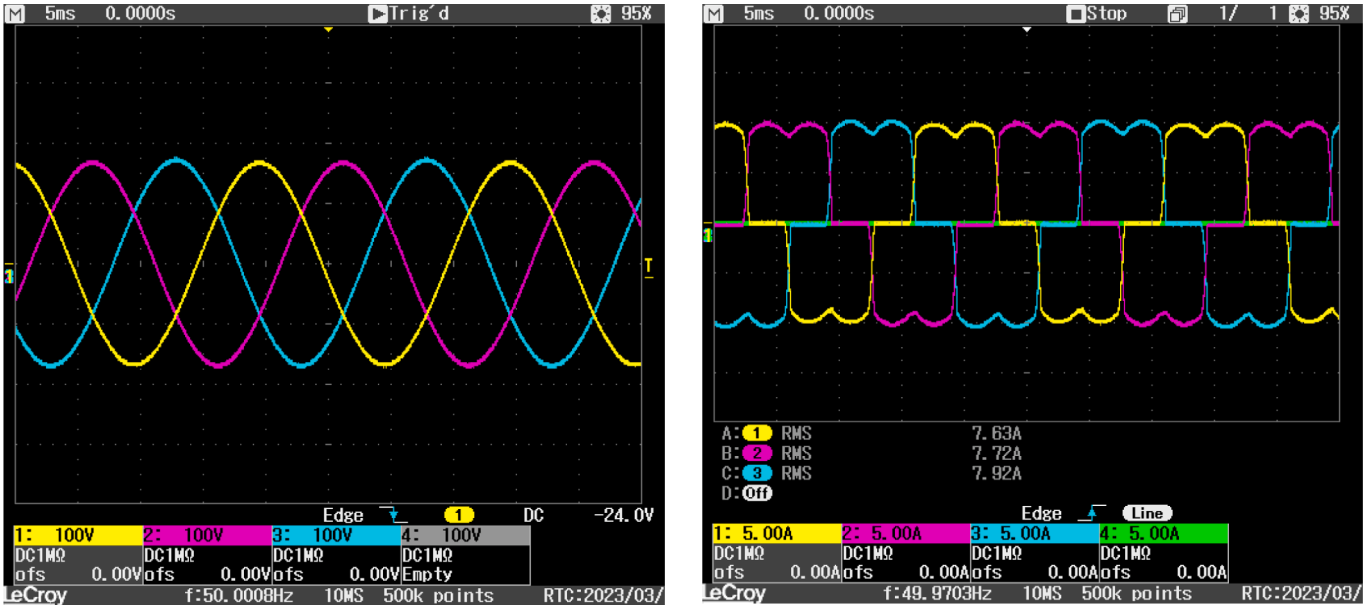
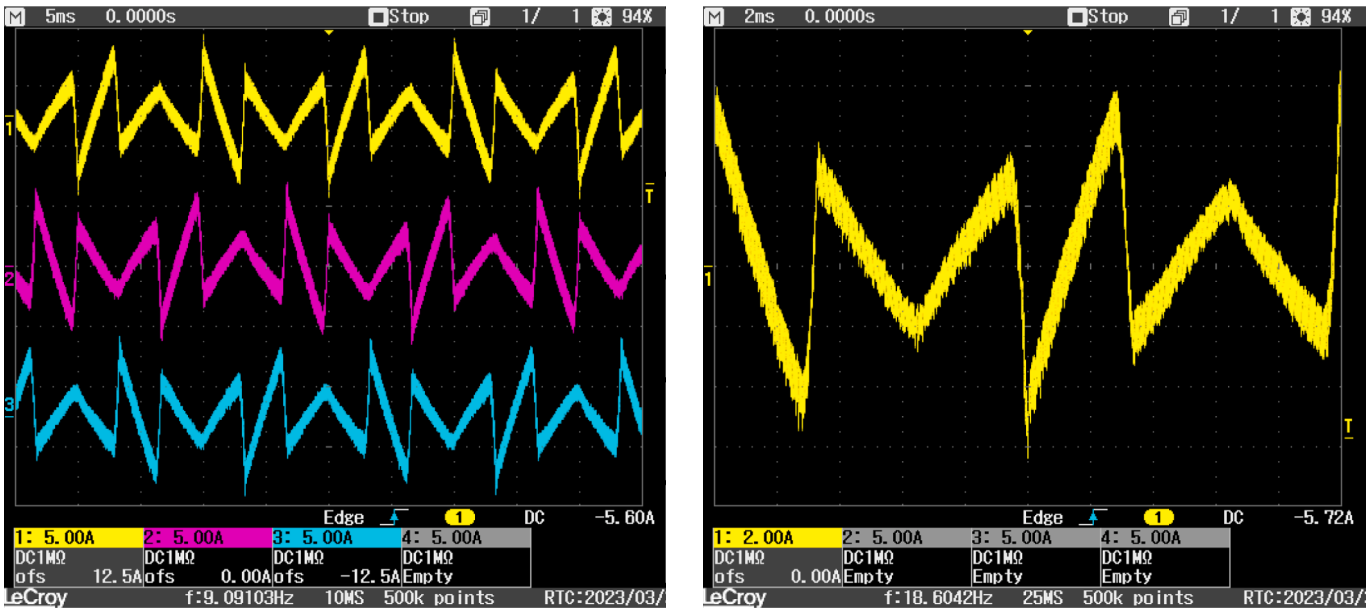


Fig. 29. Experimental setup complete block diagram.



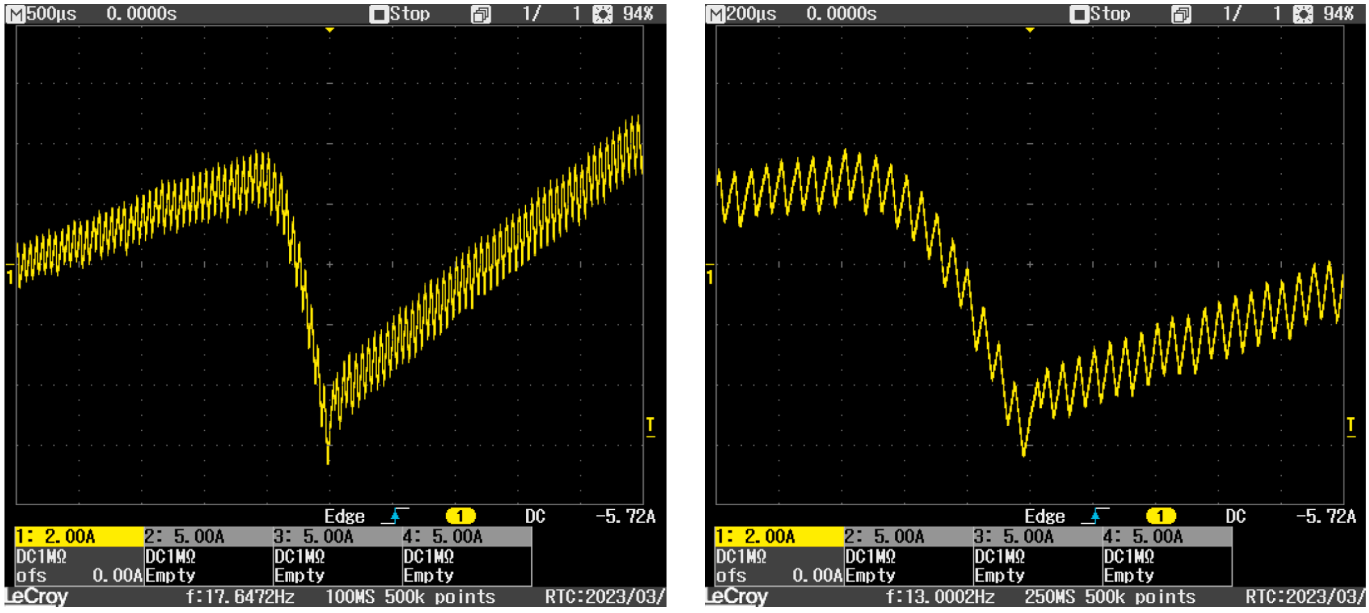
(a) (b)

Fig. 30. Supply voltages (a) and load current waveforms (b).



(a) (b)

Fig. 31. SAPF phase current waveforms (a) and phase-a detail at 2 ms/div (b).



(a) (b)

Fig. 32. Details of SAPF phase-a current waveform at 500 µs/div (a) and 200 µs/div (b).

controllers). However, when a change occurs in the load or source voltages and after the new steady state has been reached, the reference current generator generates the proper reference currents in one fundamental cycle. In this case, the use of a recursive DFT algorithm enables a soft transition to the new steady state. Other controllers like PFC or the classical implementation of OCC do not need to wait a fundamental cycle; however, these are different approaches and difficult to compare. In terms of implementation, the proposed controller needs considerable computational effort and a fast DSP to carry out all the computations, as well as six high-speed sigma/delta modulators to acquire the current measurements. The proposed implementation could be further improved with the use of an LCL filter for the SAPF grid connection. Future research will focus on calculating the optimal weighting factor considering the slope tendency.

8. Author statement

All authors have seen and approved the final version of the submitted manuscript.

CRediT authorship contribution statement

S. Orts-Grau: Conceptualization, Investigation, Methodology, Supervision, Validation, Visualization, Writing – original draft, Writing –

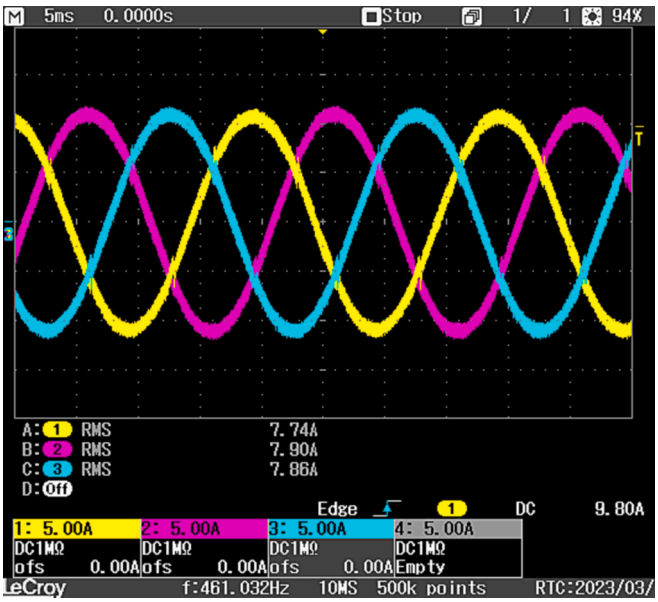
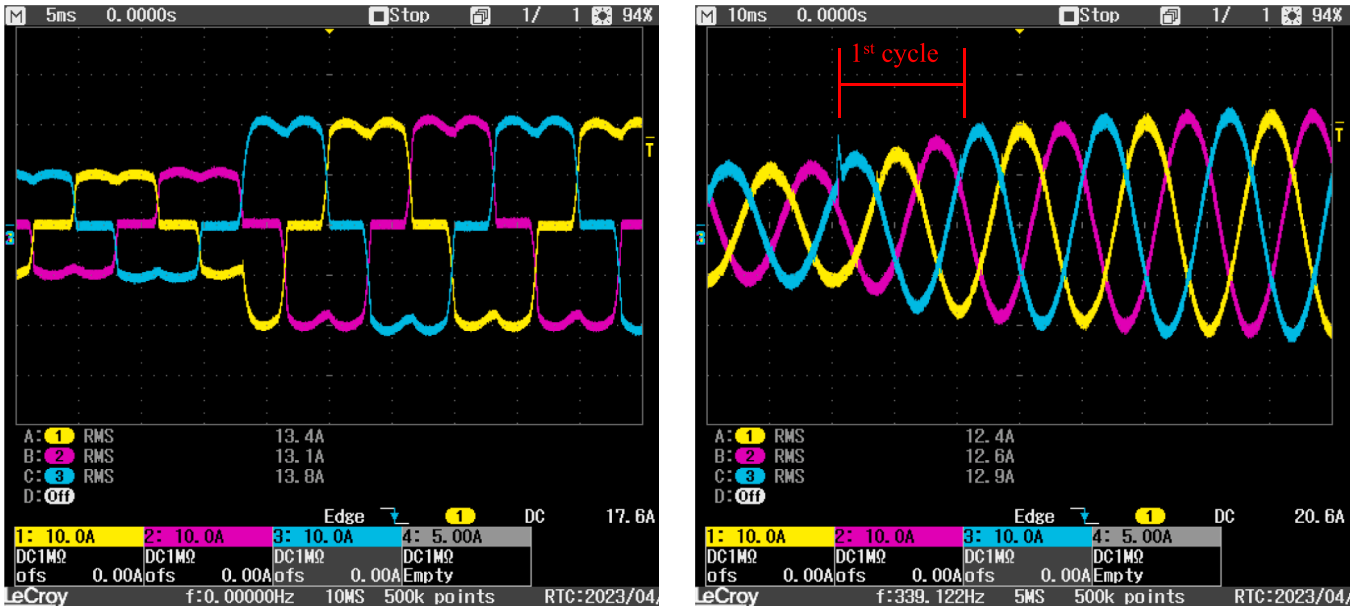


Fig. 33. Supply currents during SAPF compensation.



(a) (b)

Fig. 34. Transient behaviour experiment. Load currents step (a) and supply currents evolution (b).

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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