2022 International Seminar on Intelligent Technology and Its Applications (ISITIA)

Phase Disposition PWM for Three Phase Nine-Level Diode Clamped Inverter

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2022 International Seminar on Intelligent Technology and Its Applications (ISITIA) | 978-1-6654-6081-1/22/$31.00 ©2022 IEEE | DOI: 10.1109/ISITIA56226.2022.9855325

***Abstract*—This paper describes a nine-level three-phase diode clamp inverter. The existing power grid requires good performance especially low Total Harmonic Distortion (THD). In addition, developments have also occurred in the number of inverter levels which reach nine levels. To control the switching, phase disposition pulse width modulation is equipped. A filter that combines resistor and inductor is needed to get better THD. The simulation in MATLAB/Simulink has been used to verify. The response generated by the system shows good performance and low THD.**

Keywords—Nine-level Diode Clamped Inverter, Total Harmonic Distortion, Phase Disposition PWM.

I. INTRODUCTION

The development of renewable energy as a source of electricity generation is growing rapidly. Indonesia itself has a renewable energy mix target of 23% by 2030 [1]. To integrate these various renewable energy sources, distributed generation is developed as a system of microgrids [2]. The use of network-connected power converters is an important part. One of them is a three-phase inverter which plays an important role in a wider system [3].

Multilevel inverter applications are diverse and have a major influence on the development of the field of electrical engineering. Multilevel inverters can produce more than two levels of voltage. And can be applied up to a very large power. At present, its application is widely used in medium and high voltage.

The use of multilevel inverters has now become a solution for connecting renewable energy sources to the network [4], both single-phase systems [5], [6] and three-phase[7],[8]. The number of levels used has varied and is increasing, ranging from five[5], seven[8], to nine[6]. The more the levels, the less the harmonic content, and the sinusoidal output voltage will be of quality

Generally, Multilevel inverters are of three types: capacitor clamped, cascaded h-bridge, and diode clamped inverters. The clamped diode inverter, which will be discussed in this study, uses a diode that provides an m-level to reduce harmonics in the output voltage.

In general, the inverter consists of several switches which are controlled by Pulse Width Modulation (PWM) and equipped with filters. There are three strategies to make switching based on multicarrier modulation methods. First, Sinusoidal PWM (SPWM) which requires a high switching frequency to get maximum results. Second, Phase Disposition PWM (PD-PWM) which has the carrier signal in the same phase as the reference. Third, Phase Opposite Disposition PWM (POD-PWM) where the carrier signal is above the zero-reference.

The filter serves to eliminate unwanted harmonics. The filter on the inverter itself is a series of the inductor (L), inductor-capacitor (LC), or inductor-capacitor inductor (LCL).

In this paper, it will be shown how to design a 9-level diode clamp inverter. The switching control is based on Phase Disposition Pulse Width Modulation. The L filter will be implemented to minimize total harmonic distortion. The modeling of the nine-level Diode Clamp Inverter (DCI) is described in section II. Section III explains how PD-PWM works in a 9-level DCI system. Section IV shows the simulation results using MATLAB/Simulink and the discussion. The last section gives the conclusions of this study.

II. NINE LEVEL DCI SYSTEM

The multilevel inverter diagram is shown in Figure 1. The number of capacitors in a multilevel inverter is N-1 the number of levels connected to a direct current voltage source. Figure 2 illustrates the output voltage of a Multilevel Inverter (MLI) with 2-level, 3-level, and N-level.

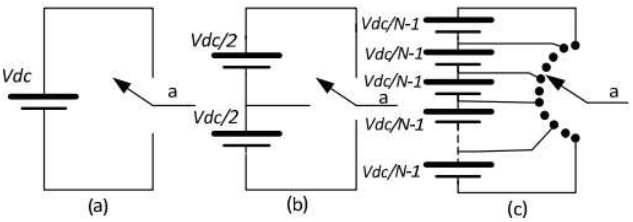


Figure 1. Multilevel inverter diagrams of (a) 2-levels, (b) 3-levels, and (c) N-l levels.[9]

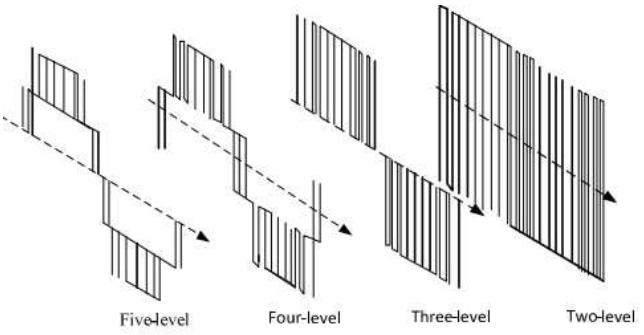


Figure 2. Output Voltage of N-level inverter[9]

In this section, a 9-level three-phase DCI system is described. The 9-level DCI is equipped with eight capacitors to provide a voltage of -4V to +4V. An Inductor and Resistor

(RL) filter was added to correct the THD [10]. For the L filter design, the inductor is connected in series with the resistor. The L filter denotes a first-order low-pass filter with a cut-off frequency of $\omega_L = R/L$[11].

Figure 3 shows a 9-level DCI design. The 9-level can be designed by using 16 switches. Every phase is structured of 8 switches for the high leg and 8 switches for the bottom leg. The clamping diode restricts the safe working voltage level across each capacitor[9]. A1-A8 and A*1-A*8 are the IGBT or MOSFET to control phase voltage A, as well as phase B and phase C. 9-level staircase wave will be the output voltage of this topology. The *m*-level DCI has a an *m*-level output phase voltage and (2m-1) level output voltage [12].

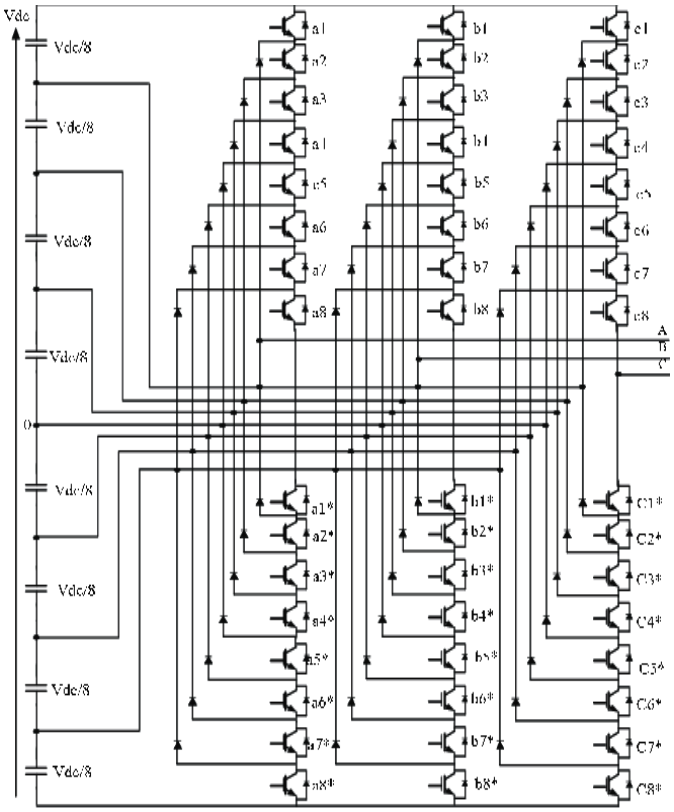


Figure 3. Nine Level Diode Clamp Inverter[9]

III. Phase Disposition Pulse Width Modulation

There are 2 types of PWM multicarrier modulation methods in level shifted PWM mode, one of which is Phase Disposition PWM. The PD-PWM method is one of the modulation strategies for the intersection of a triangular wave with a sine wave that produces a generating pulse. In the PD-PWM technique, the carrier signals have the same frequency and have no phase difference. The difference with this type of modulation technique in the same mode is that each carrier signal is different in phase angle and frequency.

The difference between the Phase Disposition-PWM (PD-PWM) and SPWM methods lies in the resulting THD value. This is due to the different output waveforms. The PD-PWM method produces an output waveform that has many levels (multilevel) so that the resulting THD is smaller than the SPWM method which produces an output waveform without levels (non-multilevel).

PD-PWM technique can be shown in Figure 4. The sinusoidal wave will be the reference. If the wave is equal to or more than the repeating sequence, then the IGBT will be on. To know the switching states for the high leg, we can see Figure 5. Then, for the bottom leg, we can see Figure 6.

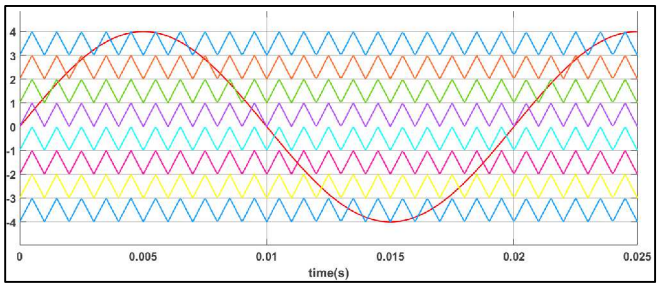


Figure 4. Phase Disposition Pulse Width Modulation

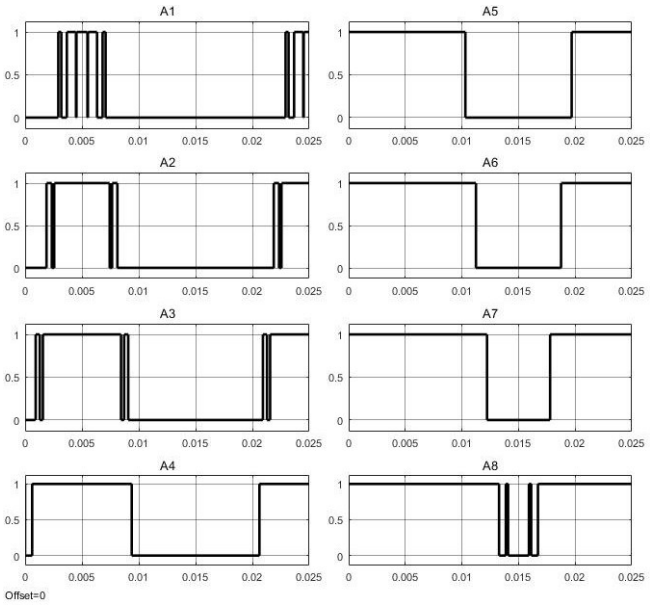


Figure 5. Switching State Based on PD-PWM for High Leg

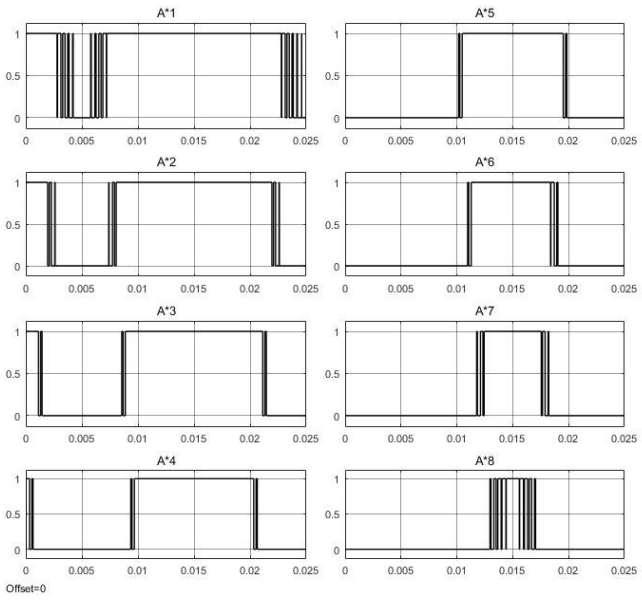


Figure 6. Switching State Based on PD-PWM for Bottom Leg

Another modulation strategy is phase opposite disposition PWM. In this method, the entire carrier signal is above the zero reference. We can see the modulation technique in figure 7.

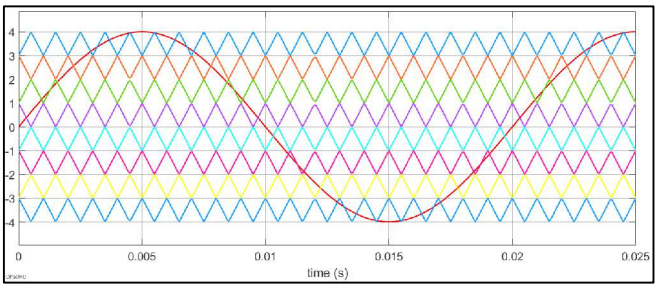


Figure 7. Phase Opposite Disposition Pulse Width Modulation

IV. Results And Discussion

The proof is done by simulation using Simulink in MATLAB software. The parameter values used can be seen in Table 1. In the simulation, a series circuit of resistors and inductors is added as a filter. The selected fundamental frequency is 50Hz, according to Indonesian conditions. Meanwhile, the inductor and resistor values are obtained by considering the maximum %THD limit, which is 5%.

Table 1. Parameter Value of Simulation

Parameter	Value
R (Resistor)	$1\ \Omega$
L (Inductor)	$5\ x\ 10^{-4}\ H$
V_{dc} (DC Voltage)	$100V$
f(Fundamental frequency)	$50Hz$

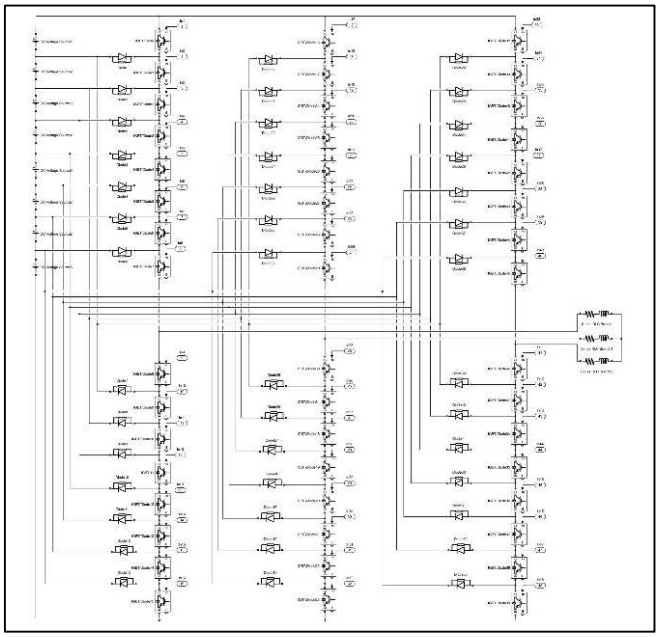


Figure 8. Block of Simulation in Simulink

To see the voltage response, we can look at figure 8. Switching based on PD-PWM makes the output signal close to pure sinusoidal.

Figure 9 shows the current response of the nine-level DCI. The phase difference between the three is 120 degrees. From the results shown in Figures 9 and 11, PD-PWM produces a better current signal than POD-PWM. With the use of a nine-level multilevel inverter, the resulting voltage level can be greater. With a 100V DC voltage source, voltages up to nearly 400V can be generated. The voltage response can be seen in Figure 10. Like current output, compared to POD-PWM, the voltage output by the PD-PWM method gives better results.

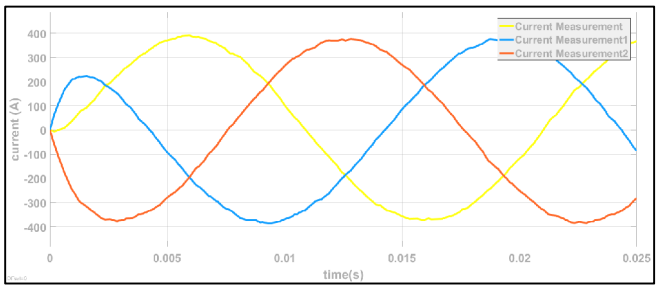


Figure 9. Current Response of 9-Level DCI using PD-PWM

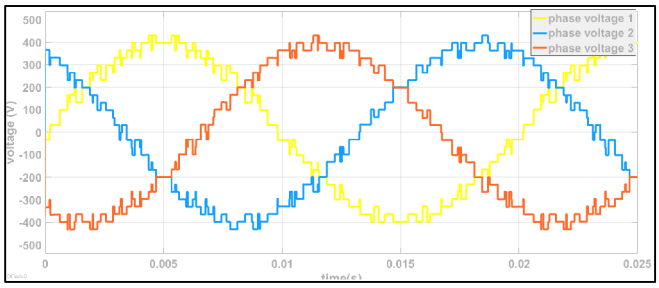


Figure 10. Voltage Response of 9-Level DCI using PD-PWM

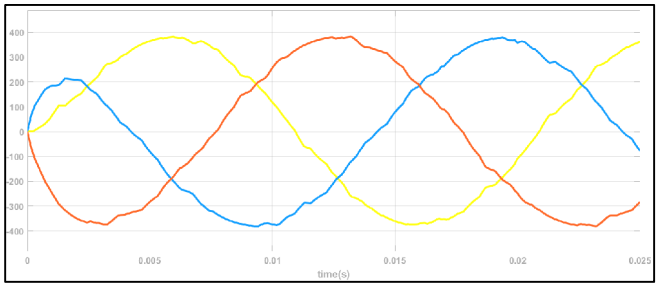


Figure 11. Current Response of 9-Level DCI using POD-PWM

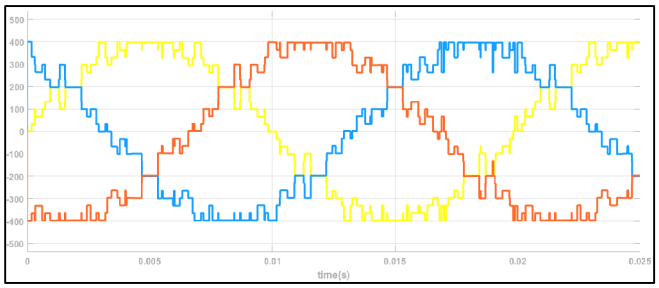


Figure 12. Voltage Response of 9-Level DCI using POD-PWM

One of the performance indicators that need to be considered is THD. From the results shown in Figure 13, the THD of this phase voltage is 3.16%. Likewise, from Figure

14, the current harmonic shows a 2.16% value. Meanwhile, shown in Figures 15 and 16, the POD-PWM method shows a current harmonic of 6.35% and a voltage harmonic of 12.80%. This value is still below the maximum standard of 5%. In comparison to [9] that using Sinusoidal PWM (SPWM), the THD of phase voltage is still 3.90%.

The %THD comparison of each method is shown in Table 2. From the Table, we know that PD-PWM gives better performance of THD than the SPWM method and POD-PWM method.

The use of filters also has a major contribution to improving harmonics. In [10], without using a filter, the resulting voltage harmonic is 7.84%. The THD value is dependent on the selection of the inductor value. By getting the appropriate inductor value, a small %THD value can be obtained.

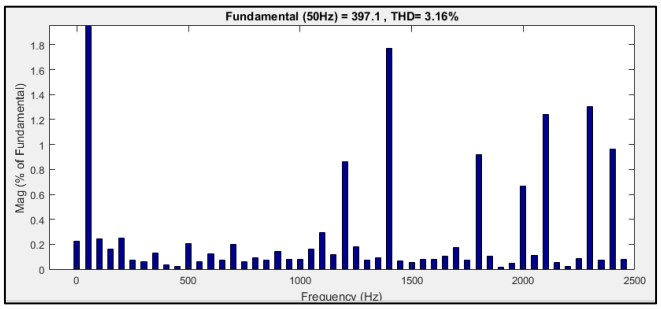


Figure 13. Voltage Harmonic of PD-PWM method

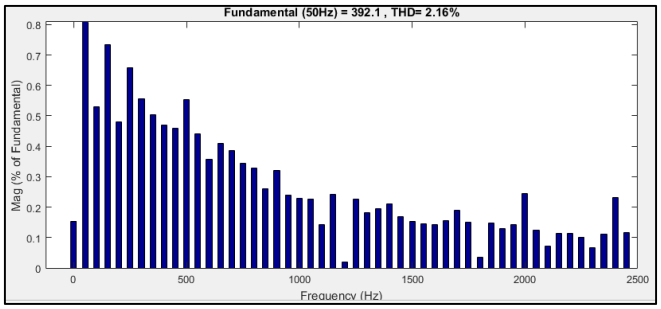
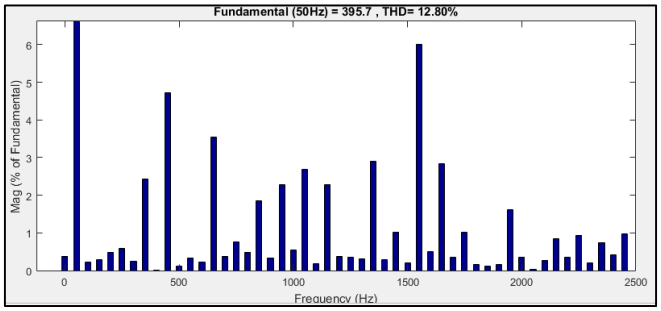


Figure 14. Current Harmonic of PD-PWM method



Fifure 15. Voltage Harmonic of POD-PWM method

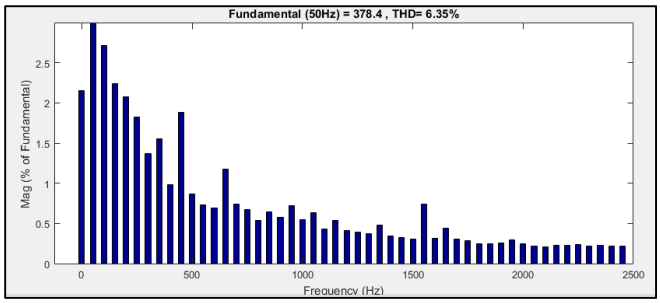


Figure 16. Current Harmonic of POD-PWM method

Table 2. %THD comparison of switching method

Method	%THD of Current	%THD of Voltage
SPWM[9]	-	3.90%
PD-PWM	2.16%	3.16%
POD-PWM	6.35%	12.80%

V. Conclusion

The design of Diode Clamped Inverter using switching based on phase disposition pulse width modulation has been investigated. From the results shown, 9-level DCI with PD-PWM provides good performance and follows the IEC standard. Switching based on PD-PWM gives better performance than Sinusoidal PWM. Furthermore, the implementation of inductor filters contributes to getting a better %THD of the system.

Acknowledgment

The authors wish to thank Institut Teknologi Sepuluh November that facilitating this research.

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