

# Fast protection strategy for monopole grounding fault of low-voltage DC microgrid

Yuhang Peng<sup>a</sup>, Ziang Song<sup>a</sup>, Xiankai Zeng<sup>a</sup>, Zhaoyang Pan<sup>a</sup>, Shuye Zhang<sup>a</sup>, Xi Shen<sup>b</sup>, Lujun Wang<sup>a,\*</sup>

<sup>a</sup> Hubei University of Technology, Hubei Key Laboratory for High-efficiency Utilization of Solar Energy and Operation Control of Energy Storage System, Wuhan 430068, Hubei Province, China

<sup>b</sup> China Ship Research and Design Center, Wuhan 430000, Hubei Province, China

## ARTICLE INFO

### Keywords:

DC solid-state circuit breakers  
DC microgrid  
PMOS  
Self-powered  
Topological structure  
Coupled energy

## ABSTRACT

Low voltage DC microgrid has attracted more and more attention in smart grid with its advantages such as low network loss, large transmission capacity and easy direct access to distributed power supply. However, compared with the traditional AC microgrid, the DC microgrid lacks inertia support and the fault develops rapidly, which makes the existing short-circuit current protection technology difficult to meet the requirements of accurate and efficient troubleshooting. Therefore, this paper presents a low-voltage DC microgrid ground short-circuit fault protection system based on positive channel metal oxide semiconductor (PMOS) self-powering DC solid-state circuit breaker protection elements, and verifies the feasibility and effectiveness of the protection system through simulation experiments. The experimental results show that the proposed protection system based on solid state circuit breaker will not affect the voltage of DC microgrid when it is normally on; In case of ground short-circuit fault in DC microgrid, the coupling energy of the short-circuit current makes the PMOS to be turned off reliably. In addition, because the primary inductance of the transformer plays a certain current limiting role, the turn-off current of PMOS will not increase sharply. The solid-state circuit breaker can effectively block the fault without a buffer circuit, which has a good application prospect.

## 1. Introduction

With the increasing global energy consumption, the depletion of traditional fossil energy sources and the increasing electricity consumption in load-intensive areas, distributed power generation technologies based on renewable energy sources have become a hot spot for research. The view that microgrids are a way to effectively utilize distributed power sources for power distribution is widely recognized [1–3]. For the access of many DC loads and distributed power sources, DC microgrids have become one of the important networking methods for future smart grids with the advantages of low network losses and simple control strategies [4,5].

However, the short-circuit protection problem has been one of the key challenges of DC microgrid. DC micro-network after a short-circuit fault rapid increase in current, rapid voltage reduction, may endanger the fragile power electronics and network recovery after fault removal is slow. Trying to protect vulnerable equipment and improve power supply reliability requires fast communication and expensive DC circuit

breakers, increasing the cost of protection configurations. Therefore, for the short-circuit protection of DC microgrid, it is urgent to develop a simple and efficient protection system [6–9].

Voltage level is a prerequisite for the study of DC microgrid short-circuit protection. The voltage level of DC microgrid should be classified into 2 categories: medium voltage DC microgrid (1.5~22 kV) and low voltage DC microgrid (below 1500 V) [10–12]. Among them, medium voltage DC microgrid is mainly used in ship systems, while low voltage DC microgrid is used in telecommunication systems and residential and commercial power supply. Low-voltage DC microgrid is easy to connect to 380 V AC grid due to suitable modulation ratio, and the power semiconductor devices such as Insulated Gate Bipolar Transistor (IGBT) and MOS tube are more mature and reliable in this voltage range [13–15].

In the literature [16], a solid-state DC circuit breaker structure based on power electronics was proposed, which contains a set of anti-parallel fully-controlled power electronics connected in parallel with energy absorbing branches to improve the open-end speed, but suffers from

\* Corresponding author.

E-mail address: [wanglujun@zju.edu.cn](mailto:wanglujun@zju.edu.cn) (L. Wang).

<https://doi.org/10.1016/j.epsr.2022.108919>

Received 28 August 2022; Received in revised form 27 September 2022; Accepted 20 October 2022

Available online 28 October 2022

0378-7796/© 2022 Elsevier B.V. All rights reserved.

large through-state losses and complex structure. The literature [17] proposed a solid-state DC circuit breaker structure based on power electronics composed of thyristor and IGBT in parallel, which reduces the large on-state losses, but the breaker is too large. The literature [18] proposed a technical solution for a DC solid-state current-limiting circuit breaker based on Integrated Gate Commutated Thyristor (IGCT) and Silicon Controlled Rectifier (SCR) to improve the interrupting capacity of the breaker by improving the reliability of the main switching tube IGCT working in parallel. The literature [19] proposed a DC circuit breaker topology with current-limiting function, which uses IGBT as the main switching device with both breaking and current-limiting functions, has the advantages of small through-state loss, high turn-off current, and high voltage level, but the number of switching tubes is large and the control logic is complex.

The design advantages of the above circuit breaker technology are: compared with mechanical circuit breakers, arc-free breaking and significantly shorter breaking time, but there are also shortcomings: the operation of such circuit breakers must be carried out according to very precise and strict timing, requiring detection, control with consistent. Circuit breakers require additional control and drive circuits in addition to the power circuit, this part of the circuit work requires an external power supply, increasing the complexity of the system, especially in the event of a failure of the grid itself, the power supply may also be unstable, reducing the reliability of the circuit breaker.

To address the above shortcomings, this paper proposes a PMOS-based self-taking DC solid-state circuit breaker as a ground short-circuit fault protection system for low-voltage DC microgrid based on the controllability characteristics of power electronics. The system consists of PMOS as the main switching tube, working in series in the DC microgrid. When a short-circuit fault does not occur in the DC microgrid, the solid-state circuit breaker conducts normally and has no effect on the microgrid line flow; when a short-circuit fault occurs, the short-circuit current coupling energy is used to make the PMOS turn off reliably without additional power supply. The PMOS-based self-powering DC solid-state circuit breakers use devices that can be adjusted according to voltage levels, effectively reducing manufacturing costs. Furthermore, PMOS-based self-powering DC solid-state circuit breakers having a simple structure that does not require additional auxiliary circuits or complex control strategies, effectively speeding up the response time and improving the reliability of DC microgrid operation.

Finally, the protection scheme was simulated and verified by PSCAD/EMTDC.

## 2. Low-voltage DC microgrid ground fault protection system

As shown in Fig. 1, the low-voltage DC microgrid mainly consists of DG (wind turbine, photovoltaic), energy storage device (fuel cell), converter (AC-DC, DC-DC) and DC load, which is connected to the AC microgrid through rectification modules when connected to the grid. In Fig. 1, module A (main switching module) contains PMOS tube  $Q_1$ ; module B (driving module) contains voltage regulator  $Z_1$ , diodes  $D_1$  and  $D_2$ , and resistor  $R_1$ ; module C (power take-off module) contains transformer  $T_1$ , diode  $D_3$ , resistor  $R_2$ , and capacitor  $C_1$  at the same name end; the three modules together constitute the PMOS-based self-powering DC solid-state circuit breaker proposed in this paper, where F1 is the microgrid single-pole ground fault.

### 2.1. Circuit breaker on-state analysis

Most of the fully-controlled devices used in traditional solid-state circuit breakers are N-Metal-Oxide-Semiconductor (NMOS), which are turned off under normal conditions. The solid-state circuit breaker designed in this paper needs to be turned on under normal conditions, and only turned off when a short-circuit fault occurs, so, PMOS is selected as the main switch tube. The physical structure of PMOS is shown in Fig. 2.

Fig. 3(a) shows the equivalent circuit diagram of the DC solid-state circuit breaker circuit topology when the blocking function is not activated.

Based on the PMOS without additional power supply short-circuit current blocking circuit connected in series in the DC power line, do not start the blocking function, the role of the voltage regulator diode  $Z_1$  in the driver module is when the circuit works normally, so that the drive signal along  $Z_1 - R_1$  to the PMOS gate power supply, the PMOS gate voltage and the source voltage to form a voltage difference, the PMOS conduction, at this time the current flows along the path of P1-  $Q_1$ -P2, transformer  $T_1$  can be equated to an inductor  $L_1$ . Fully conduction state, ignoring the voltage drop of the main switching tube  $Q_1$  and transformer  $T_1$ , to obtain a simplified circuit diagram as shown in Fig. 3(b), in which

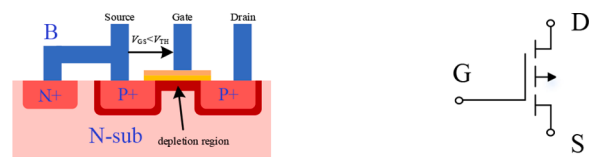


Fig. 2. PMOS structure diagram.

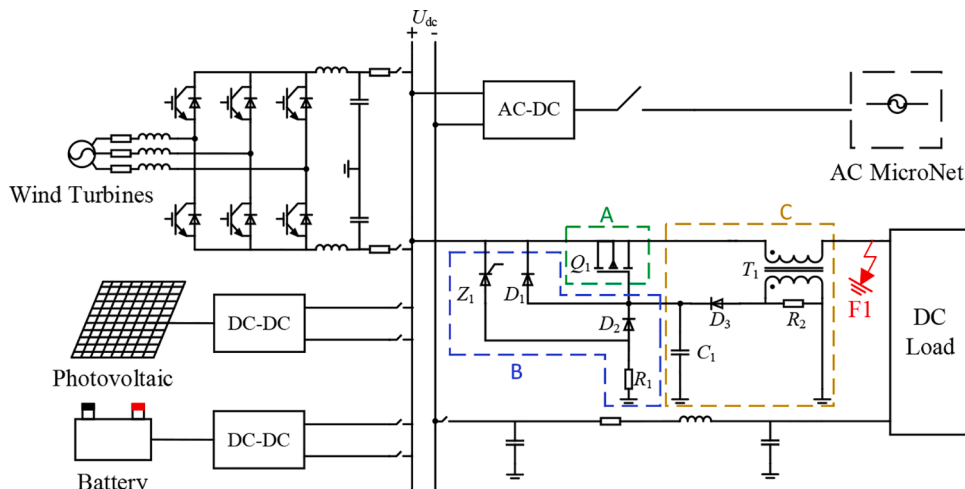


Fig. 1. Low voltage DC microgrid system.

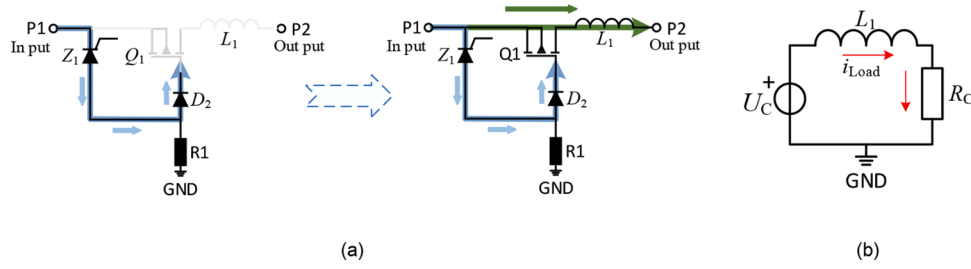


Fig. 3. Equivalent circuit diagram of the auxiliary.

$U_C$  is the supply voltage;  $L_1$  is the transformer series connected in the circuit equivalent inductor;  $R_C$  is the load resistance; the initial value of the load current is 0.

According to the KVL and KCL laws, the system of equations can be obtained as:

$$\begin{cases} iR_C + L_1 di/dt = U_C \\ i_0 = i_{0-} \end{cases} \quad (1)$$

The solution is:  $i_{Load} = \frac{U_C}{R_C} (1 - e^{-t/R_C})$

When the circuit breaker designed in this paper is on normally, the current will rise exponentially to the normal operating current. The gate voltage of the main switching tube forms a sufficient voltage difference with the source voltage due to the role of the drive module, and the main switching tube is fully on with almost zero voltage drop, which has no effect on the normal operation of the line.

### 2.2. Ground fault analysis

Fig. 4 shows the equivalent circuit diagram of the DC solid state circuit breaker circuit topology after activating the fault blocking function.

A short-circuit current blocking circuit based on PMOS without additional power supply as described herein, when a short circuit occurs in the line, at which time the current surge at the primary coil end of transformer  $T_1$  in the power extraction module, the secondary coil will generate coupling energy, and then the energy extraction module uses the coupling energy to charge capacitor  $C_1$ , after charging is complete capacitor  $C_1$  discharges, and the drive signal along  $T_1$ - $D_3$ - $C_1$ - $Q_1$  to the main switching tube gate power supply, so that the PMOS gate voltage rises until it reaches the PMOS shut down conditions, the PMOS automatically shut down, the excess voltage through the diode  $D_1$  back to the grid, to achieve the short-circuit current blocking effect without additional power supply.

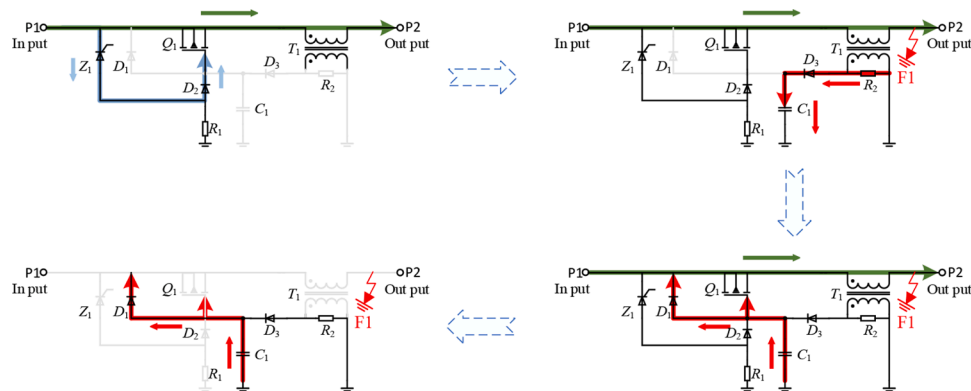


Fig. 4. Fig. 4 shows the blocking function analysis diagram, and the simplified circuit diagram will be used later in the theoretical analysis section.

## 3. Theoretical derivation and parameter design

### 3.1. Theoretical derivation

This section focuses on the theoretical derivation of the transformer and capacitor in the circuit breaker pickup module, using a short circuit fault to ground on the DC outlet side as an example.

When a short-circuit fault occurs on the load side, the DC circuit breaker is considered as a switch, and the short-circuit current characteristics can be analyzed using the first-order equivalent circuit diagram in Fig. 5.

When a ground fault occurs in a low-voltage DC microgrid, let the line current be  $i_L(t)$ , before and after the ground fault occurs.

$$i_L(0^+) = i_L(0^-) = \frac{U_C}{R_{dc} + R_S} \quad (2)$$

In the Eq. (3):  $U_C$  is the DC power supply;  $R_{dc}$  is the line resistance;  $R_S$  is the load resistance.

From the full response of the first-order circuit, the fault current can be found as follows:

$$i_f(t) = i(\infty) + [i(0^+) - i(\infty)]e^{-t/\tau} = U_C \left[ \frac{1}{R_{dc}} + \left( \frac{1}{R_{dc} + R_S} - \frac{1}{R_{dc}} \right) \right] e^{-t/\tau} \quad (3)$$

In the Eq. (3)  $\tau$  is the time constant,  $\tau = \frac{L_{W1}}{R_{dc}}$ ,  $L_{W1}$  is the transformer primary winding inductance.

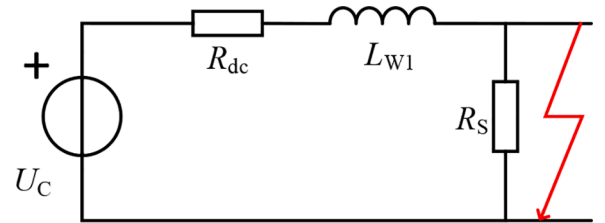


Fig. 5. Equivalent diagram of short-circuit first-order circuit.

In turn, the derivative of  $i_f(t)$  yields the short-circuit current rise rate:

$$\frac{di_f(t)}{dt} = \frac{U_C}{L_{W1}} \bullet \frac{R_S}{R_{dc} + R_S} e^{-t/\tau} \quad (4)$$

Then the maximum rise rate of short-circuit current is:

$$\left[ \frac{di_f(t)}{dt} \right]_{\max} = \frac{U_C}{L_{W1}} \bullet \frac{R_S}{R_{dc} + R_S} \quad (5)$$

The short-circuit current  $I_{W1MAX}$  in the transformer primary winding in the short-circuit fault transient condition is:

$$I_{W1MAX} = I_N + \left( \frac{U_C}{L_{W1}} \bullet \frac{R_S}{R_{dc} + R_S} \right) \Delta t \quad (6)$$

Where:  $I_N$  is the rated system current and  $\Delta t$  is the fault current rise time. At this time, the energy stored in the primary winding of the transformer is shown in Eq. (7).

$$W_{L1Tran} = \frac{1}{2} L_{W1} \left[ I_N + \left( \frac{U_C}{L_{W1}} \bullet \frac{R_S}{R_{dc} + R_S} \right) \Delta t \right]^2 \quad (7)$$

Then the energy of the secondary side:

$$W_{L2} = \alpha W_{L1Tran} (\alpha < 1) \quad (8)$$

According to Eqs. (2) and (6) can be found in the short-circuit fault transformer secondary winding current is:

$$I_{W2} = \sqrt{\frac{2W_{L2}}{L_{W2}}} \quad (9)$$

Where:  $I_{W2}$  is the secondary side current of the transformer,  $W_{L2}$  is the energy stored in the secondary winding of the transformer,  $L_{W2}$  is the inductance of the secondary winding of the transformer.

Then the secondary winding of the transformer can be equated to a current source, and since the internal resistance of the current source is infinite, ignoring the resistance  $R_2$ , the circuit can be equated to a current source to charge the capacitor  $C_1$  directly. Then the voltage at the end of the capacitor is:

$$U_{C1} = \int_0^t I_{W2} dt \quad (10)$$

As the transformer in the power take-off module is not an ideal pre-voltage, there are magnetic losses leakage inductance, etc., the following supplement transformer loss calculation.

The IGSE algorithm for core loss calculation under non-sinusoidal excitation considers that the core loss is not only related to the rate of change of flux but also to the magnetization period, and the accuracy of the calculation results is related to the three coefficients in the Steinmetz equation, and the IGSE algorithm is shown in Eq. (11) [20].

$$P_{core} = \frac{1}{T} \int_0^T k_i \bullet \left| \frac{dB(t)}{dt} \right|^\alpha |\Delta B|^{\beta-\alpha} dt \quad (11)$$

Where:  $P_{core}$  is the core loss,  $\Delta B$  is the change in magnetic flux,  $T$  is the magnetization period.

Among them,

$$k_i = \frac{K}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha 2^{\beta-\alpha} d\theta} \quad (12)$$

The winding losses are related to the way the windings are wound in the core window. The transformer winding loss calculation is based on the Dowell one-dimensional electromagnetic field model [21–24], which is based on three prerequisite assumptions: first, the winding conductor is copper skinned; second, the core permeability is infinite; and third, the winding height is equal to the core window height. The magnitude of the conductor AC resistance factor is shown in Eq. (13) when the three assumptions are satisfied.

$$F_{r,n} = \frac{R_{ac}}{R_{dc}} = \Delta \bullet \left[ \varphi_1 + \frac{2}{3} (m^2 - 1) \varphi_2 \right] \quad (13)$$

Where:  $F_{r,n}$  is the conductor resistance factor. Among them,

$$\begin{cases} \varphi_1 = \frac{\sinh(2\Delta) + \sin(2\Delta)}{\cosh(2\Delta) - \cos(2\Delta)} \\ \varphi_2 = \frac{\sinh\Delta - \sin\Delta}{\cosh\Delta + \cos\Delta} \\ \Delta = \sqrt{n} \bullet d_w / \delta \end{cases} \quad (14)$$

$R_{dc}$  is the DC resistance of winding conductor;  $m$  is the number of winding layers;  $d_w$  is the thickness of copper skin;  $\delta$  is the depth of skin collection.

When the transformer primary excitation current is non-sinusoidal, the AC resistance factors at different harmonic frequencies are calculated separately, and the total winding loss is calculated as shown in Eq. (15), where  $N$  is the number of current harmonics.

$$P_{windings} = \sum_{n=1}^N F_{r,n} R_{dc} I_{rms,n}^2 \quad (15)$$

Where:  $P_{windings}$  is the total conductor winding loss

The leakage inductance is calculated based on the leakage energy as shown in Eq. (16).

$$W_{leakage} = \frac{1}{2} \mu_0 \int H^2 dV = \frac{1}{4} L_\delta I_1^2 \quad (16)$$

$I_1$  is the peak primary excitation current;  $H$  is the magnetic field strength;  $L_\delta$  is the total leakage inductance converted to the primary side together with the primary side leakage inductance.

The current distribution in the winding at high frequency is no longer linear with the winding depth, the skin effect is more significant, and the field strength distribution in the winding is shown in Fig. 6.

Based on the Dowell one-dimensional electromagnetic field model, the distribution of magnetic field intensity magnitude with distance  $x$  in the original secondary winding in Fig. 6 is obtained by solving Maxwell's equations (as in Eq. (17)), where  $m$  is the number of winding layers.

$$H_1(x) = H_0 \frac{n \sinh(\gamma x) + (n-1) \sinh(\gamma t - \gamma x)}{\sinh(\gamma t)} \quad (17)$$

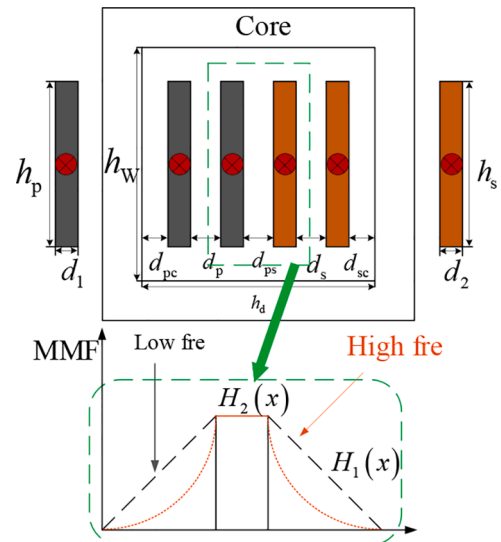


Fig. 6. Magnetomotive force distribution in transformer winding conductors.

Among them,

$$\begin{cases} \gamma = \frac{1+j}{\delta} \\ H_0 = mI/h_w \end{cases} \quad (18)$$

From Fig. 6, the field strength between winding layers is related to the current magnitude and the number of windings  $m$ , as shown in Eq. (19).

$$H_2(x) = \frac{m \cdot I}{h_w} \quad (19)$$

According to Eq. (18) and Eq. (19), the total transformer leakage energy can be expressed as:

$$W_{\text{leakage}} = W_{\text{pri}} + W_{\text{sec}} + W_{\text{isolation}} + W_{\text{ins(pri)}} + W_{\text{ins(sec)}} \quad (20)$$

$W_{\text{pri}}$ ,  $W_{\text{sec}}$  are the transformer primary winding and secondary winding leakage energy;  $W_{\text{ins(pri)}}$ ,  $W_{\text{ins(sec)}}$  are the primary winding layer and secondary winding layer leakage energy;  $W_{\text{isolation}}$  is the primary winding and secondary winding leakage energy between the winding.

### 3.2. Parameter design

This section focuses on the analysis and design of the transformer and capacitor values within the circuit breaker, with an input DC voltage of 48 V (communication power supply voltage level). From the above analysis, the transformer and capacitor are obviously the key equipment

in the circuit breaker and play the role of cutting off the circuit. Its value will directly determine whether the main switching tube PMOS reliable shutdown, but also affect the speed of fault isolation.

According to the transformer loss calculation in 3.1, the short-circuit current reaches the maximum value  $I_{W1MAX}$  at  $t_m$  moment, and the energy generated by the primary winding is transferred to the secondary winding, then the secondary winding energy is  $\alpha W_{L1Tran}$  as shown in Eq. (8), after considering the magnetic loss impedance (impedance is 3%~4%) and other factors, the primary winding energy  $\alpha$  is taken as 0.92~0.96, according to the 48 V DC system. Based on the actual needs of the 48 V DC system, this paper initially determines the capacitance selection range from 1 to 5  $\mu\text{F}$ , with 1  $\mu\text{F}$  as the step, based on the formula derived from the theory of each stage in Section 3.1, the short-circuit current situation under different capacitance values is simulated and analyzed. The current waveform is shown in Fig. 7, the calculation process of transformer primary inductance  $L_{W1} = 20 \mu\text{H}$ , transformer secondary inductance  $L_{W2} = 100 \mu\text{H}$ , the transformer turns ratio is 1:5. According to Fig. 7, as the value of  $C_1$  increases, the capacitor charging and discharging time required to grow, the fault current  $I_{W1MAX}$  rise duration grows, so the peak fault current increases, the fault isolation time grows, that is fault isolation slows down. To avoid excessive current stress and to ensure faster fault isolation, the value of  $C_1$  should not be too large. Eventually,  $C_1$  was determined to be 3  $\mu\text{F}$ .

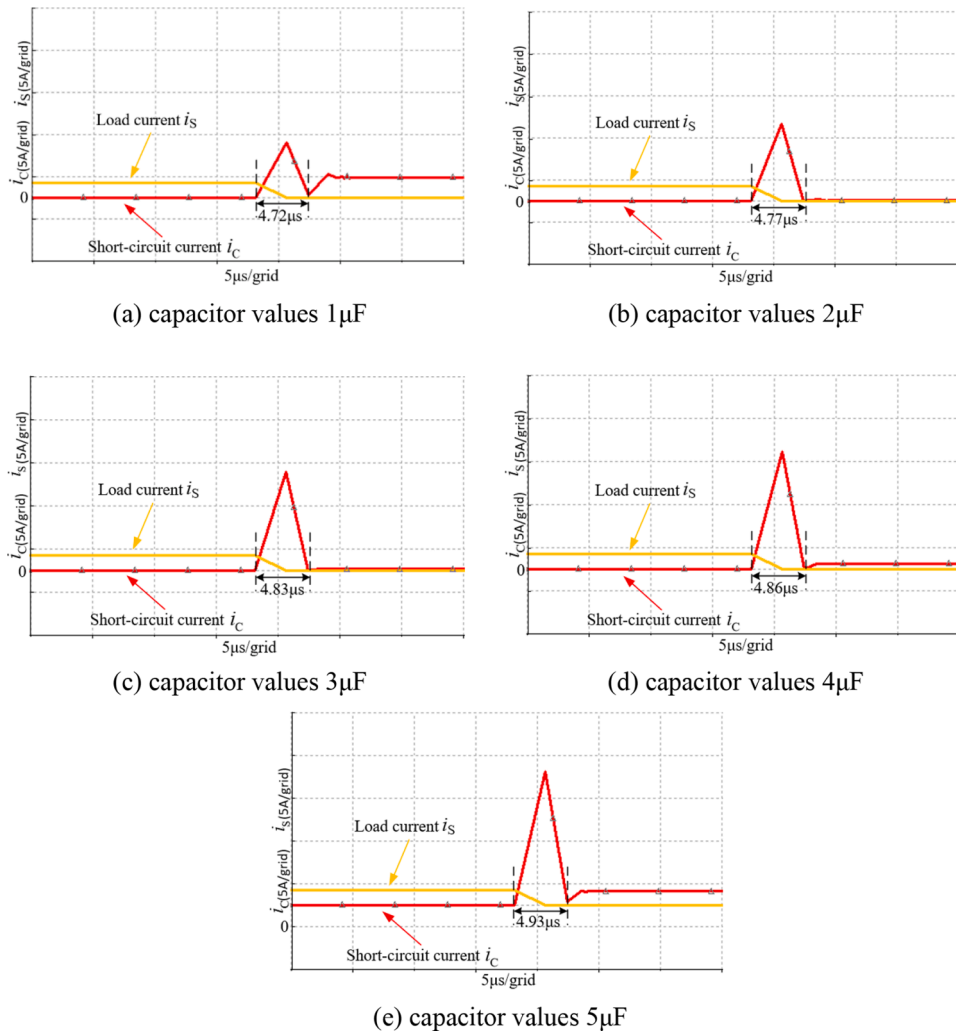


Fig. 7. Charging current and PMOS gate voltage for different capacitor values.

#### 4. Simulation analysis

Based on the above analysis of the structure and modules of the proposed solid-state circuit breaker, Construct the simulation model of the low-voltage DC microgrid shown in Fig. 1. The model includes the main switch module, the driver module, the power extraction module, and the energy extraction module. The simulation parameter design is shown in Table 1: System voltage  $U_C = 48$  V (communication power supply voltage level), regulator tube  $Z_1 = 27$  V, resistor  $R_1 = 1$  K $\Omega$ ,  $R_2 = 1$  M $\Omega$ , transformer primary inductance  $L_{W1} = 20$   $\mu$ H, transformer secondary inductance  $L_{W2} = 100$   $\mu$ H, leakage inductance  $W_{leakage} = 100$  hm, and resistor  $R_3 = 10\Omega$ . Two states are simulated: steady-state and short-circuit state.

Fig. 8 shows the voltage and current waveforms under steady-state conditions in normal operation. From the waveform diagram in Fig. 8, it can be obtained that when the difference between PMOS gate voltage and source voltage is  $U_{GS} = -27$  V, the PMOS is fully on and the tube voltage drop is negligible, so the input voltage is nearly equal to the output voltage, at this time, the load current  $i_s = 4.8$  A. It is proved that the PMOS-based self-powered DC solid-state circuit breaker in this paper has no effect on the original line during normal operation.

When a single-pole grounding fault F1 occurs in the microgrid, the voltage and current waveforms of the solid-state circuit breaker protection system are shown in Fig. 9. It is assumed that the single-pole grounding fault of the DC microgrid occurs at time  $t_1$ , as shown in Fig. 9, the voltage, and current waveforms before and after the fault are split and analyzed. After the ground fault occurs at time  $t_1$ , the short-circuit current  $i_c$  at the fault point increases rapidly, and the secondary winding of the transformer induces coupling energy. After charging the capacitor  $C_1$ , the capacitor  $C_1$  charges the gate of the PMOS tube, and the gate voltage  $U_G$  rises rapidly until time  $t_2$ . The output voltage  $U_{OUT}$  drops to zero, at this time, the difference between the gate voltage and the source voltage of the PMOS tube rises from  $U_{GS} = -27$  V to  $U_{GS} = -6$  V, and the PMOS tube is completely turned off. It takes  $t_2 - t_1 = 3.68\mu$ s from the occurrence of the fault to the complete shutdown.

When a short-circuit fault occurs, the primary-side inductance of the transformer plays a certain current limiting role, so the turn-off current of the PMOS tube will not increase sharply. When the PMOS is turned off, the PMOS tube current has experienced two stages of linear increase and decrease, and its  $di/dt$  is  $di/dt = 4.75$  A/ $\mu$ s in the rising stage respectively; falling stage  $di/dt = 8.136$  A/ $\mu$ s. Therefore, the solid-state circuit breaker designed in this paper does not need to configure a snubber circuit while efficiently blocking faults.

The results of the simulation analysis show that the PMOS-based self-taking DC solid-state circuit breaker has no effect on the original line voltage and current during normal conduction; in the event of a short-circuit fault, the coupling energy of the short-circuit current can be used to quickly cut off the circuit and block the short-circuit current, and the blocking process can be completed within 4  $\mu$ s.

#### 5. Conclusion

This paper proposes a solid-state circuit breaker without additional power supply for DC microgrid ground fault protection is proposed, and its working principle and breaking mode are analyzed. The simulation

Table 1

The circuit parameters.

Components	Parameters
P-MOSFET	
Transformer	1:5
Schottky Tubes	
Zener Diodes	$Z_1 = 27$ V ( $\pm 2\%$ )
Resistors	$R_1 = 1$ K $\Omega$ , $R_2 = 1$ M $\Omega$ , $R_3 = 10\Omega$
Current Checking Resistors	10 m $\Omega$ /2W
Capacitors	$C_1 = 3$ $\mu$ f/50V

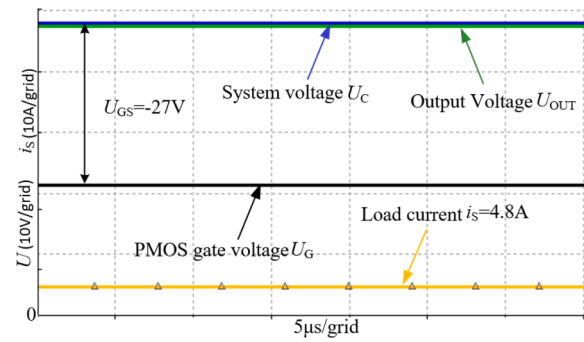


Fig. 8. DC solid state circuit breaker waveforms during normal operation.

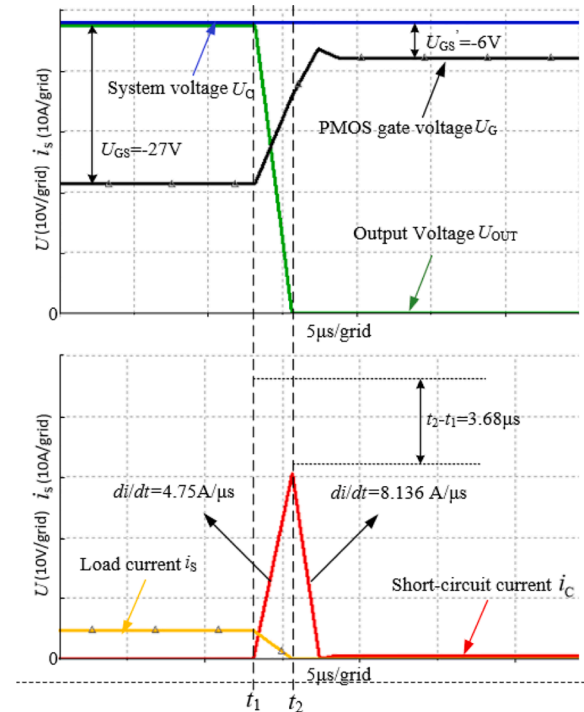


Fig. 9. Voltage and current waveforms when starting the locking function.

model is established, and the simulation of normal closing and fault short-circuit immediate protection are completed. The simulation results are consistent with the theoretical analysis. The DC solid state circuit breaker proposed in this paper has the following advantages:

- 1) Using the working characteristics of PMOS to realize the quick closing of circuit breaker, the solid-state circuit breaker has simple structure and reliable performance.
- 2) In case of short circuit fault in the circuit, PMOS is used to cut off the positive terminal to ensure safe operation. (NMOS needs to be cut off from the negative terminal, which may cause electric shock.)
- 3) When a short-circuit fault occurs, the primary inductance of the transformer plays a certain role in limiting the current, and the turn-off current of the PMOS will not increase sharply, so there is no need to configure a buffer circuit.
- 4) To sum up, the DC microgrid grounding protection system proposed in this paper has the advantages of current limiting protection function, low manufacturing cost and low conduction loss, and has broad application prospects.

## CRedit authorship contribution statement

**Yuhang Peng:** Methodology, Writing – original draft, Visualization, Resources. **Ziang Song:** Supervision. **Xiankai Zeng:** Supervision. **Zhaoyang Pan:** Supervision. **Shuye Zhang:** Software. **Xi Shen:** Software. **Lujun Wang:** Methodology, Writing – original draft, Visualization, Resources.

## Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data Availability

Data will be made available on request.

## Reference

- [1] Z.H.U. Xiaorong, C.H.E.N. Chaoqian, Z.H.A.N.G. Yumeng, Comprehensive control strategy of grid-connected current and DC microgrid voltage under unbalanced grid voltage[J], *High Voltage Eng.* 45 (8) (2019) 2562–2570.
- [2] A. Hirsch, Y. Parag, J. Guerrero, Microgrids: a review of technologies, key drivers, and outstanding issues[J], *Renew. Sustain. Energy Rev.* 90 (2018) 402–411.
- [3] L.E.I. Zhifang, W.A.N.G. Fei, G.A.O. Yanxia, et al., Research status and application analysis of bidirectional DC-DC converters in DC micro-grids[J], *Trans. China Electrotech. Soc.* 31 (22) (2016) 137–147.
- [4] Z.H.A.N.G. Songjie, Q.I.N. Wenping, R.E.N. Chunguang, et al., Control strategy for hybrid energy storage system in bipolar-type DC micro-grid[J], *High Voltage Eng.* 44 (8) (2018) 2761–2768.
- [5] Y.A.N.G. Fan, Z.H.A.N.G. Fengyu, L.I. Dongdong, Adaptive passivity-based control for DC micro-grid based on equivalent input disturbance[J], *High Voltage Eng.* 45 (1) (2019) 236–242.
- [6] L.I. Bin, H.E. Jiawei. Research on the DC fault isolating technique in multi-terminal DC system[J]. *Proceedings of the CSEE*, 2016, 36(1): 87–95.
- [7] X.U.E. Shimin, Q.I. Jinlong, L.I.U. Chong. A research review of protection for DC microgrid[J]. *Proceedings of the CSEE*, 2016, 36(13): 3404–3412, 3359.
- [8] X.U.E. Shimin, Q.I. Jinlong, L.I.U. Chong, et al., A research of grounding mode and new protection principle for DC microgrids[J], in: *Power Syst. Technol.*, 42, 2018, pp. 48–55.
- [9] Oliveira T R De, A.S. Bolzon, P.F. Donoso-Garcia, Grounding and safety considerations for residential DC microgrids[C], in: *40th Annual Conference of the IEEE-Industrial-Electronics-Society*, IEEE, Dallas, USA, 2014, pp. 5526–5532.
- [10] F.J. ENG, Z CHEN, Design of protective inductors for HVDC transmission line within DC grid offshore wind farms[J], *IEEE Trans. Power Deliv.* 28 (1) (2013) 75–83.
- [11] R.R. Xie, Q. Chen, Z.M. Zhang, et al., Fault characteristics study of VSC converter and protection design in DC microgrids[C], in: *2018 IEEE International Conference on Energy Internet*, IEEE, Beijing, China, 2018, pp. 241–246.
- [12] L.I. Bin, H.E. Jiawei, L.I. Ye, et al. DC fault protection scheme for multi-terminal flexible DC systems [J]. *Proceedings of the CSEE*, 2016, 36(17): 4627–4637.
- [13] M. Farhadi, O.A. Mohammed, Event-based protection scheme for a multiterminal hybrid DC power system[J], *IEEE Trans. Smart Grid* 6 (4) (2015) 1658–1669.
- [14] M. Onadi, M.A. Zamani, C. Koch-Ciobotaru, et al., A communication-assisted protection scheme for direct-current distribution networks[J], *Energy* 109 (2016) 578–591.
- [15] A.A.S. Emhemed, G.M. Burt, An advanced protection scheme for enabling an LVDC last mile distribution network[J], *IEEE Trans. Smart Grid* 5 (5) (2014) 2602–2609.
- [16] J.P. Dupraz, G.F. Montillet, New network concepts using electronic hybrid circuit breakers[C], in: *Transmission and Distribution Conference and Exposition*, 2008. T&D. IEEE/PES, IEEE, 2008.
- [17] C. Meyer, R.D. Doncker, Solid-state circuit breaker based on active thyristor topologies[J], *IEEE Trans. Power Electron. PE* (2006).
- [18] P.E.N.G. Zhendong, R.E.N. Zhigang, J.I.A.N.G. Nan, et al. Design and analysis of a new DC solid-state current-limiting circuit breaker [J]. *Proceedings of the CSEE*, 2017, 37(04): 1028–1037.
- [19] Li Shuai, Zhao Chengyong, Xu Jianzhong, Guo Chunyi. A new topology for current-limiting HVDC circuit breaker[J], *Chin. J. Electrical Eng.* 32 (17) (2017) 102–110.
- [20] Venkatachalam K., Sullivan C. R., Abdallah T., et al. Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters[C]//*IEEE Workshop on Computers in Power Electronics*, 2002:36–41.
- [21] J.A. Ferreira, Appropriate modeling of conductive losses in the design of magnetic components[C], in: *21st Annual IEEE Power Electronics Specialists Conference (PESC'90)*, IEEE, 1990, pp. 780–785.
- [22] A. Reatti, M.K. Kazimierczuk, Comparison of various methods for calculating the AC resistance of inductors [J], *IEEE Trans. Magn.* 38 (3) (2002) 1512–1518.
- [23] F. Tourkhani, P. Viarouge, Accurate analytical model of winding losses in round Litz wire windings[J], *IEEE Trans. Magn.* 37 (1) (2001) 538–543.
- [24] M. Bartoli, N. Noferi, A. Reatti, et al., Modeling Litz-wire winding losses in high-frequency power inductors[C], in: *27th Annual IEEE Power Electronics Specialists Conference (PESC)*, IEEE, Baveno, 1996, pp. 1690–1696.