NUMERICALLY EFFICIENT MODELING OF MODULAR MULTILEVEL CONVERTER WITH INTEGRATED BATTERY ENERGY STORAGE FOR HIGH VOLTAGE DIRECT CURRENT TRANSMISSION

by

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The following individuals certify that they have read, and recommend to the College of Graduate Studies for acceptance, a thesis entitled:

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ABSTRACT

The incorporation of large-scale energy storage into the existing power grid has resulted in a shift in the focus and interest of research and development efforts from traditional two- or three-level converters to modular multilevel converters. This is due to the flexibility of modular multilevel converters in allowing for the integration of battery energy storage systems within their submodule capacitors. Modular multilevel converters with integrated energy storage are currently being targeted for use in low- to medium-voltage grids, where the small battery cells can be efficiently distributed within the converter arms to increase the reliability of the power grid and maintain the necessary dc-link voltage. Therefore, it is essential to model and simulate these energy-storing converters in order to fully understand their operations, control, and performance in all scenarios prior to hardware implementation. However, modeling the complete, detailed circuit structure of modular multilevel converters using Electro-Magnetic Transient (EMT) simulation software, such as PSCAD/EMTDC, EMTP-RV, or MATLAB®/Simulink, can be a cumbersome and computationally expensive task, requiring significant CPU execution time due to a large number of submodules and circuit complexity.

In this thesis, a numerically efficient modeling method is proposed for modular multilevel converters with integrated energy storage. The method involves the use of a detailed equivalent model, which is capable of retaining the information and accuracy of the detailed model while eliminating the need of representing a large number of electrical nodes. This is achieved by using Thevenin equivalent circuits in the discrete-time domain, which reduces the dimension of the equivalent conductance matrix in the EMT simulation. As a result, the computational burden of implementing the detailed converter model on a three-phase system is significantly reduced. When compared to the results of the detailed model, it was found that the equivalent model produces

accurate simulation results and achieves a remarkable improvement of simulation efficiency by 38 folds, compared to that of the DM for the 30-SM-per-arm modular multilevel converters with integrated energy storage.

LAY SUMMARY

This thesis explores a new way to design a type of converter that helps connect clean energy sources to traditional power grids. This converter is called a modular multilevel converter, and it can work with batteries to store unstable power from renewable energy sources and stabilize the power flow between the energy source and the existing power grid. However, using lots of batteries for smaller power grids can be challenging because they need to be charged and discharged evenly. Additionally, the converter has many electronic components that make it difficult to simulate on a computer. The thesis proposes a new, more efficient way to simulate the converter that will help researchers better understand its performance and control. This could help make the use of clean energy sources more efficient and practical in the future.

PREFACE

This thesis was developed and conducted in the School of Engineering, University of British Columbia, Okanagan Campus, under the supervision of Dr. Liwei Wang. I was able to compose and gather all of the contents in this thesis with proper guidance and instructions on the basic working concepts of the power converter from Dr. Wang, modelling suggestions and supports from Dr. Levi Bieber, and Dr. Jintao Han. Future publications of the content in this thesis are planned.

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LIST OF ABBREVIATIONS

AC	Alternating Current
CD	Clamped diode
CHB	Cascaded Half Bridge
CPU	Central Processing Unit
DC	Direct Current
DEM	Detailed Equivalent Model
DM	Detailed Model
EMT	Electro-Magnetic Transient
FB	Full Bridge
HB	Half Bridge
HSM	Hybrid Submodule
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Thyristor
IGCT	Insulated Gate Commutated Thyristor
LCC	Line Commutated Converter
LSC-PWM	Level-Shifted Carrier Pulsed Width Modulation
MATLAB	MATrix LABoratory
MMC	Modular Multilevel Converter
MMC-ES	Modular Multilevel Converter Energy Storage
MNA	Modified Nodal Analysis
MW	Mega Watt
MWh	Mega Watt hour
NLM	Nearest Level Modulation
PCC	Point of Common Coupling
PI	Proportional Integral
PLL	Phase Locked Loop
PQ	Active/Reactive Power
PS-PWM	Phase-Shifted Pulsed Width Modulation
PV	Active/DC Voltage
PWM	Pulsed Width Modulation
RE	Renewable Energy
SMs	Submodules
VSC	Voltage Sourced Converter

ACKNOWLEDGEMENTS

First and foremost, I want to express my praise to the Almighty God, who helped me complete this project by giving me resources, strength, and good health.

I want to express my sincere gratitude to a number of people for their supports during my graduate studies. First, I want to sincerely thank my supervisor, Dr. Liwei Wang, for his enthusiasm, patience, insightful comments, helpful information, wise counsel, and never-ending ideas, all of which have been of great assistance to me throughout the course of my research and writing for this thesis. His vast knowledge, extensive experience, and professional research expertise have made it possible for me to successfully complete this study. It would not have been possible to complete this project without his assistance and direction. I could never have envisioned having a better supervisor in my graduate study.

My gratitude also goes to my supervisory committee members, for their invaluable knowledge, critique and feedbacks that helped polishing this thesis. My special thanks go to Dr. Levi Bieber, who withstood my endless questions and provided me with immense support to get my simulation right.

My heartfelt gratitude goes to the members of my family who were encouraging at all times. I want to express my gratitude to Mrs. Robyn King and family, Mrs. Anne Dyck, and Mrs. Heather Kelz for their unmeasurable support and care throughout my academic journey here in Canada. The most important person I want to thank is my beloved husband, Chris, whose love and encouragement are unconditional.

CHAPTER ONE – INTRODUCTION

1.1 Background

High voltage direct current (HVDC) technology is an alternative, effective, and dependable solution to transmit clean energy from remote locations over long distance which has demonstrated significantly improved performance than high voltage alternating current (HVAC) technology, a traditional method of transmitting large amounts of power generated from fossil fuel energy like coal, oil, and natural gas over long distances. The increasing need to tackle global climate change and the rising global energy demands to achieve clean energy targets propelled researchers to develop advanced HVDC technologies to transmit bulk power over long distance with high efficiency and reliability [1], [2].

The integration of large-scale renewable energy sources, such as onshore/offshore wind farms and solar PV-based plants, with new technologies has become increasingly popular in recent years. These renewable energy sources are often located in remote areas, but can be efficiently connected to the existing power grid through the use of high voltage direct current (HVDC) power transmission systems. This not only improves efficiency and stability of power transmission, but also helps to reduce harmful greenhouse gas emissions. HVDC technology is dominant and well-established innovation that meets the necessary requirements for this integration [3].

Over time, HVDC technology has developed a channel of using fully controllable semiconductor devices like insulated-gate bipolar transistors (IGBTs) and voltage-sourced converter (VSC) topologies to facilitate this interconnection to provide effective voltage support and real power transmission to the power grid [4]. The earliest advancements in HVDC technology

were the thyristor-based and mercury arc valve line-commutated converter (LCC) types. But they were lacking in several areas compared to modern VSC topologies. These older technologies did not have the sophisticated converter control capabilities of newer systems that use turn-on/off switches such as IGBTs [4], [5]. Additionally, they were not able to handle reverse current polarity and could not be easily integrated with weak or passive AC networks, such as offshore wind power plants [4], [6].

Modern VSC technology has several advantages over the LCC, including the ability to control both real and reactive power and to offer a smaller converter footprint due to the elimination of bulky passive filters. As a result, VSC-HVDC topologies have become widely used in the electric power industry due to their improved harmonic performance, high voltage capability, efficiency, superior power quality, and flexibility in converter control functions [7]. Multilevel VSCs have been of particular interest in this field due to their significant impacts and advantages, especially in low-to-medium power applications [8]. The VSC-HVDC system, used for connecting offshore wind farms are illustrated in Fig. 1.1.

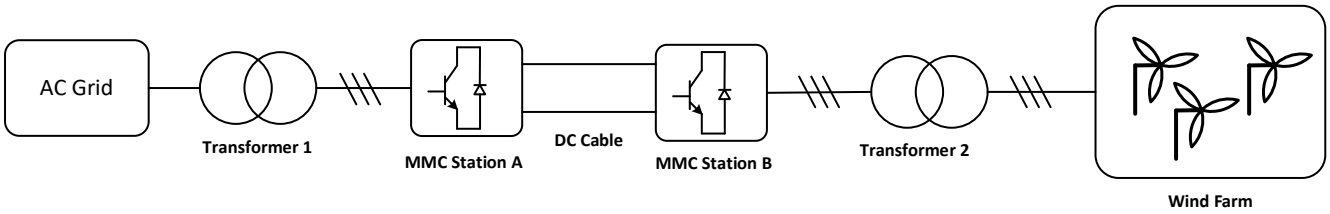


Fig 1.1 VSC-HVDC technology interconnecting an offshore wind farm [4]

HVDC technology is known for its low-loss properties and can be used to interconnect two regional power grids with different frequencies. More recently, it has also been used to provide additional energy generation or storage in areas where it is needed, reducing the stress on the AC

power grid during times of high demand such as the early morning and late evening, or in urban areas where load levelling and power buffering are desired. HVDC transmissions can also support local areas where renewable energy planning is being considered, making it a cost-effective and environmentally friendly solution with minimal technical constraints [9]–[11].

Modular Multilevel Converters (MMCs) are a class of VSC-HVDC technology known for their modularity and high efficiency. They are constructed from a number of identically connected submodules (SMs) in each of the upper and lower arms of a phase, which helps to reduce the switching frequency very close to the fundamental frequency and lowers the level of harmonic content in the output voltage due to its many voltage levels [2], [12]. The MMC is flexible and scalable, as it can easily be expanded by adding additional submodules per converter arm to meet higher DC voltage needs. The scalability of the MMC allows for hundreds of SMs to be used per converter arm.

The MMC technology was first proposed by Siemens and the first commercial project was the Trans Bay Cable project, commissioned in 2010 in the United States, which included 216 SMs for each arm [7], [13]. Since then, many MMC HVDC projects have been implemented and are in operation. MMCs can be connected together within a converter station using similar power submodules to create various conversion designs, such as AC/DC, AC/AC, and DC/DC, and can also be used for energy storage to improve grid performance.

The MMC converter being studied consists of passive elements like inductors, resistors, capacitors, and transformers, as well as semiconductor switches. It allows for the exchange of power between renewable energy sources or energy storage and the AC power grid through the

HVDC transmission system [14], [15]. The structure of the MMC converter is shown in the schematic diagram in Figure 1.2 [4] below.

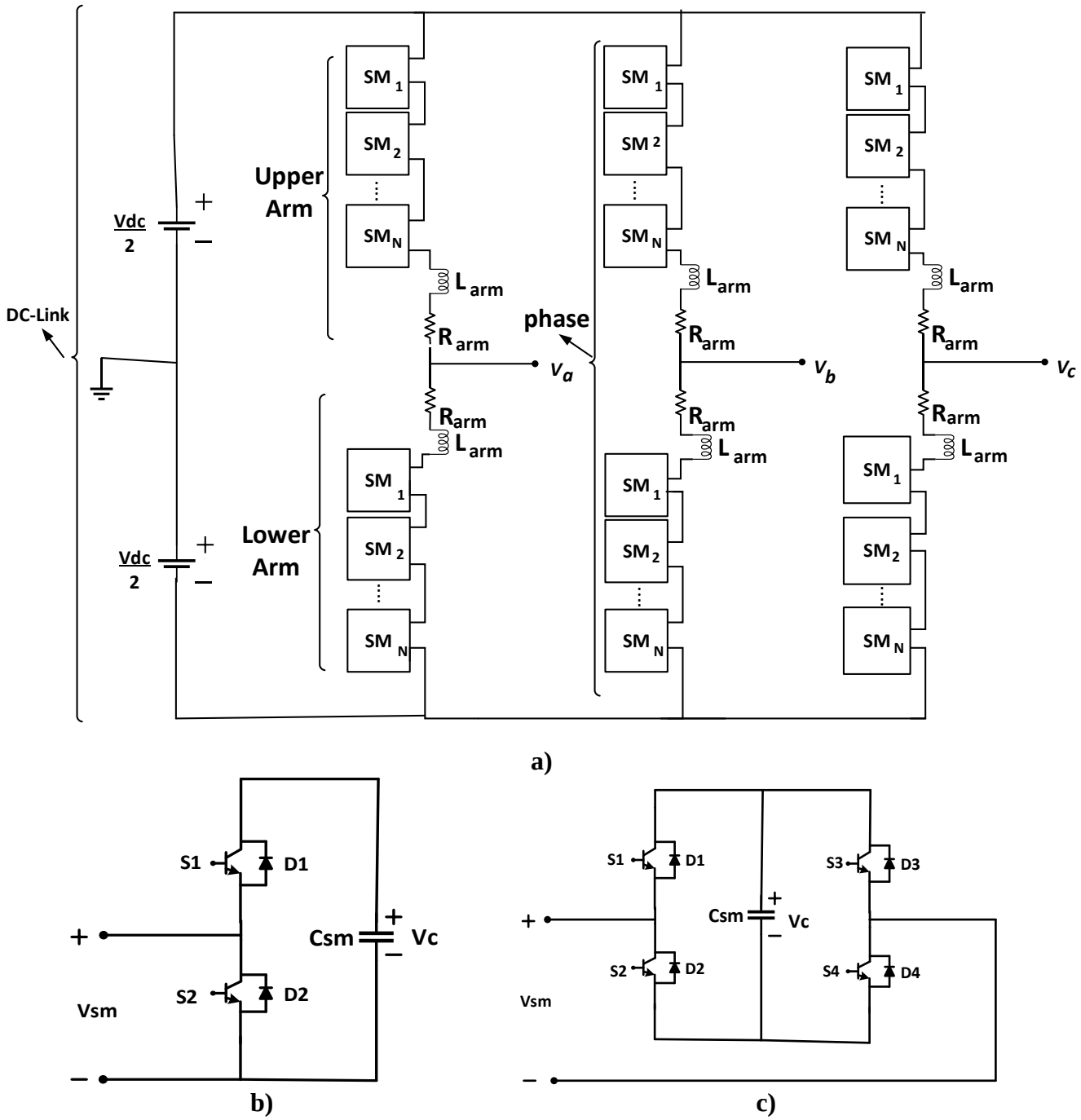


Fig 1.2 (a) MMC Three-Phase Structure (b) Half-Bridge Submodule Topology (c) Full-Bridge Submodule Topology.

As of present, the MMCs' innovation has been extended into different SM topologies like the Half Bridge (HB), Full-Bridge (FB), Clamped-Double (CD), and Hybrid half- and full-bridge Submodule (HSM), where the primary difference between these SM topologies is the polarity (positive or negative) of the output voltage produced by these SMs. The HBSM is the simplest, best-known, and most often employed kind. It also serves as the foundation for other SM types, which provide DC-fault block capabilities [16]. The HBSM single phase MMC can be extended to the three-phase MMC structure. Its dynamics and control are often evaluated on the basis of the working principles of the HBSM [17]. Figure 1.2 shows the MMC structure with the most commonly used conventional submodule topologies.

It is necessary to consider and assess factors such as converter efficiency, functionality, and cost before constructing an MMC due to the different dynamic behaviors of various converter topologies and their DC and AC voltage outputs. To understand the behaviors of the converter during both normal and abnormal operations, dynamic analysis of MMC topologies can be performed using computer simulation. An electromagnetic transient program (EMTP) can be used to obtain information on the switching transition, current, and voltage dynamics of the converter during operations [3].

Simulating the complete circuit structure of a converter for small to medium voltage applications using a detailed model can represent hundreds to thousands of components, such as resistors, capacitors, arresters, transformers, and switching devices. This model captures all the characteristics of the power electronic converter components [18]–[20]. However, as shown in [7], [21], the large number of components in the detailed model generate thousands of electrical

nodes that require the voltages to be calculated at every simulation time step from the system nodal equations with high dimensions. This increases the complexity of the simulation tool and slows down the simulation speed.

To ensure the numerical accuracy of the converter model, it is necessary to use small numerical integration/simulation time steps during the simulation process to capture switching transients [13]. To address this complexity, simpler and more efficient models such as the simplified and averaged value models have been proposed. However, these models do not take into account the individual submodule switching events and individual voltage ripples [22], but rather focus on the slow dynamic behavior of the converter.

1.2 Energy Storage Integration

Integrating renewable energy into the existing power grid presents certain challenges, such as the fluctuating and variable nature of renewable energy sources influenced by weather and environmental/geographical factors, as well as their different power and frequency characteristics that are incompatible with direct connection to the AC system [23], [24]. This deviation in power and frequency can significantly affect the stability and efficiency of the power system. Therefore, researchers must carefully consider an appropriate integration interface. It is essential to maintain power equilibrium and stability during power system disturbance and to provide quick response when there is sudden load growth or a need for supply [25], [26].

An energy storage system integrated into the grid can operate to provide a fast power adjustment. As in [27], [28], the MMC with embedded energy storage was used to offer isolation to the power grid during temporary DC and AC faults as well as maintain the DC link voltage by

balancing the AC/DC power transfer. Energy storage applications can help address power imbalances while promoting energy efficiency for both renewable energy and three-phase synchronous generator energy systems. Flywheels, pumped hydro, batteries, and ultra-capacitors have been the most commonly used energy storage technologies in power systems, and they have been successful in ensuring reliability and power quality since their early implementations [9], [29]–[31].

The direct battery integration method is more commonly used and has a wider range of applications due to its cost-effectiveness, ability to easily scale power rating, lower pollution output, high efficiency, and reliability. However, as discovered in [14], frequent charging and discharging of the batteries can lead to voltage imbalances within the cells, resulting in ripples that shorten their lifespans. To this end, the batteries are integrated in a distributed manner with an efficient control method for the batteries' charging and discharging, which reduces the voltage imbalance within the converter arms.

According to [32], balancing the energy equally among the series-battery strings of energy storage is challenging. However, utilizing a DC-DC bidirectional converter or chopper to connect each of the SM-capacitors of the MMC to a battery cell can improve the traditional direct battery-stacking energy storage technique. This bidirectional DC-DC converter can be operated to charge up each battery voltage to its rated value, as a buck converter, or to maintain the SM-capacitor voltage at its nominal voltage (when acting as a boost converter during times of heavy power demand) [10], [27], [33].

By using the DC-DC converter with the embedded energy storage source, the voltage balance across the DC-link is maintained and equally distributed among each SM. Each bidirectional DC-DC converter is composed of IGBT semiconductor switches with anti-parallel diodes [24]. The energy storage system may be connected at various voltage levels depending on the specific needs and location. It also has the ability to adjust the current ratings of the battery and/or converter to increase output power and energy capacity. The energy storage solution can offer up to 100 MWh of energy capacity and may operate for periods ranging from a few seconds to several hours [34].

1.3 Research Challenge

As the amount of large-scale renewable energy sources integrated into the grid rises to help combat climate change, there is a growing need to manage voltage fluctuation and power difference between the power generated by conventional synchronous generators and the power consumed by loads. One solution being considered is to coordinate the power and energy transfer between the energy storage and the existing AC system to deal with the instantaneous energy balance in power grid. The MMC has the potential to facilitate this integration, but it is complex and time-consuming to simulate it due to the large number of SMs and semiconductor switching events. Therefore, it is important to study the behavior of this converter topology with energy storage systems whose DC-DC converter operates at much higher switching frequency than that of the SMs in the conventional MMC.

Therefore, Electromagnetic Transient Simulation (EMT) tools are used for this type of study. This involves carrying out a detailed simulation study with semiconductor switching that

represents the complete dynamic behavior of the converter system. The EMT simulator converts the converter circuit system in continuous time domain into nodal equations of current sources and conductance in discrete time domain, so that at every switching instance, the network nodal equation is formulated to solve for the node voltages. However, this process requires a large computation time, making it resource-intensive and slow. As a result, an efficient method for system studies is required. First, the Detailed Model (DM) of the MMC with the energy storage system is developed to represent the full converter behavior as benchmark/reference solution. Then, an equivalent model of the converter system, called the Detailed Equivalent Model (DEM), is developed and compared against the DM for improved simulation efficiency and preserved simulation accuracy.

1.3 Research Objectives

The objectives of this thesis and the tasks implemented to achieve them are outlined below:

1. **To implement a control scheme that can manage the energy exchanged between the AC power grid and the MMC with energy storage:** The power transfer between the power grid and the stable steady state and dynamic operations among the six arms will be made possible by a control scheme that incorporates the conventional MMC control with that of the proposed DC-DC converters.
2. **To develop the DC-DC converter control for the energy storage of the HBSM-based MMC:** A complementary switching scheme of the DC-DC converter is designed to operate in boost and buck conditions, defining the charging and discharging of the battery interface and controlling the inductor current within these modes. This is shown through a detailed model simulation with the electromagnetic transient simulation tool (Simulink/MATLAB)

to explore and demonstrate the effectiveness of this type of MMC with integrated battery energy storage.

3. **To develop a Thevenin equivalent circuit of the MMC arm and detailed equivalent model of MMC for accelerated simulation:** A Thevenin equivalent circuit approach is used to formulate the converter arm equivalent circuit in the detailed equivalent model of the MMC to simplify the network nodes and reduce the computational load requirements while preserving the simulation accuracy.
4. **To verify the correctness and viability of the Detailed Equivalent Model (DEM) in comparison with the Detailed Model (DM):** Simulation studies of an MMC with energy storage will validate that the DEM is as accurate as the DM and can be used for the various dynamic system studies.

1.4 Thesis Organization

The thesis is organized into 5 chapters, with a summary of their contents as follows:

Chapter 1: Gives a broad introduction to the HVDC technology, outlining the developed dominant types with their importance, energy storage integration into the grid with the motivation behind it, the research challenge, and the objective steps proposed.

Chapter 2: Provides a complete review of the conventional MMC type with its three-phase structure, presenting an analysis of a single-phase modeling extendable to the other two phases. This also includes the half-bridge SM topology with the common switching techniques, details regarding the MMC-ES operation, and circuit component size selection.

Chapter 3: Presents a complete control methodology for both the energy storage side and the MMC side, outlining the various control schemes implemented on both sides to achieve efficient power transfer, circulating current suppression, and balanced capacitor voltages. Furthermore, the framework for formulating the equivalent circuit, evaluating the nodal voltages, and switching algorithms for the simplified single circuit for the $\boldsymbol{N}$ SMs per arm is developed.

Chapter 4: Entails the simulation result and discussion of the simulation of the numerically efficient DEM of the MMC-ES in comparison to that of the DM. Different numbers of SM per arm will be simulated to validate the capability and numerical accuracy of the DEM in the MMC-ES complex scenarios. Transient behaviors on power change and CPU run time performance speed analysis are to be considered too.

Chapter 5: Gives a concise summary of the MMC-ES study and modeling, outlining the relevant conclusion, and future work recommendations.

CHAPTER TWO – REVIEW ON THE CONVENTIONAL MMC

2.1 Modular Multilevel Converter Circuit Structure

The circuit structure of the three-phase MMC is illustrated in Fig. 2.1 below. It is divided into two parts: a DC side (also known as the DC-link) and an AC side. The AC phase voltages, $\boldsymbol{v_a}, \boldsymbol{v_b}$ and $\boldsymbol{v_c}$ are measured from the phase terminals to the midpoints of the two DC voltage sources**.** The illustration in Fig. 2.1 shows three phase legs and the AC voltages $\boldsymbol{v_a}, \boldsymbol{v_b}$ and $\boldsymbol{v_c}$, for the respective phases [8].

Each phase leg is composed of an upper and lower arm, each of which uses $\boldsymbol{N}$ number of identical submodules that are all connected in series. Each SM can act as a controllable voltage source such that by stacking the SMs serially, the MMC is granted high modularity and scalability characteristics [8], [12]. Furthermore, to achieve higher voltage and power ratings, more SMs can be stacked in each arm without modifying the overall MMC topology.

In this three-phase MMC system, the upper SMs are connected to the positive DC rail and the lower SMs are connected to the negative DC rail. The two arms are connected to the AC-side through inductors and resistors, which act as filters to limit the potential circulating current brought in by voltage difference between the arms and DC-link. The final configuration of the converter system consists of six arms, six arm inductors, and six arm resistors. To generate the required AC phase voltage, the SMs must be switched in accordance with specific switching signals [12].

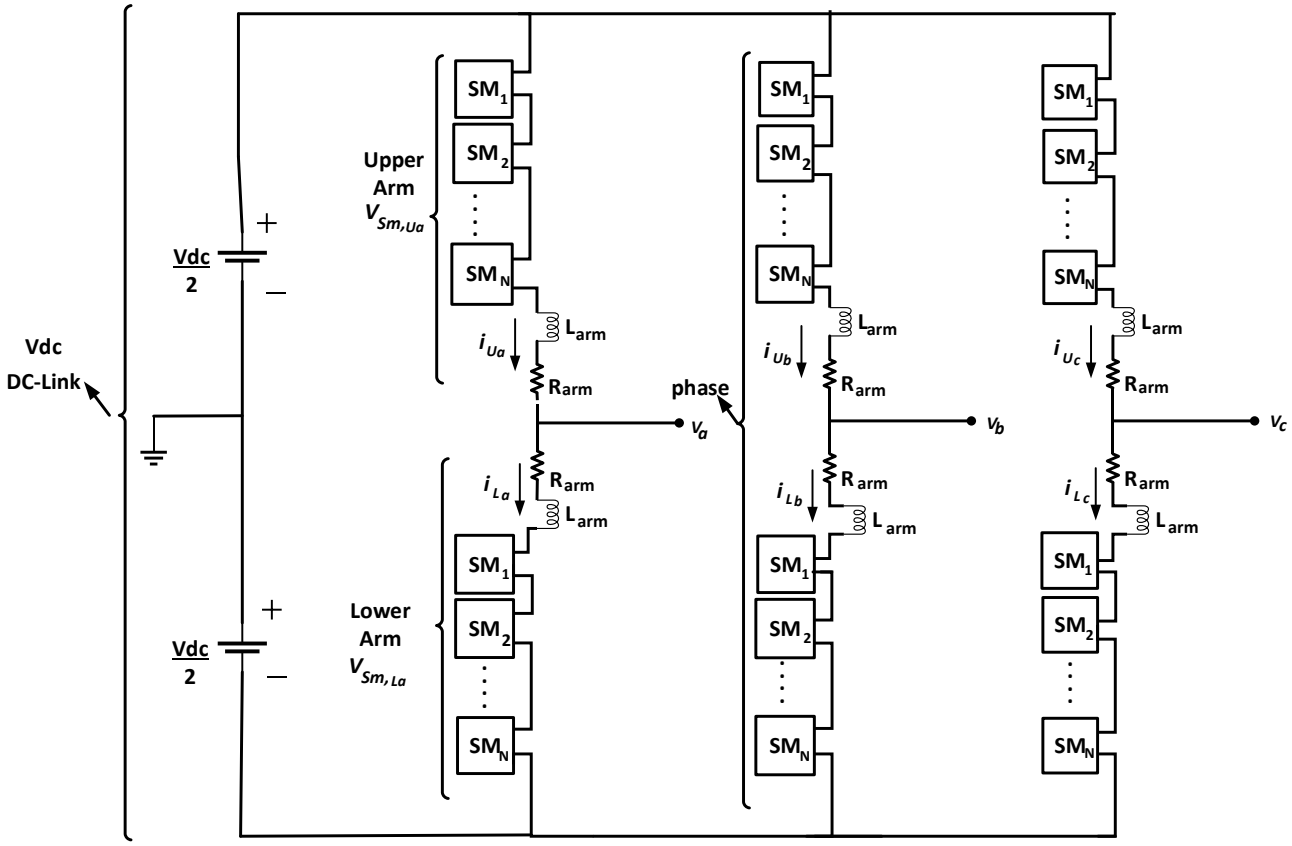


Figure 2.1 Three-phase representation of the MMC structure

At each instant, N_{on} SMs are turned on to insert the submodule capacitors and N_{off} SMs are turned off to bypass the submodule capacitors in each of the a, b, and c phases to produce the phase-to-ground voltage for that phase. The rated voltage of a SM can be calculated using (2.1) based on the number of SMs per arm. The individual SM voltages are assumed to be similar due to SM capacitor voltage balancing control in an arm [2]:

$$V_{sm,rated} = \frac{V_{dc}}{N} \tag{2.1}$$

The maximum voltage level that each MMC phase can generate, at the ac output is of $(\boldsymbol{N+1})$ form. The output voltages of the N SMs in Fig. 2.1 for the upper and lower arms of phase a,

(represented as $V_{sm,Ua}$ and $V_{sm,La}$ in the 2.2 and 2.3 below) can be expressed using Kirchhoff's voltage law (KVL) as:

$$V_{sm,Ua} = \frac{V_{dc,U}}{2} - R_{arm} i_{Ua} - L_{arm} \frac{di_{Ua}}{dt} - V_a(t) \tag{2.2}$$

$$V_{sm,La} = \frac{V_{dc,L}}{2} - R_{arm} i_{La} - L_{arm} \frac{di_{La}}{dt} + V_a(t) \tag{2.3}$$

where $\boldsymbol{i_{Ua}}$ and $\boldsymbol{i_{La}}$ are the upper and lower arm currents, the half DC-link of the upper arm, $\frac{V_{dc,U}}{2}$, and lower arm, $\frac{V_{dc,L}}{2}$, are equal to half of the DC-side voltage, V_{dc}, as:

$$V_{dc,U} = V_{dc,L} = \frac{V_{dc}}{2} \tag{2.4}$$

For the sum of the output voltages of both the upper and lower arms of each phase to be equal to $\boldsymbol{V_{dc}}$, it is necessary for the number of total inserted of SMs of the upper and lower arms to equal N, given as:

$$n_U + n_L = N \tag{2.5}$$

It is noted that the analysis for phase $\boldsymbol{a}$ is valid for the other two phases as well. The AC current can then be expressed from the upper and lower arm currents, $\boldsymbol{i_{Ua}}$ and $\boldsymbol{i_{La}}$ as:

$$i_a = i_{Ua} - i_{La} \tag{2.6}$$

An important objective of the MMC is to achieve a balanced power flow among the upper and lower arms and scale the total voltage to the rated voltage [2], [23].

There are various types of MMC SMs, including half-bridge submodule, full-bridge submodule, mixed half- and full-bridge submodules. For the purpose of this analysis, we will focus solely on half-bridge submodule MMC, which are the fundamental building blocks for other

topologies. While full-bridge submodule MMC has the advantage of additional voltage levels and DC fault-blocking capability, it has increased conduction losses compared to half-bridge submodule MMC due to the use of double number of switches in each submodule [35].

2.2 The Half-Bridge Submodule Topology

The basic structure of the MMC is the half-bridge SM, shown in Fig. 2.2. It includes two IGBT switches (S_1 and S_2), each with an accompanying anti-parallel diode (D_1 and D_2). Both IGBT switches are connected to a DC capacitor (C_{SM}) and operate in complementary manner, meaning that only one can be switched on at a time by the switching signal while the other is switched off. The triggering switching signals determine which switch (S_1 or S_2) is selected to conduct, allowing the SM capacitor to be inserted or bypassed to synthesize the desirable arm voltage and to regulate SM capacitor voltage to the rated value [36].

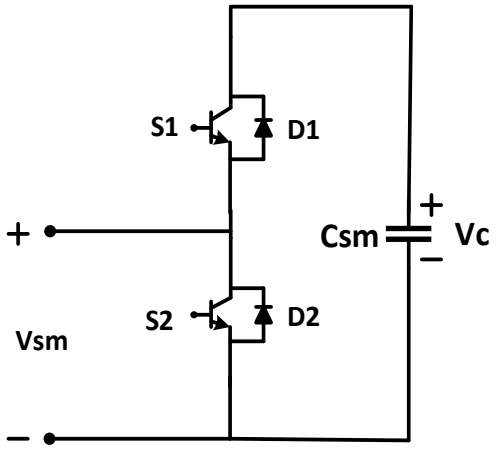


Figure 2.2 Half-Bridge Submodule

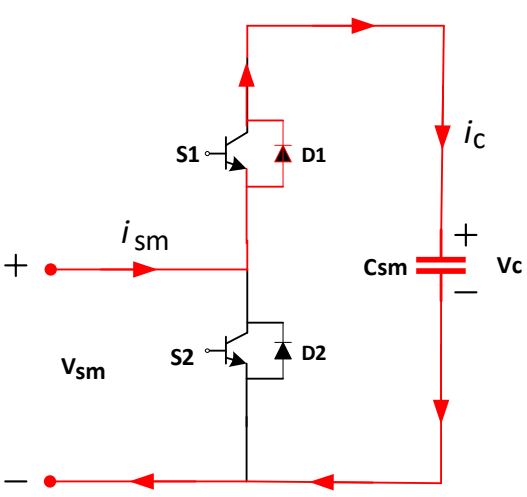
The HBSM is able to operate in two different states: inserted or bypassed state. When in the inserted state, the SM capacitor is included in the conduction path. As both positive and negative current flow through the upper diode/IGBT (D_1 and S_1), the output voltage of the SM (V_{sm}) is equal to the voltage of the SM capacitor (V_c), as shown in Fig. 2.3 and expressed as

$$V_{sm} = V_c \tag{2.7}$$

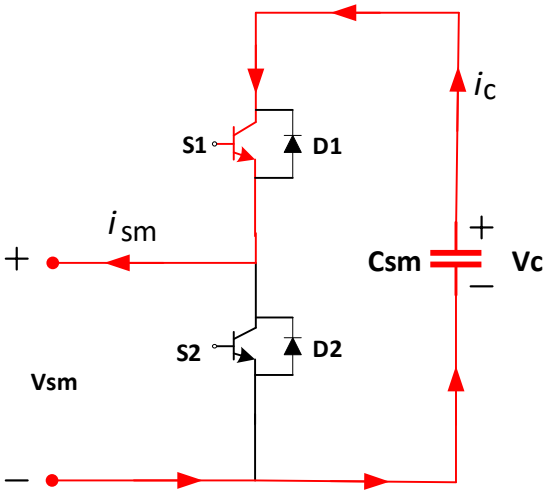
Conversely, in the bypassed state of the SM, with both positive and negative current directions, the conduction is along the lower IGBT/diode, $\boldsymbol{S_2}$ and $\boldsymbol{D_2}$, resulting in the SM output voltage being zero.

The SM capacitor can be charged in the positive current direction and discharged in the negative current direction in the insertion state, as shown in Fig. 2.3. When bypassed, the capacitor maintains its voltage value. The output voltage of each arm is determined by the number of SMs that are selectively inserted or bypassed to achieve the desired voltage [37], [38]. During uncontrolled events such as DC-side faults, the SMs become blocked and the IGBTs are turned off, causing the arm current to flow through the antiparallel diodes. This causes the SM capacitor to charge and discharge through the diodes [19]. The switching status of the switches S_1 and S_2 is determined by whether the SM is inserted or bypassed, and can be represented by the SM switching signal, "$s = 1$" for insertion and "$s = 0$" for bypass. This allows the SM voltage in (2.8) to be re-expressed as:

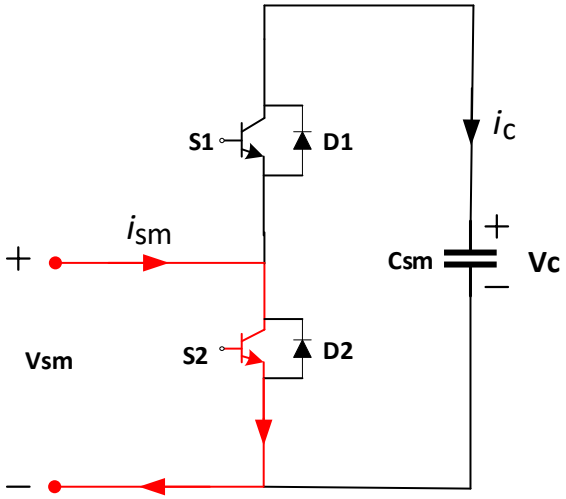
$$V_{sm} = sV_c \tag{2.8}$$



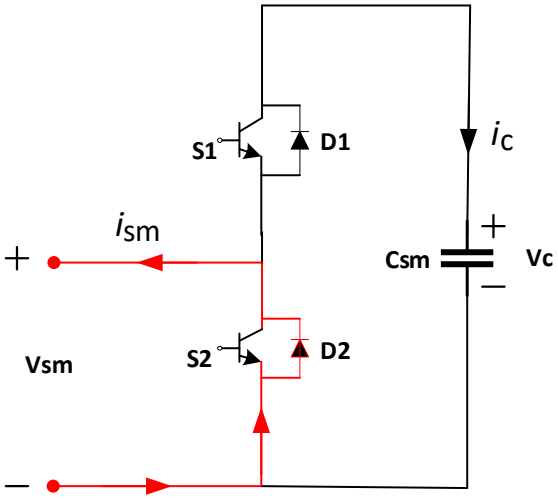
a) Positive current direction when inserted



b) Negative current direction when inserted



c) Positive current direction when bypassed



b) Negative current direction when bypassed

Figure 2.3 Half-Bridge SM in inserted state for a) positive current direction b) negative current direction; bypassed state for c) positive current direction d) negative current direction.

As presented in [39], the SM current can then be deduced as

$$i_c = s i_{sm} \tag{2.9}$$

Extending the switching status to the SMs to determine the total output voltage of the upper (U) or the lower (L) arm, one may first consider that the SM capacitor V_c is charged and has an initial voltage V_o, then

$$i_c = C\frac{dV_c}{dt} \tag{2.10}$$

$$V_c = V_o + \frac{1}{C}\int_0^T i_c dt \tag{2.11}$$

In addition, the overall power loss in the MMC is reduced by 1% compared to earlier converter types [39] and the power exchange across SM can be given as;

$$P_{dc} = P_{ac} + P_{loss} \tag{2.12}$$

$$V_{dc}i_{dc} = \sum_{j=a,b,c} V_{ac,j}i_j + P_{loss} \tag{2.13}$$

Table 2.1 shows the summarized switching operations of the HB and its equivalent output voltages.

Table 2. 1 summarized switching operations of the HB and its equivalent output voltages

SM status	S_1 state	S_2 state	i_{SM}	V_c status	i_{SM} direction	V_{SM}
ON	ON	OFF	Positive (> 0)	Charging	D_1	V_c
ON	ON	OFF	Negative (< 0)	Discharging	S_1	V_c
OFF	OFF	ON	Positive (> 0)	Maintained	S_2	0
OFF	OFF	ON	Negative (< 0)	Maintained	D_2	0

2.3 Switching Control of the Half Bridge SM

In order to maintain the rated values of the capacitor voltage of the individual HB SMs, the switching of the SMs is carefully selected. The decision of which SM capacitor to insert or bypass, as well as the number of SMs to be in inserted or bypassed state, allows for the output voltage of each arm to be equal to the arm voltage reference [32]. The SM output voltage is controlled by pulse width modulation (PWM), which varies the duration of the switches' ON and OFF periods through the use of a switching or modulation technique. Different techniques have been proposed based on the number of voltage levels that the MMC SMs need to reach in order to produce a high-quality output voltage while minimizing harmonic distortion. These techniques will be discussed in the following section.

2.3.1 Pulse Width Modulation Methods

The ON/OFF switching of the individual SMs is controlled through the use of an individual modulating signal, often called PWM. There are various PWM strategies that differ based on the switching frequency used, including high, low, and fundamental frequencies [33]. The commonly used method is the carrier-based PWM technique, which involves comparing a carrier signal (usually a triangular waveform) with a reference signal (the desired sinusoidal waveform).

The reference signal's amplitude fluctuates between the maximum and the minimum of the carrier wave. The carrier wave signal typically has an amplitude between 1 and -1. If the carrier wave's amplitude is outside this range, there will not be a pulsed or gated signal output. The generated pulsed signal produced by comparing the carrier and reference signals, triggers the complementary states of the switches at a specific instant, resulting in the fast average output voltage being sinusoidal on the AC side [33].

In order to determine the appropriate PWM method to use in [40], the switching frequency and control of the number of inserted or bypassed SMs were considered. When few SMs are present and high switching frequencies are necessary, techniques such as Phase-Shifted Modulation (PS-PWM) and Level-Shifted Carrier Modulation (LSC-PWM) from [41] may be utilized. However, as the number of SMs increases, it is more effective to use PWM schemes with low or fundamental switching frequencies, such as Nearest Level Modulation (NLM), to minimize losses [31], [36]. Fig. 2.4 below showcases examples of different categories of PWM schemes.

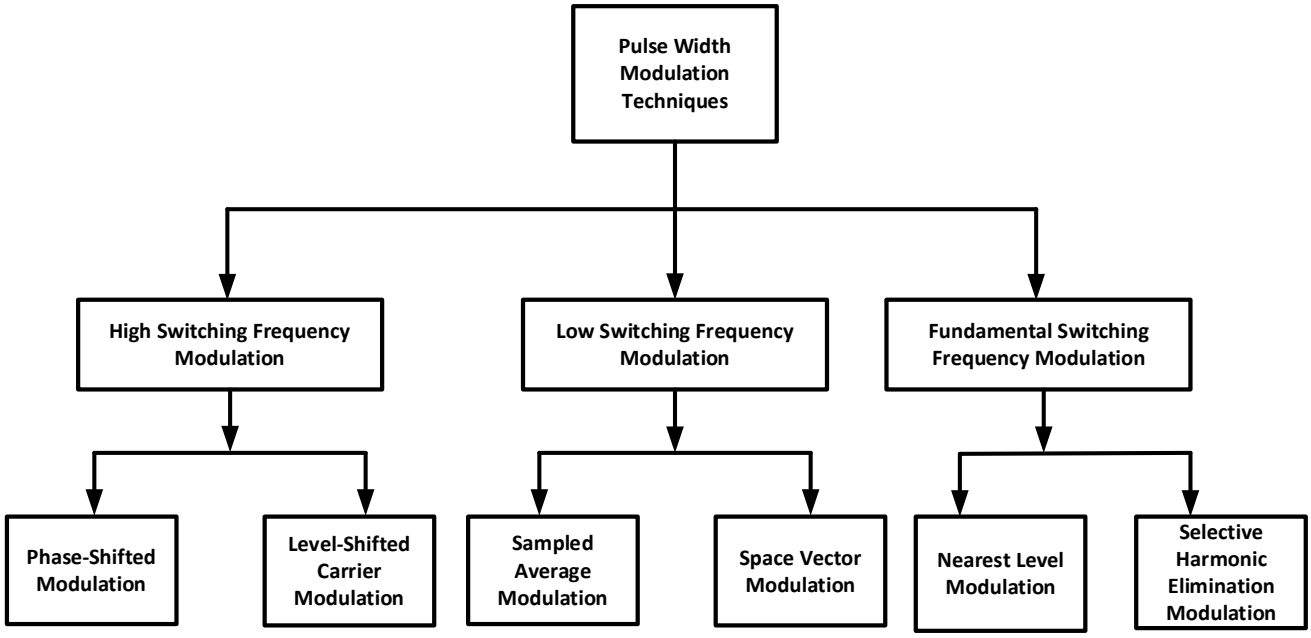


Figure 2.1 Pulse Width Modulation Scheme Classification [41]

2.3.2 Phase-Shifted Modulation Technique

For Phase-Shifted (PS) PWM in an MMC, $2N$ carrier waveforms are required for each phase, resulting in N carrier signals per arm at the same switching frequency and peak amplitude. These carrier signals are phase-shifted at various angles and positioned within the range of the reference

signal's frequency. The number of switched SMs in each arm is determined by the number of carrier signals that fall below the reference waveform at any given time [18]. The angle at which the carrier signals are shifted can be calculated using the following formula:

$$\theta_c = \frac{2\pi}{N} \tag{2.14}$$

The phase angle for i^{th} carrier signal in the upper arm is

$$\theta_{U(i)} = \theta + \frac{2\pi}{N} \times (i-1) \tag{2.15}$$

while the i^{th} carrier signal in the lower arm can also be calculated as

$$\theta_{L(i)} = \frac{2\pi}{N} \times (i-1) \tag{2.16}$$

where N is the number of SMs per arm and θ is the displacement angle between the upper and lower carriers [42]. This method is categorized as a high-frequency switching modulation type and is often used because it produces high voltage levels and balances the SM capacitor voltages with a high-frequency carrier wave. Fig. 2.5 illustrates the phase-shifted modulation technique.

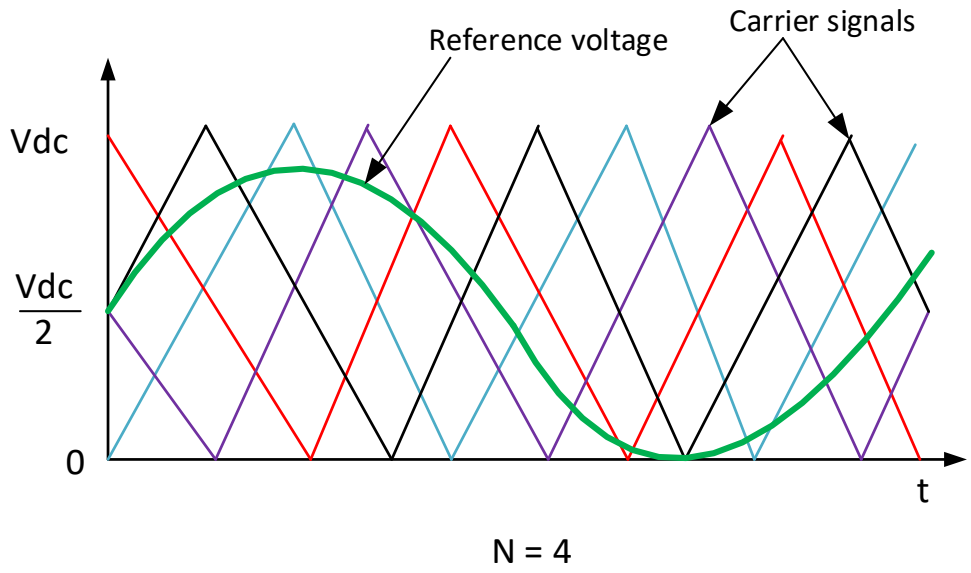


Figure 2.2 Phase-Shifted Modulation Method

2.3.3 Nearest Level Modulation Technique

The Nearest Level Modulation (NLM) technique, shown in Fig. 2.6, is a method of fundamental frequency modulation that is used when a large number of SMs with potentially low switching frequencies are needed to generate medium to high voltage output. This technique, referred to as "staircase modulation," reduces switching losses from the individual SMs by combining them into a voltage level that resembles a staircase [43], [44]. It does this through the use of a round function, which rounds the voltages from the inner control to the nearest integer of the converter's voltage level. The SM capacitor voltages must be balanced, requiring the gating or switching signals of the SMs to be determined by the predicted voltage levels. Each of the three phases will have its own control, as implemented in [45], [46].

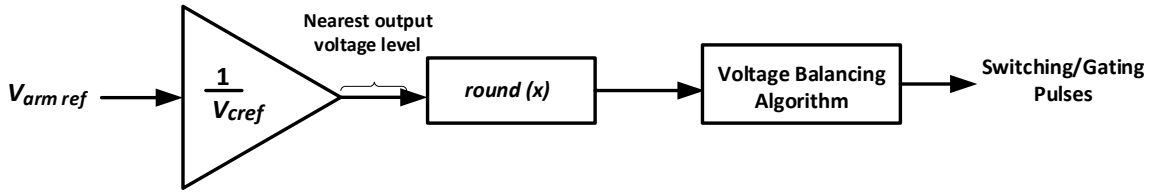


Figure 2.3 Nearest Level Modulation Method

2.4 MMC with Integrated Energy Storage

The modular multilevel converter with integrated energy storage, or MMC-ES, is a variant of the conventional MMC topology that includes batteries as a means of energy storage. One advantage of the MMC-ES is its simplified topology, in which the interfacing DC-DC converter between the batteries and SMs can provide a low-current ripple flow into the batteries and the SM capacitors.

As shown in Fig. 2.7, the MMC-ES has a three-phase structure with battery cells distributed across each individual SM, which improves the efficiency and lifespan of the batteries and allows for better management of the current discharge, compared to a centralized battery connection where battery discharge is more difficult to control.

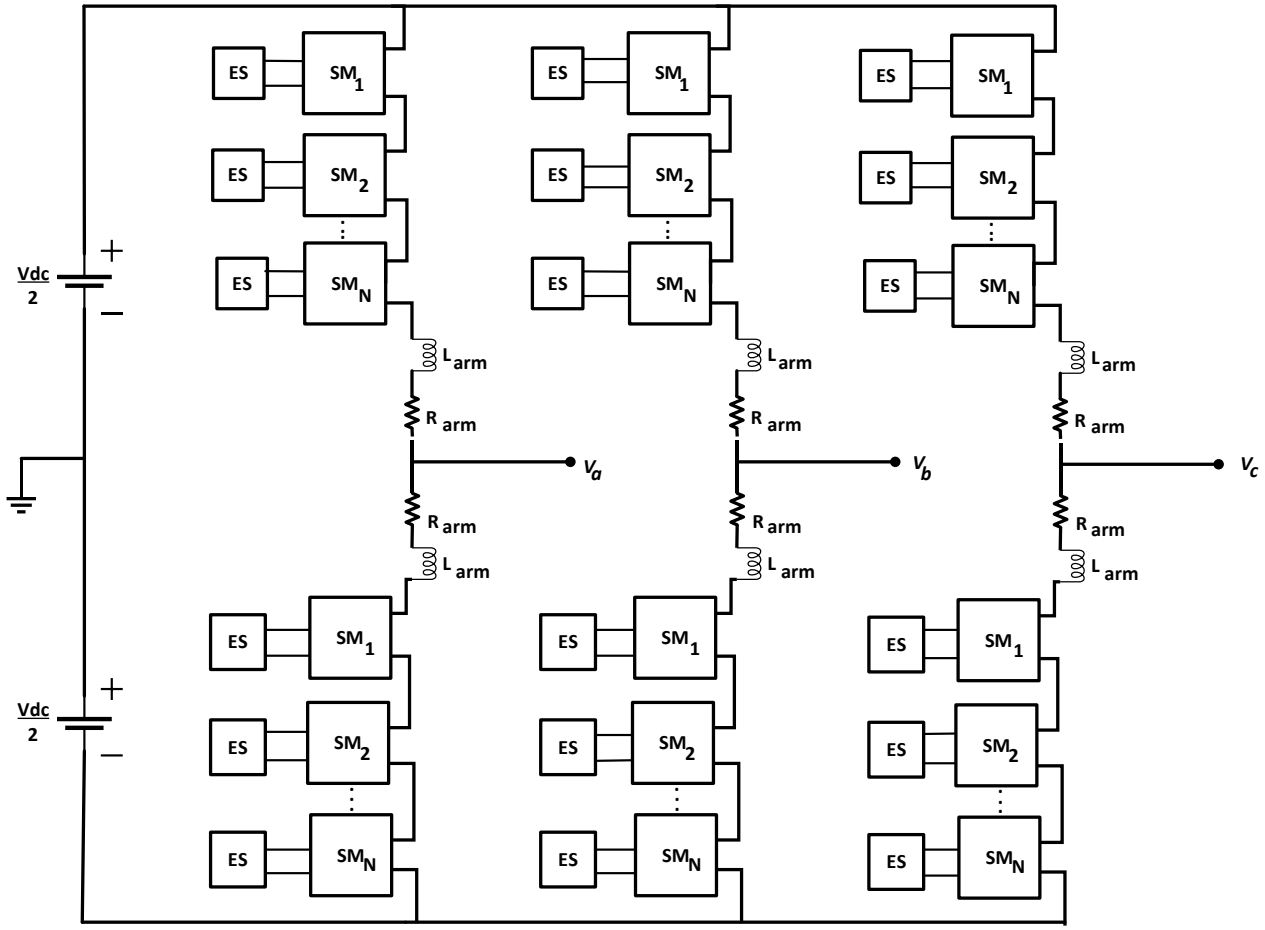


Figure 2.4 Three-phase MMC with distributed battery storage

Each of the phases shares a common DC link, with the individual SMs contributing to the total power exchanged between the three-phase AC grid and the DC side. This enables uniform distribution of the high voltage concentration at the DC-link to various SM circuits with lower voltage ratings [14], [29]. The power transfer is expressed as

$$P_{DC} = P_{AC} + P_{Bat} \tag{2.17}$$

The addition of ES to the three-phase conventional MMC increases the complexity of the converter circuit structure and control methods for the batteries' charge and discharge in both inverter and rectifier operations of the MMC-ES [47].

2.4.1 SM Structure of the MMC-ES

The HBSM structure of the MMC-ES is depicted in Fig. 2.8 [22]. The simple and basic structure of the HBSM topology has been chosen to connect the battery cell to the SM capacitor through a bidirectional DC-DC converter. The DC-DC converter consists of two IGBT switches, $\boldsymbol{S_3}$ and $\boldsymbol{S_4}$, with anti-parallel diodes, $\boldsymbol{D_3}$ and $\boldsymbol{D_4}$, an equivalent resistance $\boldsymbol{R_{dcdc}}$ and an inductor $\boldsymbol{L_{dcdc}}$. This inductor acts as a filter that limits the current ripples from the SM switches from entering the battery [48]. The AC-DC side of the MMC operates in the same manner as a conventional MMC without ES technology.

The bidirectional DC-DC converter facilitates the active power transfer between the battery and SM capacitor through the use of buck and boost modes. This is in contrast to the typical MMC, which has zero average real power absorption for the SM capacitors [14], [27]. The storage batteries are often operated at a voltage that is lower than the SM capacitor voltage.

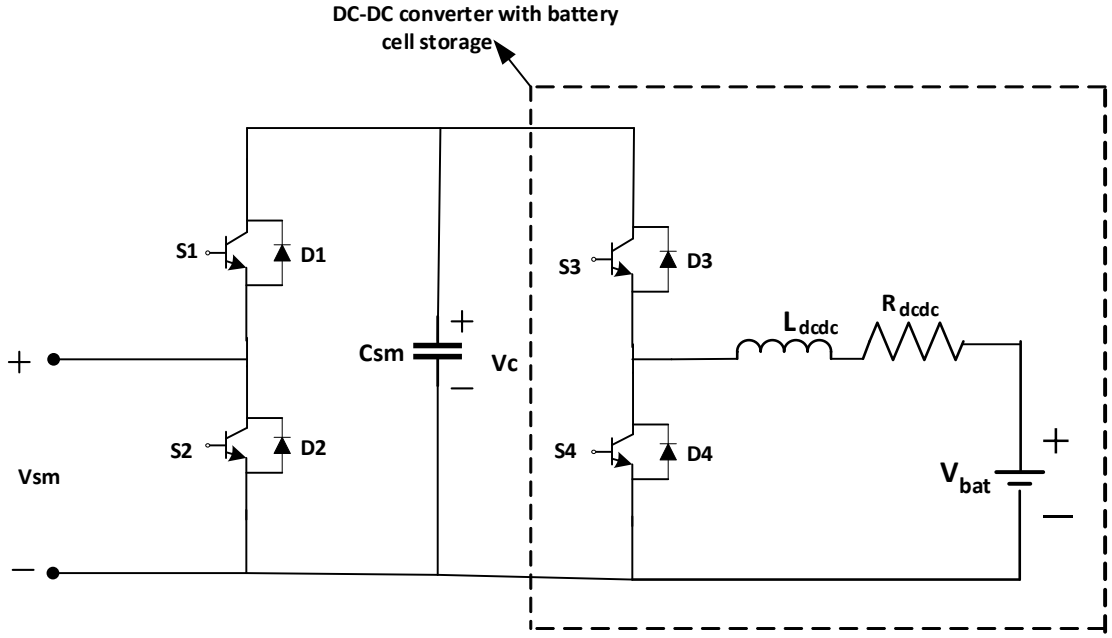
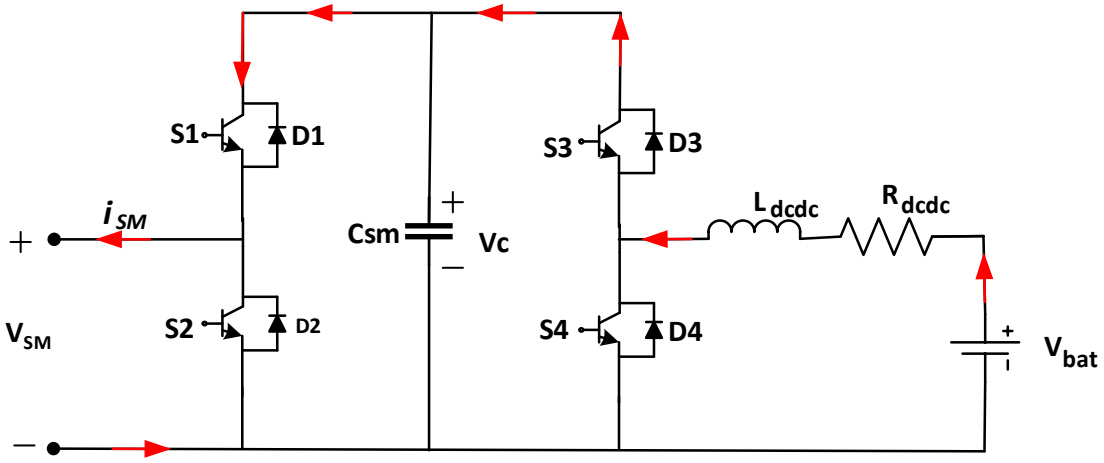


Figure 2.5 Half-bridge SM topology with energy storage

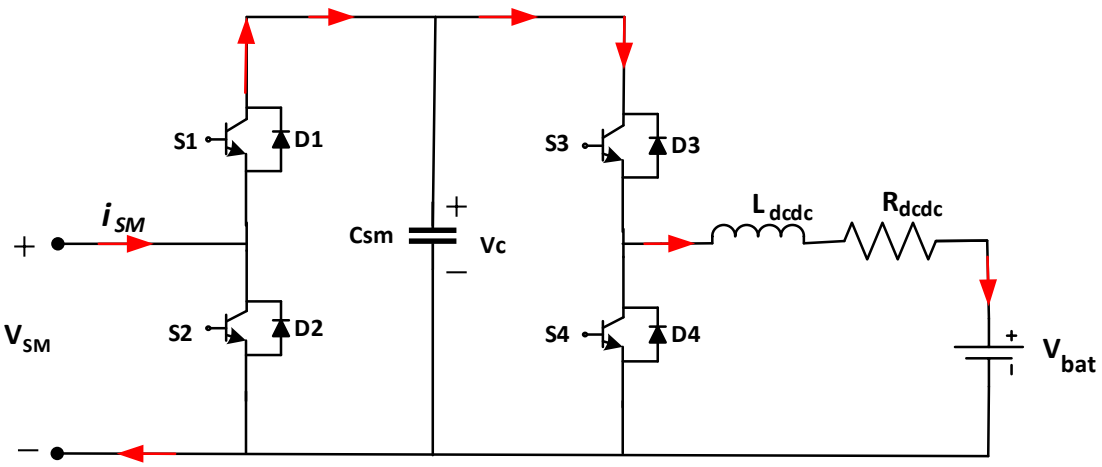
2.4.2 DC-DC Converter Structure of the MMC-ES

The DC-DC converter acts as a boost converter when charging the SM capacitor and as a buck converter when recharging the battery. This process must be consistent in order to maintain the power balance in (2.17). The conduction path during the positive current direction is via the upper diode, D_1, and upper switch, S_1, during the negative current direction in the boost mode, while, the buck mode conduction paths are via the lower switch, S_2, and lower diode, D_2, during the positive and negative current directions, respectively [21], [27]. The power flow for the boost and buck modes is illustrated in Fig 2.9 with the use of red arrows.



Power flow within SM energy storage in Boost mode of DC-DC converter

a)



b)

Figure 2.6 Switching direction of power flow in the DC-DC converter a) Boost mode b) Buck mode

The total power contributed by the energy storage side can be calculated as

$$P_E = 6NV_{bat}I_L \tag{2.18}$$

when the energy storage is in the discharging state (that is, buck mode), $P_E > 0$ and during charging state (boost mode), $P_E < 0$ [43]. The Full-Bridge SM can also be applicable to the operation of the MMC-ES, but the focus herein is on the HB type of MMC-ES which is simpler and more widely adopted in the industry.

The switching operation of switches $\boldsymbol{S_3}$ or $\boldsymbol{S_4}$ is controlled by a pulsed gating signal generated by comparing a carrier triangular wave with an amplitude that varies between 1 and 0 to a duty ratio value calculated by a proportional integral (PI) controller. This comparison is summarized below in two cases [43], [44] for both the ON and OFF states of the branch switches.

- When duty ratio is greater than the carrier wave, $\boldsymbol{GS_{(t)} = 1}$ and $\boldsymbol{S_1\ or\ D_1}$ will conduct in the boost mode when the time $\boldsymbol{t}$ ranges from $\boldsymbol{0 < t \leq DT}$.
- When duty ratio is less than the carrier wave, $\boldsymbol{GS_{(t)} = 0}$ and $\boldsymbol{S_2\ or\ D_2}$ will conduct in the buck mode when the time $\boldsymbol{t}$ ranges from $\boldsymbol{DT < t < T}$.

Above, $\boldsymbol{GS_{(t)}}$ is the gating of switching signal for $\boldsymbol{S_1}$, $\boldsymbol{T}$ is the period of one ON and OFF switching interval, and $\boldsymbol{DT}$ is the ON duration. A complementary output for the inductor current and voltage that matches the gating signal is likewise produced by these switching states and the dynamic relations of the SM capacitor voltages and the inductor currents can be determined by the behavior of the switches in the ON and OFF states.

Controlling the switching status of the DC-DC converter allows for precise regulation of the charging and discharging of the battery current as well as the power transferred or contributed by the battery. By choosing high switching frequencies in the kHz range, the inductor current ripples can be effectively controlled and reduced while maintaining the rated SM capacitor voltages, as demonstrated in studies [44], [45].

2.4.3 Inductor and Capacitor Size Selection

Previous research, such as that in [49], has demonstrated that the size of the SM capacitor has a direct relationship with current ripple and an inverse relationship with AC output frequency for a given voltage ripple. The ability of the MMC-ES system to sustain high voltages and peak currents while remaining reliable over its lifespan is crucial. Careful selection of the SM capacitor size is also important to prevent the need for large, costly capacitors, which would increase the overall size and cost of the system [46], [48].

While ensuring the size of the capacitor meets the required maximum voltage ripple, it is important to avoid overcharging or undercharging the capacitor as this could lead to failure or impaired arm current controllability, which can compromise the overall stability of the converter [46]. The minimal capacitance of the series-connected SMs in the MMC-ES was determined through various methods that consider the energy and voltage variations of the SMs during normal operation. The SM capacitance can be directly linked to the number of SMs, the voltage ripple, and the energy capacity of the MMC-ES. To determine the minimum capacitance required for maintaining the voltage ripple within a certain range, the circulating current scheme and voltage injection method were utilized in [50], [51]. The minimum capacitance of the SM capacitor can be calculated based on the amount of energy the SMs can store, taking into account both the bound voltage and peak-to-peak energy deviation [46]:

$$E_{SM(t)} = N\frac{C_{SM}}{2}{V_{SM(t)}}^2 \tag{2.19}$$

When the minimum and maximum deviations are set in the assumption, the capacitance can be represented as

$$C_{SM} = \frac{\Delta E_{SM}}{2N{V_{SM,nom}}^2\Delta V} \tag{2.20}$$

$\boldsymbol{\Delta E_{SM}}$ is the peak-to-peak energy deviation of the SMs, $\boldsymbol{\Delta V}$ is the maximum relative voltage deviation around the SM capacitor normal voltage, $\boldsymbol{V_{SM,nom}}$.

The inductor is a crucial component for the efficient operation of the ES, as its inductance plays a key role in limiting voltage ripple of the SM capacitor and suppressing the switching current ripple into the battery side. To determine the appropriate inductance, factors such as the ON state period of the switches, particularly the upper switch of the DC-DC converter, and the

battery voltage level must be taken into consideration. The goal is to keep the inductor current ripple within 20% of the rated average inductor current for normal operation. To calculate the instantaneous voltage-drop across the inductor, the following formula can be used:

$$V_L = L\frac{di_L}{dt} \tag{2.21}$$

For a small time period Δt of which the upper switch is in ON state, (2.21) can be evaluated as:

$$v_L = L\frac{\Delta i_L}{\Delta t} \tag{2.22}$$

Relating (2.22) to the DC-DC converter side circuit in Fig. 2.6, the battery voltage V_{bat} can be calculated in the ON state time period of $0 < t \leq DT$ as:

$$V_{bat} = \frac{L_{dcdc}\,\Delta i_L}{DT} \tag{2.23}$$

then evaluating the equation above for the inductance is given as:

$$L_{dcdc} = \frac{V_{bat}DT}{\Delta i_L} \tag{2.24}$$

Furthermore, if the steady state switching operation of the DC-DC converter only in one cycle is considered, the relationship between the battery voltage V_{bat}, and the SM capacitor voltage V_c across the loop in Fig. 2.9 can be expressed as:

$$V_{bat}DT + V_{bat}(1-D) - V_c(1-D) = 0 \tag{2.25}$$

Re-arranging the equation as:

$$V_{bat}DT + (V_{bat} - V_c)(1 - D) = 0 \quad (2.26)$$

Re-evaluating to define the duty ratio in one cycle of a steady state is given as:

$$D = 1 - \frac{V_{bat}}{V_c} \quad (2.27)$$

2.5 Operation of the MMC with Energy Storage

In order to accommodate the normal operation of the MMC with the battery storage integrated, a larger size capacitance is typically needed compared to a conventional MMC to accommodate the possible voltage ripples across the SM capacitor. However, the SM capacitor voltage ripple reduction control should be designed to decrease and maintain the voltage ripple to a specific limit, even though this may result in additional expenses [29]. Many approaches have been proposed by researchers to maintain the rated SM voltage objective. One approach, described in [25], involved using the circulating current along the arms to reduce ripples in conventional MMC control. This method also had the added benefit of increasing peak arm currents through the injection of harmonics into the circulating current, though it also increased power losses in the MMC-ES.

The MMC-ES system control requires two types of control as shown in Fig. 2.10. The first category is at the MMC side, where the chosen PWM scheme work in conjunction with SM capacitor voltage balancing and arm voltage controls to generate a command that regulates the voltage levels and average SM capacitor voltage. These controls help to eliminate the arm circulating current. The second category is the management of battery power and current on the ES side in order to either limit the injection of arm circulating current or decrease the capacitor

voltage ripples, which can alter the active power in the upper and lower arms [42]. The MMC-ES control hierarchy is depicted in Fig. 2.10 and will be discussed in the following chapter.

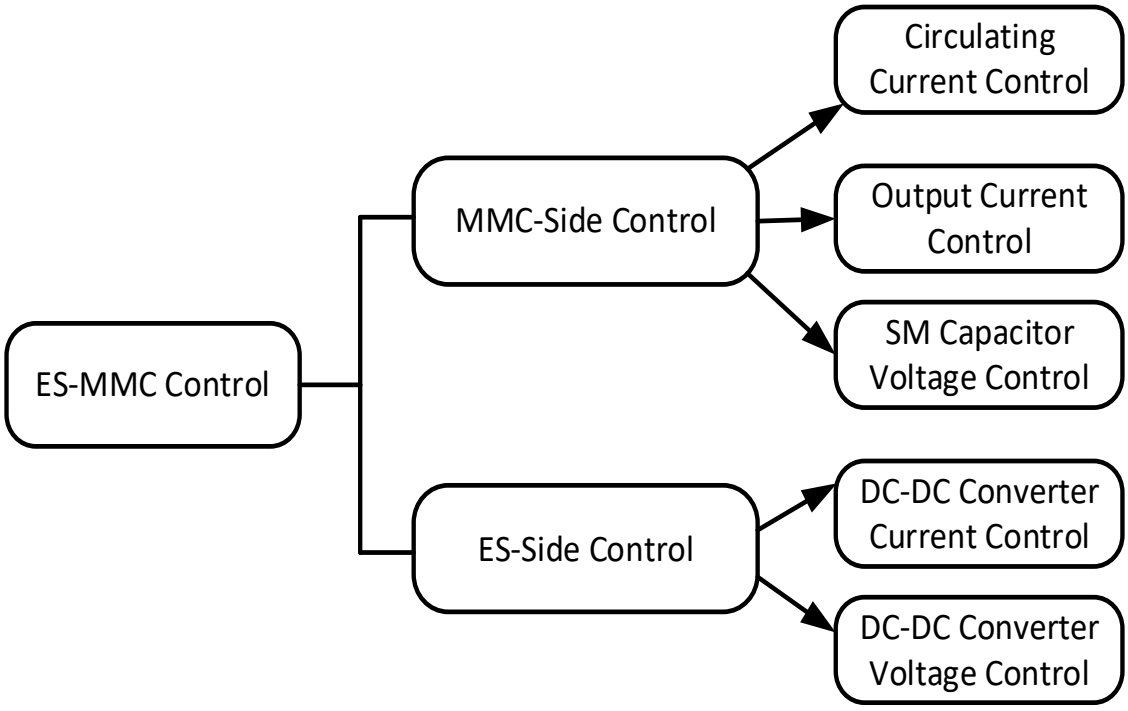


Figure 2.7 Overview of the MMC-ES Control Classification

CHAPTER THREE – CONTROL METHODOLOGY AND EFFICIENT MODELING

3.1 Control of the MMC-Side

Power converters often utilize proportional integral (PI) regulators in their control methods to improve transient performance and ensure proper system behavior at steady state. These PI regulators or controllers help to align the actual output parameters with the desired reference parameters, thereby minimizing error. The main focus of converter operations and goals of the MMC will be to control reactive power/AC voltage magnitude and real power/DC voltage [42].

In [52], a back-to-back HVDC system with two converters were utilized to facilitate bidirectional power transfer between two AC grids. One converter functioned as a rectifier, feeding AC real power to the DC-link and controlling the reactive power or AC voltage, while the other MMC-ES acted as an inverter, converting the DC power to AC real power [7]. Alternatively, a single-point MMC-ES with a large energy storage capacity can be implemented to support an existing AC grid.

There are several approaches to MMC-side power control that have been proposed in the literature, including direct power control and vector control methods. Direct power control involves directly regulating the AC voltage through the modulation index, while vector control, also known as "decoupled control", is a more commonly used method that considers voltage and inner current control loop regulations [53]. This thesis focuses on vector control as the primary method of MMC-side power control.

3.1.1 Decoupled Control Methods on the MMC-Side

In this thesis, the MMC-ES system was evaluated under balanced AC grid conditions, with a constant DC-link voltage on the DC-side. The nonlinear characteristics of the system and the functionalities of the MMC-ES are determined by the control loop implemented. In balanced grid operations, an outer and inner current loop were utilized to manage real and reactive power or voltage using a dq reference frame [2], [10], [33].

3.1.2 Phase Locked Loop (PLL)

First, the three-phase voltages at the point of common coupling (PCC) between the grid and the converter were measured using a phase-locked loop (PLL) system. This was done to determine the angular speed and frequency at which the converter was synchronized with the grid. To ensure the stability of the grid, an real and reactive power were injected into it. The control system utilized a technique similar to that described in [36] and depicted in Fig. 3.1 to achieve this stability.

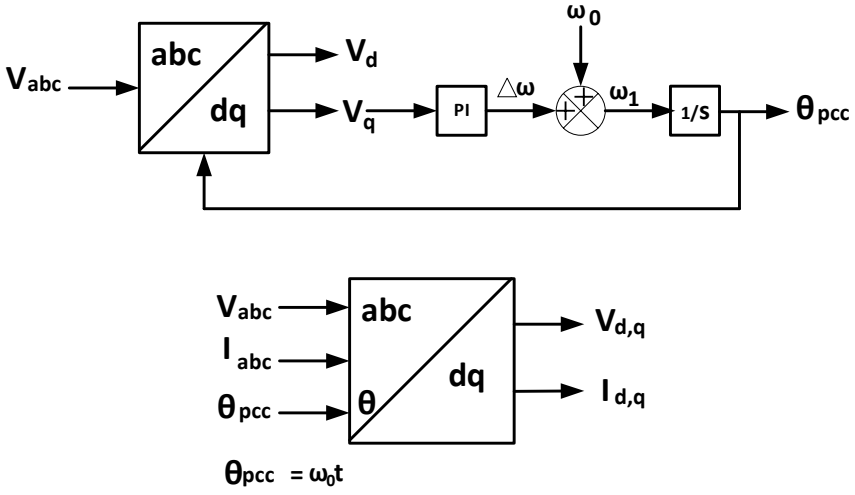


Figure 3.1 Block diagram of PLL

Furthermore, the Park transformation method was utilized to convert the grid voltages and currents from ABC coordinates to synchronous dq-frame reference parameters, which have a DC nature and rotate at the angular phase angle determined by the previously mentioned PLL. The performance of the MMC-ES was influenced by the control in the dq coordinate, which serves as the input to the outer loop control.

3.1.3 Outer Loop Power Control

A real and reactive power control or an AC/DC voltage control can be used in the outer loop control of the converter. The grid voltage is first transformed into the dq vector domain using a phase-locked loop (PLL) and then is combined with the desired real and reactive power references for the AC grid to generate the current reference parameters in the dq coordinate [54]. The voltage in the q-axis is set to zero by properly choosing the initial angle of the dq-axis coordinate, while the voltage in the d-axis is only used by the controller to determine the reference currents for the inner current loop. The reactive power compensates the system in the q-axis and is responsible for the controller's output in the q-axis. The real and reactive powers controlled by the power controller, as shown in Fig. 3.2, are defined as follows [43], [55].

$$P_{ref} = \frac{3}{2} v_d i_{dref} \tag{3.1}$$

$$Q_{ref} = -\frac{3}{2} v_d i_{qref} \tag{3.2}$$

where v_d is the grid voltage along the d-axis [55], [56].

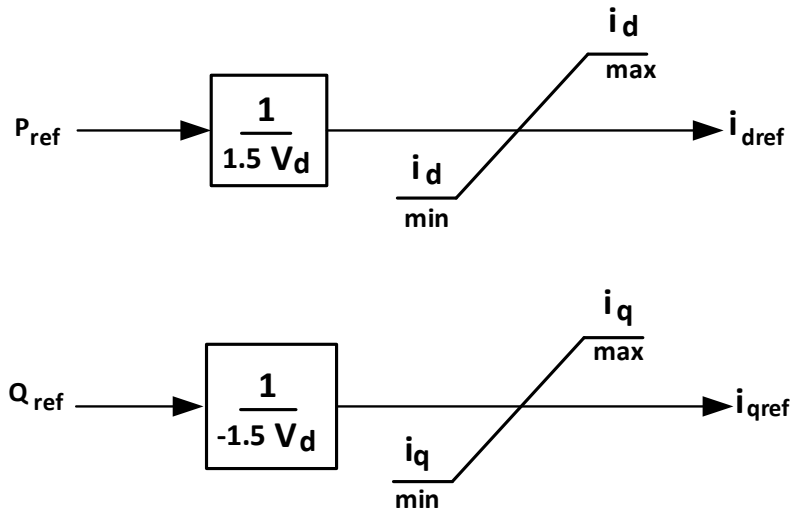


Figure 3.2 PQ Outer Loop Controller

The AC/DC voltage control method can also be used for an MMC-ES, whether it is acting as a rectifier or inverter, depending on the control objective. In this scenario, the reference RMS/DC value of the AC/DC voltage on the AC grid or DC system is linked with either the instantaneous real or reactive power to produce the inner current control input parameters in the dq-coordinate [56]. In general, the current based vector control method is chosen to prevent the converter current exceeding its limit which could cause converter and semiconductor damages [43].

3.1.4 Circulating Current Suppression Control

The addition of battery cells to the conventional MMC impacts the power flow of the system, potentially causing an unbalanced state of charge in the batteries. This unbalanced state can lead to unequal averaged voltages between the upper and lower arms of a phase and fluctuations in the capacitor voltages [33], [57].

The internal voltage difference between the arms or phases generates a circulating current that flows through the three phases and is composed of both DC and AC current components. The

AC and DC currents contribute to power transfer from the arms to the AC grid and from the DC side to the arms, respectively [27].As previously illustrated in Fig. 2.1, the upper and lower arm currents are represented, respectively as:

$$i_{Ua} = \frac{i_a}{2} + \frac{i_{dc}}{3} + i_{cir,a} \tag{3.3}$$

$$i_{La} = -\frac{i_a}{2} + \frac{i_{dc}}{3} + i_{cir,a} \tag{3.4}$$

The circulating current can be derived using (3.3) and (3.4), as follows:

$$i_{cir,a} = \frac{i_{Ua} + i_{La}}{2} - \frac{i_{dc}}{3} \tag{3.5}$$

where the phase-a AC output voltage of the MMC is characterized by the equations:

$$V_a = U_a - \frac{R_{arm}}{2} i_a - \frac{L_{arm}}{2} \frac{di_a}{dt} \tag{3.6}$$

$$L_{arm} \frac{di_{cir,a}}{dt} + R_{arm} i_{cir,a} = \frac{V_{dc}}{2} - \frac{V_{sm,Ua} + V_{sm,La}}{2} \tag{3.7}$$

U_a term is defined as the controlled inner voltage generated between the upper and lower arms given as:

$$U_a = \frac{V_{sm,La} - V_{sm,Ua}}{2} \tag{3.8}$$

Therefore, phase-A circulating current $i_{cir,a}$ can be controlled via the difference voltage:

$$V_{diff,a} = L_{arm} \frac{di_{cir,a}}{dt} + R_{arm} i_{cir,a} \tag{3.9}$$

where

$$V_{diff,a} = \frac{V_{dc}}{2} - \frac{V_{sm,Ua} + V_{sm,La}}{2} \tag{3.10}$$

The presence of a circulating current amplifies the harmonics presented with a frequency of twice the fundamental component. The most significant harmonics in the circulating current are given as follows:

$$i_{cir,a} = \frac{i_{dc}}{3} + I_{2f} \sin(2\omega_0 t + \varphi_0) \tag{3.11}$$

$$i_{cir,b} = \frac{i_{dc}}{3} + I_{2f} \sin(2\omega_0 t + \varphi_0 - \frac{2\pi}{3}) \tag{3.12}$$

$$i_{cir,c} = \frac{i_{dc}}{3} + I_{2f} \sin(2\omega_0 t + \varphi_0 + \frac{2\pi}{3}) \tag{3.13}$$

where I_{2f} is the peak value of the double-line frequency, φ_0 is the phase angle and ω_0 is the fundamental frequency [51], [58].

Furthermore, the Park transformation is used to transform variables from abc coordinate to the dq reference frame. Substituting (3.11) into (3.9), and doing same for the phases b and c, the dynamics for the voltage difference are given as:

$$\begin{bmatrix} V_{diff,d} \\ V_{diff,q} \end{bmatrix} = L_0 \frac{d}{dt} \begin{bmatrix} i_{cir,d} \\ i_{cir,q} \end{bmatrix} + R_0 \begin{bmatrix} i_{cir,d} \\ i_{cir,q} \end{bmatrix} + \begin{bmatrix} 0 & -2\omega_0 L_0 \\ 2\omega_0 L_0 & 0 \end{bmatrix} \begin{bmatrix} i_{cir,d} \\ i_{cir,q} \end{bmatrix} \tag{3.14}$$

The reference currents of zero in the dq domain are used to suppress the 2nd order circulating current in the arms in the dq rotating reference frame through the use of a pair of PI controllers, as depicted in Figure 3.3. The Circulating Current Suppression Control (CCSC) output V_{cir_ref} is generated by the PI controllers in the dq coordinate and is then transformed back to the abc coordinates using inverse Park's transformation. The CCSC output voltage V_{cir_ref} of each arm is added to the reference voltage of the corresponding arm to regulate the 2nd order harmonic current in the arm to zero [41], [58], [59].

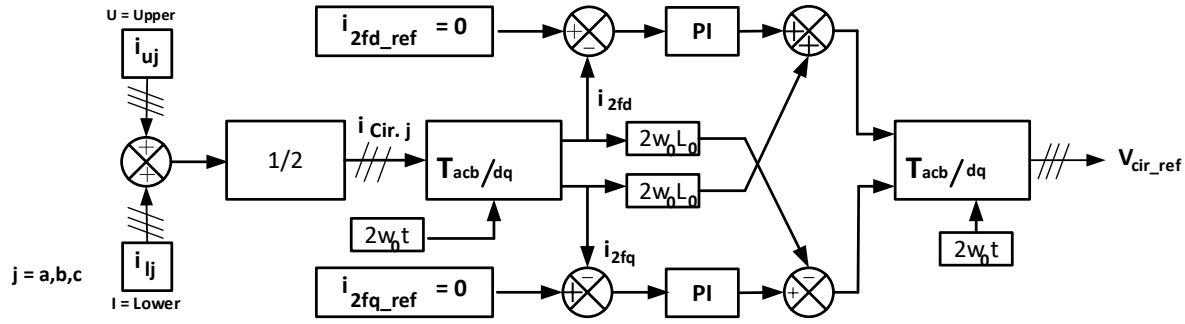


Figure 3.3 Circulating Current Suppression Control

The Park transformation matrix $T_{acb/dq}$ used in the circuit above is of this format;

$$T_{acb/dq} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.15}$$

3.1.5 Inner Loop Current Control

The inner current loop plays a crucial role in regulating the error signal by comparing the reference current from the outer loop to the measured grid current in the dq reference frame. The d- and q-axis voltage variables are coupled to enable voltage compensation, in which any error is sent to the controller for correction. This helps to cancel the impedance or resistance in the grid voltages and drives the output voltages to follow the desired reference values decomposed in the dq coordinate [19], [52] and [56]. Two PI controllers are used to regulate the steady-state errors to zero in the inner-loop control of the current variables in the dq frame variables [41], [52]. The current controllers are obtained as [43]:

$$V_{dref} = V_d + \omega L i_q - [K_p(i_d{}^{ref} - i_d) + K_i \int (i_d{}^{ref} - i_d)dt] \tag{3.16}$$

$$V_{qref} = V_q - \omega L i_d - [K_p(i_q{}^{ref} - i_d) + K_i \int (i_q{}^{ref} - i_d)dt] \tag{3.17}$$

Fig. 3.4 gives the schematic diagram of the inner current control where the K_p and K_i are the gains of the PI; V_d and V_q are the grid voltage at the Point of Common Coupling (PCC). The inner loop control output variables V_{dref} and V_{qref} are first transformed back from dq reference frame to the abc coordinate to serve as the input signals to the PWM control of the converter.

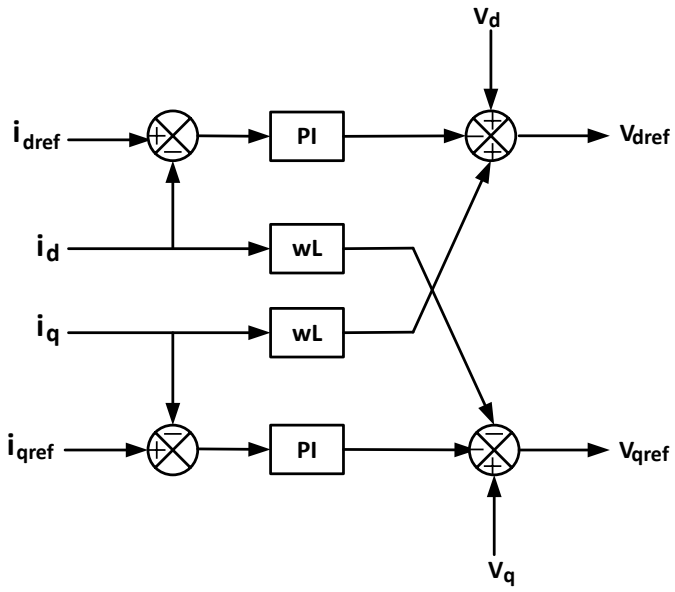


Figure 3.4 Inner Loop Current Controller

3.1.6 SM Capacitor Voltage Balancing and Sorting Algorithm

As stated in [60], balancing the SM capacitor voltages and maintaining the energy stored in SM capacitors is crucial for the stable operation of the MMC. The SM capacitor voltage balancing algorithm requires the input of the number of submodules that are in the inserted state per arm and the arm current direction (positive or negative) when the active SMs are inserted. When a SM is in the bypassed state, the SM capacitor voltages remain unchanged. During normal operation, when a positive arm current flows, the SM capacitor balancing algorithm selects the SM capacitors with their voltages below the nominal value to charge, which raises their voltages

to the rated value. On the other hand, a negative arm current discharges those inserted SM with the highest SM voltages to maintain the SM voltages at the nominal value. Therefore, the SM capacitor voltages in each arm will be sorted in ascending or descending order before each SM switching event occurs [57]. The stable arm voltages can be maintained by ensuring the balancing of the SM capacitor voltages within the arms. The SM capacitor voltage sorting algorithm and balancing control, combined with the arm voltage modulation method that supplies the switching signals and controls the charging and discharging states of the SMs in each arm, are used to generate the switching signals for the SMs.

However, incorporating a battery side to a typical MMC can make converter control more challenging. It is important to monitor each battery cell to ensure they are not charged or discharged beyond a certain capacity. The controlled charging state of the SM capacitors can significantly affect the normal operation of each battery. Therefore, the state-of-charge equalization and DC-link voltage control must be combined in the MMC-ES [33], [41]. The overall control structure of the MMC is shown in Fig. 3.5, which includes various control loops such as the circulating current suppression controller, inner current and outer power controllers, and SM voltage balancing control.

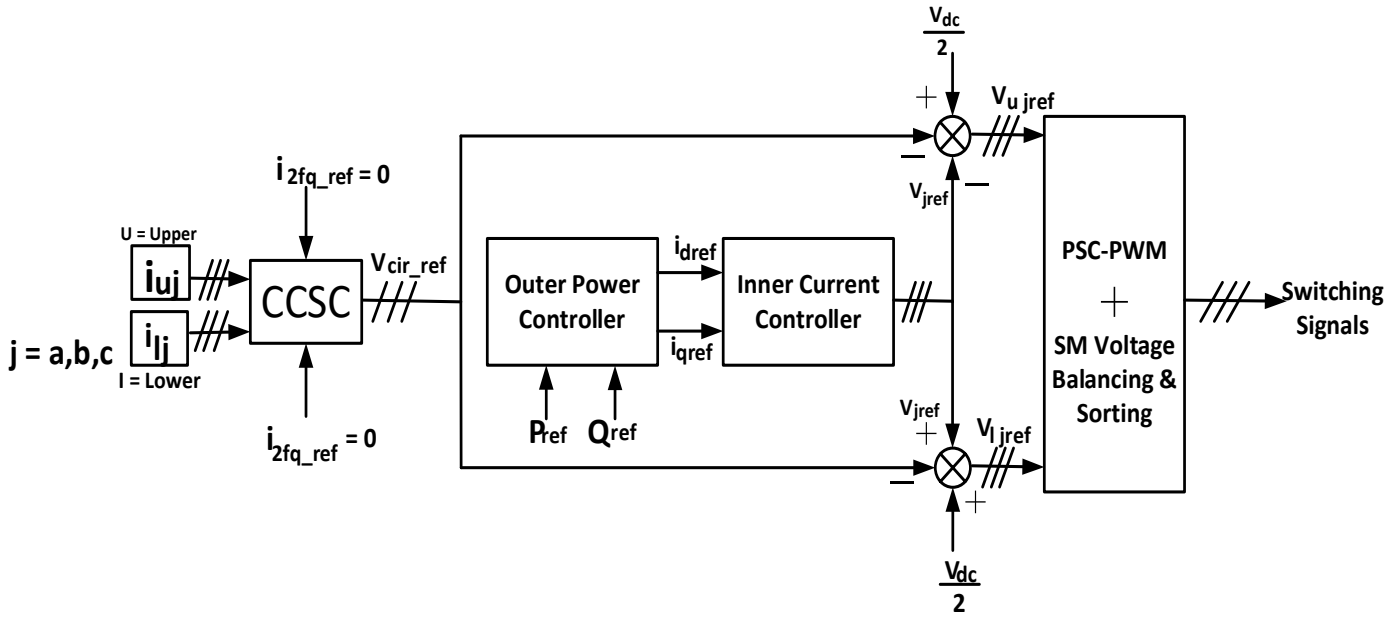


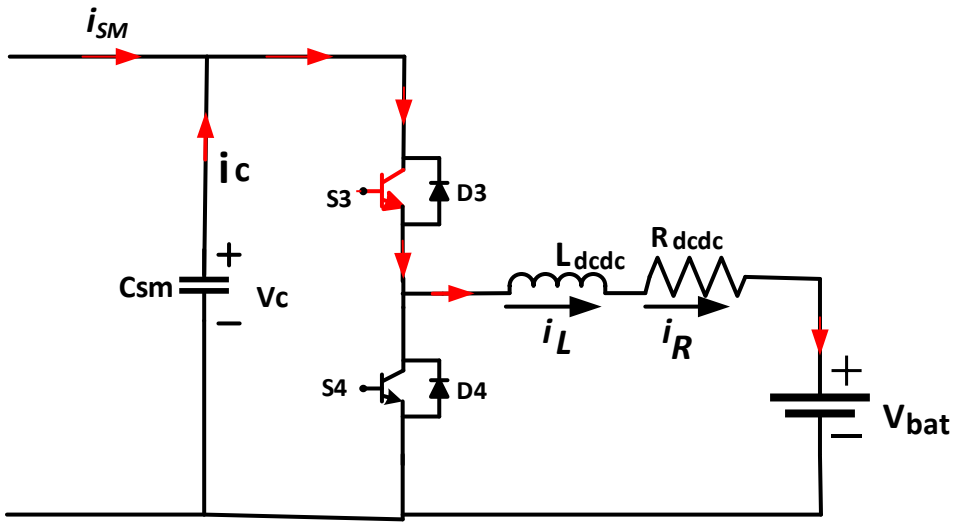
Figure 3.5 Overall control structure showing the various control steps

3.2 Battery-Side Control

Both the voltage balancing of the SM capacitors and the stability of the converter can be affected by the presence of battery storage. To prevent interference of the battery current with the capacitor voltage control during charging and discharging, a battery control strategy is implemented, which involves using a DC-DC converter controller to manage the voltage and current of the SM capacitor and the DC-DC converter inductor on the energy storage side. It may also include the battery's charging control if the SM capacitor voltage balancing is not adequately managed by the DC-link [60]. The capacitor voltage balance can be maintained as long as the system's DC link remains stable, limiting the contribution from the ES side to the voltage balancing efforts.

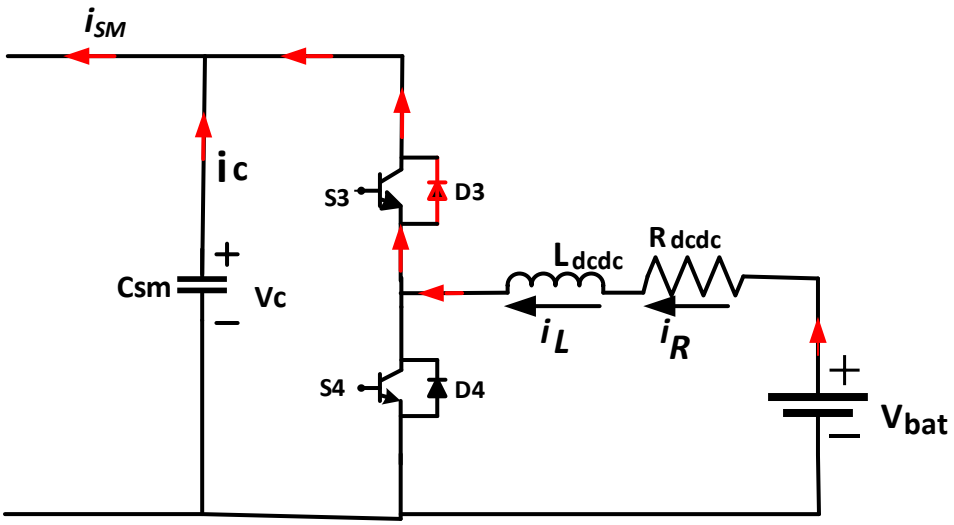
3.2.1 DC-DC Converter Control

The DC-DC converter connects the energy storage side to a SM capacitor and consists of two control loops: an inner loop that controls the inductor current and an outer loop that controls the capacitor voltage. To prevent excessive drainage of battery current, current limiters are utilized to set bound limits to inductor current to increase battery lifespan and durability. Bidirectional operations – the buck discharging mode and the boost charging mode – are regulated through the management of peak current injection using one switch in each mode, as previously discussed. To further analyze the operation of the DC-DC converter in Section 2.2, the inductor current for each state is linearized using the equivalent circuit derived from the red arrows shown in Fig. 3.6.



DC-DC converter operation in the Buck mode when it charges the Battery cell

a)



b)

Figure 3.6 Submodule DC-DC Converter operations

First, analyzing the state variables for the switches in the boost mode considering small signals are expressed as follows [43]. When S_3 is OFF and S_4 is ON:

$$L_{dcdc}\frac{di_L(t)}{dt} + i_R R_{dcdc} = V_{bat}(t) \tag{3.18}$$

$$C_{SM}\frac{dv_c(t)}{dt} = -i_{SM}(t) \tag{3.19}$$

When S_3 is ON and S_4 is OFF:

$$L_{dcdc}\frac{di_L(t)}{dt} + i_R R_{dcdc} = V_{bat}(t) - v_c(t) \tag{3.20}$$

$$C_{SM}\frac{dv_c(t)}{dt} = i_L(t) - i_{SM}(t) \tag{3.21}$$

3.2.2 Inductor Current Controller

The inductor current loop is designed as a PI regulator for the battery current flowing into the DC side of the MMC in boost mode. The equivalent inductor current per switching cycle can be calculated from (3.18) to (3.21) through following equations:

$$L_{dcdc}\frac{di_L}{dt} + R_{dcdc}i_L = V_{bat} - V_o \tag{3.22}$$

where the V_o is the output voltage of the DC-DC converter in a period of time T_s depending on the switching state;

$$V_o = \begin{cases} 0 & S_4\ ON,\ S_3\ OFF \\ V_c & S_3\ ON,\ S_4\ OFF \end{cases} \tag{3.23}$$

The average voltage output $\bar{V}_o$ over a switch period of T_s is given below.

$$\bar{V}_o = \frac{(1-D)T_s\ V_c}{T_s} \tag{3.24}$$

where D is the duty ratio, calculated using the ON time of S_4 over the switching period, we can further simplify (3.24) into the following:

$$\bar{V}_o = (1-D)V_c \tag{3.25}$$

Re-evaluating the differential equations in (3.22) using Laplace transformation gives:

$$V_{bat}(s) - \bar{V}_o(s) = R_{dcdc}I_L(s) + L_{dcdc}sI_L(s) \tag{3.26}$$

$$I_{L(s)} = \frac{1}{s}\frac{V_{bat}(s) - \bar{V}_o(s) - R_{dcdc}I_L(s)}{L_{dcdc}} \tag{3.27}$$

The inductor current controller designed based on (3.27) is presented in Fig. 3.7.

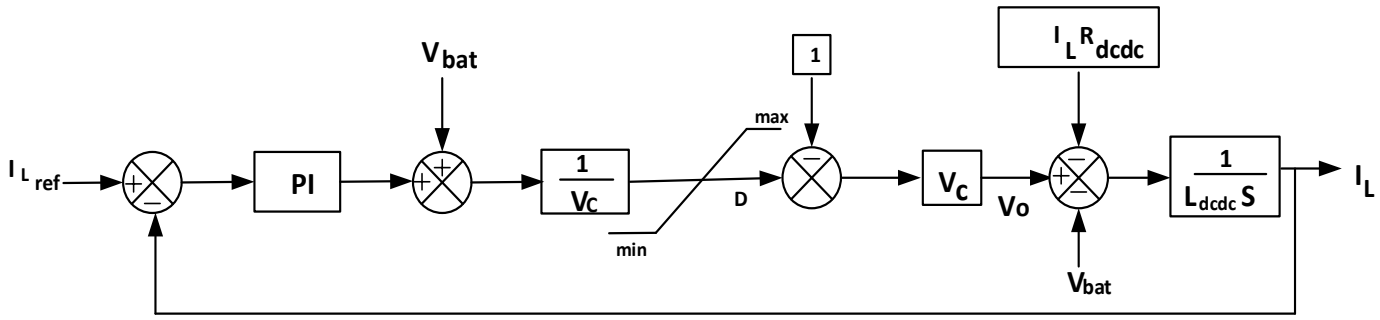


Figure 3.7 Inductor Current Loop

To ensure accurate control, the closed loop system monitors the inductor current, which is used as the control variable to correct any errors generated by the difference between the actual inductor current and the reference. The PI controller, with its integral and proportional gains carefully tuned, is used to ensure that the output value accurately followed the input command. In Fig. 3.7, the limiter constrains the controller's output to ensure that the duty cycle from the controller to the PWM generator is comparable to the carrier signal at frequencies. To ensure a stable charge and discharge of the battery current, the reference current value is determined by normalizing the rated power of the six arms and dividing it equally among the SMs in each arm as:

$$I_{L,ref} = \frac{P_{Eref}}{6NV_{bat}} \tag{3.28}$$

P_{Eref} is the battery power reference from the energy management system and was expected to contribute a percentage of the DC-link power as stated in (2.17) and (2.18), *N* is the number of SMs per arm, V_{bat} is the battery voltage, selected to be lower than the V_c. The output of the voltage controller, $I_{L,ref}$, can be used to set the current reference for discharging the battery through the closed loop system. This ensures that the power is evenly distributed and the battery current is equal for all inductors.

3.2.3 Inductor Voltage Controller

The DC-DC converter in this system uses a voltage loop controller with a current loop controller for double closed-loop control to calculate the duty ratio of the pulse signals that direct the switching of the devices. As depicted in Fig. 3.8, this controller operates as a closed-loop system, similar to the current loop controller. The two loops are placed in parallel to superimpose their signals, resulting in improved battery current discharge and minimized SM capacitor voltage ripples. The error difference between the reference and actual voltage is also effectively reduced through the use of a PI controller.

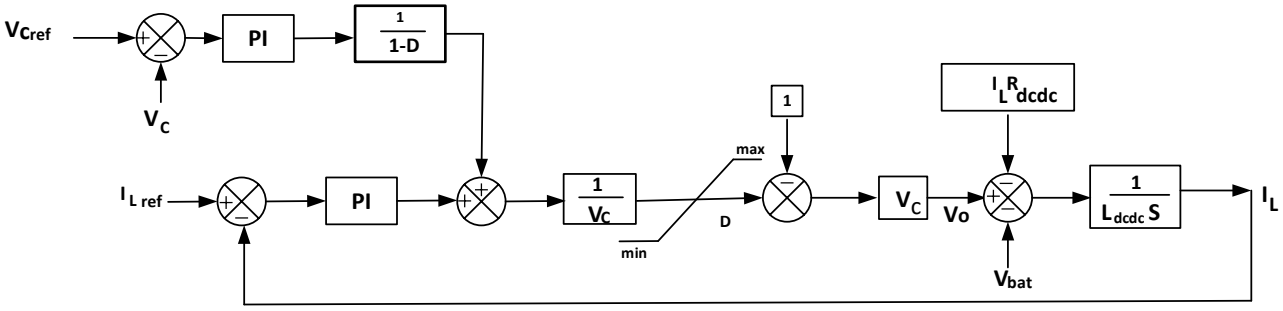


Figure 3.8 Inductor Voltage Loop Controller

3.3 Detailed Equivalent Model of MMC-ES

The conventional MMC structure is complex due to the large number of semiconductor switches used, making numerically efficient simulation very challenging. This converter complexity and computational cost for electromagnetic transient (EMT) simulation increase with the addition of integrated energy storage (MMC-ES). To address this issue, a simplified model called the Detailed Equivalent Model (DEM) has been developed. The DEM can effectively model the MMC-ES while still maintaining numerical accuracy, and is intended to replace the Detailed Model (DM) which provides a complete representation of the converter [38]. This section first

provides fundamental analysis of the EMT method used in the DEM for the converter network, followed by a detailed analysis of the MMC-ES within the DEM. The material in [61] serves as the foundation for the basic knowledge utilized in the analysis presented below.

3.3.1 Electromagnetic Transients Simulation in Power Systems

The EMT simulation utilizes Kirchhoff's law to evaluate the behavior and operation of the converter circuit under various transient events and disturbances by constructing differential equations. The program models the network with small time intervals at a high computing rate to accurately replicate the fast transients of power system. The EMT simulation is based on three-phase instantaneous value models of the electrical components of the converter, including resistors, inductors, capacitors, semiconductor switches, and others [61], [62].

Due to the non-linearity and fast switching of these components, small fixed time intervals of tens of microseconds are used in the EMT simulation to accurately capture the behavior and variations of the network [63]. As the numerical simulation is discrete while the electrical network model is continuous, it was necessary to simulate the system in a discrete time domain in order to adequately account for switching events and disturbances. Various approaches to creating discrete differential equations for the network are evaluated in [61].

One technique that the Electromagnetic Transient (EMT) tool, utilized to analyze large electrical networks is the nodal voltage analysis approach, proposed by H. W. Dommel [64], which involves discretizing the network components' differential equations into its equivalent admittance and current sources for nodal voltage analysis. To model the various functions, the differential equations of the circuit components can be solved using numerical integration methods such as

Trapezoidal or Backward Euler integration rule with small time steps. To perform simple nodal voltage analysis, the circuit components must first be transformed into their Thevenin voltage equivalent or Norton current equivalent. The following steps outline the process of discretizing the circuit components [61].

3.3.2 Resistor

A resistor is the simplest element of a circuit with two terminals, as illustrated in Fig. 3.9, which shows a resistor with its current and voltage direction in a circuit.

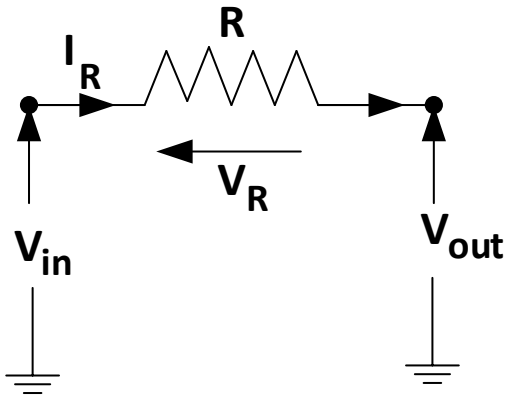


Figure 3.9 A resistor with its current and voltage directions in a circuit

The admittance G, is the reciprocal of the resistance;

$$G = \frac{1}{R} \tag{3.29}$$

The voltage across the resistor R is given as;

$$i_{R(t)} = \frac{1}{R}\left(V_{in}(t) - V_{out}(t)\right) \tag{3.30}$$

3.3.3 Inductor

Inductors are electromagnetic passive components with two terminals that store energy in their magnetic fields as current passes through them and create an opposition when the current

flowing through them changes. The rate of this opposition to the current change is referred to as its inductance. A representation of an inductor with its current and voltage direction in a circuit is shown in Fig. 3.10.

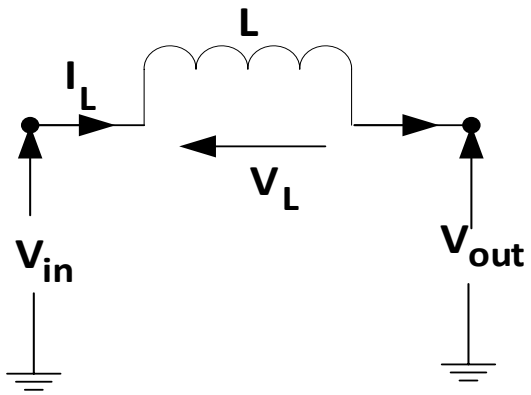


Figure 3.10 Representation of inductor with its current and voltage direction in a circuit

The voltage across the inductor *L* is given as:

$$v_L = L\frac{di_L}{dt} \tag{3.31}$$

Integrating Eq. 3.27 to evaluate the inductor current is as follows;

$$i_{L(t)} = \frac{1}{L}\int_{t=0}^{t} v_L\, dt \tag{3.32}$$

Applying the trapezoidal numerical integration method over a time step considering the initial states, the inductor current is given as:

$$i_L(t) = i_L(t-\Delta t) + \frac{\Delta t}{L}\frac{v_L(t)+v_L(t-\Delta t)}{2} \tag{3.33}$$

Considering the previous time step of both current and voltage in determining the next time step, the current source equivalent is given as:

$$i_L(t) = i_L(t-\Delta t) + \frac{\Delta t}{2L}v_L(t) + \frac{\Delta t}{2L}v_L(t-\Delta t) \tag{3.34}$$

where $i_L(t-\Delta t)$ is the inductor current from previous time step and the equivalent admittance of the inductor is $\frac{\Delta t}{2L}$. Importantly, the history current source can be established as:

$$I_{hist}\,(t-\Delta t) = \; i_L(t-\Delta t) \; + \; \frac{\Delta t}{2L} v_L(t-\Delta t) \tag{3.35}$$

Eq. 3.30 can be evaluated to define the inductor voltage equivalent as:

$$v_{L(t)} \; = \frac{2L}{\Delta t} i_{L(t)} \; - \; \frac{2L}{\Delta t} i_{L(t-\Delta t)} \; - \; v_{L(t-\Delta t)} \tag{3.36}$$

$$v_{L(t-\Delta t)} \; = \; R_L i_L \; + \; V_{L(t-\Delta t)} \tag{3.37}$$

Therefore, the Thevenin equivalent resistance and history voltage source of the inductor circuit is the R_L and $V_{L(t-\Delta t)}$, respectively.

3.3.4 Capacitor

Capacitors are known as the passive components of an electrical circuit that have the abilities to store the energy they draw from a battery cell, therefore acting as a charged battery. It has two terminals, through which it charges and discharges. Capacitance is the amount of electrical energy it stores, such that a higher capacitance means a higher energy storage capacity, and vice versa. Representation of capacitor with its current and voltage direction in a circuit is shown in Fig. 3.11.

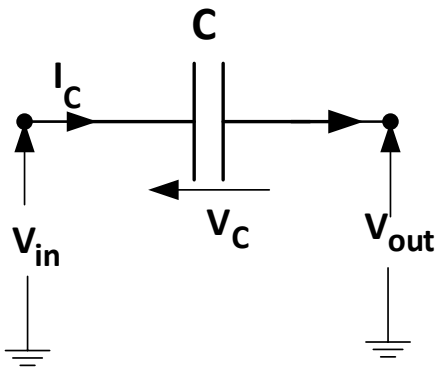


Figure 3.11 Representation of capacitor with its current and voltage directions in a circuit

The equation for the capacitor current is given as

$$i_c(t) \;=\; C\,\frac{dV_c(t)}{dt} \tag{3.38}$$

Integrating (3.37) to calculate the capacitor voltage gives:

$$v_c(t) \;=\; \frac{1}{C}\int_{t=0}^{t} i_c\,dt \tag{3.39}$$

Applying the Trapezoidal numerical integration produces:

$$v_c(t) \;=\; v_c(t-\Delta t) \;+\; \frac{\Delta t}{C}\frac{i_c(t)+i_c(t-\Delta t)}{2} \tag{3.40}$$

Evaluating (3.39) to calculate the capacitor current gives:

$$i_c(t) \;=\; \frac{2C}{\Delta t}v_c(t) \;-\; i_c(t-\Delta t) \;-\; \frac{2C}{\Delta t}v_c(t-\Delta t) \tag{3.41}$$

Similarly, the capacitor current history can be evaluated as

$$I_{hist}(t-\Delta t) \;=\; -i_c(t-\Delta t) \;-\; \frac{2C}{\Delta t}v_c(t-\Delta t) \tag{3.42}$$

From (3.40), the equivalent admittance of the capacitor is $\frac{2C}{\Delta t}$.

The corresponding Thevenin equivalent circuit can be derived from (3.40) as

$$v_c(t) \;=\; R_c i_c(t) \;+\; V_c(t-\Delta t) \tag{3.43}$$

Therefore, the Thevenin equivalent resistance and history voltage source of the capacitor circuit is R_c and $V_{c(t-\Delta t)}$, respectively.

3.3.5 Power Electronic Semiconductor Switch

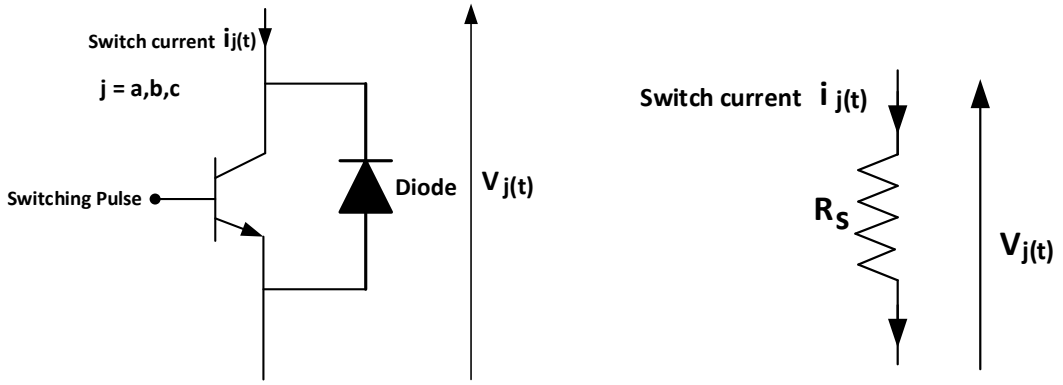
Formulating the power network solution composed of these RLC branches can be done using the above discretized Thevenin equivalent equations for each branch component. However, the foundational operation of a power converter is based on semiconductor switches, which must be accounted for in an EMT program. Generally, in an ideal operation, the switch properties in both the ON and OFF states are presented below:

- When turned on, there is no resistance or voltage drop, indicating that there is no conduction loss.
- When turned off, there is infinite resistance of the switch.
- The ON/OFF switch is instantaneous.

Accordingly, in an EMT simulation program, the switching operation is accounted for as in practical operation, and the properties are given below:

- Finite resistance (small resistance) when a switch is in ON state
- Infinite resistance (large resistance) when a switch is in OFF state

The choice of semiconductor switch for the MMC is based on its characteristics and specifications. An IGBT switch is selected due to its widespread use and suitable capabilities for high power high voltage applications. As shown in Fig. 3.12, the IGBT switch includes a diode in parallel for conducting current in the reverse direction. In the EMT program, the switch is modeled as two-value resistor, having a small resistance during the ON state, and a high resistance during the OFF state.



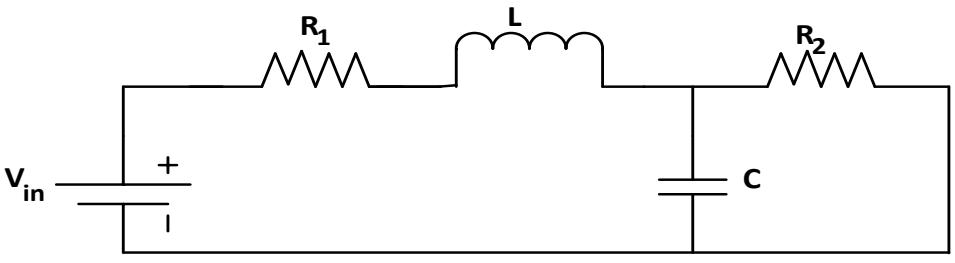
(a) (b)

(a) Circuit symbol of IGBT switch with anti-parallel diode (b) EMT resistance circuit for the switch

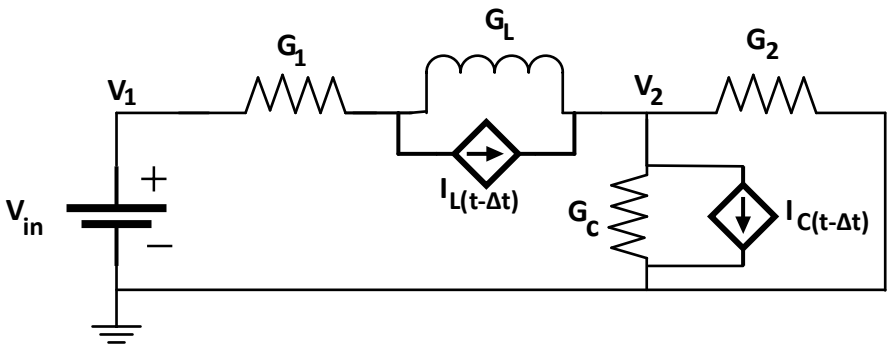
Figure 3.12 Illustration of the IGBT with a diode in parallel for reverse current conduction

3.3.6 Network Reduction for The Equivalent Circuit

The converter circuit, composed of resistors, inductors, capacitors, and switches, is now replaced by admittances and history current sources, calculated from the discretization process mentioned above. Fig. 3.13a shows a simple example circuit representation of an RLC network, while Figure 3.13b illustrates the equivalent circuit in discrete time domain.



(a)



(b)

Figure 3.13 Example of a discretized electrical network for the simplified equivalent model showing the admittance, Thevenin resistance and the history current sources.

The equivalent circuit for the network is used to derive the nodal formation below:

$$GV = I_{hist} \tag{3.45}$$

where G is the admittance matrix of the nodal network, V is the vector of the nodal voltages to be solved by the EMT program; I_{hist} is the vector of the history current sources for the nodes. It is noted that the nodal equation of (3.44) has the following form for the example in Fig. 3.13.

$$\begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{3.46}$$

The nodal voltages can be solved from (3.45) as

$$V = G^{-1} I_{hist} \tag{3.46}$$

3.4 Derivation of the Nodal Equation for the DEM of MMC-ES

The switches, capacitor, and inductor of the individual SM circuit of the MMC-ES, as shown in Fig. 3.14, are replaced with their equivalent circuits in discrete time domain, as described in the previous section and are depicted in Fig. 3.15. The Thevenin equivalent circuit of Fig. 3.15

is calculated at the input terminal of each SM. Since a large number of SMs are connected in series in each arm of the MMC-ES, the overall Thevenin equivalent circuit for each arm can be formulated which eliminates the internal nodes in each arm and reduces the dimension of the network nodal equation thus to accelerate EMT simulation of the MMC-ES [65].

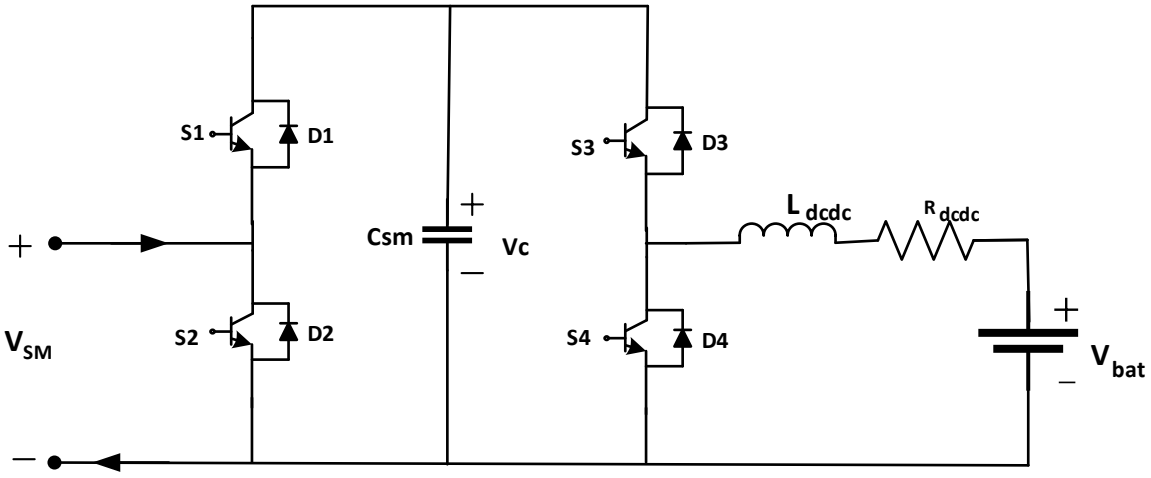


Figure 3.14 SM circuit of the MMC-ES

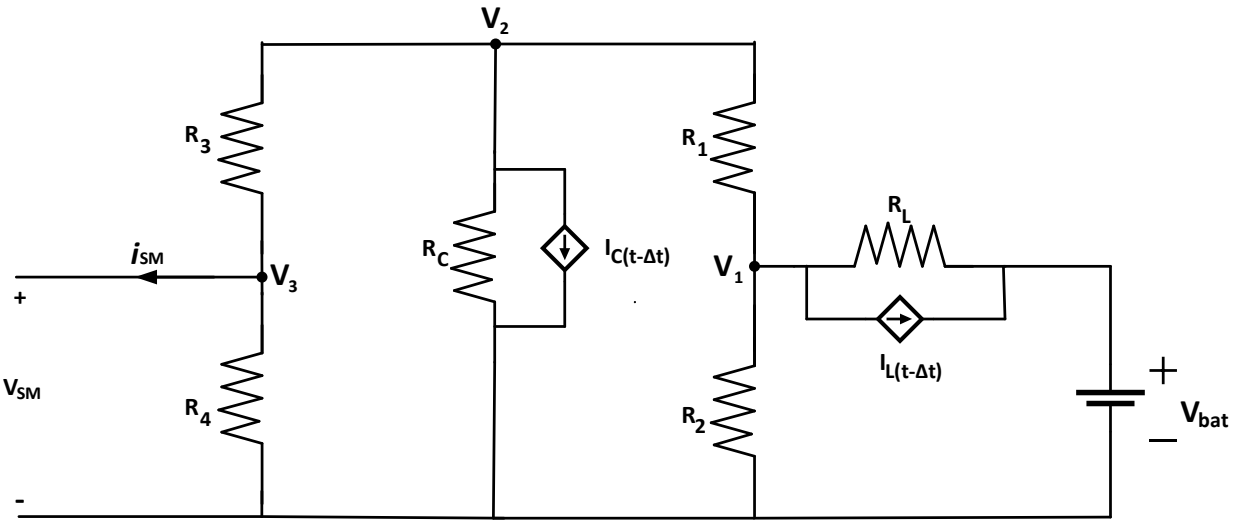


Figure 3.15 Equivalent circuit of the SM of MMC-ES

The DC-DC converter inductor equivalent resistance is $R_{eq} = \frac{2L}{\Delta t}$, where the admittance follows as $G_{eq} = \frac{1}{R_{eq}} = \frac{\Delta t}{2L}$. Similarly, the SM capacitor equivalent resistance is $R_{ceq} = \frac{\Delta t}{2C}$ such that the admittance becomes $G_{eq} = \frac{1}{R_{ceq}} = \frac{2C}{\Delta t}$. The energy storing electrical components in the circuit, that is, the inductor and capacitor equivalent resistances, are included with their history current sources as seen in the diagram. With all the Thevenin resistances represented, the admittance matrix G is formulated for each node. Formulating the equivalent circuit above is achieved using three node voltages $\boldsymbol{V_1}$, $\boldsymbol{V_2}$ & $\boldsymbol{V_3}$. The admittances for the nodes are evaluated as below:

For **node 1**,

$$G_{11} = \sum\left(\frac{T_S}{2L} + \frac{1}{R_1} + \frac{1}{R_2}\right) \tag{3.47}$$

$$G_{12} = -\frac{1}{R_1} \tag{3.48}$$

$$G_{13} = 0 \tag{3.49}$$

For **node 2**,

$$G_{21} = -\frac{1}{R_1} \tag{3.50}$$

$$G_{22} = \sum\left(\frac{1}{R_1} + \frac{2C}{T_S} + \frac{1}{R_3}\right) \tag{3.51}$$

$$G_{23} = -\frac{1}{R_3} \tag{3.52}$$

For **node 3**,

$$G_{31} = 0 \tag{3.53}$$

$$G_{32} = -\frac{1}{R_3} \tag{3.54}$$

$$G_{33} = \frac{1}{R_3} + \frac{1}{R_4} \tag{3.55}$$

where R_1 and R_2 represent the resistances of the upper and lower switches for the DC-DC converter, while R_3 and R_4 are the upper and lower switches for the HB SM of the MMC-ES. T_S represents integration time step used for the EMT simulation. The node admittances from Eq. 3.45 to 3.53 is formulated in the admittance matrix below:

$$G_{eq} = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} \tag{3.56}$$

$$G_{eq} = \begin{bmatrix} \sum\left(\frac{T_S}{2L} + \frac{1}{R_1} + \frac{1}{R_2}\right) & -\frac{1}{R_1} & 0 \\ -\frac{1}{R_1} & \sum\left(\frac{1}{R_1} + \frac{2C}{T_S} + \frac{1}{R_3}\right) & -\frac{1}{R_3} \\ 0 & -\frac{1}{R_3} & \frac{1}{R_3} + \frac{1}{R_4} \end{bmatrix} \tag{3.57}$$

Furthermore, the SM capacitor current source variable, I_C and DC-DC converter current source variable I_L as shown in Fig. 3.15 are calculated as;

$$I_{L(t-\Delta t)} = (V_1 - V_{bat})\frac{T_s}{2L} + (V_{1(t-\Delta t)} - V_{bat})\frac{T_S}{2L} + I_{L(t-\Delta t)} \tag{3.58}$$

$$I_{C(t-\Delta t)} = \frac{2C}{T_S}V_2 - I_{C(t-\Delta t)} - \frac{2C}{T_S}V_{2(t-\Delta t)} \tag{3.59}$$

Finally, the nodal voltages were evaluated using (3.46) and any change in the admittance along a node causes the need to reinvert the admittance matrix. It is important to note that the node voltage at node 3 is assigned to be the output voltage of the SM:

$$V_3 = V_{SM} \tag{3.60}$$

A switching algorithm is implemented to model the semiconductor switching operations with their on-state and off-state resistances in the equivalent model [38], as illustrated in the following steps:

1. Retrieve the arm voltage $\boldsymbol{V_{arm}}$ from the SM equivalent circuits to calculate the converter and power network solution and the arm current $\boldsymbol{I_{arm}}$.
2. For the iteration $\boldsymbol{i = 1, 2, \ldots\ldots, N}$:
    a. Set the DC-DC converter resistant values $\boldsymbol{R_{1i}}$ & $\boldsymbol{R_{2i}}$, and the SM resistant values $\boldsymbol{R_{3i}}$ & $\boldsymbol{R_{4i}}$ as follows;

    if (DC-DC converter is ON) $\{\boldsymbol{R_{1i} = R_{ON}; R_{2i} = R_{OFF}}\}$

    elseif (DC-DC converter is OFF) $\{\boldsymbol{R_{1i} = R_{OFF}; R_{2i} = R_{ON}}\}$

    if (SM is ON) $\{\boldsymbol{R_{3i} = R_{ON}; R_{4i} = R_{OFF}}\}$

    elseif (SM is OFF) $\{\boldsymbol{R_{3i} = R_{OFF}; R_{4i} = R_{ON}}\}$

    elseif (SM is Blocked) $\{$

    if ($\boldsymbol{i_{arm(t)} > 0}$ and ($\boldsymbol{V_{SMi(t-\Delta t)} > V_{Ci(t-\Delta t)}}$)

    $\{\boldsymbol{R_{3i} = R_{ON}; R_{4i} = R_{OFF}}\}$

    if ($\boldsymbol{i_{arm(t)} < 0}$ and ($\boldsymbol{V_{SMi(t-\Delta t)} < 0}$)

    $\{\boldsymbol{R_{3i} = R_{OFF}; R_{4i} = R_{ON}}\}$

    elseif $\{\boldsymbol{R_{3i} = R_{OFF}; R_{4i} = R_{OFF}}\}$

    }
3. Evaluate each SM capacitor voltage and current $\boldsymbol{v_{Ci}}$ and $\boldsymbol{i_{Ci}}$ for all iterations.
4. Calculate the Thevenin Equivalent voltage of each SM.

5. Determine the SM voltages $\boldsymbol{V_{SM}}$ for the next iteration.

3.5 Arm Equivalent Circuit for the Detailed Equivalent Model

Additionally, in [16], [65], node voltages are calculated for all SMs in an arm and an equivalent circuit is created to represent and accommodate the number of SMs per arm as well as their resultant voltage and current output in various modes. This arm equivalent circuit serves as a simplified single circuit that can replace the SMs in each arm of the DM and can represent various converter operations in normal states (when inserted and bypassed) and during disturbance states (when faults occur and all SMs are blocked). Fig. 3.16 shows an illustration of a simplified equivalent circuit for the N number of SMs per arm.

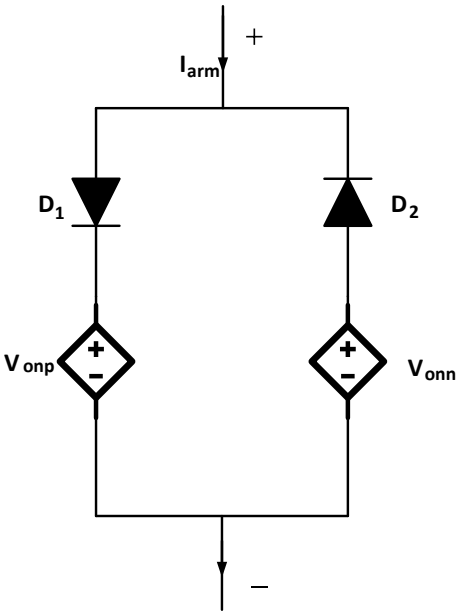


Fig. 3.16 Simplified equivalent circuit for the N number of SMs per arm

In the blocking state of MMC, different equivalent circuit branches are needed to model the converter arm, based on the orientation of the SM diodes and the direction of the arm current,

I_{arm} since the arm current is either flowing positively or negatively to the upper or lower diodes of the HBSMs. The diodes D_1 and D_2 in Fig. 3.16 are used to detect the arm current directions so that the corresponding equivalent arm voltages V_{onp} or V_{onn} can be inserted in the arm when the IGBTs of the SMs are OFF or blocked. The arm voltages for positive and negative arm current directions are represented in Fig. 3.16 by V_{onp} and V_{onn}, respectively. The operation of the equivalent circuit in relation to the MMC-ES is described in the following cases:

Case 1: During converter de-blocking mode, the IGBT switching events are controlled by their corresponding gate switching signals. The insertion and bypass states of the SMs are determined by the switching states of the IGBTs. The arm equivalent voltage for each arm can be calculated, based on Section 3.4. This arm equivalent voltage is used for V_{onp} or V_{onn}, irrespective of the arm current positive and negative directions. That is, during converter deblocking mode, the same arm voltage, calculated from Section 3.4, will be used in Fig. 3.16 of the DEM [16].

Case 2: In the case of the converter blocking mode, all the IGBT switches are turned off, the insertion or bypass state of the SM capacitors depend on the arm current direction (positive vs. negative) since the arm current flows through SM diodes during converter blocking mode. When the arm current is positive, the arm current flows through the upper diodes of the SMs, thus inserts all the SM capacitors. Therefore, the arm equivalent voltage is the sum of all the SMs capacitor voltages calculated, based on Section 3.4 as:

$$V_{onp} = \sum_{i=1}^{N} V_{sm\_i} \tag{3.61}$$

When the arm current is negative, the arm current flows through the lower diodes of the SMs, thus bypassing all the SM capacitors. Therefore, the arm equivalent voltage V_{onn} is zero.

CHAPTER FOUR – SIMULATION RESULT AND DISCUSSION

4.1 MMC-ES Modeling for the DM and DEM

To verify the numerically efficient DEM of the MMC-ES, a three-phase EMT simulation is carried out using MATLAB/Simulink/Simscape/Specialized Power Systems Toolbox. This software tool allows for the creation of a detailed semiconductor-based switching model for the MMC-ES that can be tested and analyzed in a manner similar to a physically constructed converter. In order to obtain an accurate model, it is important to carefully select and calculate the parameters to match the desired ratings and operation of the converter. The parameters used in the simulation of both DM and DEM are detailed in Table 4.1.

Table 4.1 Parameters of the simulated three-phase MMC-ES

Parameter	Symbol	Value
DC-link voltage	V_{dc}	640kV
Rated active power	P_{ref}	$0.5GW$
Rated reactive power	Q_{ref}	$0\ VAR$
Rated apparent power	S	$0.5GVA$
Number of SM per arm	N	10
SM capacitance	C	$250\mu F$
Arm inductance	L_{arm}	$500\mu H$
Arm resistance	R_{arm}	$50m\Omega$
Carrier switching frequency	f_c	$5kH_z$
Fundamental frequency	f	$50H_z$
Battery voltage	V_{bat}	32kV
Grid pole-ground voltage, RMS	V_{pg}	320kV
Time step	T_s	$20\mu s$

The transient simulation is designed to represent a balanced three-phase operation condition in which the MMC-ES is connected to an AC grid with a voltage of 400kV, a frequency of 50Hz, and a power capacity of 0.5GVA. This connection is facilitated through the use of a 400kV/300kV Y-Δ transformer. On the DC side, a 640kV DC voltage source is utilized to connect to the DC side of the MMC-ES.

4.2 Detailed Model Simulation Results

The purpose of this section is to present the scenarios that are chosen for testing the DM of the three-phase MMC-ES. The results demonstrate that the DM can accurately simulate the converter's dynamic behaviors. Initially, the normal, steady-state operation of the MMC-ES is simulated, followed by the application of power reference change transient to both the battery and MMC AC side.

The switches of the SMs are in unblocked states during the normal operation of the converter. To initiate the startup process, a reference AC power of zero is applied, resulting in zero AC grid current at the three phases, as shown in Fig. 4.2. As seen in Fig. 4.1, the AC voltages is symmetrically balanced at the rated value. The SM capacitor voltages are also balanced, as shown in Fig. 4.4. At 0.05 s, a reference power of 0.5 GW is applied to both the battery and MMC AC side, leading to increased AC currents, arm currents and SM capacitor voltage ripples as shown in Fig. 4.2 – Fig. 4.4.

It can be observed in Fig. 4.5 and Fig. 4.6 that the two arm voltages of Phase-A have opposite AC voltage components which will cancel each other when sum them up to obtain DC-side voltage of 640 kV. The arm voltages in Figs. 4.5 and 4.6 show a resultant 11-level in one

cycle, representing the $\boldsymbol{N + 1}$ steps in each arm for $\boldsymbol{N = 10}$ in this case. The same phase of the AC current and voltage shows that the system operates in unity power factor. It is shown in Fig. 4.4 that the SM capacitor balancing control is able to keep each SM capacitor voltage balanced.

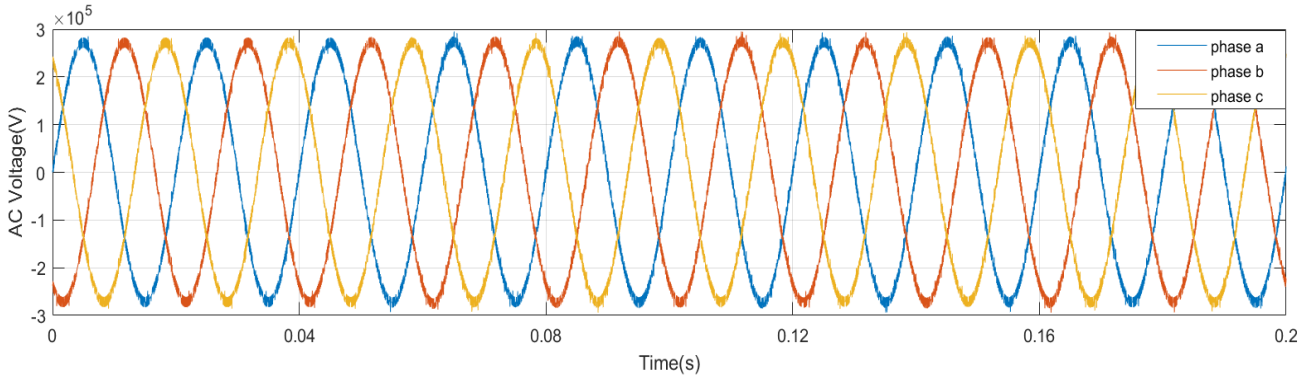


Figure 4.1 Converter AC voltages of the three-phases in steady state

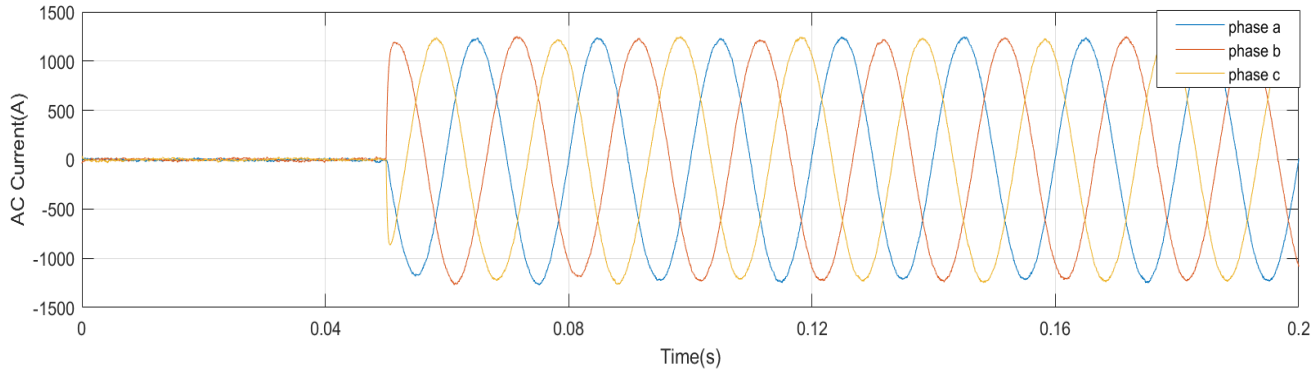


Figure 4.2 AC grid currents of the three-phases in steady state

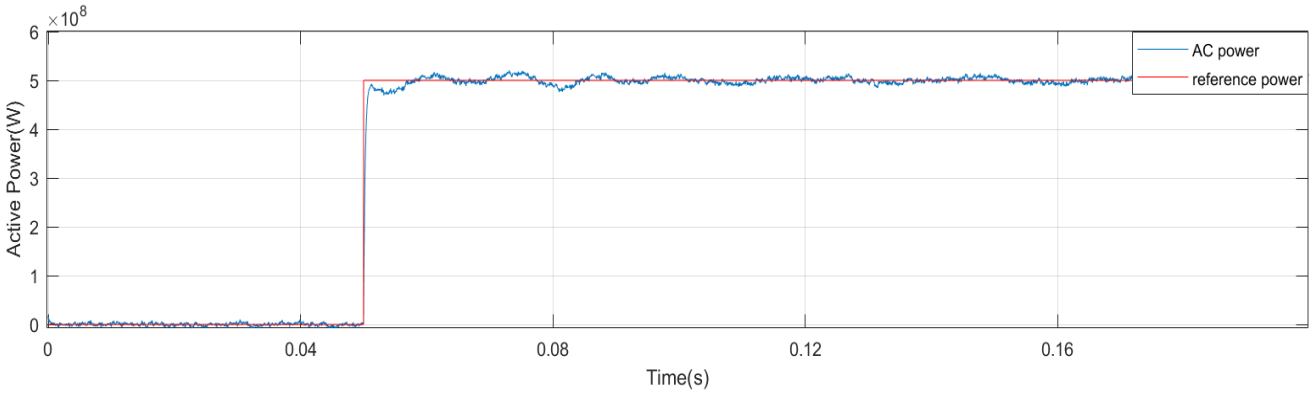


Figure 4.3 Actual and reference active powers of the AC grid during steady state operation

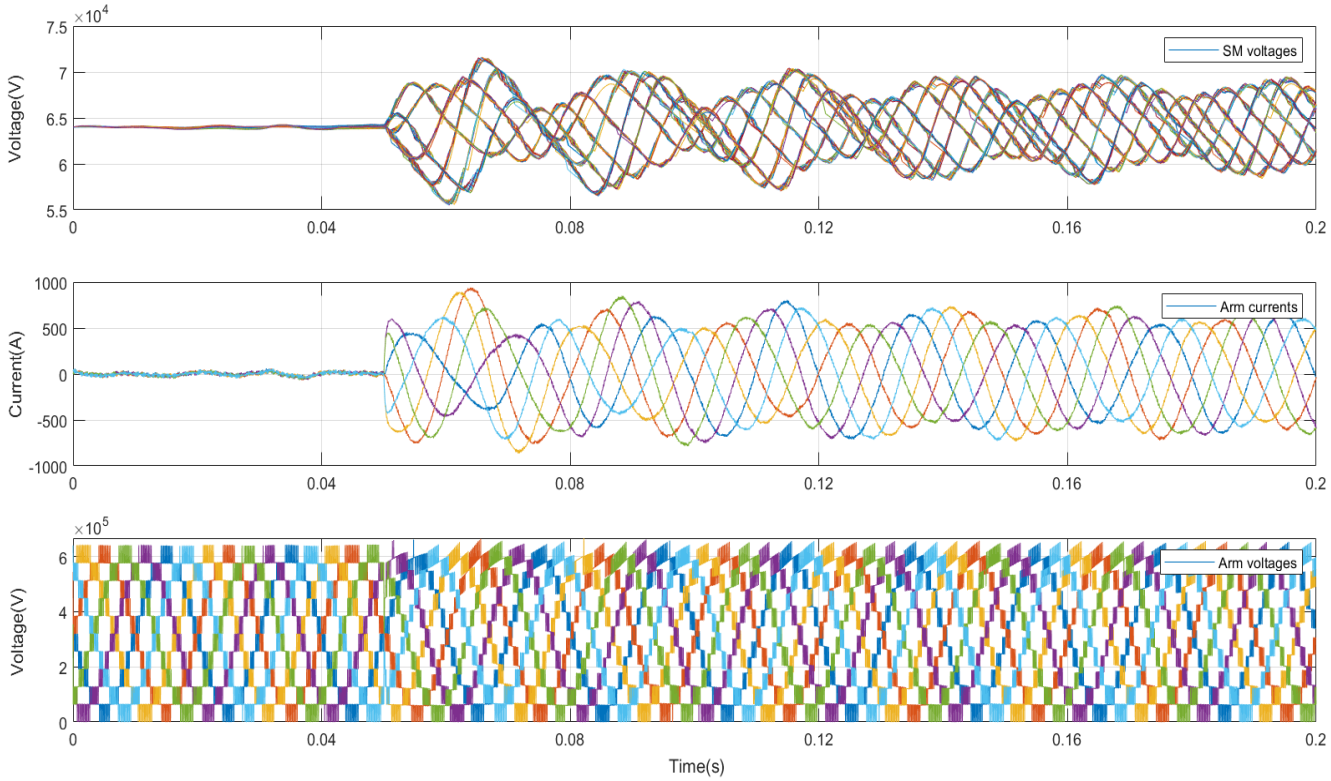


Figure 4.4 SM capacitor voltages, arm currents and arm voltages

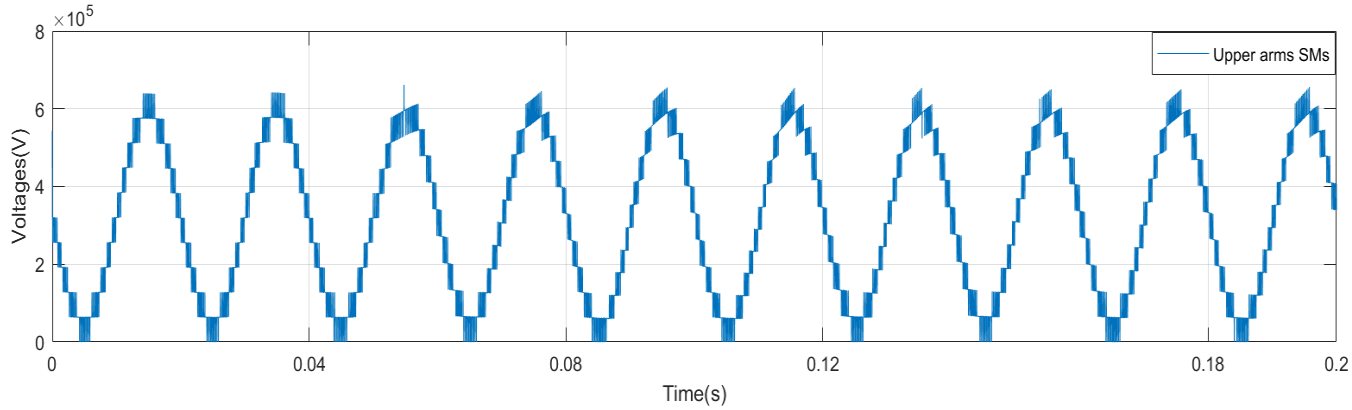


Figure 4.5 Phase-A upper arm voltage

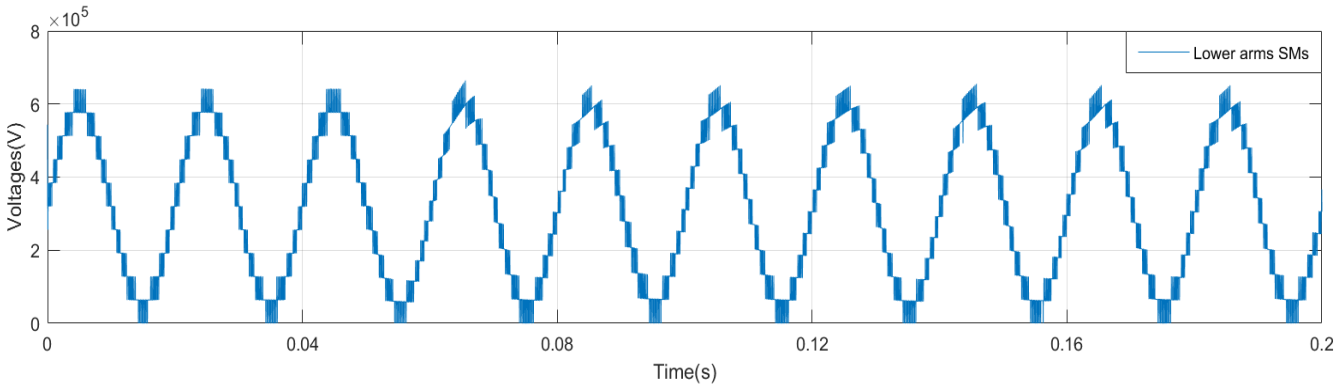


Figure 4.6 Phase-A lower arm voltage

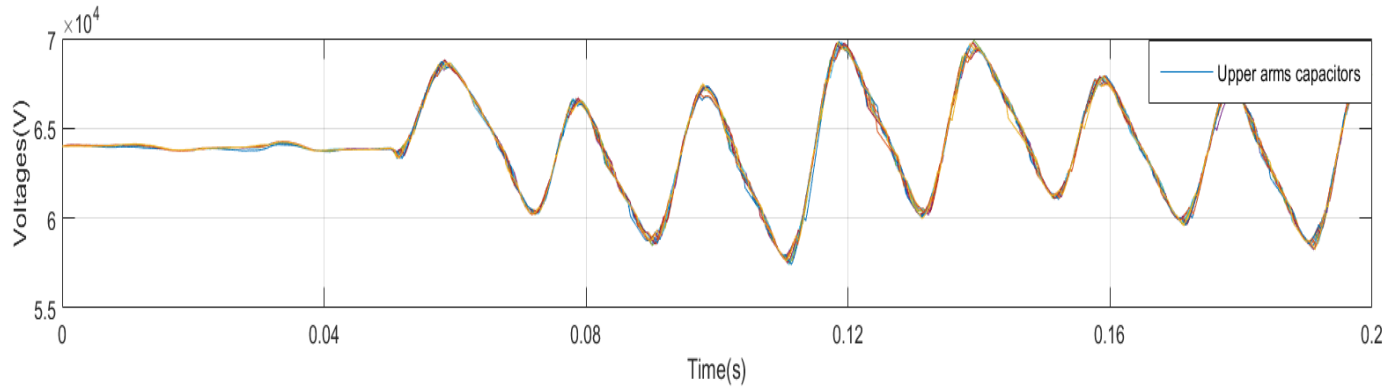


Figure 4.7 Phase-A upper arm capacitor voltage

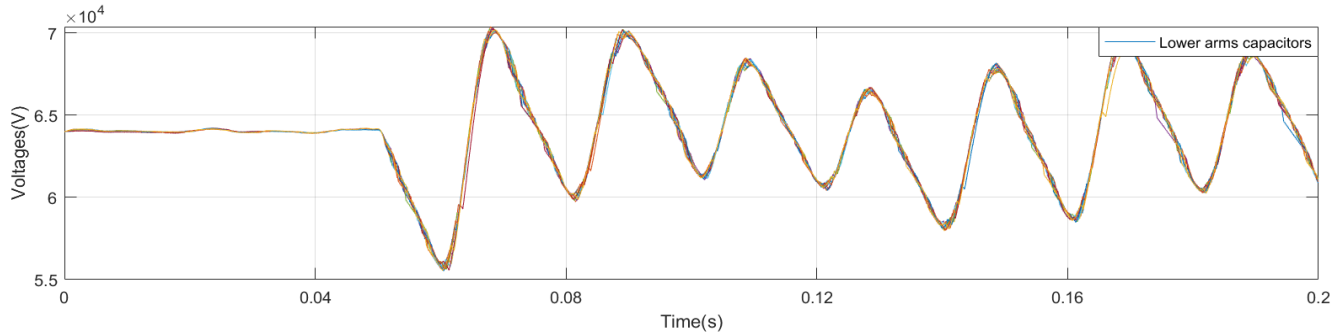


Figure 4.8 Phase-A lower arm capacitor voltage

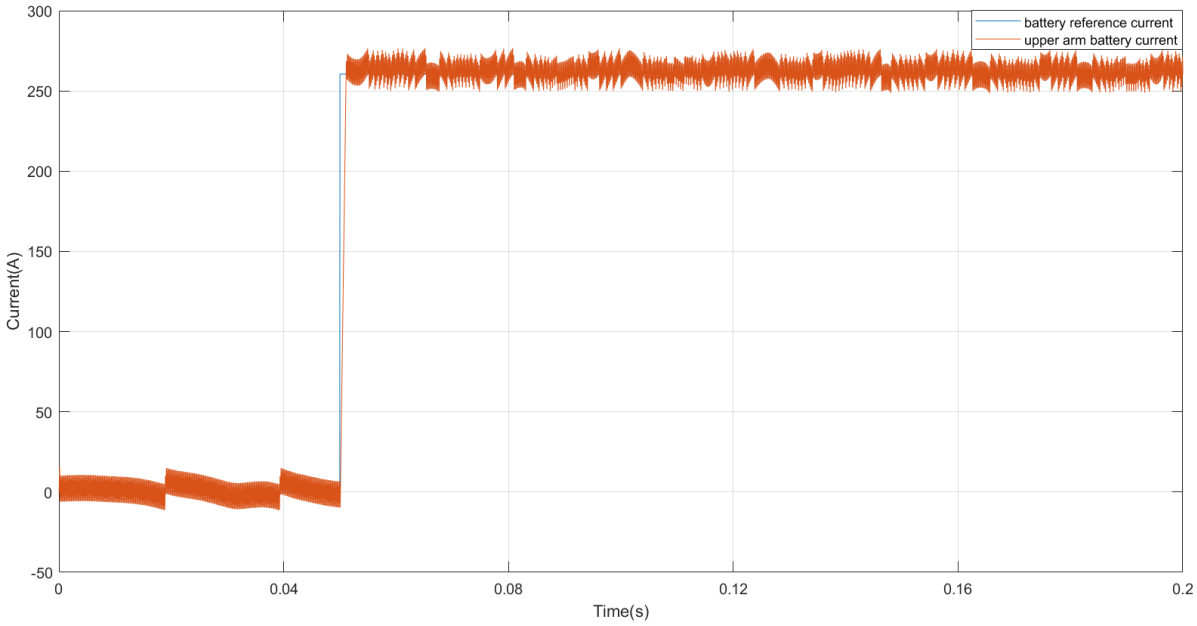


Figure 4.9 Upper arm battery current

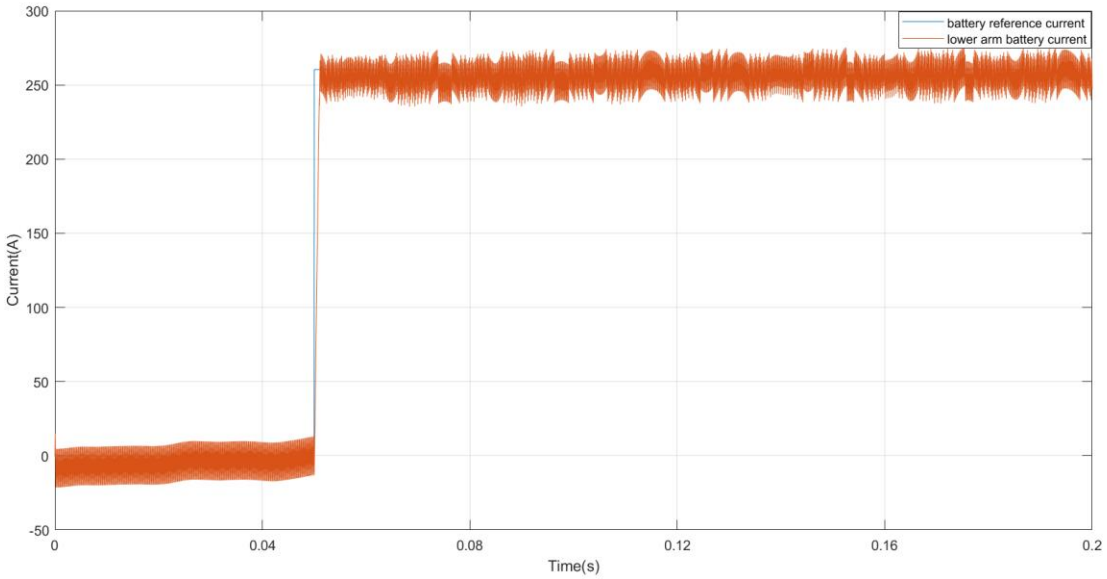


Figure 4.10 Lower arm battery current

Figures 4.9 and 4.10 shows that the output currents of the batteries on the individual energy storage side are capable of tracking the reference value. The battery storage operated at 0.5 GW, and each battery current is able to maintain 260 A. It is shown in the above-mentioned figures that the DM is able to represent the behavior of the MMC-ES.

4.3 Comparison and Verification of the DEM with $N = 10$ SMs per Arm during Steady State Operation

This section aims to validate the accuracy of the DEM by comparing its simulation results to those of the DM during steady-state operation. The waveforms, shown in the Figs. 4.11 – 4.14, indicate that both the DM and the DEM display similar results during steady state, with only a slight difference during the converter's startup due to slightly different initial conditions in the DM and the DEM. Both models also displayed similar upper and lower arm voltages in Fig. 4.11 and AC voltages and currents in Fig. 4.14. The voltage sorting and balancing control is effective for

both models to balance the SM capacitor voltages, as shown in Fig. 4.11. Additionally, the battery and AC powers at the PCC powers were able to follow the references, shown in Figs. 4.12 and 4.14. The DC link voltage is maintained at its rated value of 640kV, as shown in Fig. 4.13.

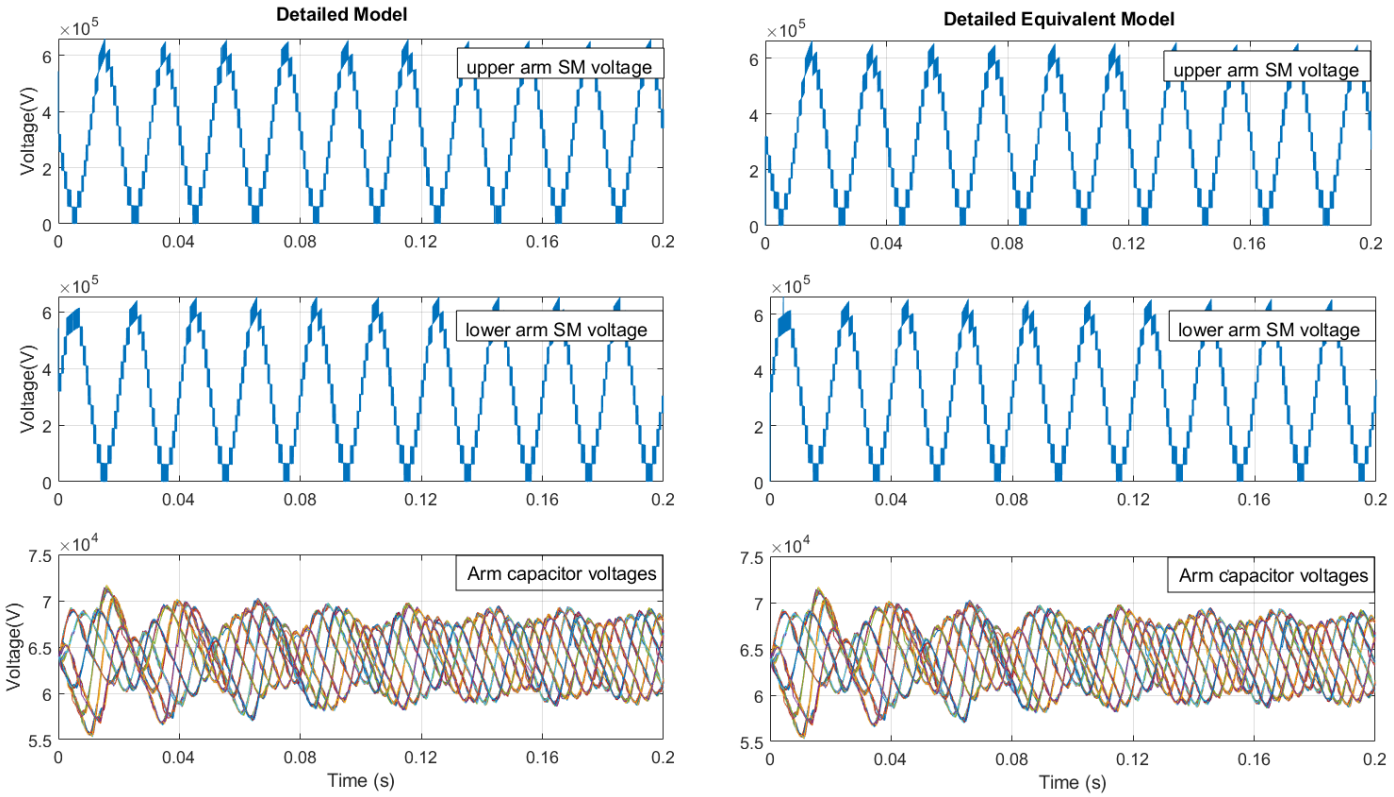


Figure 4.11 Comparison of the arm voltages and SM capacitor voltages

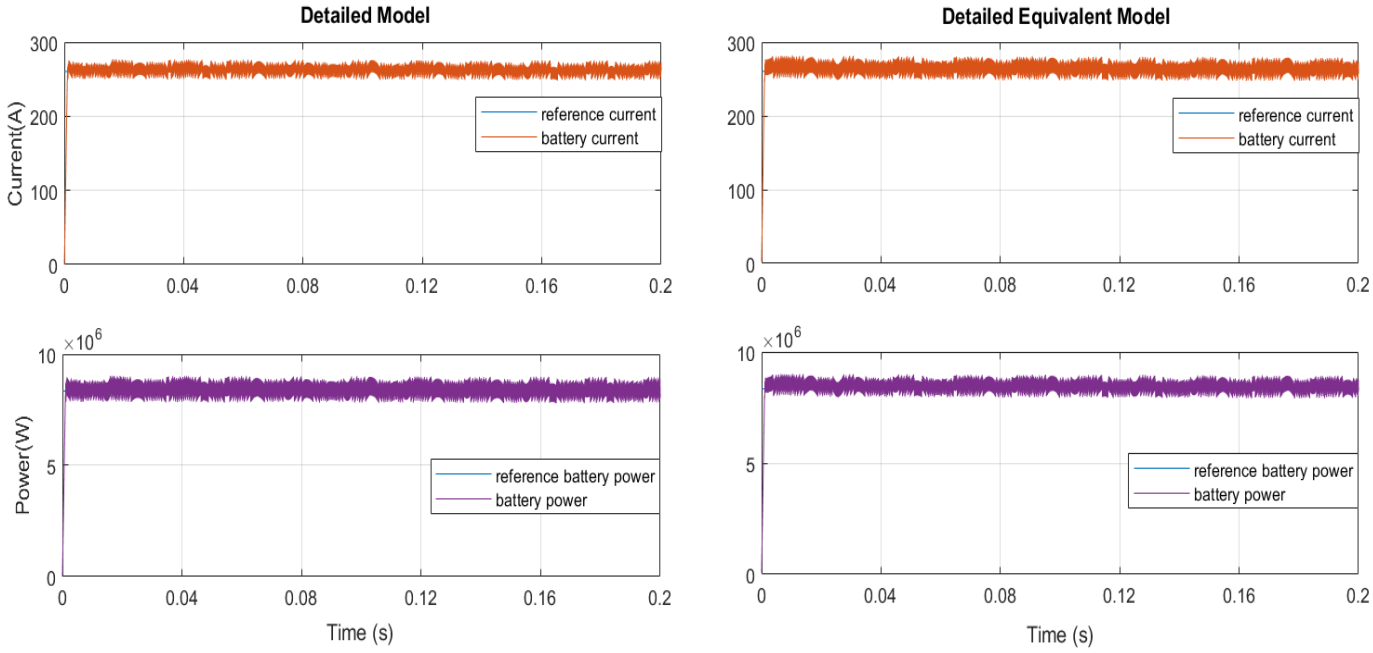


Figure 4.12 Comparison of the battery current and power

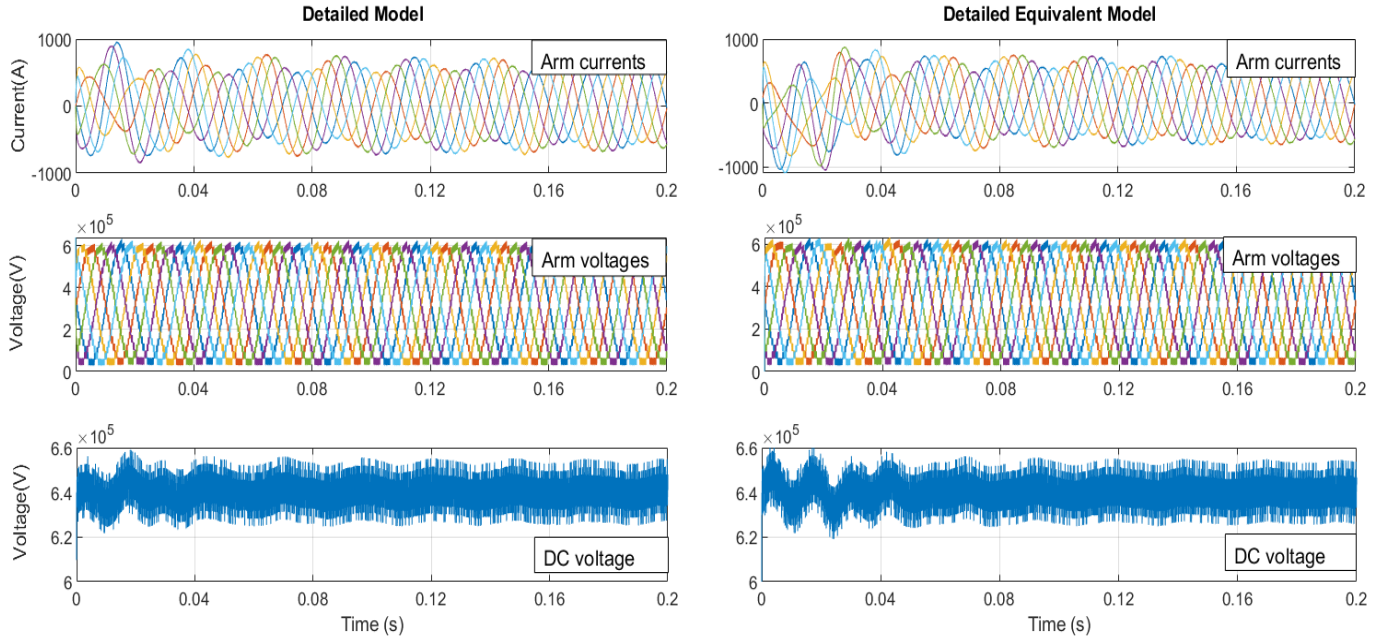


Figure 4.13 Comparison of the arm currents, voltages and DC voltage.

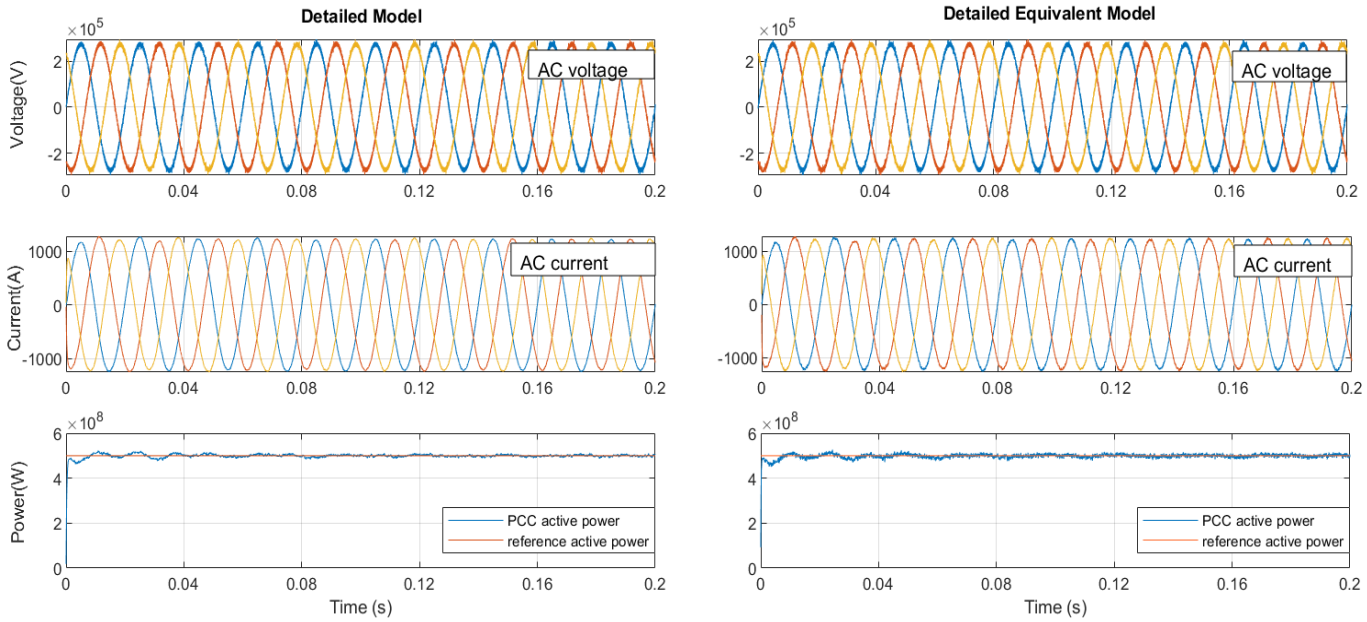


Figure 4.14 Comparison of the voltage, current, and active power at the PCC.

4.4 Comparison and Verification of the DEM with $N = 10$ SMs per Arm for AC Power Reference Change Transient

The response of the converter to a change in AC power command is studied in this section. The AC reference power is decreased from 0.5 GW to 0.1 GW at 0.05 s. This alteration often leads to a sudden decline in the AC grid current, SM arm currents, and SM capacitor voltage ripples. Upon applying the change, it is observed that the AC power at the PCC is able to follow the reference, and the converter remains in stable operation. The waveforms in the figures below demonstrate a close match between the DM and DEM.

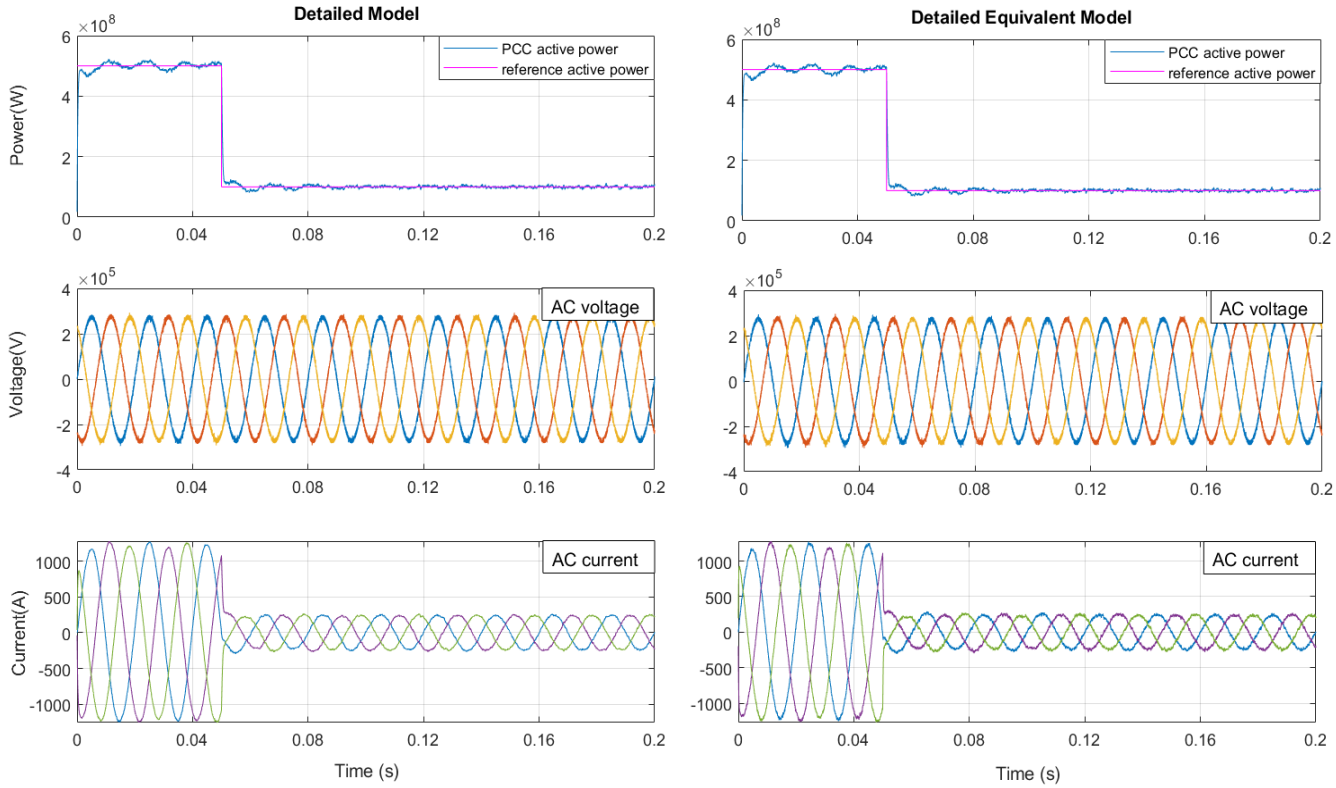


Figure 4.15 Comparison of the active power, AC voltage and AC current.

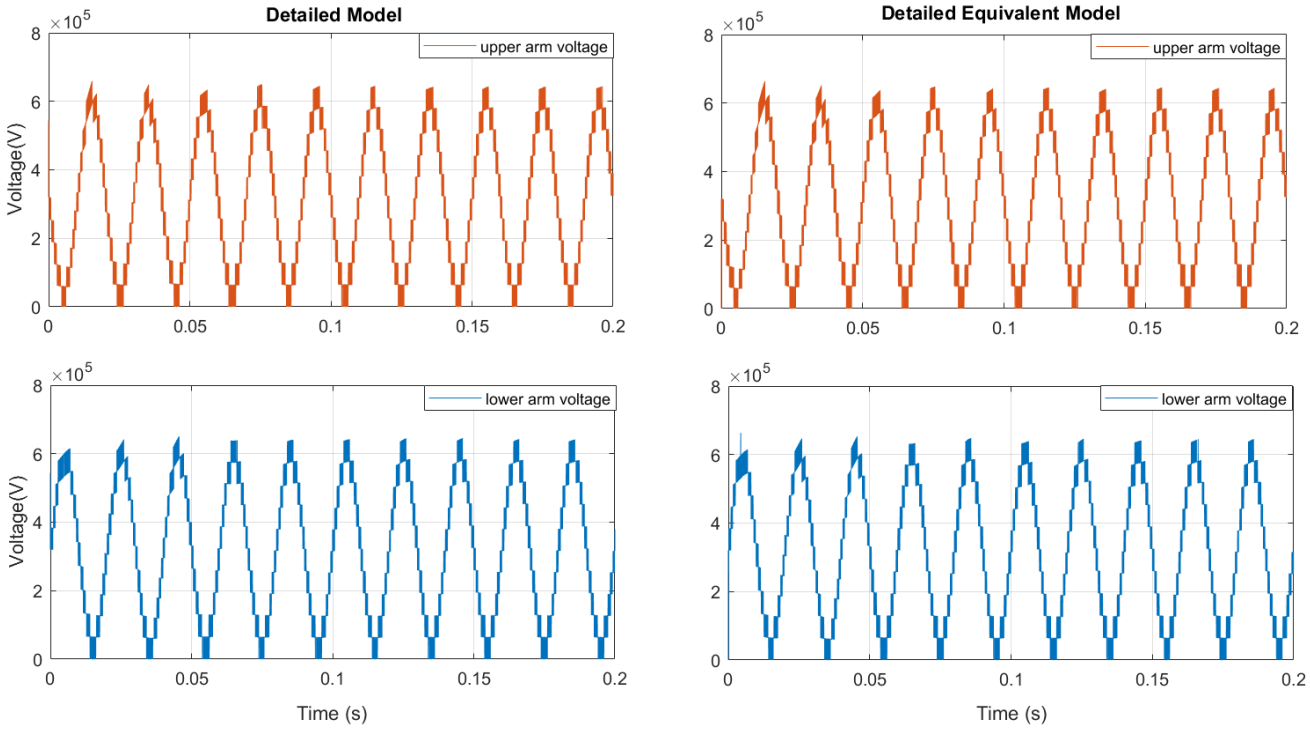


Figure 4.16 Comparison of the upper and lower arm voltages.

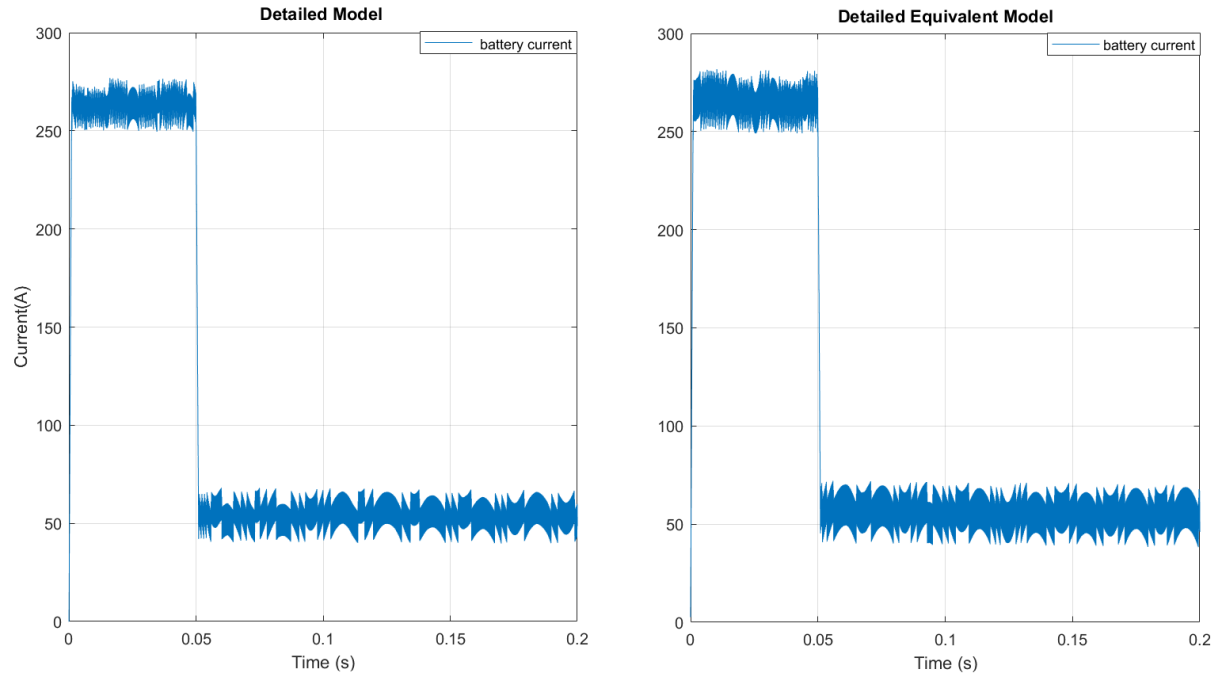


Figure 4.17 Comparison of the storage Battery current

4.5 Comparison and Verification of the DM and DEM with $N = 20$ SMs per Arm during Steady State Operation

To assess the validity of the DEM for higher number of SMs per arm, a scenario where there are 20 SMs per arm is simulated. This allows to examine the converter's ability to keep the DC-link at its rated 640 kV while handling the smaller distributed voltages from each SM. As shown in Fig. 4.18, the arm capacitor voltages decreased by half as the capacitance of each SM capacitor doubled, while the rated SM voltages are maintained. Initially, an oscillation in the DC-link voltage was observed when zero AC and battery power are applied until 0.02 s. At 0.02s, the current and power references of approximately 260 A and 4.2 MW are applied, respectively to MMC-ES, the converter reaches to loaded study state operating condition. The simulation results, shown in Figs. 4.18 – 4.21, demonstrates that the DM and DEM produce almost identical simulation results.

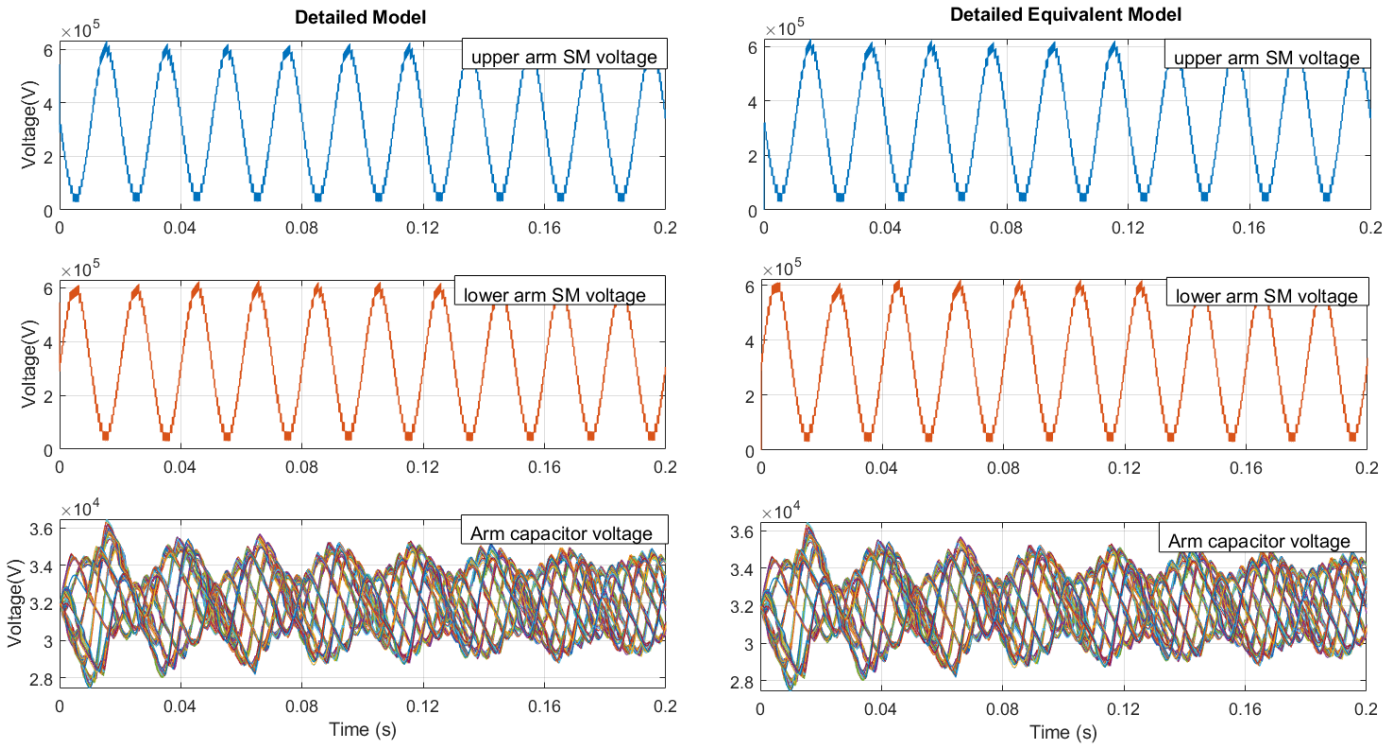


Figure 4.18 Comparison of arm voltages and SM capacitor voltages

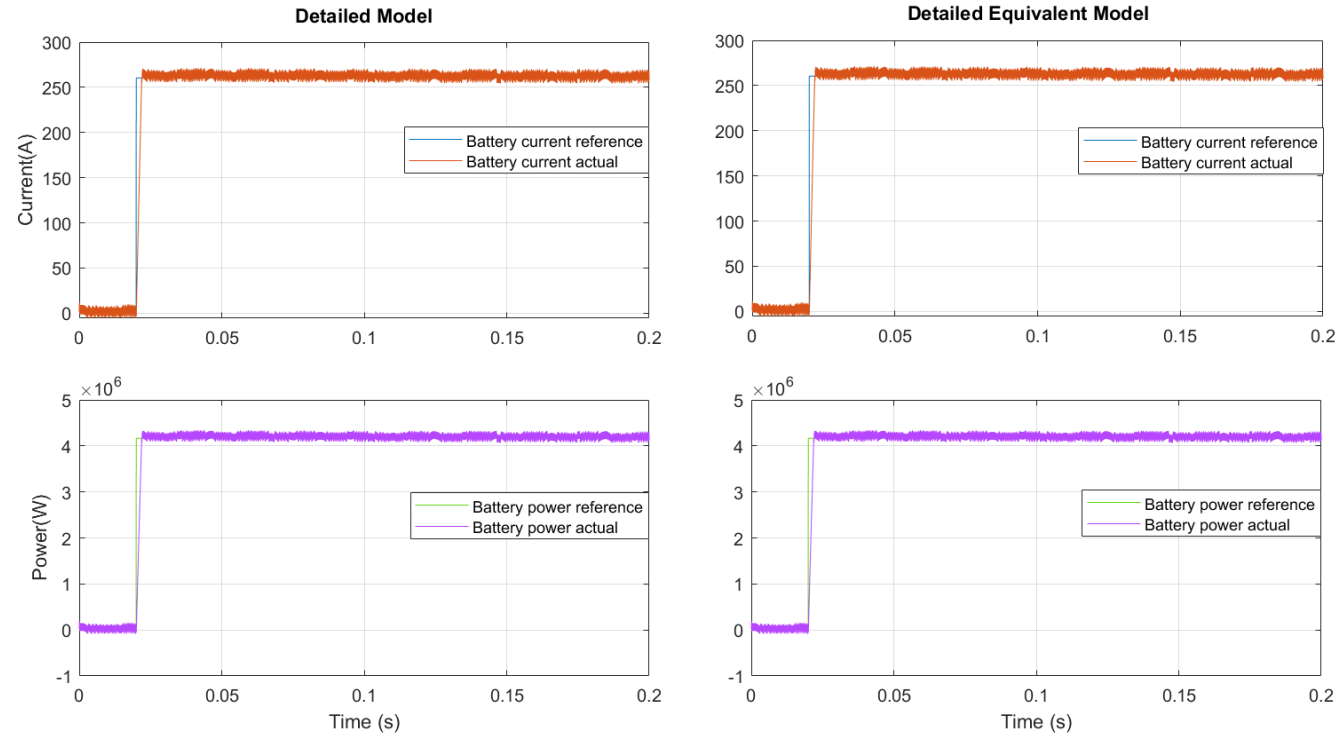


Figure 4.19 Comparison of the battery current and power

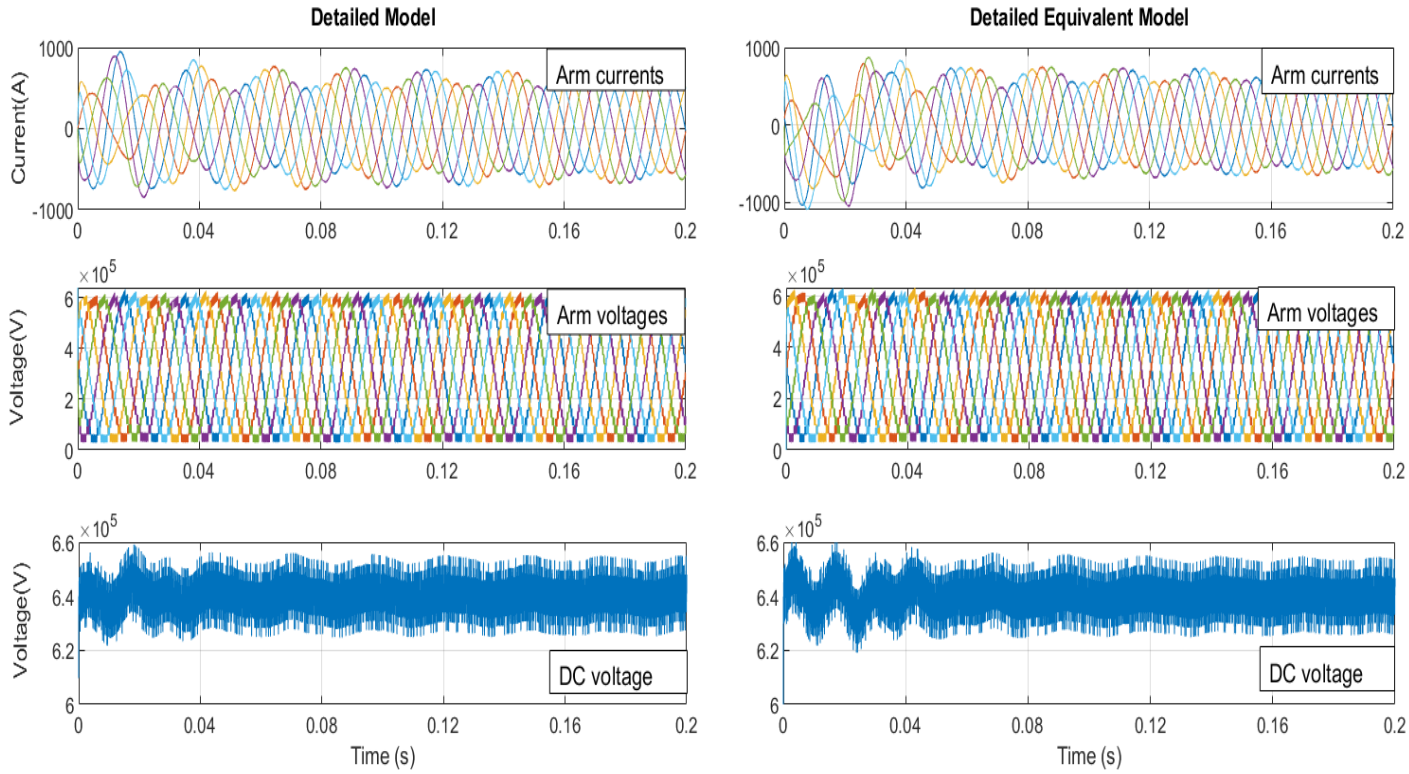


Figure 4.20 Comparison of the arm currents, voltages and the DC-link voltage

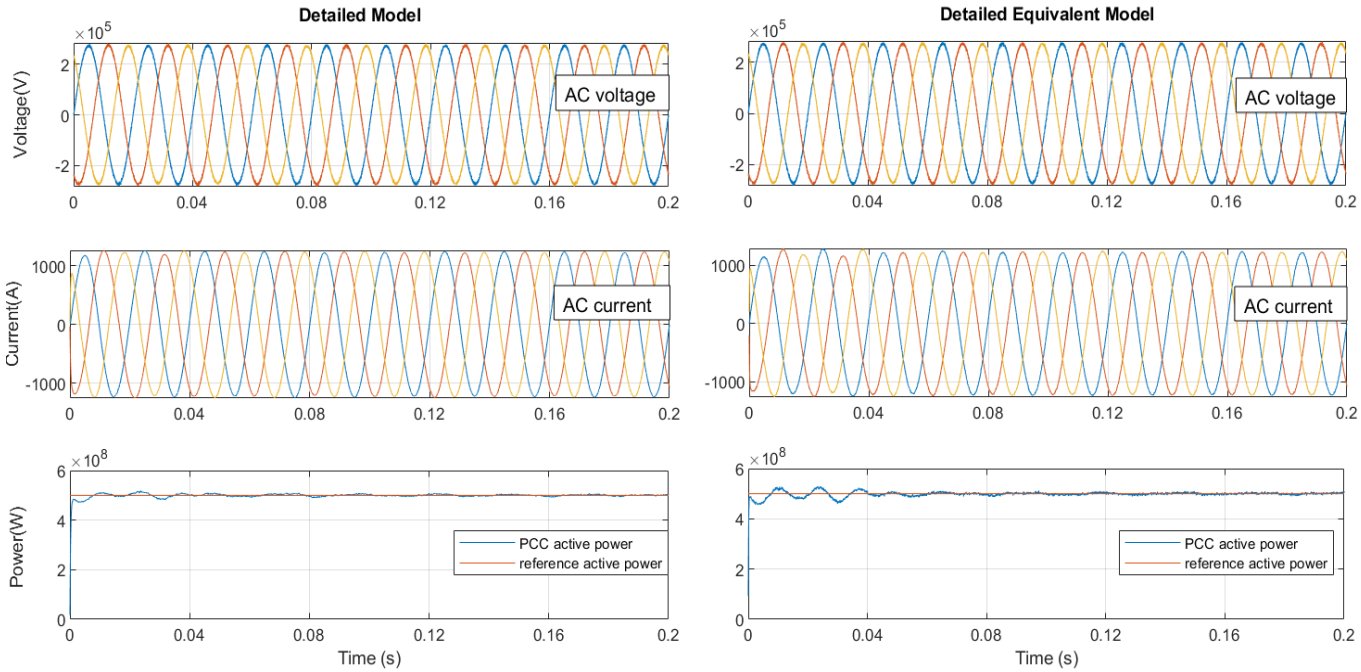


Figure 4.21 Comparison of the AC grid currents, voltages and power

4.6 Comparison and Verification of the DM and DEM with $N = 20$ SMs per Arm for Power Reference Change Transient

This section studies the power reference change transient for the DM and DEM with 20 SMs per arm. The reference AC power was reduced from 0.5 GW to 0.1 GW at 0.05 seconds. This sudden decrease leads to a drop in AC grid currents, arm currents, and SM capacitor voltage ripples. After applying the power reference change, the AC power at the PCC is able to follow the reference and the converter remains stable. The waveforms in Figs. 4.22-4.26 demonstrate a close alignment between the DM and DEM.

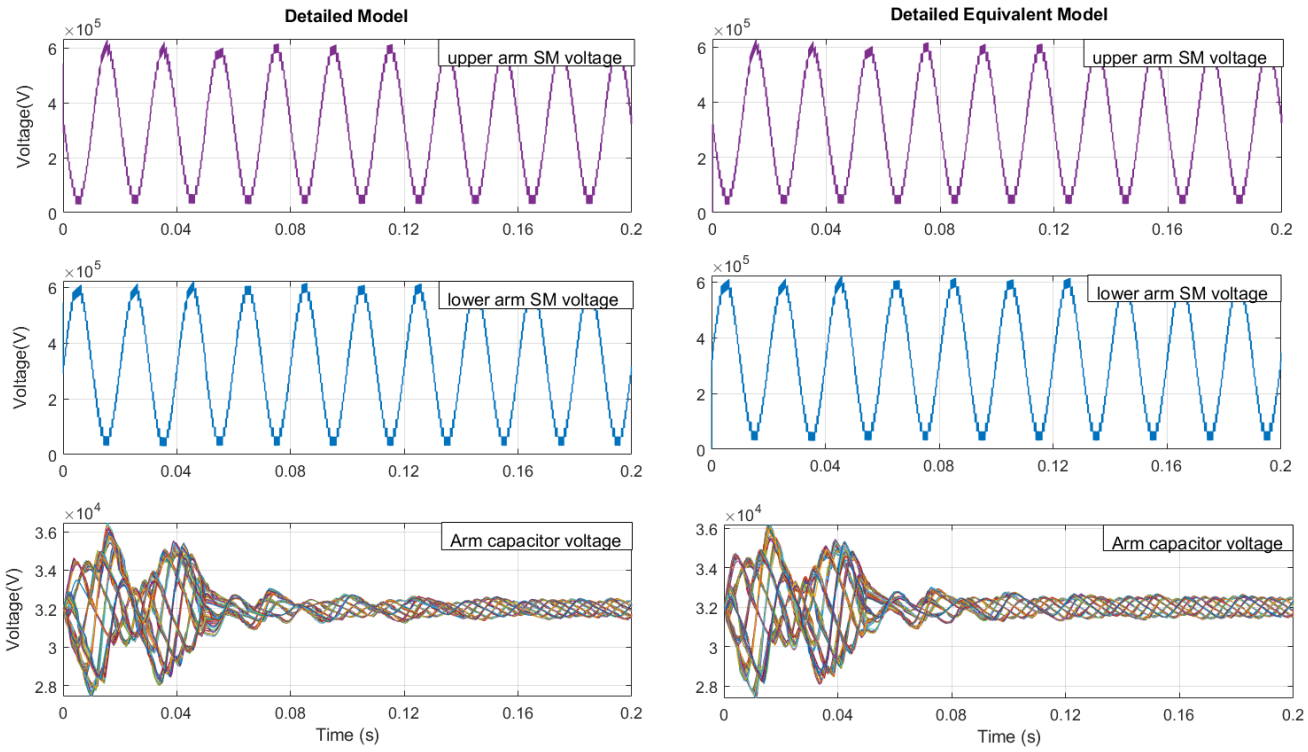


Figure 4.22 Comparison of the arm voltages and SM capacitor voltages

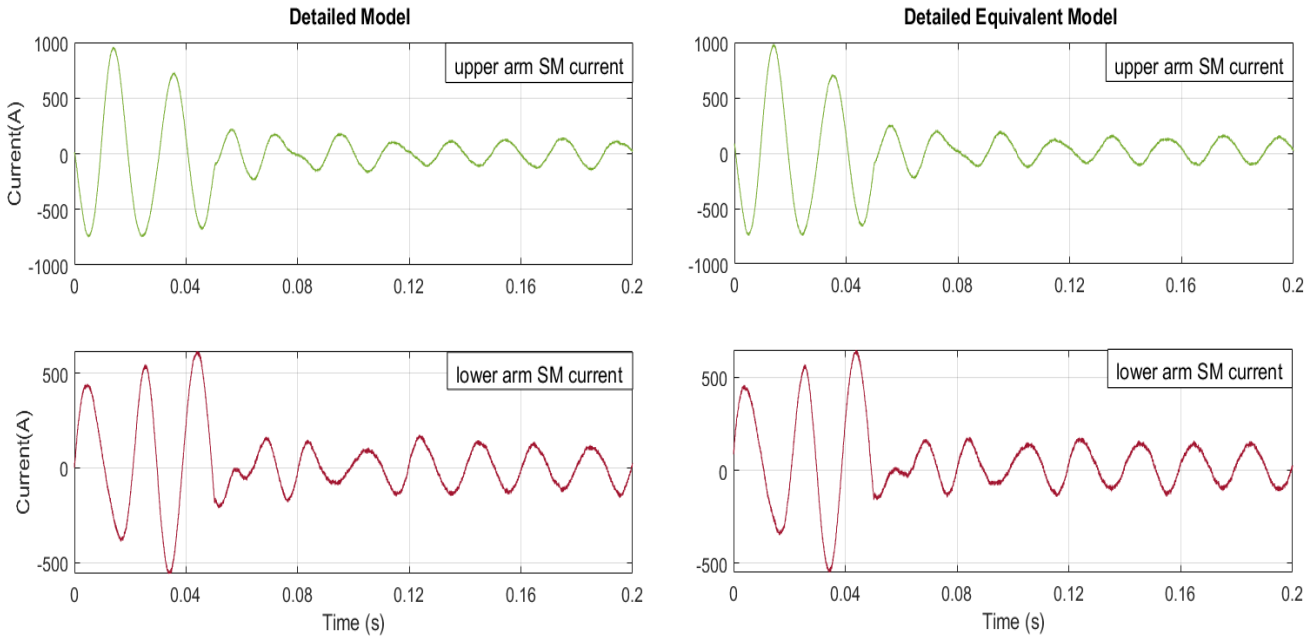


Figure 4.2311 Comparison of arm currents

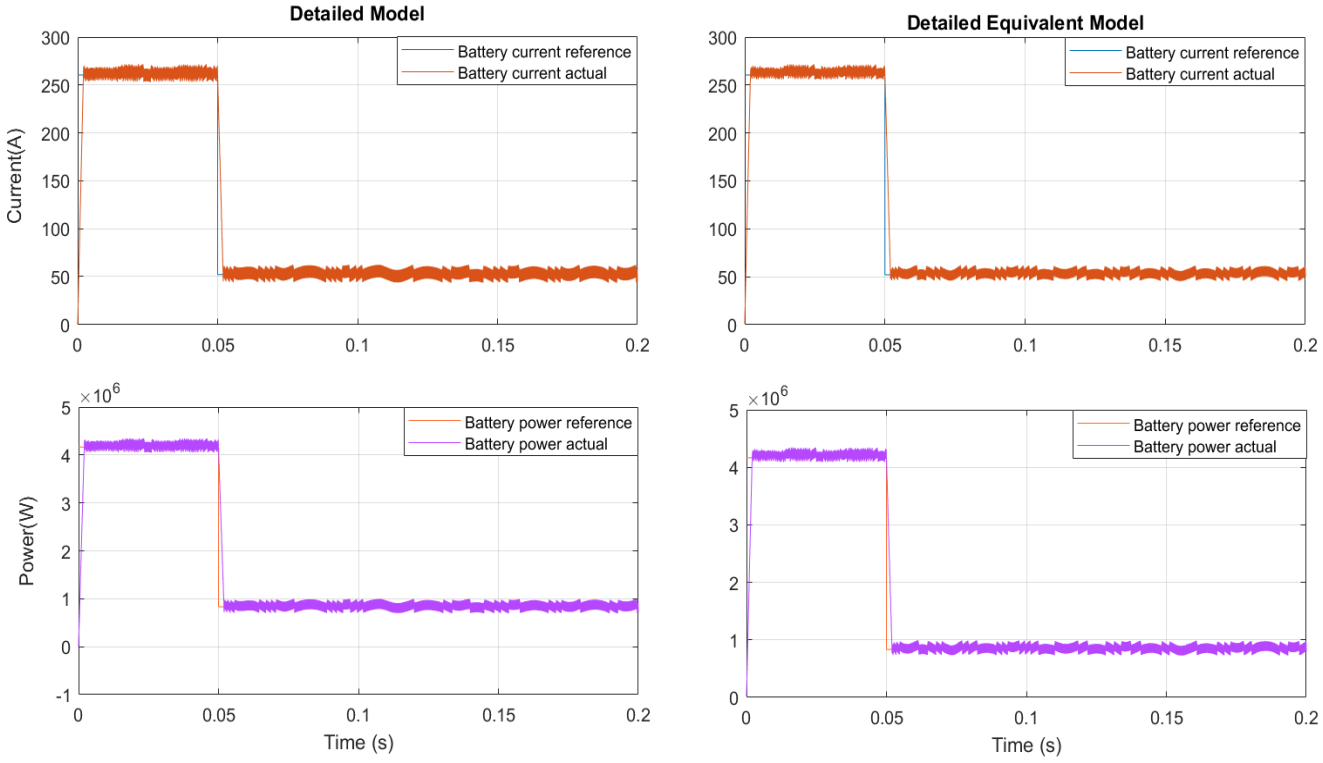


Figure 4.2412 Comparison of the battery current and power

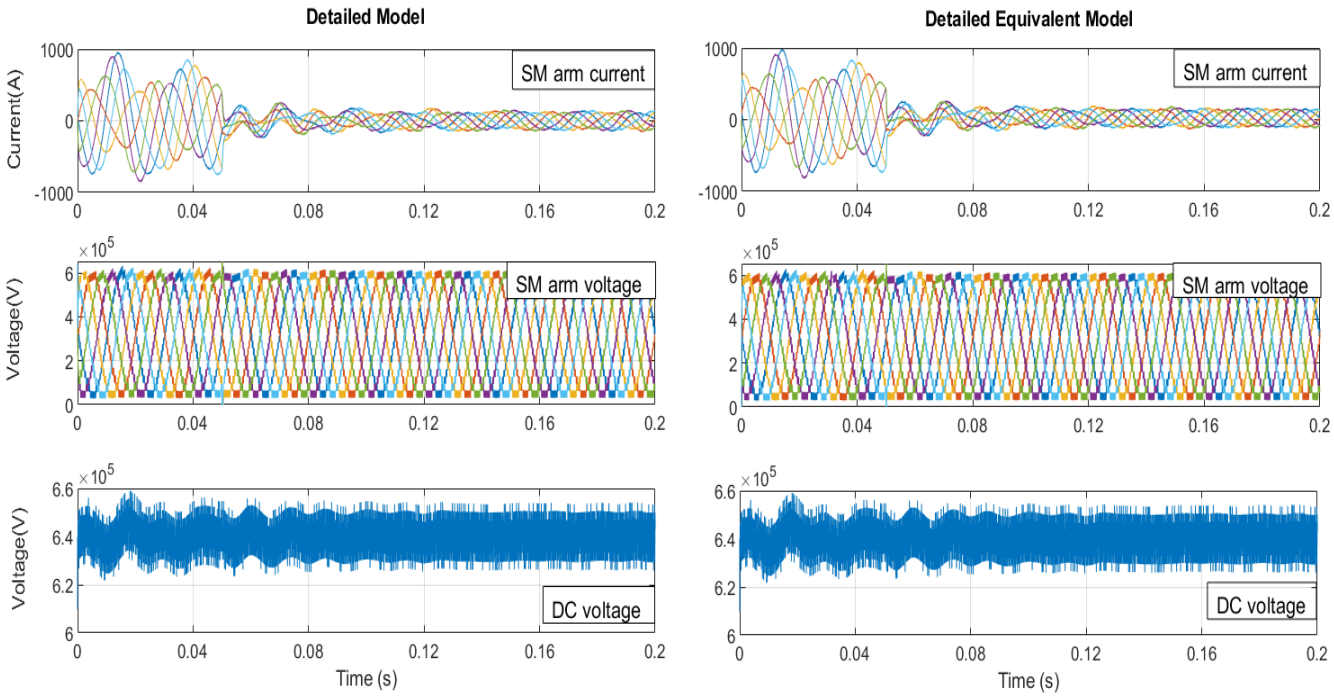


Figure 4.25 13 Comparison of the arm currents, converter voltages and the DC-link voltage

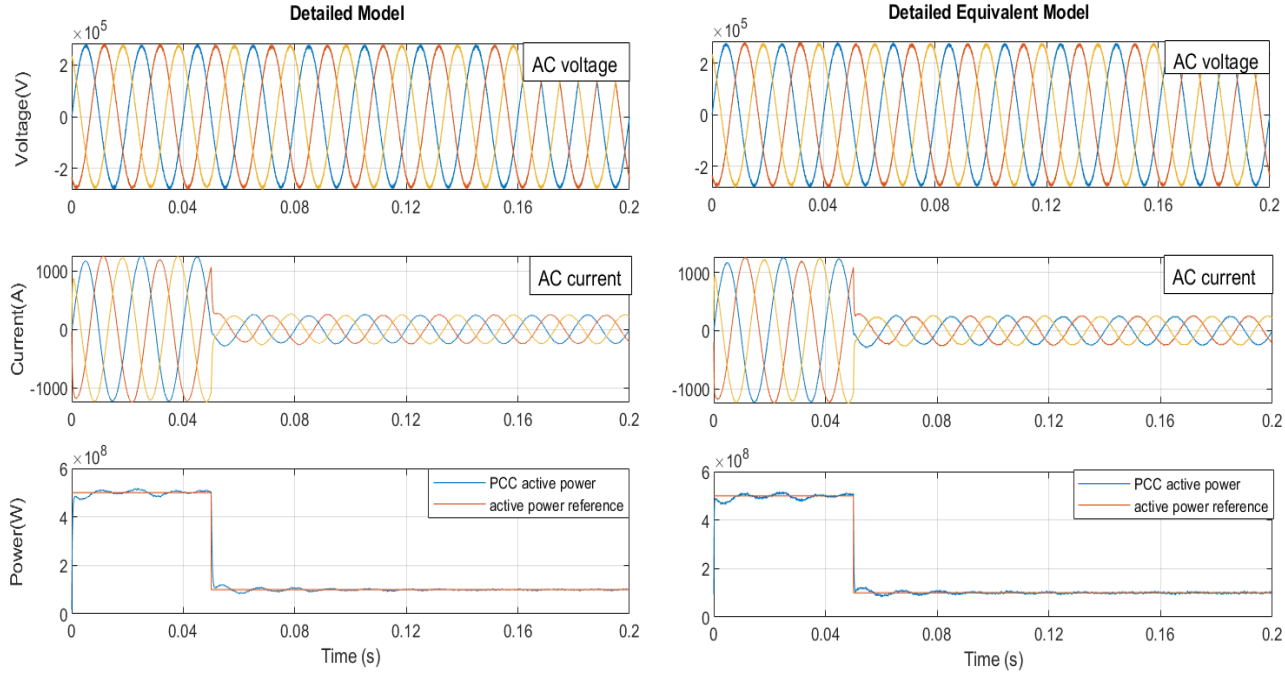


Figure 4.2614 Comparison of the AC voltage, current and power

4.7 Comparison and Verification of the DM and DEM with $N = 30$ SMs per Arm during Steady State Operation

The MMC-ES with 30 SMs per arm is used to verify the proposed DEM for steady state and transient analysis. The simulation results, depicted in Fig. 5.28, revealed that the SM capacitor voltages were reduced by one third due to the tripling the number of SMs per arm. Before 0.02 second, zero AC and battery power references are applied. After 0.02 second, 260 A and 2.1 MW of current and power are used for each SM. As the number of SMs in an arm increases, the ripples in the converter output AC voltages and currents become less noticeable, as shown in Figs. 4.27. It is observed in Figs. 4.27 – 4.30 that the DM and DEM produce very similar simulation results which validate the numerical accuracy of the DEM.

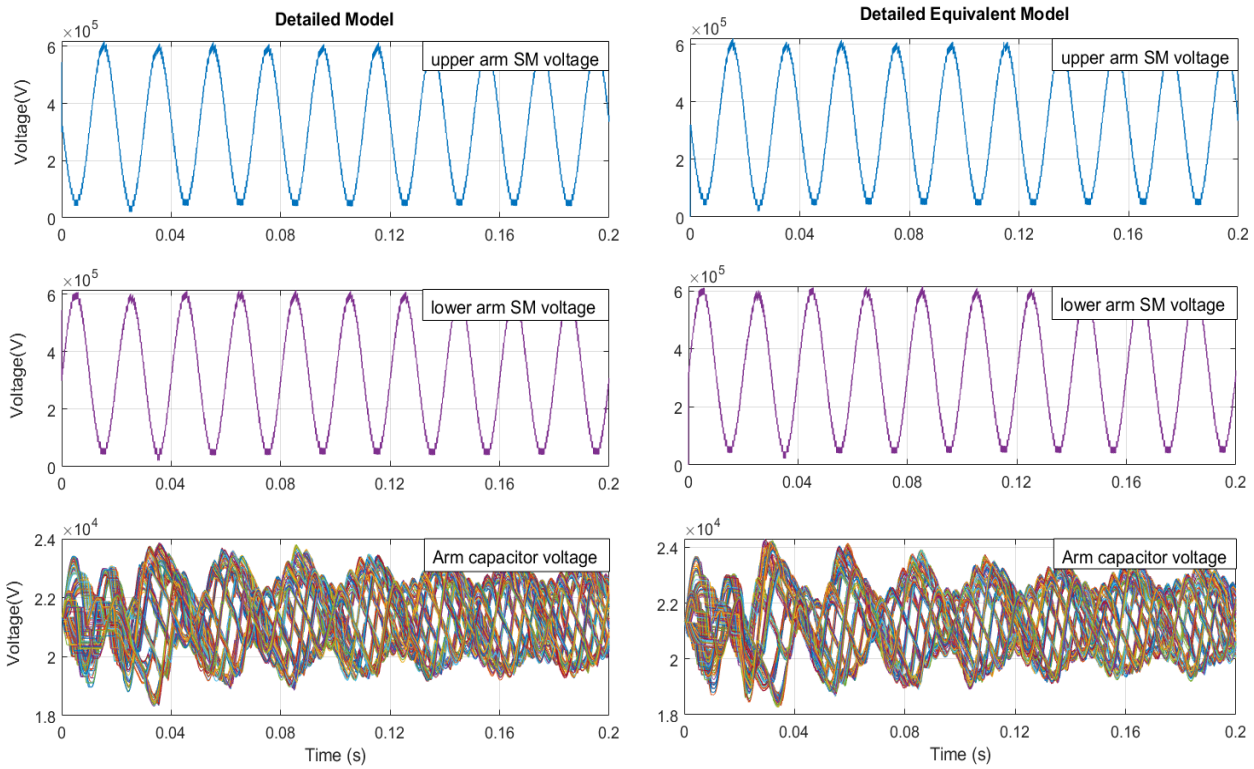


Figure 4.27 Comparison of the arm voltages and SM capacitor voltages

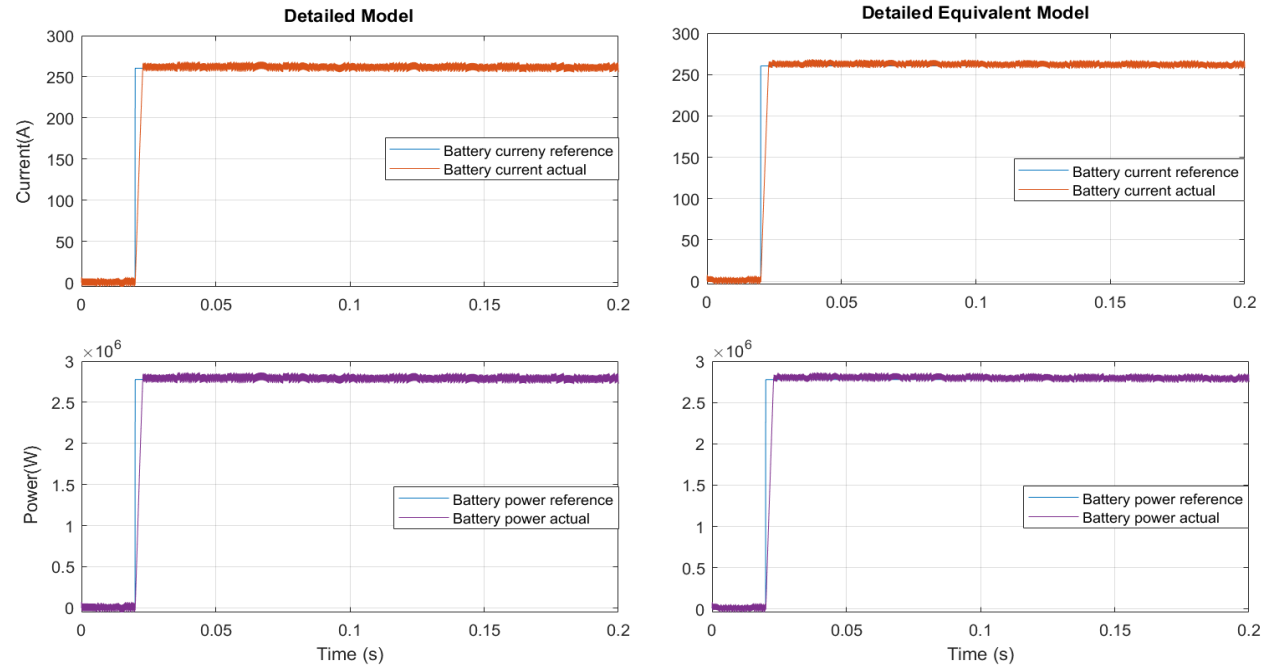


Figure 4.28 Comparison of the battery current and power

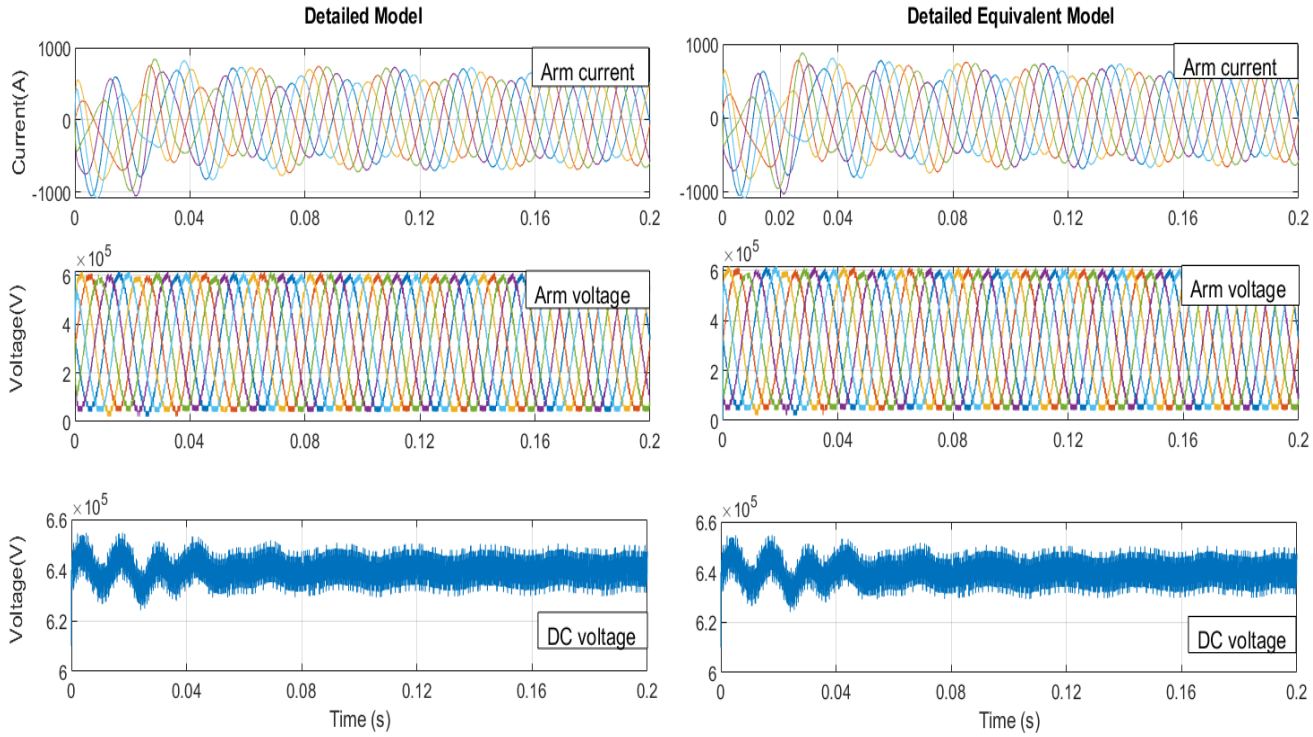


Figure 4.29 Comparison of the arm currents, voltages and DC-link voltage

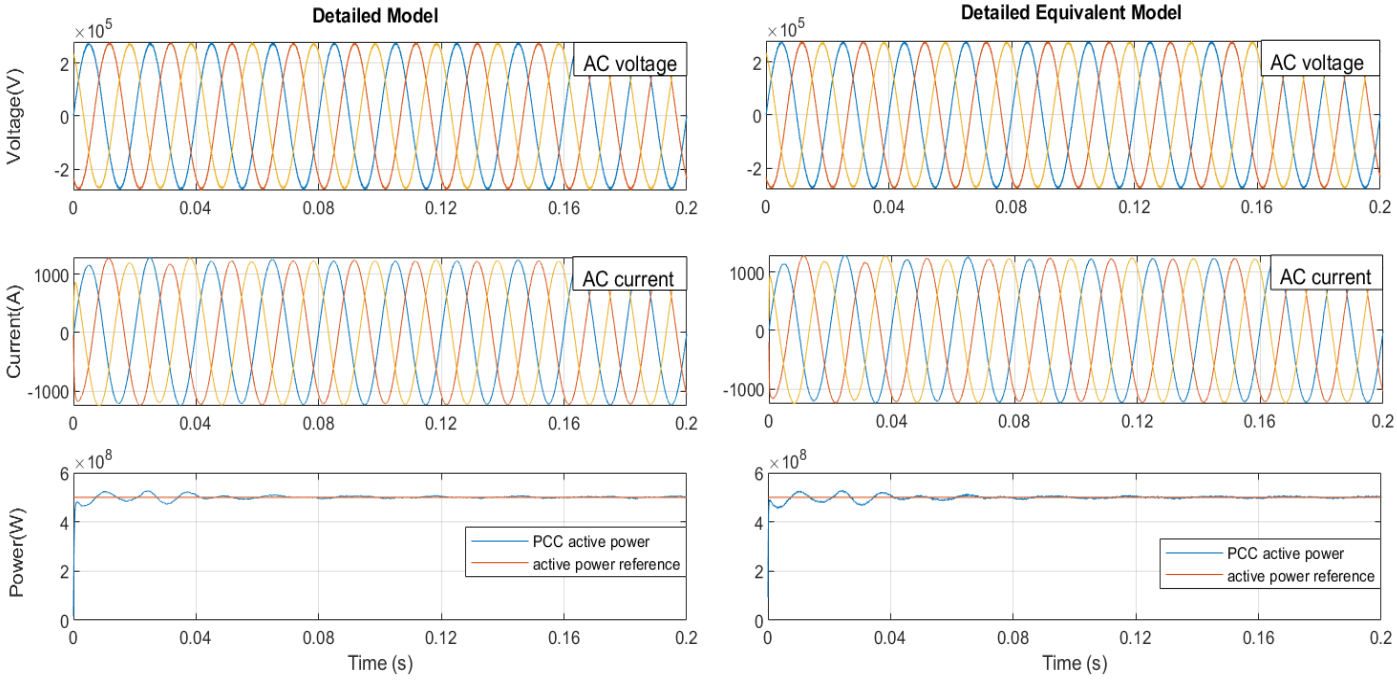


Figure 4.30 Comparison of the AC voltage, current and power

4.8 Comparison and Verification of the DM and DEM with $N = 30$ SMs for Power Reference Change Transient

In this section, the modeling accuracy of the DEM with 30 SMs per arm is verified by the DM using the power reference change transient. The AC power is decreased from 0.5 MW to 0.1 MW at 0.05 seconds. This reduction leads to a sudden decrease in the AC grid currents, arm currents, and SM capacitor voltage ripples. When the power reference change is applied, the AC power at the PCC is able to follow the reference and the converter remains stable operation. Figs. 4.31 – 4.34 demonstrate that the DM and DEM closely match each other during the power change which verifies the numerical accuracy of the DEM.

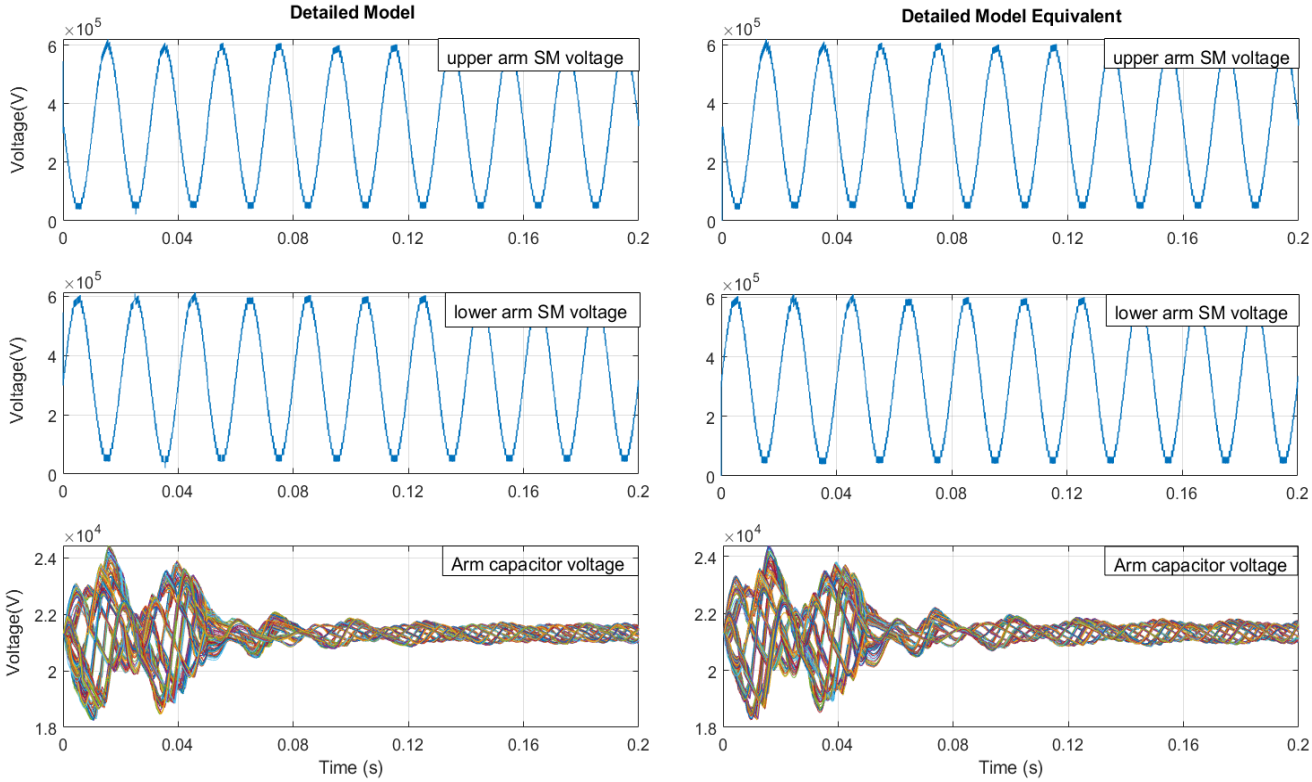


Figure 4.3115 Comparison of arm voltage and SM capacitor voltages

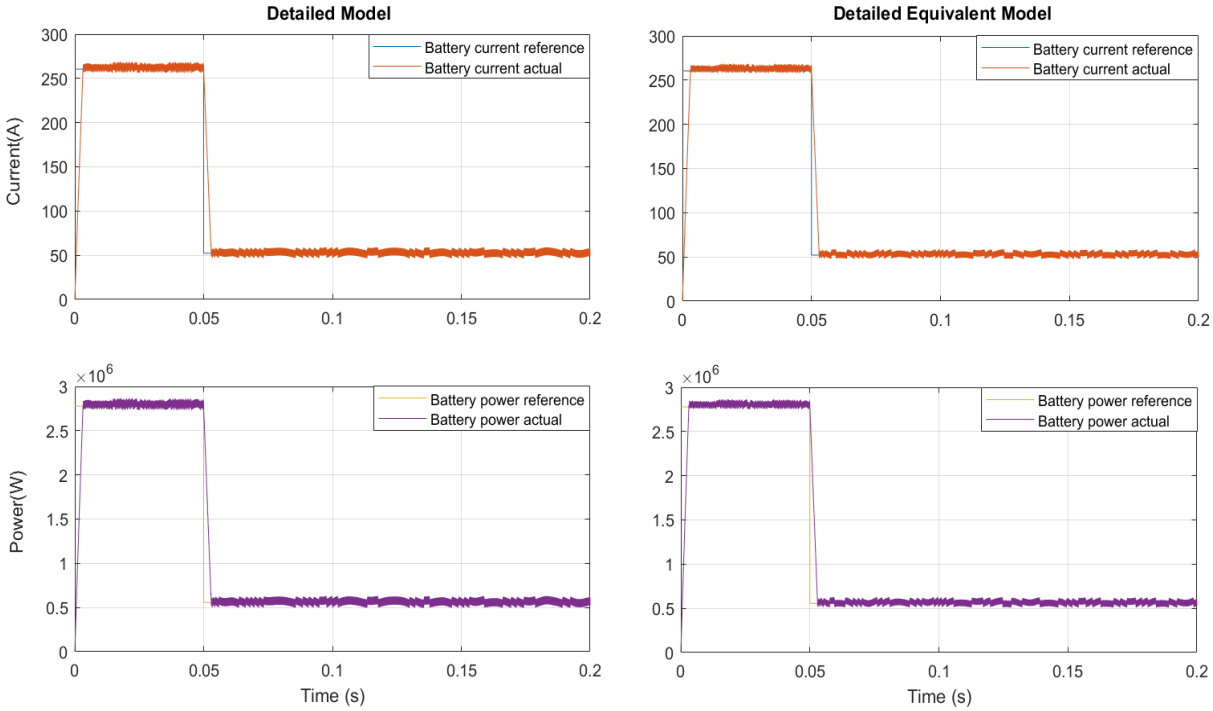


Figure 4.32 Comparison of the battery current and power

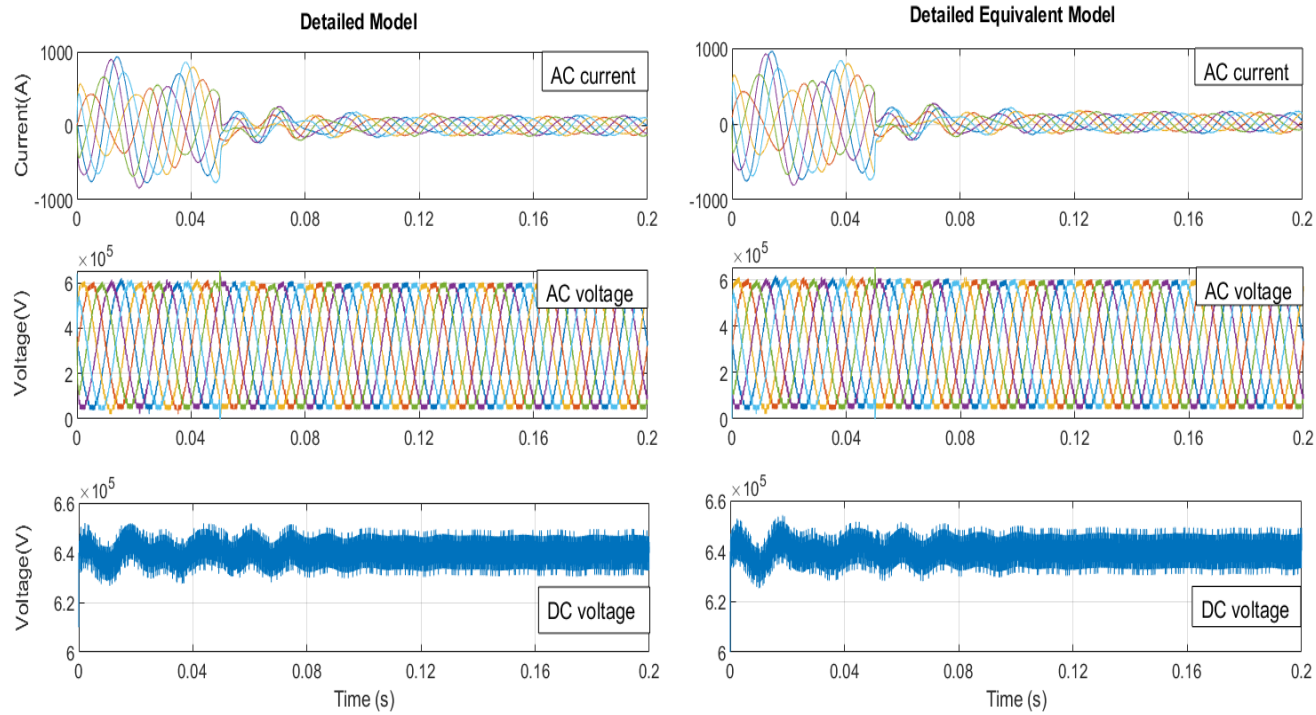


Figure 4.33 16 Comparison of the AC grid current, voltage and DC-link voltage.

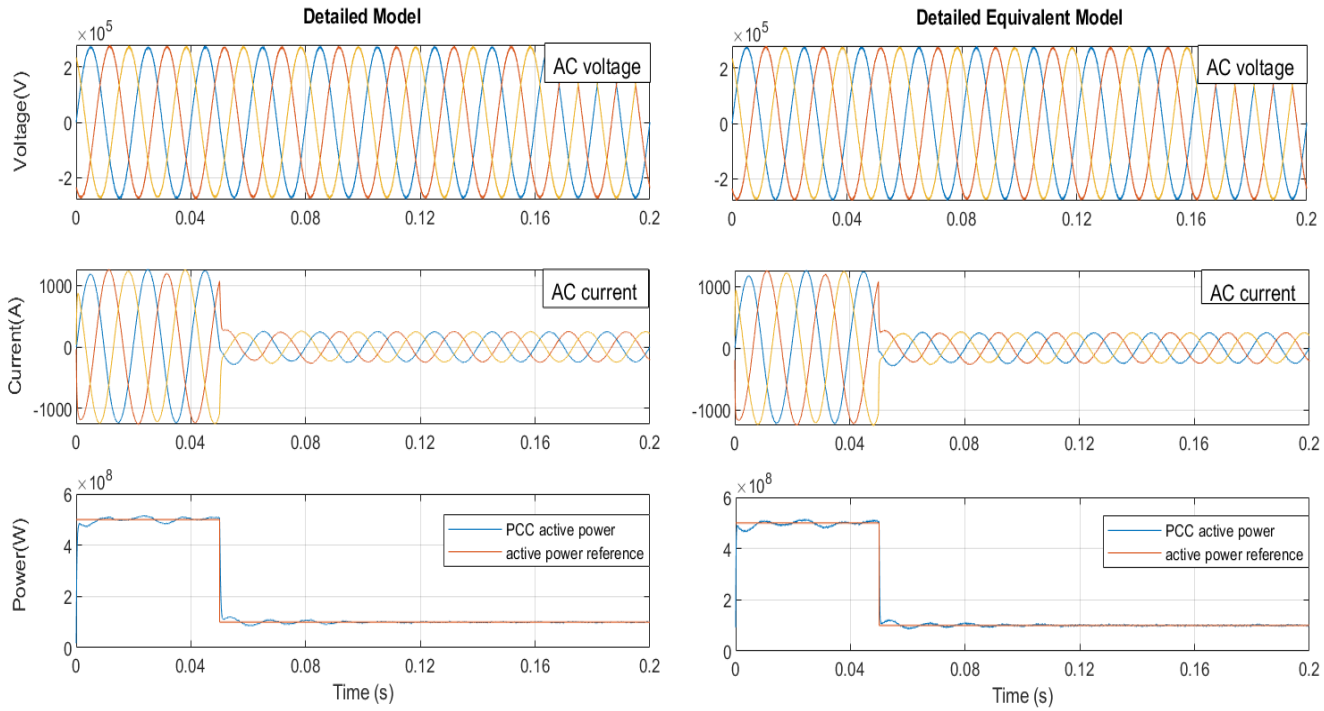


Figure 4.34 17 Comparison of the AC voltage, current, and DC-link voltage.

The numerical accuracy and close match of the DEM to the DM are concluded based on the results obtained using three error metrics: absolute error, relative error, and percentage relative error. Comparing the 10 cycles of the actual and reference battery currents of the inductor current controller of the DC-DC converter, for both models in the 10 SMs per arm simulation, a percentage relative error of 1.77% is obtained; for 20 SMs per arm, the error decreased to 1.38%; and for 30 SMs per arm, it further decreased to 0.99%. These results are within an acceptable range and show that the proposed DEM has a similar level of numerical accuracy as the DM.

4.9 CPU Performance and Efficiency

To demonstrate the proposed DEM achieves improved simulation speed over the DM, a comparison of the CPU times is conducted for both the DM and DEM using a Windows 10 Enterprise 64-bit operating system with an Intel Core i5-7440 HQ CPU running at 2.80 GHz and

8 GB of RAM. In MATLAB/Simulink, a simulation of 1 second for the MMC-ES is executed with the simulation time step of 20 μs for different numbers of SMs per arm to evaluate the numerical efficiency of the proposed DEM vs. the DM. The performance of the three-phase ES-MMC models in terms of CPU time is shown in Table 4.2, after considering an average result of 5 simulations for each number of SM in an arm for both the DM and DEM models. The DM model has a significantly longer simulation time of 77.2433s (6 times longer) for $\boldsymbol{N = 10}$ compared to the DEM model, which has a simulation time of 12.7601s.

As the number of SMs per arm increases, the simulation time for the DM model increases significantly, while it only has a minor impact on the simulation time for the DEM model. This is because the DM model's numerical efficiency decreases with an increase in the number of SMs and internal nodes in an arm circuit, leading to a consistently increasing simulation time. In contrast, the DEM model maintains a fast simulation speed due to the elimination of internal nodes in an arm circuit, which demonstrates its improved numerical efficiency and ability to handle complex power-system-level studies. The CPU simulation times for both DM and DEM are also plotted in Fig. 4.35 to show their speed performance.

Table 4. 2 CPU time comparison of the three-phase ES-MMC model

Number of SM per arm	**CPU run time (s) of Two Models**	
	DM	**DEM**
10	77.2433	12.7601
20	448.6346	15.2874
30	690.888	18.1321

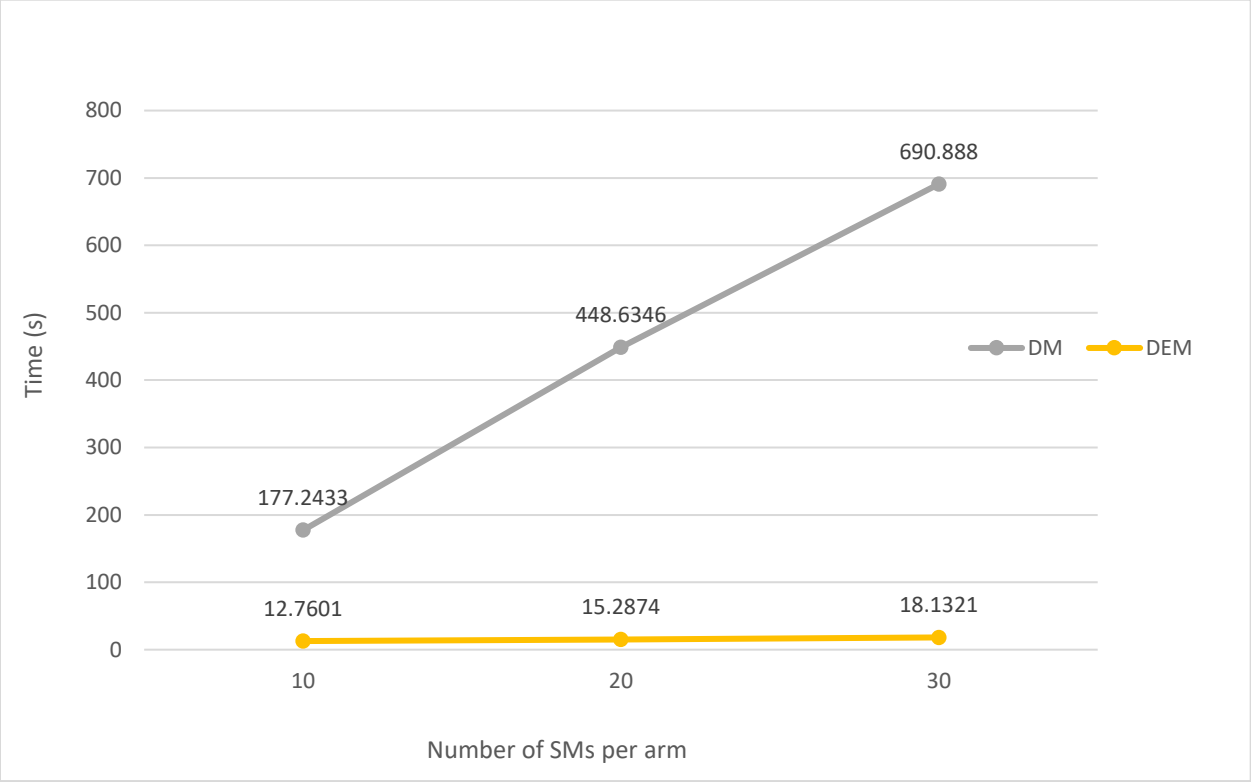


Figure 4.35 CPU speed performance comparison for DM and DEM

4.10 Simulation Limitations

The number of SMs per arm simulated for both DM and DEM for the MMC-ES were limited to 10, 20 and 30 as a result of the several challenges that can arise when attempting to model higher number of SMs in the DM. Some of these possible constraints include:

1. **Computational capacity**: The computing power needed to simulate the model increases as the number of submodules per arm increases. This may necessitate the use of more powerful computational hardware and longer simulation timeframes.
2. **Accuracy of model**: A more accurate and comprehensive understanding of the system may be developed by modeling a higher number of SMs per arm, however, increased

assumptions and complicated parameter calculations are required to effectively replicate the system. This can lead to a more complex and possibly inaccurate model.

3. **Cost**: It may not be cost-effective to increase the number of SMs per arm when the cost outweighs the benefits. In this sense, some of the cost limitations can be referred to as the computational resources, simulation run time, research budgets, and unavailable access to specialized tools, therefore, the trade-offs between the cost and the resources needed for modeling must be carefully considered first.

In addition, physical limitations may restrict the number of submodules that can be implemented in an MMC-ES in real-world applications. For instance, the amount of space that may be used or the demands of transportation may put a cap on the system's size and weight.

4.11 Summary

In this chapter, comparisons are made between the Detailed and Detailed Equivalent Models (DM and DEM) to assess the numerical efficiency and accuracy of the proposed DEM. Different (10, 20, 30) numbers of SMs per arm are used for the MMC-ES to verify the DEM. Simulation studies are taken during steady state and power change transients to examine the battery storage current and power behaviors, AC currents and voltages, SM capacitor voltages, and arm voltages of the converter. The simulation results verify the numerical accuracy of the DEM and the significantly improved numerical efficiency over the DM.

CHAPTER FIVE - CONCLUSION AND FUTURE WORK

5.1 Thesis Overview

Modular multilevel converter with integrated distributed energy storage has gained much attention as a promising technology for High Voltage Direct Current (HVDC) transmission applications. As the integration of large-scale renewable energy sources into the existing power grid increases, the MMC-ES has shown great potential in addressing challenging issues such as grid instability and reduced power quality caused by the fluctuating power output of these renewable energy sources. The MMC-ES, a complex converter circuit structure with a design that surpasses the traditional MMC, is considered in this thesis.

The scope of this thesis includes analysis and control of MMC-ES for the steady state and transient operations and the development of efficient modeling method using the DEM. Firstly, the DM, as traditional converter modeling method is constructed using standard discrete model library components from a commercial power electronic system transient simulation tool, such as Simulink/Simscape Electrical/Specialized Power Systems to represents the MMC-ES. After that, the DEM is proposed as a numerically efficient modeling method to accelerate the simulation of the MMC-ES. Different numbers of SMs per arm of the MMC-ES are used to verify the improved simulation efficiency in terms of the CPU times when executing the DM and the DEM in Simulink. This thesis is divided into five chapters, the summaries of which are outlined in the subsequent sections.

- In Chapter 1, the rationale for investigating the MMC-ES technology for the VSC-HVDC applications was presented. A foundational framework for the development of the MMC-

ES and an overview of the various converter topologies with the chosen method of energy storage integration were provided. Additionally, the objectives to be accomplished at the end of the project were outlined.

- In Chapter 2, a comprehensive examination of the traditional MMC was conducted, including a review of its various SM topology circuit structures, which can be applied to MMC-ES topologies. A single-phase mathematical model was created for the purpose of easily extending it to a three-phase structure. The various types of pulse width modulation methods were also analyzed in order to determine a particular switching modulation type should be chosen. Additionally, the sizing of inductors and capacitors, which is an important factor in controlling SM capacitor voltage ripples, was discussed.
- In Chapter 3, thorough analysis of the control operations of the MMC-ES was presented. Several control schemes were developed, including the circulating current suppression control that restricts the distorted current within the arms caused by the voltage difference between the SMs and the DC side. The MMC-ES high level outer and inner loop controls that converts the measured grid voltage and current into reference voltage and current for the closed-loop feedback controllers. Additionally, the SM capacitor voltages are carefully regulated by the MMC voltage balancing algorithm which sorts the SM capacitor voltages in an arm and charges those with lower voltages up to the rated value or discharges those with higher values by the arm current. The battery current and power transfer are effectively managed through the use of a controller designed to interface the energy storage side with the MMC side, which was accomplished by collectively controlling the inductor current and the DC-DC converter output voltage. Finally, the DEM was proposed to

accelerate the EMT simulation of the MMC-ES. The EMT model of the SM with the DC-DC converter and the arm equivalent circuit model were discussed for both de-blocking and blocking modes.

- In Chapter 4, the simulation results for the DM and DEM of MMC-ES were presented for different numbers of SMs per arm to verify the proposed DEM using the DM as the reference solution. The simulation results demonstrate that the DM and DEM give almost identical simulation results which verify the DEM's numerical accuracy. On the other hand, the CPU execution time of the DEM has remarkable improvement of 38 folds, compared to that of the DM for the MMC-ES with 30 SMs per arm.

5.2 Conclusion

In summary, a modular multilevel converter with integrated energy storage was presented using both detailed model and the detailed equivalent model to investigate its function, control method, and numerical efficiency. The detailed model was found to be slow and inefficient for an EMT simulation as the numbers of SMs per arm of the modular multilevel converter increase. The integration of the energy storage batteries with the MMC SMs via DC/DC converters technically doubled the complexity of the circuit structure and expand the control complexity of the MMC. However, a beneficial power transfer occurs between the two sides of the modular multilevel converter, while power balance was maintained in all converter arms.

The Thevenin equivalent method was implemented in the simplified detailed equivalent model to mitigate the complexity of the detailed structure by eliminating the internal nodes introduced by the large number of SMs in each converter arm. This effectively reduces the size of

the admittance matrix of the nodal voltage equation in the discrete time domain modeling. This advanced technique demonstrated accuracy and the ability to retain all relevant information from the detailed modeling method.

Furthermore, close match of the simulation results was observed between the DM and the DEM, with the DM exhibiting a much longer simulation time in comparison to the DEM as the number of SMs per arm increased from 10 to 20 and 30. Despite the simulation time constraint of the DM, both models can be effectively utilized to model the MMC-ES, including other SM and DC-DC converter topologies with high switching frequency, for power system studies. The battery charging control and SM voltage balancing algorithm were viable for both models with the circulating current control effectively suppressing any circulating current harmonics in an arm. Importantly, the battery side control impressively restricted the currents from disrupting the SM capacitor voltages balance.

5.3 Future Work

Graphics Processing Unit (GPU), a specialized processor originally designed to accelerate graphics rendering, can further improve simulation efficiency of the MMC-ES since the GPUs can process many pieces of data simultaneously. Several research works [66]–[70] haven been proposed to use GPUs for the parallel-rate simulations of power system transients. In [67], a massive thread parallel simulation of large-scale power electronic circuits was proposed which employs device-level modeling on the graphics processors (GPUs) to obtain higher data throughput and lower execution times. The parallel massive-thread modules were proposed for the nonlinear physics-based insulated gate bipolar transistor (IGBT) and power diode components in

[67]. For the future work, a multi-layer hierarchical modeling methodology can be proposed for high-performance computing of the modular multilevel converter with integrated energy storage. Heterogeneous computing platform using CPU and GPU can be investigated through which the computational tasks are properly assigned to CPU and GPU to fully exploit their multi-rate and parallel processing features. In addition, it will be desirable to develop a scaled-down prototype of the MMC-ES in order to experiment various converter controls and to verify the simulation results of the DM and DEM.

Bibliography

[1] C. Joe-Uzuegbu and G. Chukwudebe, “High Voltage Direct Current (HVDC) technology: An alternative means of power transmission,” *3rd IEEE Int. Conf. Adapt. Sci. Technol. ICAST 2011, Proc.*, no. Icast, pp. 121–125, 2011, doi: 10.1109/ICASTech.2011.6145163.

[2] K. Sharifabadi, L. Harnefors, H. P. Nee, S. Norrga, and R. Teodorescu, *Design, control and application of modular multilevel converters for HVDC transmission systems*. 2016. doi: 10.1002/9781118851555.

[3] N. Ahmed *et al.*, “Efficient Modeling of an MMC-Based Multiterminal DC System Employing Hybrid HVDC Breakers,” *IEEE Trans. Power Deliv.*, vol. 30, no. 4, pp. 1792–1801, Aug. 2015, doi: 10.1109/TPWRD.2015.2398825.

[4] J. B. Soomro, F. Akhtar, R. Hussain, J. Ahmed Ansari, and H. M. Munir, “A Detailed Review of MMC Circuit Topologies and Modelling Issues,” *Int. Trans. Electr. Energy Syst.*, vol. 2022, pp. 1–17, 2022, doi: 10.1155/2022/8734010.

[5] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, “VSC-based HVDC power transmission systems: An overview,” *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, 2009, doi: 10.1109/TPEL.2008.2008441.

[6] X. Pei, G. Tang, H. Pang, M. Kong, J. Yang, and Y. Wu, “A general modeling approach for the MMC averaged-value model in large-scale DC grid,” *2017 IEEE Conf. Energy Internet Energy Syst. Integr. EI2 2017 - Proc.*, vol. 2018-Janua, pp. 1–6, 2017, doi: 10.1109/EI2.2017.8245241.

[7] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, “Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs,” *IEEE Trans. Power Deliv.*, vol. 26, no. 1, pp. 316–324, 2011, doi: 10.1109/TPWRD.2010.2060737.

[8] L. Zhang, J. Qin, X. Wu, S. Debnath, and M. Saeedifard, “A Generalized Precharging Strategy for Soft Startup Process of the Modular Multilevel Converter-Based HVDC Systems,” *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5645–5657, 2017, doi: 10.1109/TIA.2017.2736958.

[9] M. Farhadi and O. Mohammed, “Energy storage systems for high power applications,” *IEEE Ind. Appl. Soc. - 51st Annu. Meet. IAS 2015, Conf. Rec.*, vol. 89, no. 12, 2015, doi: 10.1109/IAS.2015.7356787.

[10] M. Bragard, N. Soltau, S. Thomas, and R. W. De Doncker, “The balance of renewable sources and user demands in grids: Power electronics for modular battery energy storage systems,” *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3049–3056, 2010, doi: 10.1109/TPEL.2010.2085455.

[11] J. Harasawa and T. Ikegami, “Load leveling effects by massively introduced residential battery storage systems,” *2017 IEEE Innov. Smart Grid Technol. - Asia Smart Grid Smart Community, ISGT-Asia 2017*, pp. 1–6, 2018, doi: 10.1109/ISGT-Asia.2017.8378386.

[12] N. Ahmed, L. Angquist, S. Norrga, A. Antonopoulos, L. Harnefors, and H. P. Nee, “A computationally efficient continuous model for the modular multilevel converter,” in *IEEE*

Journal of Emerging and Selected Topics in Power Electronics, Dec. 2014, vol. 2, no. 4, pp. 1139–1148. doi: 10.1109/JESTPE.2014.2332041.

[13] S. P. Teeuwsen, "Simplified dynamic model of a voltage-sourced converter with modular multilevel converter design," *2009 IEEE/PES Power Syst. Conf. Expo. PSCE 2009*, pp. 1–6, 2009, doi: 10.1109/PSCE.2009.4839922.

[14] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 163–175, 2015, doi: 10.1109/TPEL.2014.2303297.

[15] M. Guan, Z. Xu, and H. Chen, "Control and modulation strategies for modular multilevel converter based HVDC system," in *IECON Proceedings (Industrial Electronics Conference)*, 2011, pp. 849–854. doi: 10.1109/IECON.2011.6119421.

[16] W. Li and J. Belanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time HIL test bench," *IEEE Trans. Power Deliv.*, vol. 31, no. 5, pp. 2401–2409, 2016, doi: 10.1109/TPWRD.2016.2541461.

[17] Q. Chen, R. Li, and X. Cai, "Analysis and Fault Control of Hybrid Modular Multilevel Converter with Integrated Battery Energy Storage System," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 64–78, 2017, doi: 10.1109/JESTPE.2016.2623672.

[18] S. Alotaibi and A. Darwish, "Modular multilevel converters for large-scale grid-connected photovoltaic systems: A review," *Energies*, vol. 14, no. 19, pp. 1–30, 2021, doi: 10.3390/en14196213.

[19] F. Martinez-Rodrigo, D. Ramirez, A. B. Rey-Boue, S. De Pablo, and L. C. Herrero-De Lucas, “Modular multilevel converters: Control and applications,” *Energies*, vol. 10, no. 11. MDPI AG, Nov. 01, 2017. doi: 10.3390/en10111709.

[20] J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian, and S. Nguefeu, “Detailed and averaged models for a 401-level MMC-HVDC system,” *IEEE Trans. Power Deliv.*, vol. 27, no. 3, pp. 1501–1508, 2012, doi: 10.1109/TPWRD.2012.2188911.

[21] N. Herath, S. Filizadeh, and M. S. Toulabi, “Modeling of a Modular Multilevel Converter with Embedded Energy Storage for Electromagnetic Transient Simulations,” *IEEE Trans. Energy Convers.*, vol. 34, no. 4, pp. 2096–2105, 2019, doi: 10.1109/TEC.2019.2937761.

[22] M. Coppola, A. Del Pizzo, and D. Iannuzzi, “A power traction converter based on Modular Multilevel architecture integrated with energy storage devices,” *Electr. Syst. Aircraft, Railw. Sh. Propulsion, ESARS*, pp. 3–9, 2012, doi: 10.1109/ESARS.2012.6387415.

[23] Q. Yuan, F. Yang, A. Li, and T. Ma, “A Novel Hybrid Control Strategy for the Energy Storage Modular Multilevel Converters,” *IEEE Access*, vol. 9, pp. 59466–59474, 2021, doi: 10.1109/ACCESS.2021.3073108.

[24] I. Trintis, S. Munk-Nielsen, and R. Teodorescu, “A new modular multilevel converter with integrated energy storage,” *IECON Proc. (Industrial Electron. Conf.*, pp. 1075–1080, 2011, doi: 10.1109/IECON.2011.6119457.

[25] J. M. Carrasco *et al.*, “Power-electronic systems for the grid integration of renewable energy sources: A survey,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, 2006, doi:

10.1109/TIE.2006.878356.

[26] F. Blaabjerg, Z. Chen, and S. B. Kjaer, “Power electronics as efficient interface in dispersed power generation systems,” *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, 2004, doi: 10.1109/TPEL.2004.833453.

[27] T. Soong and P. W. Lehn, “Internal power flow of a modular multilevel converter with distributed energy resources,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 4, pp. 1127–1138, 2014, doi: 10.1109/JESTPE.2014.2342656.

[28] T. Soong and P. W. Lehn, “Assessment of Fault Tolerance in Modular Multilevel Converters with Integrated Energy Storage,” *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4085–4095, 2016, doi: 10.1109/TPEL.2015.2477834.

[29] I. Trintis, S. Munk-Nielsen, and R. Teodorescu, “A new modular multilevel converter with integrated energy storage,” in *IECON Proceedings (Industrial Electronics Conference)*, 2011, pp. 1075–1080. doi: 10.1109/IECON.2011.6119457.

[30] T. Soong, “Modular multilevel converters with integrated energy storage,” *Univ. Toronto PhD Thesis*, 2015.

[31] X. Yang, P. Wen, Y. Xue, T. Q. Zheng, and Y. Wang, “Super capacitor energy storage based MMC for energy harvesting in mine hoist application,” *Energies*, vol. 10, no. 9, 2017, doi: 10.3390/en10091428.

[32] B. Ren, Y. Xu, and Q. Lan, “A control method for battery energy storage system based on

MMC," *2015 IEEE 2nd Int. Futur. Energy Electron. Conf. IFEEC 2015*, pp. 1–6, 2015, doi: 10.1109/IFEEC.2015.7361589.

[33] Z. Wang, H. Lin, and Y. Ma, "Improved capacitor voltage balancing control for multimode operation of modular multilevel converter with integrated battery energy storage system," *IET Power Electron.*, vol. 12, no. 11, pp. 2751–2760, 2019, doi: 10.1049/iet-pel.2019.0033.

[34] W. Zeng, R. Li, and X. Cai, "A New Hybrid Modular Multilevel Converter with Integrated Energy Storage," *IEEE Access*, vol. 7, pp. 172981–172993, 2019, doi: 10.1109/ACCESS.2019.2940101.

[35] R. Zeng, L. Xu, and L. Yao, "An improved modular multilevel converter with DC fault blocking capability," *IEEE Power Energy Soc. Gen. Meet.*, vol. 2014-Octob, no. October, pp. 1–5, 2014, doi: 10.1109/PESGM.2014.6938937.

[36] X. Li *et al.*, "Universal terminal model suitable for various modular multilevel converter topologies for power-system-level simulation application," *IET Gener. Transm. Distrib.*, vol. 12, no. 3, pp. 737–744, 2018, doi: 10.1049/iet-gtd.2017.0328.

[37] W. Li and J. Belanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time HIL test bench," *IEEE Trans. Power Deliv.*, vol. 31, no. 5, pp. 2401–2409, 2016, doi: 10.1109/TPWRD.2016.2541461.

[38] H. Saad *et al.*, "Modular multilevel converter models for electromagnetic transients," *IEEE Trans. Power Deliv.*, vol. 29, no. 3, pp. 1481–1489, 2014, doi: 10.1109/TPWRD.2013.2285633.

[39] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, “Operation, control, and applications of the modular multilevel converter: A review,” *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, 2015, doi: 10.1109/TPEL.2014.2309937.

[40] W. Zeng, R. Li, and X. Cai, “A New Hybrid Modular Multilevel Converter with Integrated Energy Storage,” *IEEE Access*, vol. 7, pp. 172981–172993, 2019, doi: 10.1109/ACCESS.2019.2940101.

[41] S. Du, A. Dekka, W. Bin, and N. Zargari, “Modular Multilevel Converters Analysis, Control, and Applications by Sixing Du, Apparao Dekka, Bin Wu, Navid Zargari (z-lib.org)”.

[42] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, “Analysis of the phase-shifted carrier modulation for modular multilevel converters,” *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297–310, 2015, doi: 10.1109/TPEL.2014.2299802.

[43] Y. Yabing, L. Hui, F. Ouyang, L. Wenwu, X. Hao, and W. Ding, “Design of Basic Control Strategy for Energy Storage Type MMC,” *5th IEEE Conf. Energy Internet Energy Syst. Integr. Energy Internet Carbon Neutrality, EI2 2021*, pp. 3861–3865, 2021, doi: 10.1109/EI252483.2021.9713353.

[44] Y. Tang, Z. Zhang, and Z. Xu, “IEEE PES Transactions on Energy Conversion A Novel Average Model for Modular Multilevel Converter A Novel Average Model for Modular Multilevel Converter with Embedded Energy Storage,” 2021.

[45] N. Herath and S. Filizadeh, “Average-Value Model for a Modular Multilevel Converter

with Embedded Storage," *IEEE Trans. Energy Convers.*, vol. 36, no. 2, pp. 789–799, 2021, doi: 10.1109/TEC.2020.3014793.

[46] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, F. J. Moreno, K. J. Dyke, and D. R. Trainer, "Cell capacitor sizing in modular multilevel converters and hybrid topologies," *2014 16th Eur. Conf. Power Electron. Appl. EPE-ECCE Eur. 2014*, pp. 1–10, 2014, doi: 10.1109/EPE.2014.6910972.

[47] Z. Wang, H. Lin, Y. Ma, and T. Wang, "A prototype of modular multilevel converter with integrated battery energy storage," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 434–439, 2017, doi: 10.1109/APEC.2017.7930730.

[48] Y. Ma, J. Xiao, H. Lin, and Z. Wang, "A Novel Battery Integration Method of Modular Multilevel Converter with Battery Energy Storage System for Capacitor Voltage Ripple Reduction," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12250–12261, 2021, doi: 10.1109/TIE.2020.3044780.

[49] Z. Ke *et al.*, "Optimal submodule capacitor sizing for modular multilevel converters with common mode voltage injection and circulating current control," *2017 IEEE Energy Convers. Congr. Expo. ECCE 2017*, vol. 2017-Janua, pp. 1802–1808, 2017, doi: 10.1109/ECCE.2017.8096013.

[50] M. Coppola, A. Del Pizzo, and D. Iannuzzi, "A power traction converter based on Modular Multilevel architecture integrated with energy storage devices," *Electr. Syst. Aircraft, Railw. Sh. Propulsion, ESARS*, pp. 1–7, 2012, doi: 10.1109/ESARS.2012.6387415.

[51] H. Yang, Y. Dong, W. Li, and X. He, “Average-Value Model of Modular Multilevel Converters Considering Capacitor Voltage Ripple,” *IEEE Trans. Power Deliv.*, vol. 32, no. 2, pp. 723–732, 2017, doi: 10.1109/TPWRD.2016.2555983.

[52] F. Muhammad, H. Rasheed, I. Ali, R. Alroobaea, and A. Binmahfoudh, “Design and Control of Modular Multilevel Converter for Voltage Sag Mitigation,” *Energies*, vol. 15, no. 5, pp. 1–26, 2022, doi: 10.3390/en15051681.

[53] R. Zeng, L. Xu, L. Yao, and D. J. Morrow, “Precharging and dc fault ride-Through of hybrid MMC-based HVDC systems,” *IEEE Trans. Power Deliv.*, vol. 30, no. 3, pp. 1298–1306, 2015, doi: 10.1109/TPWRD.2014.2360042.

[54] Y. Li *et al.*, “PLL synchronization stability analysis of MMC-connected wind farms under high-impedance AC Faults,” *IEEE Trans. Power Syst.*, vol. 36, no. 3, pp. 2251–2261, 2021, doi: 10.1109/TPWRS.2020.3025917.

[55] S. K. Kim, J. H. Jeon, J. B. Ahn, B. Lee, and S. H. Kwon, “Frequency-shift acceleration control for anti-islanding of a distributed-generation inverter,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 494–504, 2010, doi: 10.1109/TIE.2009.2036028.

[56] E. N. Abildgaard and M. Molinas, “Modelling and control of the modular multilevel converter (MMC),” *Energy Procedia*, vol. 20, no. Mmc, pp. 227–236, 2012, doi: 10.1016/j.egypro.2012.03.023.

[57] F. Gao, L. Zhang, Q. Zhou, M. Chen, T. Xu, and S. Hu, “State-of-charge balancing control strategy of battery energy storage system based on modular multilevel converter,” *2014*

IEEE Energy Convers. Congr. Expo. ECCE 2014, pp. 2567–2574, 2014, doi: 10.1109/ECCE.2014.6953744.

[58] Q. Tu, Z. Xu, and L. Xu, "Reduced Switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Deliv.*, vol. 26, no. 3, pp. 2009–2017, 2011, doi: 10.1109/TPWRD.2011.2115258.

[59] A. Deo Almeida, F. T. Ghetti, A. S. B. Ribeiro, P. M. De Almeida, and P. G. Barbosa, "Circulating currents suppression strategies for modular multilevel converter," *14th Brazilian Power Electron. Conf. COBEP 2017*, vol. 2018-Janua, pp. 1–5, 2017, doi: 10.1109/COBEP.2017.8257263.

[60] M. Quraan, P. Tricoli, S. D'Arco, and L. Piegari, "Efficiency Assessment of Modular Multilevel Converters for Battery Electric Vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2041–2051, 2017, doi: 10.1109/TPEL.2016.2557579.

[61] N. Watson and J. Arrillaga, "Power systems electromagnetic transients simulation (2nd edition)," *Power Syst. Electromagn. Transients Simul. (2nd Ed.)*, pp. 1–527, 2018, doi: 10.1049/PBPO123E.

[62] J. Mahseredjian, V. Dinavahi, and J. A. Martinez, "Simulation tools for electromagnetic transients in power systems: Overview and challenges," *IEEE Trans. Power Deliv.*, vol. 24, no. 3, pp. 1657–1669, 2009, doi: 10.1109/TPWRD.2008.2008480.

[63] U. V. Wali, R. N. Pal, and B. Chatterjee, "On the Modified Nodal Approach to Network Analysis," *Proc. IEEE*, vol. 73, no. 3, pp. 485–487, 1985, doi: 10.1109/PROC.1985.13168.

[64] H. W. Dommel, “Electromagnetic Transients in Single- and Multiphase Networks,” *IEEE Trans. Power Appar. Syst.*, vol. PAS-88, no. 4, pp. 388–399, 1969, doi: 10.1109/TPAS.1969.292459.

[65] F. Zhang and W. Li, “An Equivalent Circuit Method for Modeling and Simulation of Dual Active Bridge Converter Based Marine Distribution System,” *2019 IEEE Electr. Sh. Technol. Symp. ESTS 2019*, pp. 382–387, 2019, doi: 10.1109/ESTS.2019.8847728.

[66] J. K. Debnath, A. M. Gole, and W. K. Fung, “Graphics-processing-unit-based acceleration of electromagnetic transients simulation,” *IEEE Trans. Power Deliv.*, vol. 31, no. 5, pp. 2036–2044, 2016, doi: 10.1109/TPWRD.2015.2492983.

[67] S. Yan, Z. Zhou, and V. Dinavahi, “Large-Scale Nonlinear Device-Level Power,” vol. 33, no. 6, pp. 4660–4678, 2018.

[68] N. Lin, R. Zhu, and V. Dinavahi, “Hierarchical Device-Level Modular Multilevel Converter Modeling for Parallel and Heterogeneous Transient Simulation of HVDC Systems,” *IEEE Open J. Power Electron.*, vol. 1, no. June, pp. 312–321, 2020, doi: 10.1109/OJPEL.2020.3016296.

[69] J. Sun, S. Debnath, M. Saeedifard, and P. R. V. Marthi, “Real-Time Electromagnetic Transient Simulation of Multi-Terminal HVDC-AC Grids Based on GPU,” *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7002–7011, 2021, doi: 10.1109/TIE.2020.3005059.

[70] Z. Zhou and V. Dinavahi, “Fine-Grained Network Decomposition for Massively Parallel Electromagnetic Transient Simulation of Large Power Systems,” *IEEE Power Energy*

Technol. Syst. J., vol. 4, no. 3, pp. 51–64, 2017, doi: 10.1109/jpets.2017.2732360.