Negative-Sequence Current Control of Hybrid Cascaded Three-Level and Multilevel Power Converter for High Voltage Direct Current (HVDC) Transmission

by

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Negative-Sequence Current Control of Hybrid Cascaded Three-Level and Multilevel Power Converter for High Voltage Direct Current (HVDC) Transmission

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Abstract

High voltage direct current transmission (HVDC) is used for massive transmission of electricity over long distances in the form of direct current (DC). HVDC power systems enable utilities to transfer bulk power, to efficiently integrate clean renewable energies, to interconnect grids, and to improve overall network performance with low losses. The latest generation of HVDC systems make use of modular multilevel converter (MMC) topologies to convert high voltage efficiently. Hybrid converter topologies combine the basic two- or three-level converter topologies with MMC topologies to reduce the number of semiconductor switches in the current-conducting path, consequently reducing semiconductor losses. The hybrid converter investigated in this thesis is a hybrid 3-level converter (H3LC) which has been shown to have DC-fault blocking capabilities and remains compact while having less semiconductor losses than the conventional hybrid 2-level converter. The H3LC operates by using director switches (DS) composed of series connected IGBTs to generate 3-level voltage waveforms which are then passed through cascaded full bridge submodules (FBSMs) converting the 3-level voltage waveforms into multilevel sinusoidal voltage waveforms at the point of common coupling (PCC). However, in various industrial power system applications where individual phase voltage magnitude fluctuation and three-phase voltage unbalance at the PCC may occur, the H3LC would cause power quality problems during such events.

The aim of this thesis is to provide a method that will optimize the H3LC operation during the event of a grid voltage imbalance. From the various negative-sequence control techniques proposed in recent research papers, the approach taken in this thesis is to employ the use of an auxiliary controller that that works in tandem with a main controller. The research challenge undertaken is to integrate a sequence analyzer and controller technology that was proven to have

worked for other converter topologies with an emerging hybrid multilevel converter, i.e., H3LC. This thesis presents an unbalanced PCC current regulation control method with positive and negative-sequence component analyzers and an auxiliary controller for the H3LC. A sequence component analyzer is first used to separate the signals measured from the grid at the PCC into its positive and negative sequence components. With the extracted sequence components, the negative sequence current can be found and controlled. The main controller is used to regulate the positive-sequence current at the PCC with respect to the reference current while the proposed auxiliary controller is used to suppress any negative-sequence currents at the PCC. The integration of the developed technology and the H3LC is implemented and, a simulation imitating an unbalanced grid voltage case is performed for proof of concept. This thesis explores the unbalanced current regulation scheme by outlining the underlying principles and simulating case studies for operations under different modes with a detailed equivalent model of the H3LC in a MATLAB® Simulink environment.

Lay summary

HVDC power transmission systems are widely used across the world today. The transmission of power that is made possible through HVDC technology highlights the importance of power converter research. As there is an increase in the number of emerging converter circuit topology designs, the disadvantages and possible converter operation challenges are also being explored in-depth. One such challenge would be voltage magnitude fluctuations and unbalance that cause instability to the power transmission and inability for the converter to maintain voltage and power quality of the AC grid. This thesis presents one solution to this problem by adding to the conventional H3LC control a symmetrical component analyzer that detects any voltage unbalances and an auxiliary controller that suppresses unwanted negative-sequence current components. The fundamental principles will be discussed in greater detail in the thesis. The proposed control scheme will be simulated using MATLAB® Simulink/Simscape Electrical/Specialized Power System Blockset to validate the theoretical operation of the H3LC under unbalanced AC grid voltage conditions.

Preface

All the work in this thesis was completed in the School of Engineering, the University of British Columbia, Okanagan Campus (UBCO). The research was done under the supervision of Dr. Liwei Wang, an associate professor at UBCO. The principal contributor to this thesis is Paul Yoo. Mr. Levi Bieber provided the structure of the unbalanced voltage controller and advised me during the development of the simulation model. Dr. Liwei Wang provided the concept for this thesis and offered support and guidance throughout my research. This thesis contains material that is to be published in the future.

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Abbreviations

AAC	Alternate Arm Converter
DS	Director Switch
FB-MMC	Full-Bridge Modular Multilevel Converter
FBCL	Full-Bridge Chainlink
FBSM	Full-Bridge Submodule
H2LC	Hybrid Two-level Converter
H3LC	Hybrid Three-level Converter
HB-MMC	Half-Bridge Modular Multilevel Converter
HBSM	Half-Bridge Submodule
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line-Commutated Converter
MB-MMC	Mixed-Bridge Modular Multilevel Converter
MMC	Modular Multilevel Converter
PCC	Point of Common Coupling
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
SM	Submodule
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

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I would also like to give special thanks to my family who has supported me throughout this endeavor. My parents have done their utmost to ensure I have a proper education. I also express thanks to my brother who has always encouraged me every step of the way. Their love and understanding were what sustained me this far.

Chapter 1: Introduction

Electricity is essential to modern life and is important to the economics of every nation. This century is predicted to observe an unprecedented growth in electrical power usage and by the same token, challenges in electrical power generation and transmission [1]. The increase in demand for electricity worldwide creates a global race for greener energy generation and more efficient power transmission technologies to be invented. Alternatives to fossil fuels for energy production are desirable as the threat of global fossil fuel source depletion is imminent [2]. As fossil fuels become rarer, the result would be rising prices in everyday living as many applications rely on power generation for usage such as heating, cooling, lighting, computing, transportation, and machinery. Another reason to get rid of global dependence on fossil fuels would be the negative impact it has on the environment when used for power generation [3]. The research efforts in the field of renewable and environmentally friendly power sources have become increasingly important. The research in power electronic converter technologies to integrate renewable sources, such as hydro, photovoltaic and wind generations into the power grid brings forth new challenges, due to their intermittent nature, that are not present when dealing with conventional power generation systems [4]. Connecting a large-scale renewable power source to the AC grid is usually done by a power electronic converter.

The paradigm shift of the research and development of power electronic converters from thyristor-based power semiconductor technology to self-commutating semiconductor devices, e.g., insulated gate bipolar transistor (IGBT) led to the creation of multilevel voltage source converters (VSC). Multilevel VSCs are widely used as they can satisfy demanding applications such as large motor drives, renewable (wind, solar) power generation, and utility systems [5]. Due to their scalability, multilevel VSC topologies are highly sought after for power converters

with high voltage and power ratings. An emerging challenge when using multilevel VSCs would be to deliver power to the AC grid in the case of unbalanced AC grid voltage. Typical power converters cannot operate in optimal fashion when there is a voltage unbalance from asymmetric grid faults or unbalanced loads. Other examples of when voltage unbalance occurs would be for single-phase loads such as traction drives, arc-furnaces, or adjustable speed drives [6].

Under unbalanced grid voltage, power converters will not operate normally as grid voltage will fluctuate and grid currents will exhibit increased total harmonic distortion (THD) [7]. Mitigation of voltage unbalances requires load impedances to be equal among the three-phase system. Active mitigation of voltage unbalances is possible by using a controller of the power converter to compensate for the negative-sequence currents due to unbalanced grid voltage [8].

This thesis will explore a voltage unbalance control scheme that uses a VSC-based hybrid converter to test for negative-sequence current suppression. The H3LC is different from other conventional multilevel converters or modular multilevel converters (MMC). The proposed negative-sequence current suppression controller will be implemented in the H3LC model which is a representative in the family of hybrid cascaded multilevel converters. The proposed controller can be extended to other similar but more complex hybrid multilevel converter topologies derived from the H3LC.

The thesis is partitioned into five major sections as follows:

1. Chapter 1 focuses on the research objective of the thesis as well as background information relevant to its content. After the introduction, the HBSM and FBSM are discussed as they are referenced throughout this thesis. A literature review was done on a brief history of HVDC

systems, conventional power converter topologies and control methods to mitigate negative effects, caused by unbalanced grid voltage.

2. Chapter 2 describes the H3LC in greater detail. Its topology, operating principles and existing control model are discussed in this section. The capacitor energy balancing, DC-pole capacitor voltage balancing, and the switching-based detailed equivalent model of the converter are all addressed.

3. In Chapter 3, the auxiliary negative-sequence current suppression controller for the H3LC is proposed. The purpose of the proposed controller as well as its function is described in Chapter 3. The mathematical derivations for the symmetrical component extraction and individual positive and negative-sequence controllers are designed and developed.

4. For Chapter 4, the MATLAB/Simulink based simulation results are used to verify that the auxiliary negative-sequence suppression controller is working as intended. The H3LC operations undergo a series of simulation tests to demonstrate how it responds to normal grid voltage condition, unbalanced grid voltage without the proposed auxiliary negative-sequence current suppression controller, and finally, unbalanced grid voltage with the proposed negative-sequence auxiliary controller.

5. Chapter 5 states the results of the research and includes summaries and reflections on the work done. The key points from each section of the thesis are reiterated and a recommendation for possible future directions for this field of study is given.

1.1 Background

This section will provide background information that helps in understanding the terms and principles described in Chapters 2 and 3. The background context includes an explanation of half-bridge and full-bridge submodules that are referenced heavily in later chapters, and a brief explanation of symmetrical components.

1.1.1 Half-Bridge and Full-Bridge Submodules

For high voltage direct current (HVDC) applications, MMCs are the most widely used high power converter technology as they provide less losses for the same power and voltage ratings used than the conventional two- or three-level converters. The MMCs can operate with hundreds of small voltage levels without propagating complexity in semiconductor connections. A typical three-phase MMC consists of six arms each comprised of a series of submodules (SM) [9]. A SM is comprised of a capacitor and semiconductor switches. The two most common SMs are the half-bridge submodule (HBSM) and full-bridge submodule (FBSM) configurations [10].

The HBSM consists of two IGBTs and a capacitor as seen in Figure 1.1. The switching states, current polarities, output voltages and capacitor charging states are shown in Table 1.1

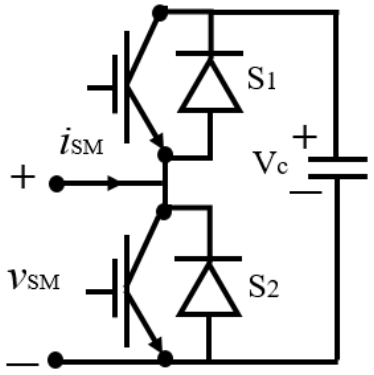

Figure 1.1 Half-bridge submodule

Table 1.1 Half-bridge submodule states

States	S_1	S_2	i_{SM}	v_{SM}	Δv_{Cap}
Inserted state					
Mode 1	1	0	+	Vc	+
Mode 2	1	0	-	Vc	-
Bypassed state					
Mode 3	0	1	+	0	0
Mode 4	0	1	-	0	0
Blocked state					
Mode 5	0	0	+	Vc	+
Mode 6	0	0	-	0	0

The FBSM has two additional semiconductor switches compared to the HBSM topology, as shown in Figure 1.2. The FBSM is capable of generating bidirectional voltage. The switching states, current polarities, output voltages and capacitor charging states are shown in Table 1.2.

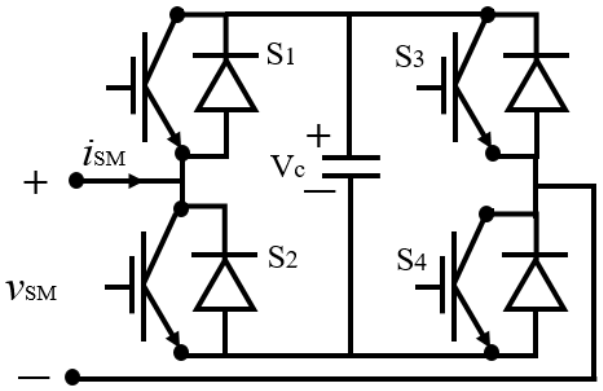

Figure 1.2 Full-bridge submodule

Table 1.1 Full-bridge submodule states

States	S_1	S_2	S_3	S_4	i_{SM}	v_{SM}	Δv_{Cap}
Positively inserted state							
Mode 1	1	0	0	1	+	Vc	+
Mode 2	1	0	0	1	-	Vc	-
Negatively inserted state							
Mode 3	0	1	1	0	+	-Vc	-
Mode 4	0	1	1	0	-	-Vc	+
Bypassed state							
Mode 5	0	1	0	1	+	0	0
Mode 6	0	1	0	1	-	0	0
Mode 7	1	0	1	0	+	0	0
Mode 8	1	0	1	0	-	0	0
Blocked state							
Mode 9	0	0	0	0	+	Vc	+
Mode 10	0	0	0	0	-	-Vc	+

1.1.2 Symmetrical Components

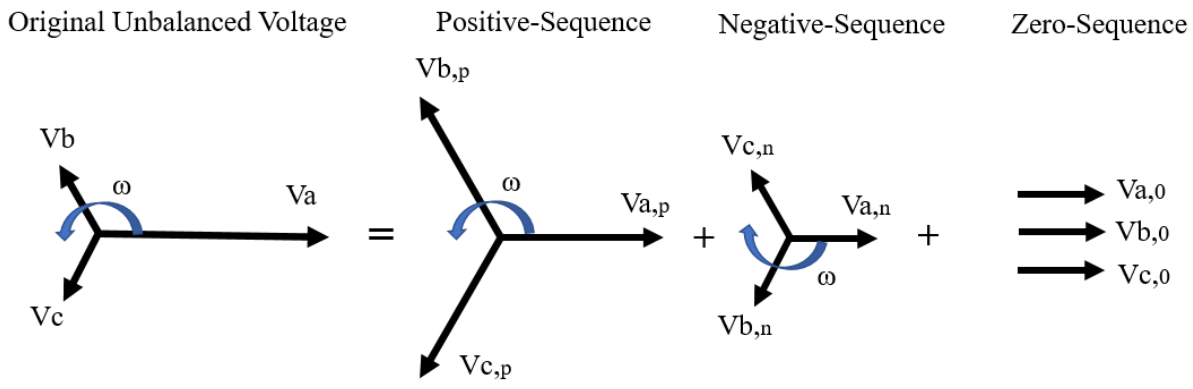

Figure 1.3 Symmetrical Component Systems

In a three-phase system, to be considered balanced, each phase must be equal in magnitude and phase shifted by 120°. The phase currents and voltages can be represented by phasors as symmetrical components. The theory of symmetrical components allows detection of any three-phase unbalance in a power system. In symmetrical component theory, there are three components to consider: the positive-sequence, negative-sequence, and zero-sequence [42]. In a three-phase balanced system where the magnitudes are equal and the phases are 120° apart, only positive-sequence components will exist. In contrast, any other situation will mean that there is negative-sequence, and zero-sequence components present in the system. In Figure 1.3, an example of a voltage unbalance is shown. By convention, positive-sequence phasors rotate counterclockwise. In the original system, Phase-A voltage has its magnitude greater than those of Phases-B and C. The positive-sequence voltage is generated by the system voltage and has the sequence a-b-c. The negative-sequence shows smaller phasors with the sequence a-c-b according to the conventional phasor rotation with counterclockwise rotation. The zero-sequence section shows three vectors with equal magnitudes and the same phase angle.

1.2 Literature Review

This section will give a brief overview on the history of HVDC systems, background knowledge of power converters, and the ongoing challenge present in the current industry that is being undertaken by the proposed research work.

1.2.1 A Brief History on HVDC Systems

Despite the advantages of using AC in the field of power transmission that overshadowed DC in its inception, the possible benefits from using DC prevented the time-tested DC technology from becoming obsolete. To experience the advantages from both AC and DC power, a method to introduce a DC link to AC systems, the HVDC system, was invented by a Swedish engineer

named Uno Lamm who rectified AC and inverted DC power for a 100-kV, 20-MW cable system in 1954 [11]. HVDC systems have advantages over using only AC such as reduction in transmission losses and negligible skin effect, improvement in system stability, enabling AC voltage and reactive power regulation, and connecting asynchronous AC grids. There exist downsides to using conventional line-commutated-converter HVDC systems such as greater harmonics in converters, greater reactive power requirements, and converter susceptibility to overload. The applications where HVDC is most effective is listed in [12] as:

- power transmission over long distances
- asynchronous operation for AC systems with differing operating frequencies
- power transmission through power cables crossing bodies of water

A power electronic converter is an essential component of a HVDC system and is directly related to the amount of power transmissible by the system. The early-years commercial HVDC converters were constructed using mercury-arc valves by Uno Lamm [11]. Due to advances in technology, once semiconductor devices were invented in the 1950's, the advent of the thyristor-based converter came in the 1970s where most mercury-arc valves used in HVDC applications were replaced by solid-state technology [13]. Thus far, the mercury-arc valve and thyristor-based converter were considered to be current controlled devices, that is, requiring external circuit operation to block current conduction or in layman terms to 'turn-off' the switches. These types of converters which utilized thyristor switches are referred to as line-commutated converter (LCC). The LCC was the dominant technology until further development into semiconductor research resulted in the invention of the Insulated-Gate Bipolar Transistor (IGBT). The IGBT is a three-terminal power semiconductor switch that offers unprecedented energy efficiency [14]. The IGBT is a self-commutating device meaning it is fully controllable and can be turned on or

off by applying gate voltage. Due to the invention of the IGBT, voltage-sourced converter (VSC) became commonplace for HVDC applications. Advantages that the VSC over the LCC include full control over reactive power of an AC system at both ends while maintaining continuous balance of real power flow between these two ends. The LCC also requires a strong grid to commutate the thyristors and relies on a synchronous voltage source. Furthermore, the self-commutating nature of the VSC-HVDC system means that it can provide power to passive AC networks such as a load on an island [15].

1.2.2 Two-level Voltage Sourced Converter

The two-level VSC is a generic power converter topology and is considered to be the foundation of VSC HVDC technology. The first VSC HVDC technology coined “HVDC Light” by ABB emerged in the 1990s and made use of IGBT devices to convert AC to DC and vice-versa [16]. The two-level VSC operates at high frequencies in the range of 1-2kHz using pulse width modulation (PWM). The fast switching allows for rapid active and reactive power control. As a result, the two-level VSC does not require separate auxiliary components such as low-order passive filters and reactive power compensation devices. Due to this advantage, the two-level VSC was physically compact and novel for its time. The two-level VSC is used for low voltage applications and is rated for power in the hundreds of Megawatt range [17]. The graphical representation of a three-phase two-level VSC is shown in Figure 1.4.

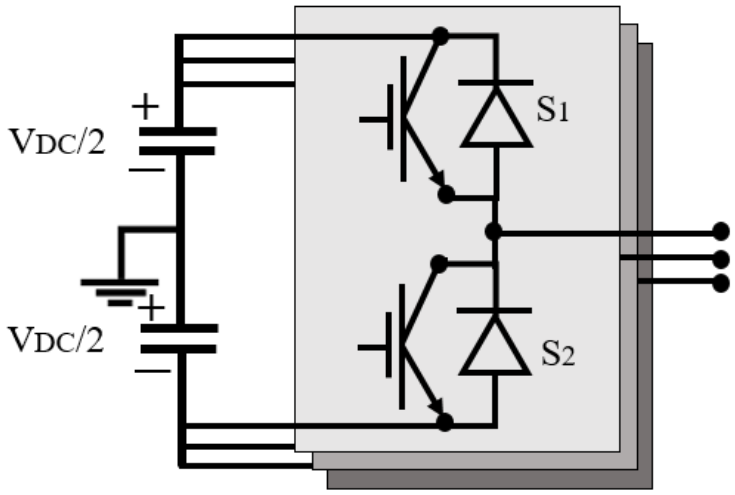

Figure 1.4 Three-phase two-level VSC

As seen in Figure 1.4, the two-level VSC has three phase legs, each grey shade of rectangle representing a phase. Each phase leg has two switches connected in series that are switched on/off to control the output voltage. The output branch or AC terminal is connected to the midpoint of a phase leg. In Figure 1.4, the switch is shown to be a combination of an IGBT and an antiparallel diode. This combination of semiconductor devices allows bidirectional power/current flow and positive DC voltage blocking. A typical method of switch modulation would be to use sinusoidal pulse width modulation (SPWM) [18]. With SPWM, there are two waveforms of note: the carrier waveform (triangle wave) and reference waveform (sine wave). The amplitude of the two waveforms is compared; if the reference waveform is greater than the carrier waveform then S1, the upper switch in Figure 1.4, is turned on while S2 is off. In this state, the output voltage is $+V_{DC}/2$. Inversely, when the reference waveform is found to be less than the carrier waveform, S1 is off while S2 is on. The output in this state would be $-V_{DC}/2$. This method of switching modulation ensures that the switches are complimentary and there are

two voltage levels observed at the AC side terminal. The output of the two-level VSC can be summarized in an equation relating the modulation signal (m_j) and the capacitor voltage as follows:

$$V_{out,j} = m_j \cdot \frac{\mathrm{V_{DC}}}{2} \ , j \in \{a, b, c\} \tag{1}$$

1.2.3 Modular Multilevel Converters

The mentioned two-level VSC in the previous section are widely used for low voltage applications. A downside to the aforementioned converters would be the need for a large amount of semiconductor switches in series and increasingly complex connections and control for higher voltage requirements in HVDC transmission. However, in 2002, a VSC topology suited for medium to high voltage applications, named modular multilevel converter (MMC), was invented by Lesnicar and Marquardt [19]. The MMC has salient features over the two-level VSC and other existing multilevel topologies, in that, the MMC is modular and scalable to any voltage level, highly efficient, eliminates the need for DC side capacitors due to the SM capacitors, and has better harmonic quality which allows a reduction in the size of passive filters [20]. The basic building block in any MMC is the converter cell or otherwise labeled in this thesis as a SM. The use of SMs allow the MMC to be scalable to any voltage level required by simply linearly increasing the number of SMs added to each converter arm. The two different types of SMs typically used in MMCs are the HB and FB SMs both of which are mentioned in Section 1.1. A MMC consists of an upper and lower arm both rated for the converter DC side voltage, $\mathrm{V_{DC}}$. Each arm consists of series connected SMs referred to as a chainlink as well as an inductor to suppress low order circulating current components. Among all the MMC topologies, the half-bridge MMC (HB-MMC), which uses HBSM is well known for its simplicity and low cost. The

disadvantage to the HB-MMC would be its vulnerability to DC side short-circuit fault. In the case of a DC side fault, the short-circuit current that occurs can bypass the HBSM through its diode path [21]. Due to the MMC's modular nature, the HBSMs in each arm can be substituted by the FBSMs. The described full-bridge MMC (FB-MMC) has the ability to block DC fault currents as the short-circuit current in the FBSMs when all the switches are turned off flows through the SM capacitors which provide reverse blocking voltage [22]. The downsides to conventional MMC topologies such as the HB-MMC and FB-MMC would be the semiconductor losses that are incurred from employing a large number of IGBTs [44]. In the case of the FB-MMC, the DC side fault blocking advantage over the HB-MMC is shadowed by the fact that twice the number of IGBTs need to be used per SM which leads increased conduction losses. Other MMC topologies use hybrid configurations with a mix of FBSM and HBSM or altered SMs aimed to improve converter efficiency. Some examples of these MMCs include the mixed bridge MMC (MB-MMC) which uses both FBSMs and HBSMs in a converter arm to reduce semiconductor losses while providing DC-fault handling capabilities; the clamp-double submodule MMC (CDSM-MMC) which uses a diode in the SM to add a conduction path to block DC fault current; and the series-connected double SM MMC (SDSM-MMC) which is designed to block fault currents while allowing the SMs to stay connected [23-25, 43].

1.2.4 Hybrid Converters

Due to the inability of the HB-MMC to cope with DC side faults and the FB-MMC's high conduction loss and cost of large quantities of semiconductor switches, extensive research is being done to create hybrid MMCs that effectively integrate the best qualities of the conventional converters. Some effective hybrid topologies that minimize losses and have reduced footprints

include the alternate arm converter (AAC), the hybrid 2-level converter (H2LC), and the hybrid 3-level converter (H3LC).

The AAC is a well-known alternative to the HB-MMC due to it being one of the first modular converter with DC side fault ride through capabilities without costing large amounts of power loss [26]. The AAC is a hybrid topology that is inspired by the conventional two-level VSC and the MMC. The basic layout of the AAC is to have series connected IGBTs called director switches (DS) in series with FBSMs in each converter arm. The operating principle of the AAC is to alternate the conduction of the upper and lower arms using the DSs to create a rectified AC current (DC current) while a small number of FBSMs are used as filters which improve the quality of the output waveforms while also maintaining DC side fault ride through capabilities. The AAC has six arms like the MMC but less costs because the voltage rating of the semiconductor devices does not have to be account for the full DC side voltage source due to the DSs [27]. The AAC is not a perfect design however, as the alternating conduction of the upper and lower arms produce large ripples in the output waveform and the control for the DSs as well as energy balancing of SM capacitors becomes a challenge at high frequencies [26][28].

In [29] the H2LC is introduced, which is a multilevel VSC-HVDC system that is based on a hybrid two-level converter design with cascaded FBSMs connected at the AC side or otherwise known as a full-bridge chainlink (FBCL). This two-level converter has many advantages over the conventional MMCs such as having inherent DC-fault reverse blocking from the FBCL. The DSs has low switching losses as the fundamental frequency voltage is controlled using selective harmonic elimination (SHE) with a switching frequency at three times the fundamental frequency. The FBCL also acts as an active power filter that smooths out the AC side output

waveforms and only requires a maximum sum of $V_{DC}/2$ voltage rating, reducing the number of SMs required to a quarter of what is needed in the MMC [29].

The H3LC, which was introduced in [30] is a new hybrid topology that was derived from the H2LC. The H3LC consists of three T-type converters with a FBCL on the AC side and a protection branch that allows the converter to block DC-fault current. The H3LC is demonstrated to have better efficiency than the H2LC and FBSM-based MMCs, due to its use of fundamental frequency switching of the DS and the third-order harmonic voltage injection which limits the voltage rating of the AC side FBCL to a sum of $V_{DC}/4$. The protection branch is required due to the low voltage rating of the FBCL which may not be sufficient to provide sufficient reverse blocking voltage to the DC side fault. Due to its novelty, modularity, and scalability, the H3LC was chosen as the topology of focus for this thesis. Due to the addition of an auxiliary controller, modifications were made to the H3LC proposed in [30]. More detail on the operating principle, control and modifications will be presented in the later chapters.

1.2.5 Unbalanced Grid Voltage

In the past decade or so, the number of power electronic devices that operate for long cycles with high power consumption/generation have become increasingly popular in demand. Due to higher reliance of modern society on devices such as electric cars, PV systems, battery storage and heat pumps, there is growing attention on how the devices may affect power transmission networks [31]. Voltage imbalance is a case that affects networks of all voltage levels. Voltage imbalance occurs due to an asymmetrical connection of loads. Some loads that may cause voltage imbalance are the rectifier or arc furnace as they are commonly known to be nonlinear and results in voltage and current distortions, voltage fluctuations and flicker [32]. In some new

HVDC systems, control methods to mitigate or inject negative-sequence current during imbalanced faults are a part of new grid code requirements [33].

In the case of an asymmetric fault, the positive-sequence voltage decreases while the negative-sequence voltage increases. A few problems arise when the voltage imbalance occurs such as disturbed power quality and increased DC-pole capacitor voltage ripple [34]. As is with the H3LC, the system described in [35] is current controlled through current reference signals that are determined from active and reactive power controllers based on the grid side voltage and current measurements. The sudden emergence of negative-sequence current causes the reference current to be time variant, which makes the measured current unable to follow the reference values. Also, as a result, the converter will have second-order harmonics at the DC side due to modulating positive and negative-sequence components causing voltage ripples in the DC capacitor [35].

In order to resolve the issue of unbalanced grid voltages, there are a couple of methods one can employ. One method is to use an external device with its own battery storage to detect when the amplitude of the negative-sequence voltage is above a certain set limit and to inject voltage to the grid [36]. This method is only cost effective and viable for low voltage applications. Most research papers start the process by decoupling the measured grid voltage and current waveforms into its positive and negative-sequence components [37]. This can be done using various methods one of which is to apply a delay to a signal in the $\alpha\beta 0$-frame. More detail on the extraction process will be explained in a later section. After the separation into the positive and negative components, the negative-sequence current is generated as a function of the negative-sequence voltage and is controlled using PI controllers [38]. It is important to note that full nullification of negative-sequence components is not possible as the reference negative-sequence

voltage value would become zero thus making the derived reference current signals undetermined, ultimately leaving the injected currents unsynchronized [39].

1.3 Research Objectives

The research objective of the work done in this thesis is to study the fundamentals of HVDC systems, modular and scalable converter topologies and to challenge an issue that is prevalent in the industry today. When the grid voltage is unbalanced, the H3LC does not operate in optimal condition due to the presence of negative-sequence current. The main goal would be to integrate a negative-sequence current suppression control method with the H3LC and verify its viability using simulation software. The literature review will provide context for the research done and show some alternative perspective to the work done in this thesis. The presentation of the H3LC topology, operating principle and modeling will facilitate future improvements in designs with more complex topologies. The simulations provide verification of a working negative-sequence current suppression controller that mitigates voltage unbalance issues.

1.4 Thesis Contributions

This thesis proposes a negative-sequence current suppression control method for the H3LC, a relatively new multilevel VSC circuit topology. The negative-sequence current suppression control method is designed for various HVDC applications which demonstrate its desirable control performance over the conventional positive-sequence-based converter control method. The contributions of the thesis are listed in greater detail as follows:

1. A symmetrical component decoupling method is introduced for the unbalanced grid operation conditions of the H3LC HVDC system. The symmetrical component decoupling method is shown to be able to decompose the unbalance voltage and current signals into symmetrical

negative, positive and zero-sequence signals during steady-state and transient operating conditions for the H3LC control hierarchy.

2. An auxiliary negative-sequence current suppression controller is integrated with the H3LC for operation in unbalanced grid voltage conditions. The negative-sequence controller for the H3LC is based on a *dq* converter reference frame which enables the use of a PI controller for the proposed negative-sequence controller.

3. The proposed negative-sequence current controller is implemented in the detailed switching based H3LC model in MATLAB/Simulink/Simscape Electrical/Specialized Power System Toolbox. The simulation results demonstrate the proposed negative-sequence current suppression controller can co-operate with the existing PI control loops of the H3LC to regulate positive-sequence real and reactive powers and suppress the negative-sequence current in unbalanced grid voltage conditions.

Chapter 2: H3LC Topology

This chapter presents the converter topology for the hybrid three-level converter (H3LC) used to test the proposed control scheme. The H3LC was chosen for this project because it is a modern hybrid type converter and is promising for the applications of the next generation medium to high voltage DC systems. It is noted that the H3LC can be extended for more complicated hybrid converter topologies. The proposed negative-sequence current suppression controller should, theoretically, be viable, when applied to similar hybrid converter topologies. The following sections will explain the operating principles of the H3LC, and any modifications made to account for the auxiliary controller.

2.1 H3LC Topology

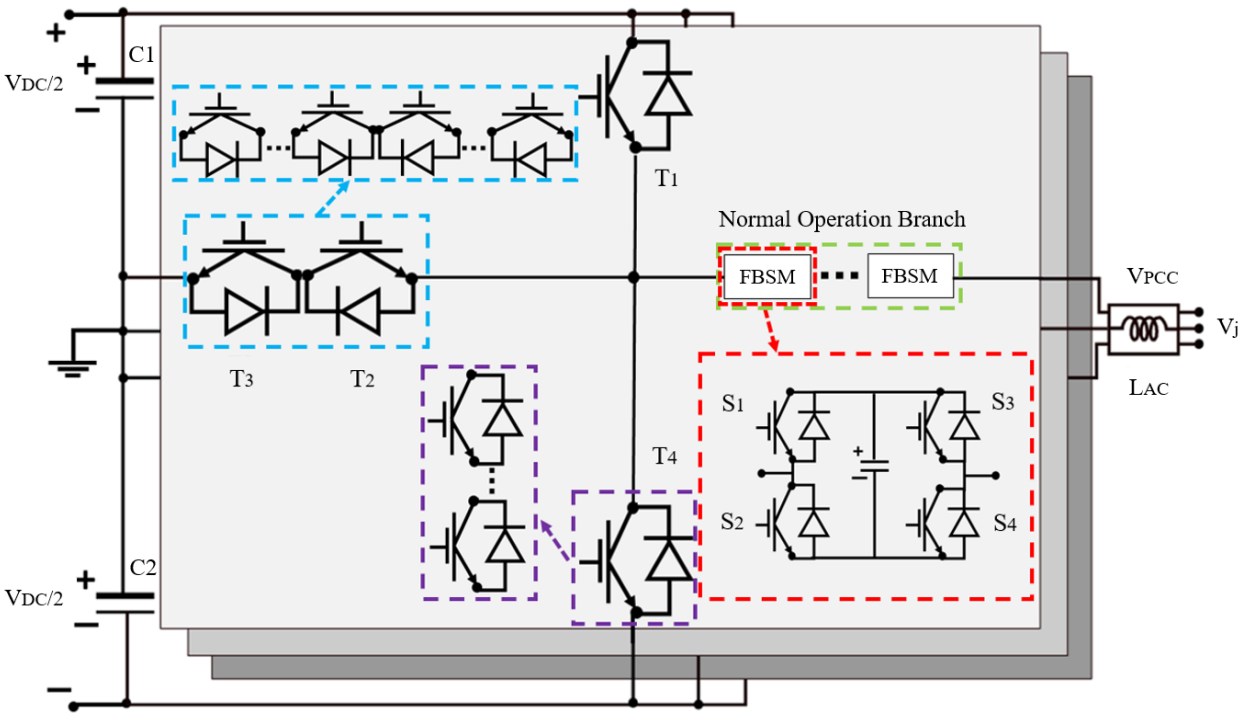

Figure 2.1 Power circuit schematic of H3LC

The circuit topology of the H3LC is shown in Figure 2.1. The H3LC performs AC/DC power conversion. The main part of the converter displays four IGBTs T_1 through T_4 which indicate the positions of the series-connected director switches (DS). The two DC pole capacitors are labeled, C1 and C2. The AC chainlink branch in Figure 2.1 consists of a series of cascaded full-bridge submodules (FBSM). This AC side branch of FBSMs act as active harmonic filters to shape the waveforms of the three-phase, three-level square wave voltages into smooth three-phase sinusoidal waveforms. The output at the AC terminals is labeled in Figure 2.1 as Vj with j representing AC phase terminals: a, b and c. It is noted that the H3LC investigated in the thesis assumes the AC side chainlink FBSMs in each phase has the blocking voltage rating of $V_{DC}/2$ and ignores the AC side protection branch to simplify the converter analysis. The AC side protection branch and its DC side fault blocking operation can be used in the proposed modified H3LC, similarly to [30].

2.2 Operating principle

Table 2.1 shows the switching states for the H3LC. The director switches T_1 through T_4 output fundamental frequency square waves with three AC voltage levels, $V_{DC}/2$, 0 and $-V_{DC}/2$. The fundamental frequency voltage is regulated through the pulse width of the square wave. This implies that the switching of the DSs is done at fundamental frequency. The DSs, T_1 and T_4, are the upper and lower leg series-connected switches, respectively. Due to their location, they are rated for voltages of up to V_{DC}. The DSs, T_2 and T_3, are anti-series connected and are located in the midpoint of the 3-level converter, thus both have a voltage rating of $V_{DC}/2$.

The chainlink FBSMs in the normal operation branch smooths the square wave voltages into sinusoidal waveforms with peak amplitudes $\pm V_{DC}/2$. This means that the sum of N number of

FBSM voltages must be limited to $\pm V_{DC}/2$. Each chainlink FBSM has a DC-link voltage of $\pm V_{DC}/2N$.

Table 2.1 Voltage rating of H3LC components

Director Switches					**Full-Bridge Submodules**				
Output Voltage	T1	T2	T3	T4	Output Voltage	S1	S2	S3	S4
$\frac{V_{DC}}{2}$	1	1	0	0	$\frac{V_{DC}}{2N}$	1	0	0	1
0	0	1	1	0	0	1 0	0 1	1 0	0 1
$-\frac{V_{DC}}{2}$	0	0	1	1	$-\frac{V_{DC}}{2N}$	0	1	1	0
Voltage rating	V_{DC}	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$	V_{DC}	Voltage rating	$\frac{V_{DC}}{2N}$	$\frac{V_{DC}}{2N}$	$\frac{V_{DC}}{2N}$	$\frac{V_{DC}}{2N}$

2.2.1 Fundamental Voltage Component

The H3LC outputs a three-phase square wave with three voltage levels, $V_{DC}/2$, 0 and $-V_{DC}/2$. The switching angle α, is used to regulate the fundamental frequency sinusoidal waveform shown in Figure 2.2(a). The fundamental frequency voltage waveform is calculated using (1)

$$V_{1H,j} = \frac{2}{\pi}\cos(\alpha_j) * V_{DC} \tag{1}$$

Equation (1) can be rearranged to find the switching angle α, as is shown below:

$$\alpha_j = \cos^{-1}\left(\frac{\pi}{2} * \frac{V_{1H,j}}{V_{DC}}\right) \tag{2}$$

When the switching angle α = 0, the modulation index of the H3LC is $\hat{m}_{1H} = \frac{V_{1H}}{\frac{V_{DC}}{2}} = \frac{4}{\pi}$.

The chainlink voltage can be calculated using the equation (3) where θ is the converter angle. The chainlink voltage is equal to the three-level square wave minus the fundamental frequency waveform as:

$$v_{\mathrm{CL}}(\theta) = v_{\mathrm{3LC}}(\theta) - \mathrm{V_{1H}}\sin(\theta) \tag{3}$$

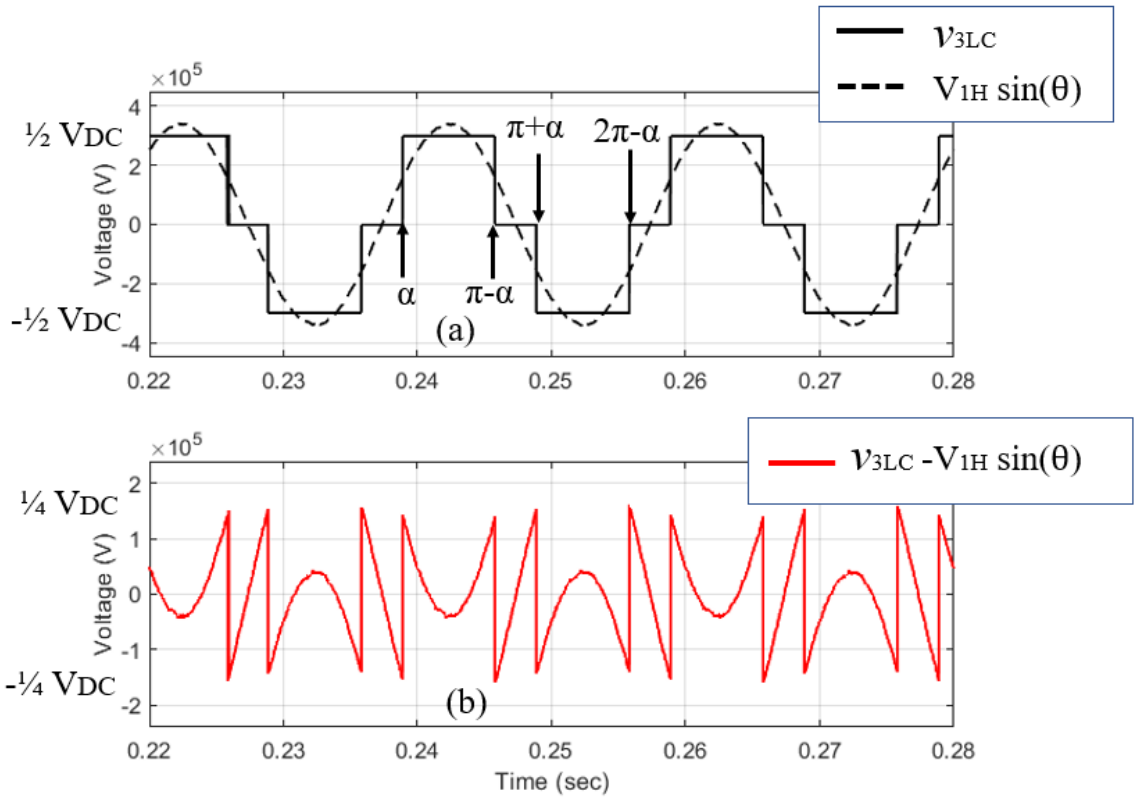

Figure 2.2 (a) Three-level converter voltage with corresponding fundamental frequency voltage. (b) Chainlink voltage

In the prior-art works of the H2LC [29] and the H3LC [30], the third order harmonic voltage injection technique is used to reduce the voltage ratings of the AC side chainlink FBSMs to $V_{DC}/2$ and $V_{DC}/4$, respectively for the H2LC and H3LC. The use of the third order harmonic voltage injection has the implicit assumption that the converter output fundamental frequency

voltage is symmetrical or balanced, leading to balanced three-phase third order harmonic voltage injection to the AC side FBSM chainlink. The balanced three-phase third order harmonic voltage is canceled at the Delta side transformer, which is connected to the AC power grid. Therefore, the use of the third order harmonic voltage injection technique for the H2LC and the H3LC is only viable for symmetrical 3-phase AC grid voltage.

Unlike the H2LC and H3LC proposed in [29] and [30], the proposed negative-sequence current suppression control requires negative-sequence voltage regulation which exclude the use of the third order harmonic voltage injection in the AC side FBSM chainlinks. The absence of the third order harmonic injection means that the chainlink voltage of H3LC is not bound within $\pm V_{DC}/4$ but $\pm V_{DC}/2$. This means that in order to compensate the negative-sequence current, the voltage rating of the FBSMs must be at greater than $\pm V_{DC}/4$, i.e., $\pm V_{DC}/2$. The increased FBSM chainlink rating of the H3LC from $V_{DC}/4$ to $V_{DC}/2$ indicate the higher semiconductor conduction losses which is the trade-off of the negative-sequence current suppression control. In order to avoid the extra semiconductor conduction losses of the AC side FBSM chainlink, the addition of the extra FBSM chainlink with the $V_{DC}/4$ voltage rating can be realized in the protection branch, as proposed in [30]. The FBSM chainlink in the protection branch is bypassed through the use of a fast mechanical switch in the normal operation of the H3LC and is inserted into the converter AC side main circuit during DC side fault [30] or negative-sequence current suppression control operations.

2.2.2 Chainlink Capacitor Energy Balancing and FBSM Capacitor Voltage Balancing

In the AC side FBCL, the FBSMs act as active harmonic filters to smooth out the output three-phase square wave voltage from the H3LC. This results in the total energy of the capacitors of the FBSMs being constant with zero deviation over the fundamental cycle. However, there are

losses to be accounted for due to imperfect semiconductor switches with conduction and switching losses. The consequence of a lossy chainlink is energy drifting observed in each individual SM making each capacitor have slightly differing voltages. This may lead to an undesirable situation such as the total average capacitor voltage of the FBSMs experiencing drift. To counteract the possible total FBSM capacitor energy drift, a PI controller is used, as seen in Figure 2.3, to modulate positive fundamental frequency voltage into the FBCLs as necessary to balance the total energy of the FBSM capacitors. It is noted that the injected fundamental frequency voltage, Δv_{abc}, is small and is a negligible demand for the converter system.

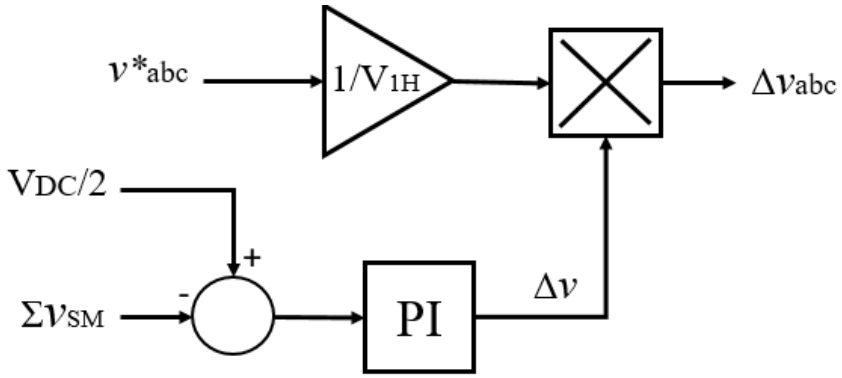

Figure 2.3 Chainlink energy balancing loop (adapted from [30])

To reduce the FBSM capacitor voltage ripple, Level-Shifted PWM (LSPWM) or Nearest Level Modulation (NLM) can be used to generate a switching function N_{ins} for the chainlink FBSM. Similar to the conventional MMC or H2LC, a voltage sorting algorithm can be used to generate switching signals for every IGBT. With N_{ins} and AC phase current direction, the FBSM capacitors are selected based on highest or lowest voltage and inserted into the chainlink. In this thesis, the voltage sorting algorithm is tightly balanced, reducing FBSM capacitor voltage ripple for better proof of concept.

2.2.3 DC-Pole Capacitor Balancing

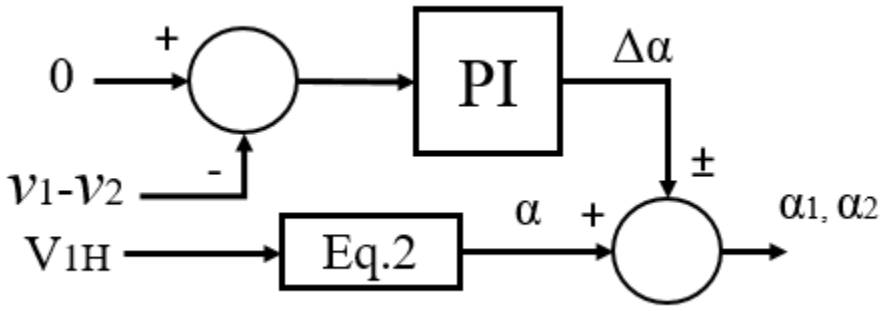

Figure 2.4 DC-pole capacitor control loop (adapted from [30])

Typically for a VSC, the DC side voltage is maintained constant using a capacitor since it functions as an energy storage device. For the H3LC, two capacitors are used for DC link voltage as they allow the converter to operate in three voltage levels. These two capacitors are connected in series with a ground connected in-between the pole capacitors, also known as the midpoint (neutral point) of the DC side. Due to the slight varying charging and discharging states that may differ between the two DC pole capacitors, a DC-pole balancing controller needs to be employed to prevent the DC pole capacitor voltage drifting from the rated half of the DC pole-to-pole voltage ($V_{DC}/2$). The DC-pole capacitor balancing loop shown in Figure 2.4 injects small currents into the upper and lower pole capacitors to compensate for voltage differences $v_1 - v_2$. This method of modulation appears similar to that of the fundamental voltage injection loop. However, in this loop the calculation of two switching angles, α_1, α_2 are required for modulating the upper and lower legs DSs separately. As seen in Figure 2.5, when $\theta = \{\alpha_1, \pi-\alpha_1\}$, $v_{3LC}(\theta) \approx V_{DC}/2$ and when $\theta = \{\alpha_2, \pi-\alpha_2\}$, $v_{3LC}(\theta) \approx -V_{DC}/2$. Any difference in voltage of the DC-pole capacitors is mitigated by $\Delta\alpha = \alpha_1 - \alpha_2$ from the output of a PI controller. As $\alpha_1 = \alpha+\Delta\alpha$ and $\alpha_2 =$

α−Δα, any voltage differences will be eliminated by injecting a positive or negative DC voltage component.

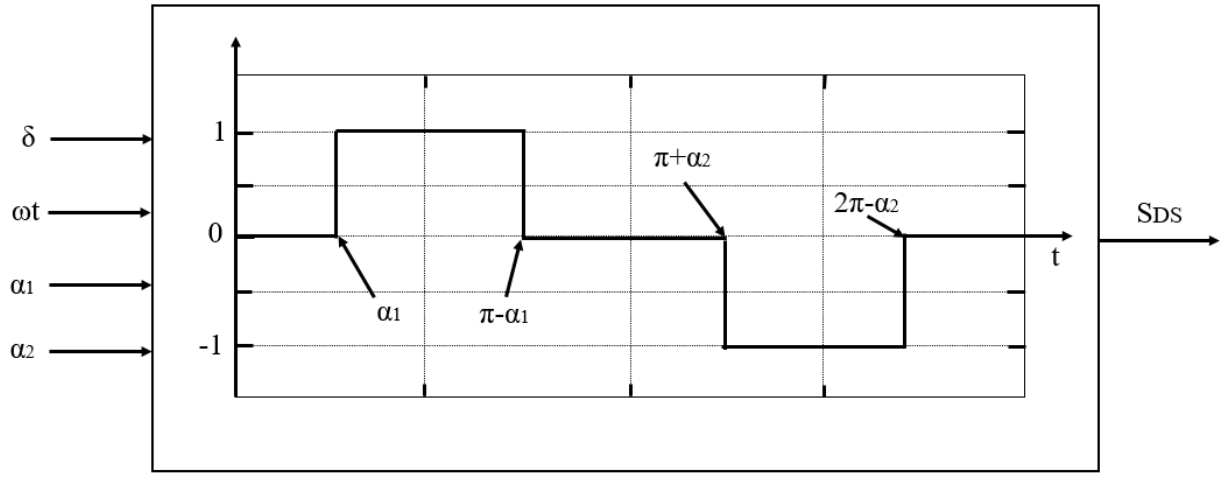

Figure 2.5 DS switching generation block (adapted from [30])

Chapter 3: H3LC Control Design and Modeling

This chapter discusses how the negative-sequence current suppression controller of the H3LC operates, the theory behind its design and the modeling performed using MATLAB/Simulink /Simscape/Specialized Power System Toolbox. The fundamental operating principle and lower-level controls of the H3LC were reviewed in Chapter 2. In this chapter, the current mode control of a VSC is reviewed first. Then, the negative-sequence current suppression control design is presented for the H3LC system operating under unbalanced network conditions. The chapter is separated into three parts: a description of the proposed control method, the switching signal generation for the modified H3LC, and the detailed-switching-based simulation model to verify the proposed converter control method.

3.1 Current-Mode Power Control

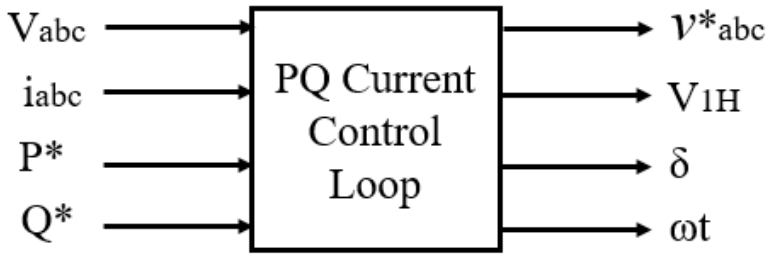

Figure 3.1 H3LC real and reactive power control scheme (adapted from [30])

For the H3LC, the basic upper-level current control system is similar to the conventional VSC HVDC controllers [53]. The control system consists of an outer P, Q control and inner-loop *dq*-frame current control. In more detail, the control system creates reference fundamental frequency waveforms combined with other reference waveforms that generate all the switching signals for the DS and FBSM chainlinks. This is done by transforming the measured voltage and current at

the AC terminal to *dq* converter synchronous reference frame. The transformed values calculated to instantaneous real and reactive power, P* and Q*, respectively, and are then compared to the set real and reactive power reference values. Resulting error signals are input into PI controllers which minimize the variation between the reference value and measured value with a small tolerance.

The proposed current control system is analyzed in the positive and negative synchronous reference frames. The control system is split into a main controller and an auxiliary controller as seen in Figure 3.2. The main controller works within the positive *dq*-frame while the auxiliary controller works within the negative *dq*-frame.

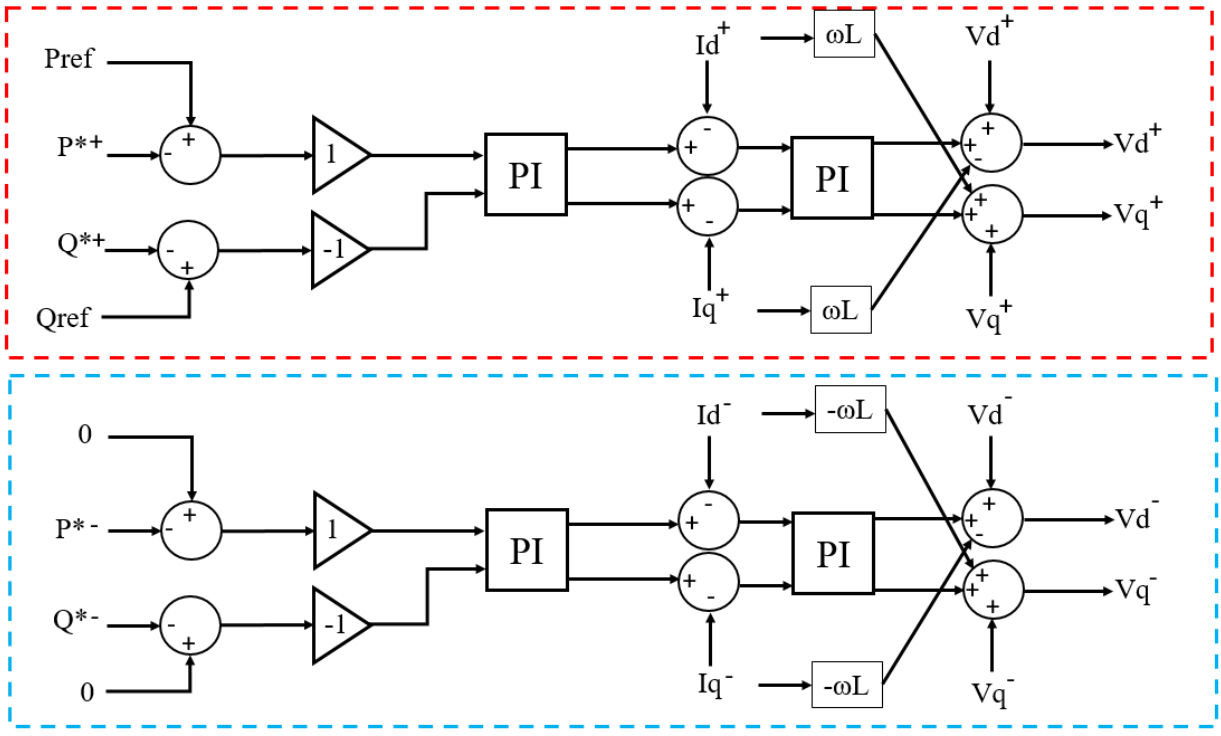

Figure 3.2 Main controller (red) and auxiliary controller (blue)

As PQ control is formulated in the *dq*-frame, a phase-locked loop (PLL) is required to synchronize the three-phase sinusoidal signals. The angular position of the rotating frame is found using the PLL, thus a different ω needs to be used for positive-sequence and negative-sequence components. As mentioned in Section 1.1.2, the positive-sequence currents and voltages are rotating in the counterclockwise direction, following convention while the negative-sequence rotates in the opposite direction. Therefore, the PLLs for positive-sequence and negative-sequence output ωt and –ωt, respectively.

To generate the input for the auxiliary controller, the original grid signals need to be decomposed into positive and negative-sequence components. The extraction of the positive and negative-sequence components is done by first transforming from the *abc*-frame to the *αβ*-frame using Clarke transformation (4).

$$f_{\alpha\beta\gamma}(t) = T f_{abc}(t) = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{4}$$

Assuming there is no zero-sequence voltage component, as there is no simple method to control zero-sequence current due to the absence of a neutral wire and the placement of the decoupling transformer [7], the three-phase voltage and current may be decomposed into its positive and negative components as seen in (5).

$$f_{\alpha\beta}(t) = f_{\alpha\beta+}(t) + f_{\alpha\beta-}(t) \tag{5}$$

To obtain the separate sequence components, the original grid signals are split into two parts, the original $\alpha\beta$ signal and the said signal delayed by a quarter of the fundamental frequency period [40].

$$f_{\alpha\beta+}(t) = \frac{\left[f_{\alpha\beta}(t) + j * f_{\alpha\beta}\left(t - \frac{T}{4}\right)\right]}{2} \tag{6}$$

$$f_{\alpha\beta-}(t) = \frac{\left[f_{\alpha\beta}(t) - j * f_{\alpha\beta}\left(t - \frac{T}{4}\right)\right]}{2}$$

The subsequent step would be to take each sequence signal found using (6) and apply the inverse Clarke transformation (7) to obtain the positive and negative-sequence voltage and current in the *abc*-frame.

$$f_{abc}(t) = T^{-1} f_{\alpha\beta\gamma}(t) = \frac{2}{3}\begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}\begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \\ f_\gamma(t) \end{bmatrix} \tag{7}$$

The sequence signals are transformed from the *abc*-frame to the *dq*-frame using Park transformation (8).

$$f_{dq0}(t) = T f_{abc}(t) = \frac{2}{3}\begin{bmatrix} \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{8}$$

The *dq* signals are then fed through a PI controller. The positive-sequence voltage is regulated to the rated positive-sequence real and reactive power at the PCC while the negative-sequence voltage is used to suppress the negative-sequence current or power to null. For the previously mentioned H3LC control such as DC-pole capacitor balancing and switching generation, the

positive and negative-sequence *dq* signals are transformed into the *abc*-frame using the inverse Park transform (9) for the three-phase voltages seen in (10). The fundamental frequency voltage amplitude for each phase is found by taking the root-mean-square value of the calculated summations and multiplying by $\sqrt{2}$ to find the peak of each phase (11). Note that φ_j angle $[-\frac{2\pi}{3}, 0, \frac{2\pi}{3}]$ is from (10). Using (11), the phase voltage amplitudes can be found as seen in (12).

$$f_{abc}(t) = T f_{dq0}(t) = \begin{bmatrix} \sin(\theta) & \cos(\theta) & 1 \\ \sin\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \sin\left(\theta + \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} f_d(t) \\ f_q(t) \\ f_0(t) \end{bmatrix} \tag{10}$$

$$v_j^*(\theta_j) = V_d^+ \sin(\theta + \varphi_j) + V_q^+ \cos(\theta + \varphi_j) + V_d^- \sin(-\theta + \varphi_j) + V_q^- \cos(-\theta + \varphi_j) \tag{10}$$

$$\mathrm{V_{1H,j}} = \sqrt{2} \sqrt{\frac{1}{2\pi} \int_0^{2\pi} v_j^{*2}(\theta)\, d\theta} \tag{11}$$

$$\mathrm{V_{1H,a}} = \sqrt{\begin{matrix} V_d^{+2} - 2V_d^+ V_d^- + V_q^{+2} \\ +2V_q^+ V_q^- + V_d^{-2} + V_q^{-2} \end{matrix}} \tag{12}$$

$$\mathrm{V_{1H,b}} = \sqrt{\begin{matrix} V_d^{+2} + V_d^{-2} + V_q^{+2} + V_q^{-2} + \sqrt{3} V_d^+ V_q^- \\ +\sqrt{3} V_q^+ V_d^- + V_d^+ V_d^- - V_q^+ V_q^- \end{matrix}}$$

$$\mathrm{V_{1H,c}} = \sqrt{\begin{matrix} V_d^{+2} + V_d^{-2} + V_q^{+2} + V_q^{-2} - \sqrt{3} V_d^+ V_q^- \\ -\sqrt{3} V_q^+ V_d^- + V_d^+ V_d^- - V_q^+ V_q^- \end{matrix}}$$

With $\mathrm{V_{1H,abc}}$ found in (13), α_j, from (2) can be found. The per-phase voltages $v_{abc}^*(\theta_{abc})$ can be described using (13)

$$v_j^*(\theta_j) = \mathrm{V_{1H,j}} \sin(\theta_j) \tag{13}$$

The phase angles, θ_j, can be found using (12) and (13) and are summarized in (14).

$$\theta_a = -\sin^{-1}\left(\frac{\sin(\theta)\left(V_d^+ - V_d^-\right) - \cos(\theta)\left(V_q^+ + V_q^-\right)}{\sqrt{V_d^{-2} - 2V_d^-V_d^+ + V_d^{+2} + \left(V_q^+ + V_q^-\right)^2}}\right) \tag{14}$$

$$\theta_b = -\sin^{-1}\left(\frac{V_d^- \cos\left(\theta + \frac{\pi}{6}\right) - V_q^- \sin\left(\theta + \frac{\pi}{6}\right) + V_q^+ \cos\left(\theta + \frac{\pi}{3}\right) + V_d^+ \sin\left(\theta + \frac{\pi}{3}\right)}{\sqrt{\begin{matrix} V_d^{+2} + V_d^{-2} + V_q^{+2} + V_q^{-2} + \sqrt{3}V_d^+V_q^- \\ +\sqrt{3}V_q^+V_d^- + V_d^+V_d^- - V_q^+V_q^- \end{matrix}}}\right)$$

$$\theta_c = -\sin^{-1}\left(\frac{V_d^+ \cos\left(\theta + \frac{\pi}{6}\right) - V_q^+ \sin\left(\theta + \frac{\pi}{6}\right) + V_q^- \cos\left(\theta + \frac{\pi}{3}\right) + V_d^- \sin\left(\theta + \frac{\pi}{3}\right)}{\sqrt{\begin{matrix} V_d^{+2} + V_d^{-2} + V_q^{+2} + V_q^{-2} - \sqrt{3}V_d^+V_q^- \\ -\sqrt{3}V_q^+V_d^- + V_d^+V_d^- - V_q^+V_q^- \end{matrix}}}\right)$$

The magnitude and angle of the resulting three-phase signal are used in generating the input signals for switching signal generation.

3.2 Switching Signal Generation

The model uses level shifting PWM (LSPWM), as seen in Figure 3.3, to generate switching signals for FBSMs. The LSPWM determines the number of FBSMs used in the AC side FBCL using the control signals from all the control loops described in Chapter 2 and the output in Section 3.1 [47].

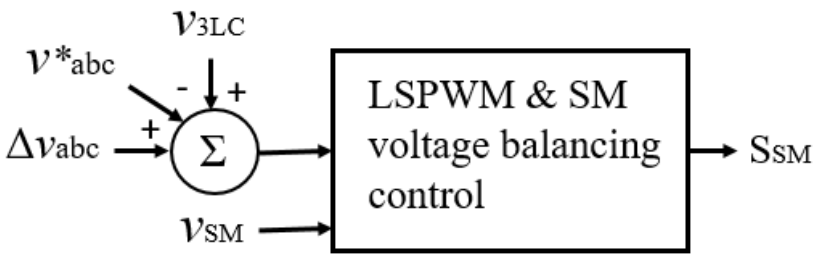

Figure 3.3 Submodule switching signal generation (adapted from [30])

3.3 DEM Model

This thesis places importance on making the simulated model as scalable and modular as possible. To simulate a large number of FBSMs for higher voltage levels, each electromagnetic transient simulation would be computationally expensive when the discrete circuit components are used in the so-called Detailed Model (DM) to construct the FBSMs in the chainlinks of the H3LC due to the large amount of internal electrical nodes of the AC side chainlinks. To reduce simulation time compared to the DM as described in [30], the Detailed Equivalent Model (DEM) of the H3LC based on [41] is used instead. The DEM discretizes the FBSM capacitors using a numerical integration rule and sum up all the FBSM output voltages based on the SM switching functions, the equivalent history sources, and equivalent resistances of the SMs in each chainlink in the discrete-time domain. Thus, each chainlink can be represented by a Thevenin equivalent circuit to eliminate all the internal electrical nodes which greatly reduces the dimension of the system matrix to be solved by the electric circuit solver of Simulink/Simscape Electrical/ Specialized Power System.

Chapter 4: Simulation Results

This chapter shows the simulation results of the H3LC using the proposed sequence controller in the MATLAB/Simulink/Simscape Electrical/Specialized Power System. These simulation studies cover the scenarios when the H3LC operates in healthy balanced grid condition, without the proposed negative-sequence current suppression controller during unbalanced grid voltage condition, and finally, with the addition of the proposed negative-sequence current controller during unbalanced grid voltage condition. These simulation scenarios are performed with a fixed 10μs simulation time step for 2s simulation time. The simulation model is shown in Figure 4.1 and consists of a H3LC connected to a 600kV DC source through 100 km transmission lines, based on the π-section model. The converter output is connected to a 360 kV AC grid through a Delta-Wye three-phase transformer. The DEM model is used to simulate the H3LC as opposed to the DM for accelerated simulation without compromising on the accuracy of the simulation results. The H3LC consists of four discrete IGBT positions which act as director switches and twenty AC side FBSMs in each chainlink of an AC phase, with a voltage rating of $V_{DC}/2$. The IGBT positions simulated are based on the series connected multiple T1800GB45A Westcode IGBT modules [52] with specifications listed in Table 4.1.

Table 4.1 IGBT specifications

V_{ref}	2.5 kV
I_{ref}	1.8 kA
E_{on}	11 J
E_{off}	11 J
E_{rec}	2.8 J
v_{T0}	1.82 V
r_T	1.21 mΩ
v_{D0}	2.27 V
r_D	1.07 mΩ

Since the chainlink has the voltage rating of $V_{DC}/2$ and twenty FBSMs, each FBSM has the nominal DC capacitor voltage of 15kV. The specification of the H3LC is listed in Table 4.2.

Table 4.2 H3LC model parameters

V_{DC}	600 kV
Vgrid	440 kV
SM voltage in AC side chainlink	15 kV
Number of SMs in AC side chainlink	20
DC pole-to-pole capacitance	400 µF
Transformer leakage impedance	0.001+0.18j pu
Transformer winding ratio	360 kV/600 kV
AC inductance	60 mH
DC inductance	70 mH

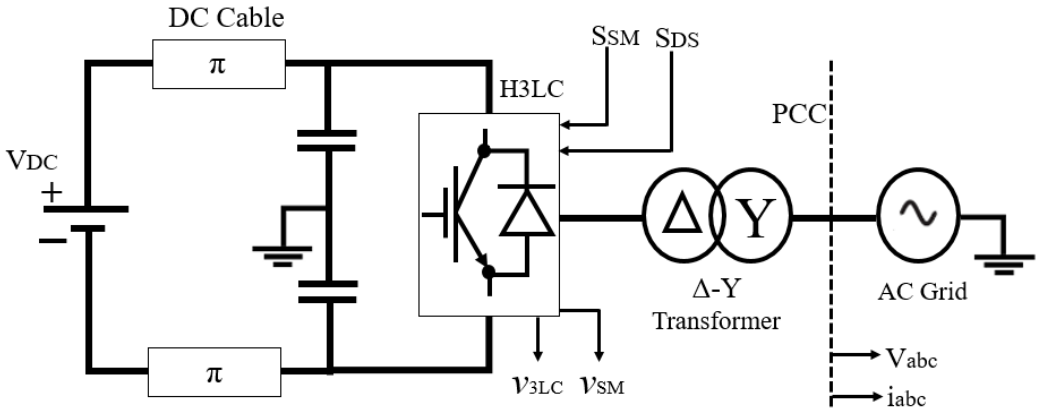

Figure 4.1 Schematic of simulation model (adapted from [30])

4.1 Performance Evaluation

The simulation starts at t = 0s during which the model works in balanced grid voltage operation mode. At the beginning of the simulation, the H3LC acts as an inverter supplying real power to the grid. The real and reactive power references are set to 1GW and 0GVAR, respectively. At t = 0.5s, a voltage imbalance at the grid is simulated, where the peak voltage values of each phase are unequal, thus causing negative-sequence components to appear. The conventional PQ controller mentioned in [30] is used during the imbalance state from t = 0.5s to 1s. Without the auxiliary negative-sequence current suppression controller, the original signals, which contain unbalanced grid voltage, is fed into the main controller. The performance of the original controller under unbalanced AC voltage operation will be compared with the case with the auxiliary negative-sequence current suppression controller. From t = 1s and beyond, the proposed auxiliary negative-sequence suppression controller is implemented. The simulation is similar to the previous case where an imbalance to the AC grid voltage amplitudes is introduced. In this case, however, the input from the AC grid into the PQ-controller passes through a sequence analyzer, which decomposes the signal into its positive and negative-sequence components. The proposed auxiliary controller is used to suppress the negative-sequence current. The benefits of using the proposed auxiliary negative-sequence current suppression controller will be demonstrated in this section through the following figures that show various waveforms that undergo the normal operation state, imbalance state and negative-sequence suppression state.

During normal operation, t = 0s to 0.5s, the closed-loop control of the H3LC operates as intended with balanced three-phase converter voltage and current outputs. The converter-side three-phase voltage has the amplitude of around 590kV while the three-phase converter current is around

2000A, as shown in Figure 4.2. In the second case where t = 0.5s to 1s, using a gain block, the three-phase AC grid voltages are made to have different amplitudes to create unbalanced grid voltage intentionally. As expected, with unbalanced grid voltage, the output line currents displayed on the converter side is likewise unbalanced. The line-to-line voltages on the converter side are filtered through the AC side FBSM and have an amplitude of around 350kV, 320kV and 300 kV for phases a, b and c, respectively, at steady state. The average grid voltage is calculated as $(260kV + 320kV + 360kV)/3 = 313.33kV$. The maximum voltage devation from the average is $360kV - 313.33kV = 46.67kV$, which represents the voltage unbalance of 14.9%.

As can be seen in Figure 4.2 when t = 0.5s to 1s, the H3LC without the negative-sequence current suppression controller does not perform well in maintaining a proper balanced three-phase sinusoidal waveforms of the converter output voltage and current. The asymmetrical voltage and current waveforms are a good indicator that the power measurements will also display undesirable oscillations, as shown in Figure 4.6.

The line-to-line voltages and line currents measured from the converter side of the transformer terminals are displayed in Figure 4.2 from t = 1s to 1.6s. It is evident that the three-phase voltages are not equal in amplitude, yet the phase currents remains balanced. As a result, the auxiliary controller suppresses the flow of negative-sequence current thereby canceling negative-sequence power flow as well. The implications of supressing negative sequence current will be shown later in this chapter.

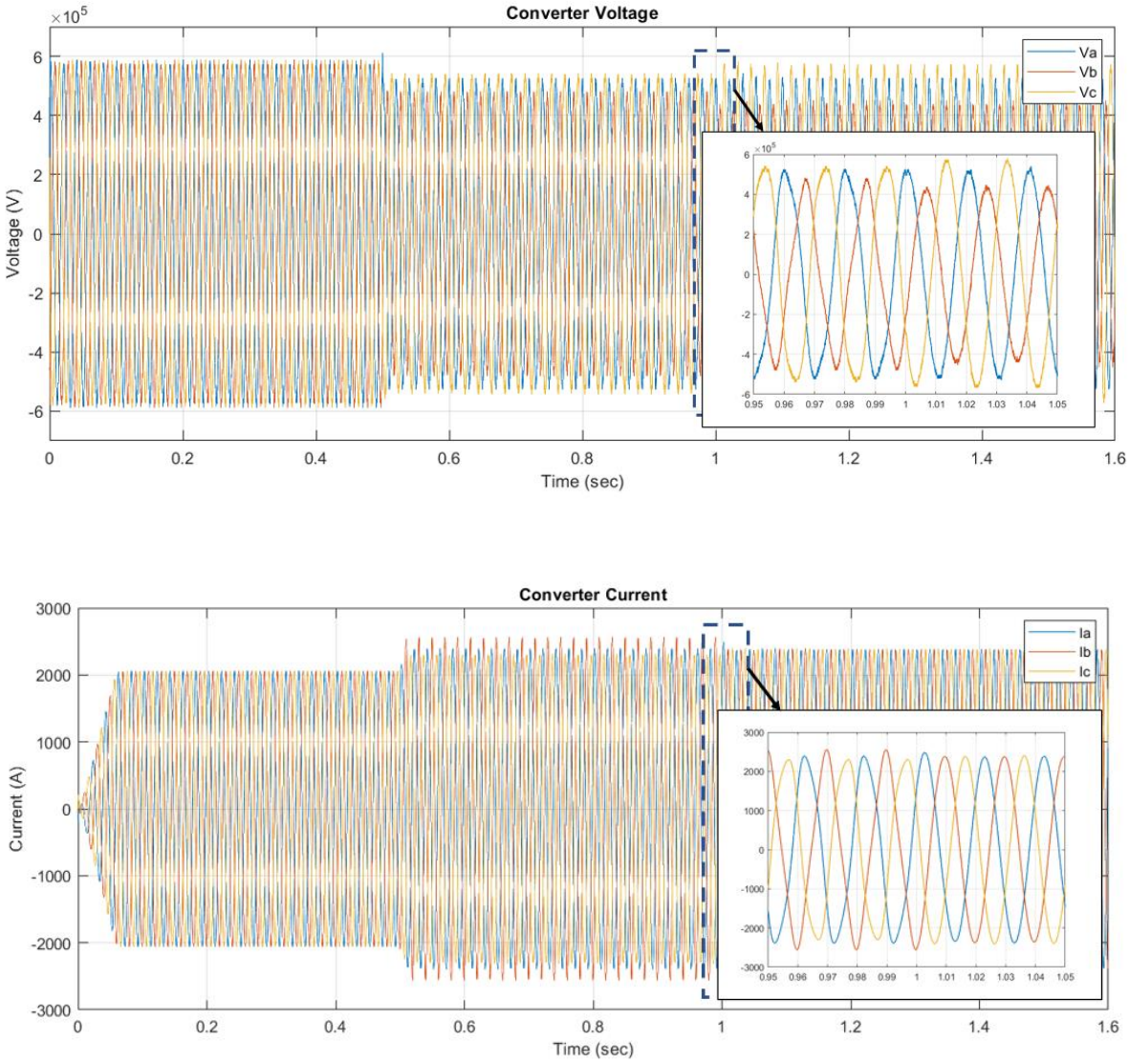

Figure 4.2 Three-phase output measured at converter side. Converter voltage (Top) and converter current (Bottom)

As shown in Figure 4.3, the total SM capacitor voltages of each AC side chainlink phase in the normal operation case do not experience much voltage ripples and stay within 2% of 300kV during the first 0.5s. Past t = 0.5s, the waveforms display more ripple and are not reduced when the negative-sequence current is suppressed. This is because the energy variation of a chainlink depends on the chainlink voltage and AC current flow through the chainlink. The unbalanced

grid voltage condition causes different chainlink energy variations for each of the three phases and a different operating condition before and after the unbalanced grid voltage is applied. It is shown in Figure. 4.3 that the chainlink energy variations in Phase-B and Phase-C are larger than Phase-A after the unbalanced grid voltage is applied, which results in greater SM capacitor voltage ripples. Figure 4.4 shows the individual SM voltages in each chainlink. As seen in the subfigure, there is relatively small voltage ripple which is due to the voltage balancing scheme described in section 2.2.2.

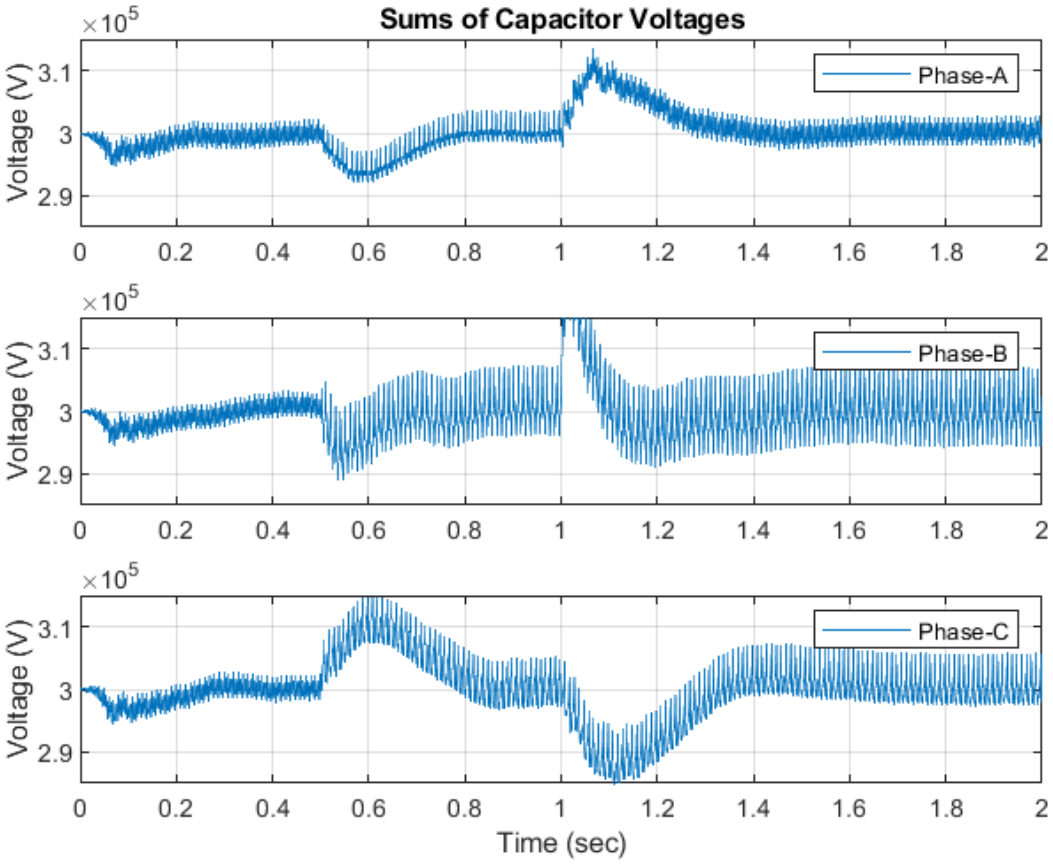

Figure 4.3 Summation of three-phase FBSM capacitor voltages

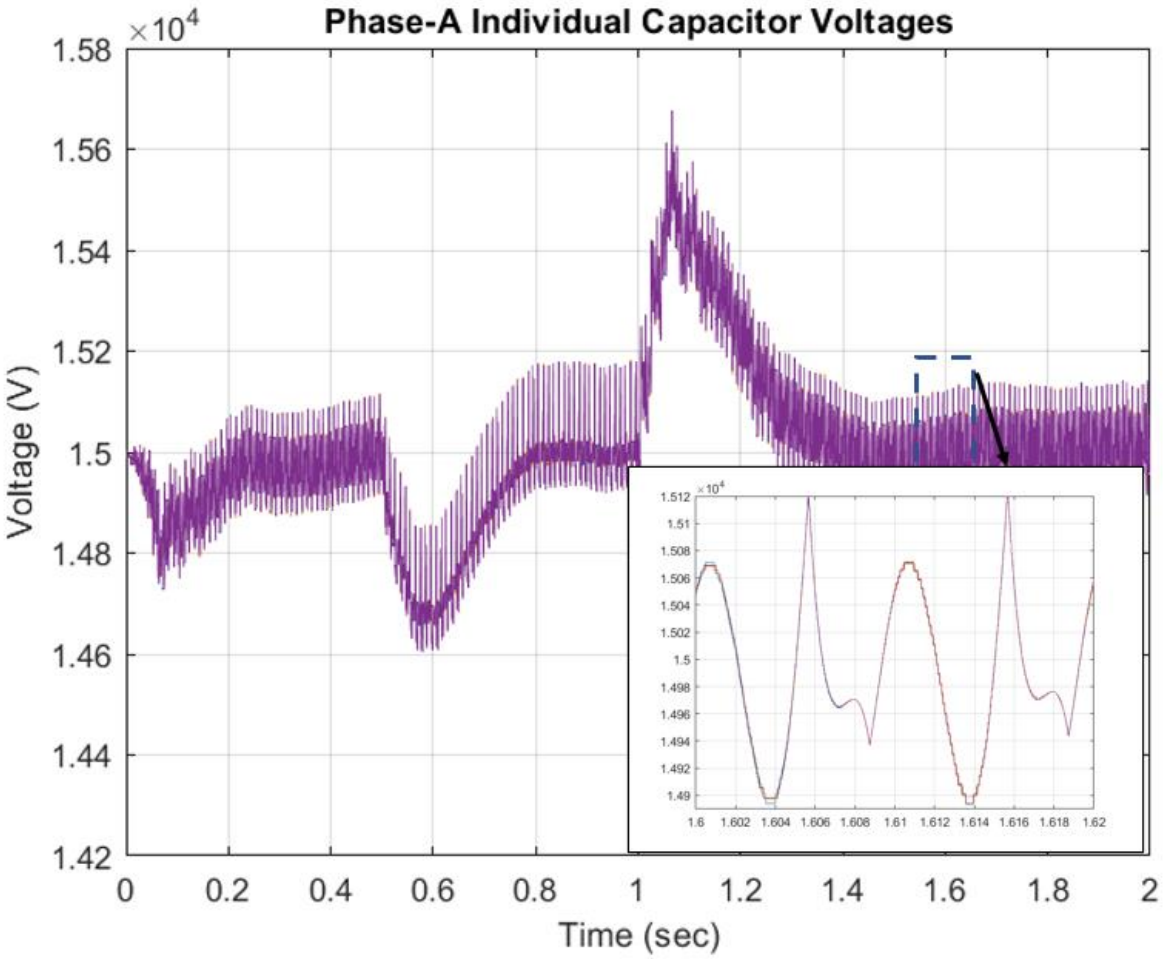

Figure 4.4 Individual capacitor voltages showing 4 out of 20 SMs

For Figure 4.5, the DC-pole capacitor voltages do not fluctuate much from t = 0s to 0.5s. From t = 0.5s to 1s, without the auxiliary negative-sequence current suppression controller, the DC-pole capacitor voltages show greater fluctuation due to the unbalanced grid voltage. From t = 1s to 2s, the negative-sequence current is suppressed. However, the auxiliary negative-sequence current suppression control does not reduce the DC-pole capacitor voltage ripple and the total DC-link voltage ripple, as shown in Figure 4.5.

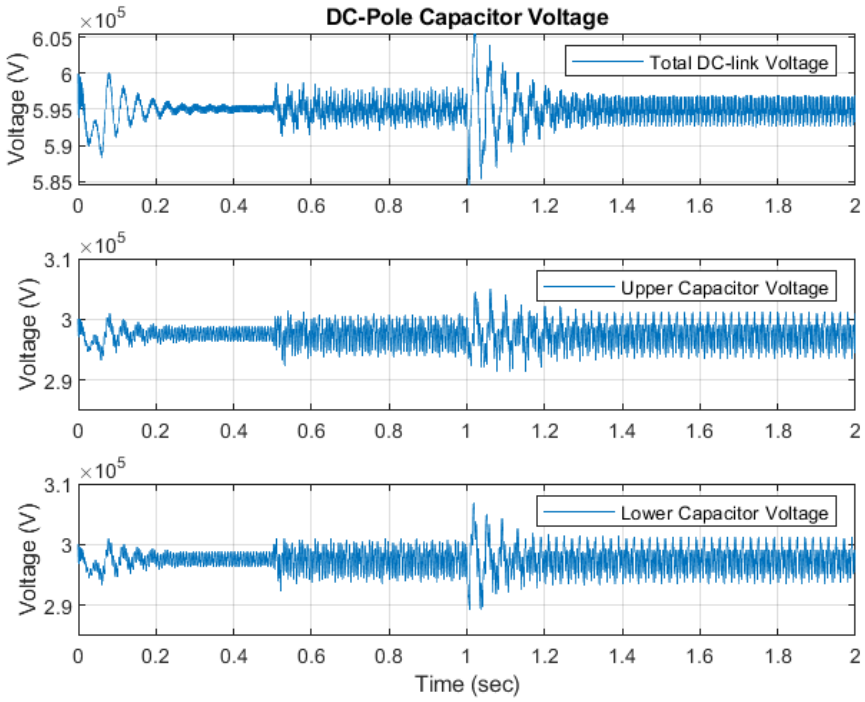

Figure 4.5 DC-pole capacitor voltages

The real power reference for the positive-sequence control is set to be 1GW. For the negative-sequence real power, the power reference is 0W as any existing negative-sequence current is targeted to be suppressed. Similarily, the reactive power reference for the positive-sequence control is 0VAR. For the negative-sequence reactive power, the power reference is also 0VAR as any negative-sequence current is suppressed. The real and reactive power waveforms in Figure 4.6 behave as expected from t = 0s to 0.5s and follow the reference lines well. There is negligible negative-sequence real or reactive power present during normal operation. However, during the grid voltage imbalance state, the real power and reactive power plots are shown in Figure 4.6 to have an order of magnitude of greater oscillations, meaning significant negative-sequence power flow. There exists some oscillatory instantaneous reactive power due to switching harmonics, but it is orders of magnitude less than the real power measured as seen in the combined scaled figure.

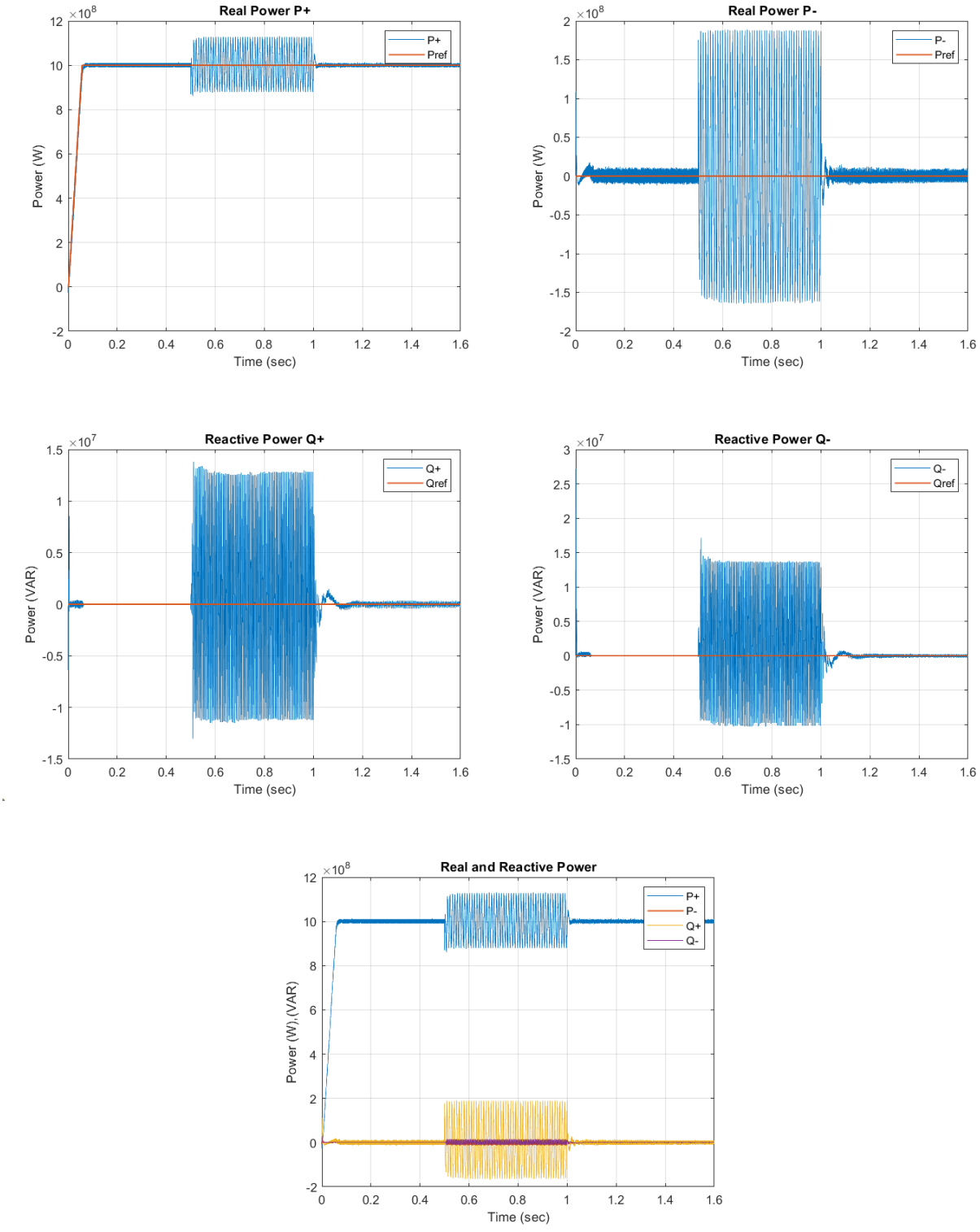

Figure 4.6 Real and reactive power waveforms

Figures 4.7 and 4.8 show the cascaded FBSM voltage and three-level NPC voltage for Phase-A respectively. As third-order harmonic injection is not employed concurrently with the auxiliary controller, there the cascaded FBSM voltage is not bound within $V_{DC}/4$. To account for the voltage ripples that exceed 150kV present during the grid voltage imbalance state in Figure 4.7, the voltage rating for the FBSMs is set to $V_{DC}/2$.

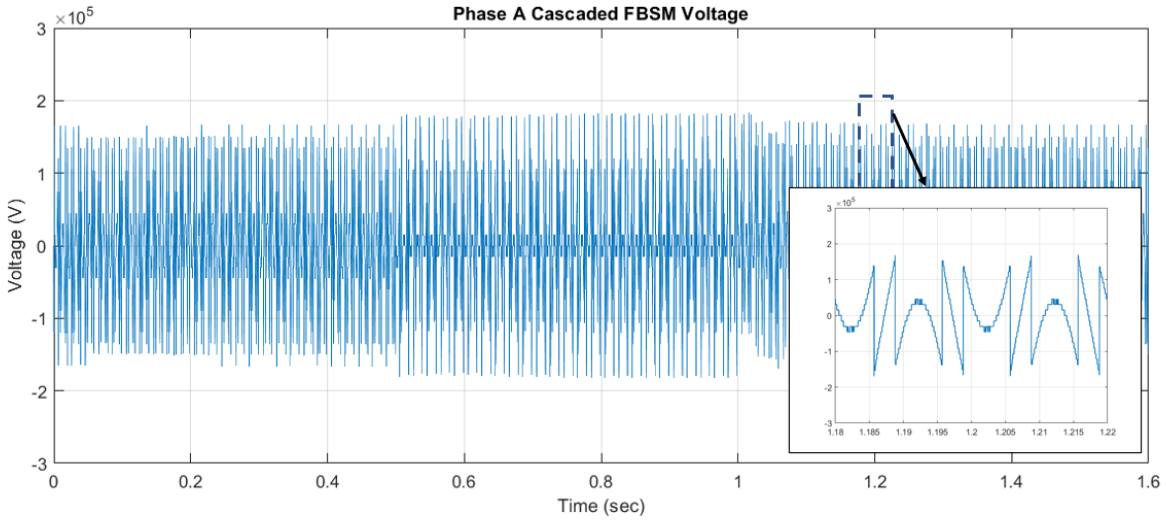

Figure 4.7 Cascaded FBSM voltage for Phase-A

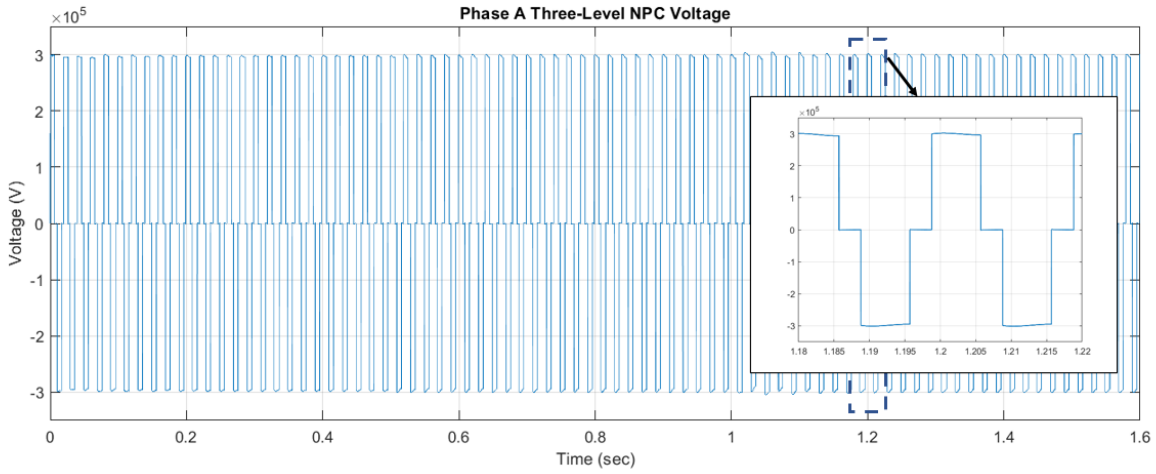

Figure 4.8 Three-level Phase-A NPC output

Figure 4.9 shows the positive and negative-sequence *dq* components of the grid voltage. Prior to the grid voltage imbalance, the negative-sequence components are null. During the grid voltage imbalance case, the voltage waveforms display high oscillations showing high degree of voltage imbalance among the three phases. The oscillations are suppressed from t = 1s to 1.6s as the auxiliary controller is employed. In Figure 4.10, the different sequence grid current components are plotted. As shown in Figure 4.10, the negative-sequence current has an amplitude of less than 5A once it is suppressed.

From figures 4.9 and 4.10, the oscillations that occur during the voltage unbalance case indicate the presence of double-line frequency components otherwise known as 2nd order harmonics. When the *dq* voltages and currents are transformed back to the *abc*-frame in the control scheme, the cosine and sine functions in the inverse Park transformation matrix translate 2nd order harmonics into fundamental and 3rd order harmonic components in the converter sinusoidal three-phase voltage and current waveforms. The THD caused by the harmonics are undesirable

and are eliminated by using the auxiliary controller at t = 1s which removes the double-line frequency components in the *dq* voltage and currents as seen in the magnified subplots in the figures 4.9 and 4.10.

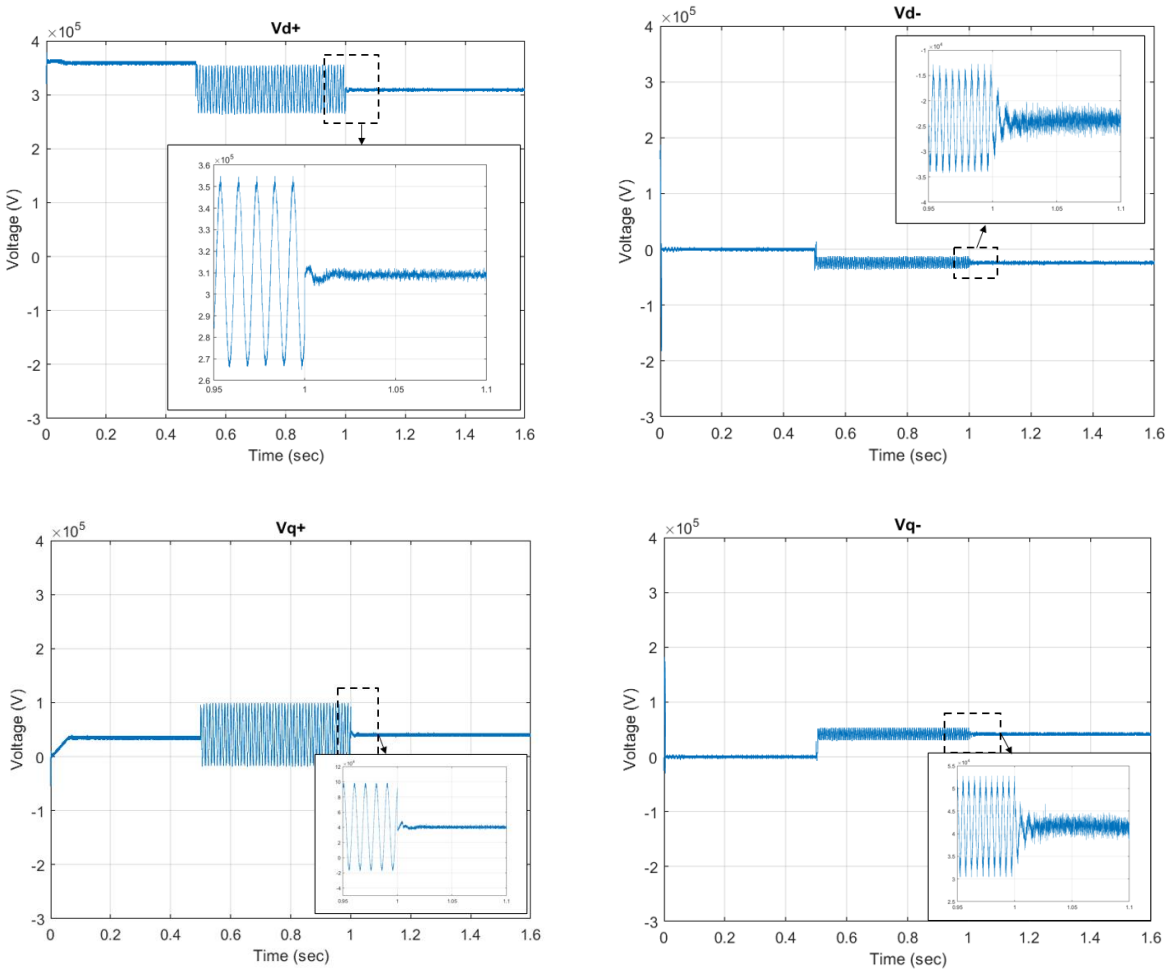

Figure 4.9 Positive and negative-sequence dq voltage components

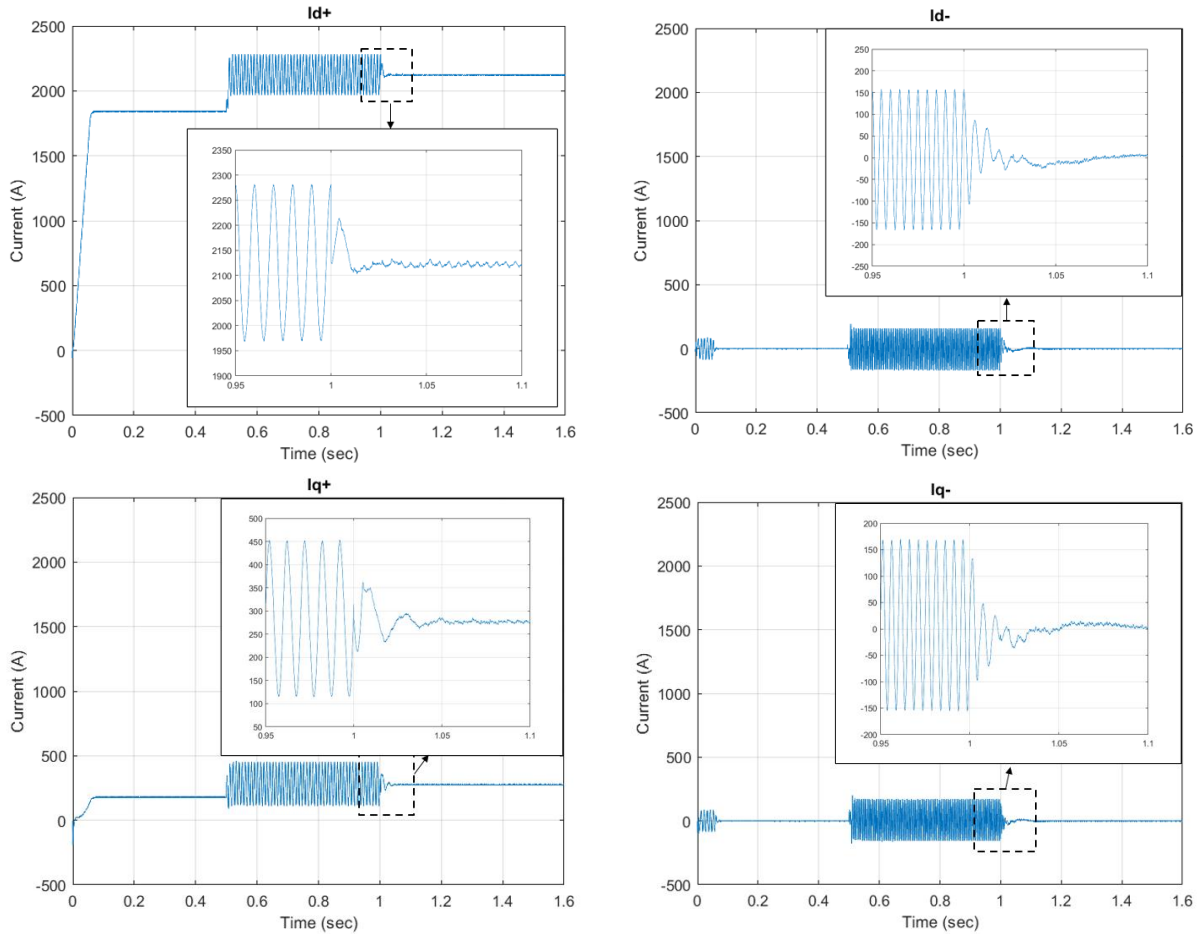

Figure 4.10 Positive and negative-sequence dq current components

Figures 4.11 to 4.14 show the results of Fast Fourier Transform (FFT) applied on the converter three-phase AC voltage and current. The analysis is done for two cases, where t = 0.8 to 1s for the case of unbalanced grid voltage and t = 1.4 to 1.6s for when the negative-sequence current is suppressed. The FFT is done to compare the THDs for the cases with and without large negative-sequence current.

Figure 4.11 displays the FFT results of the converter sinusoidal three-phase voltage when the grid voltage is unbalanced. From the figure, the THD ranges from 8.04% to 10.19% and shows very high fundamental and 3rd order harmonics in the magnitude of 10^4 V. The results can be

compared to figure 4.12 where the THD ranges from 1.78% to 2.41% and the 3rd order harmonics are negligible in magnitude compared to the previous case.

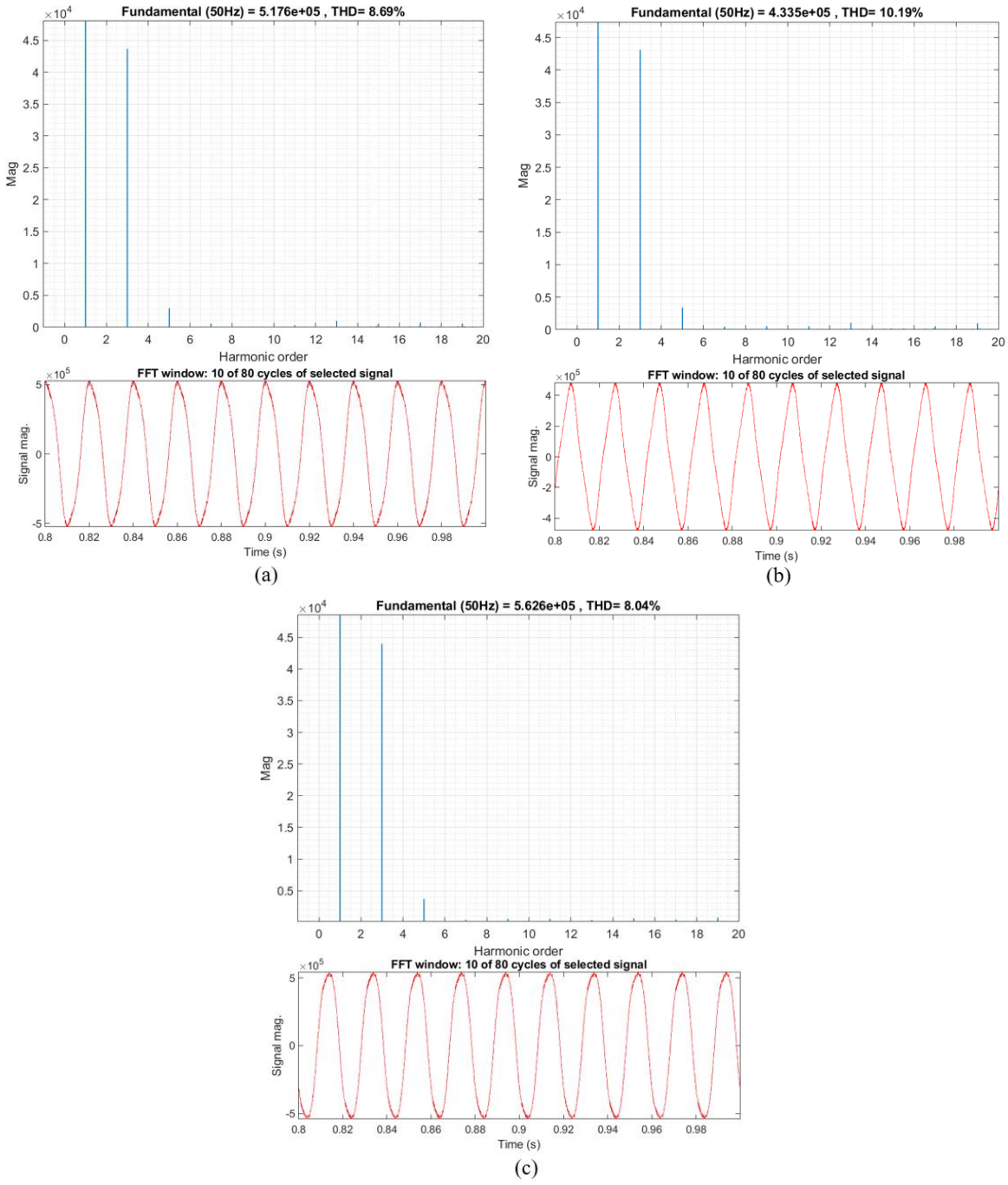

Figure 4.11 FFT analysis of converter sinusoidal three-phase voltage during grid voltage unbalance case. (a) Phase-A voltage. (b) Phase-B voltage. (c) Phase-C voltage.

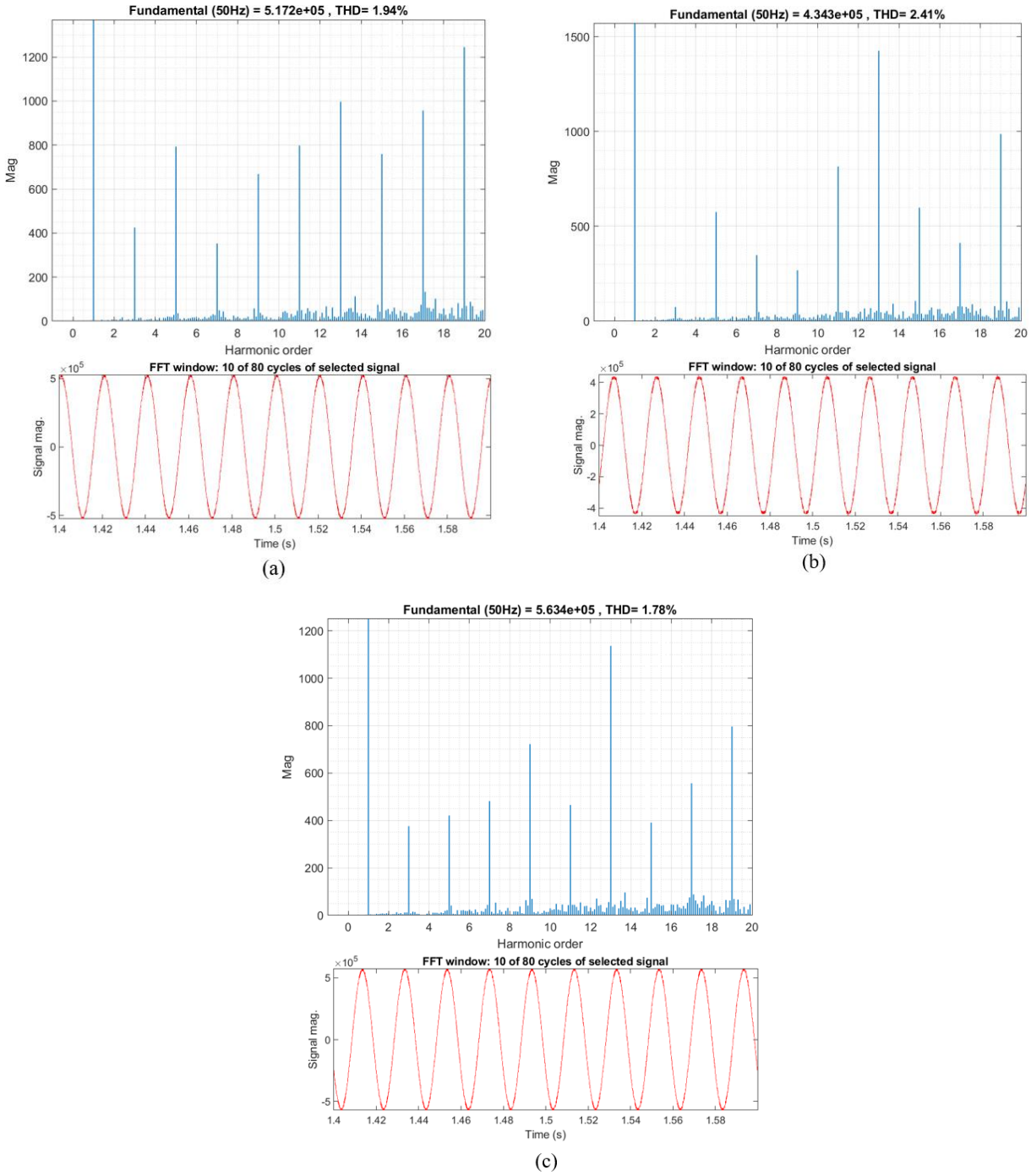

Figure 4.12 FFT analysis of converter sinusoidal three-phase voltage after the auxiliary controller is employed. (a) Phase-A voltage. (b) Phase-B voltage. (c) Phase-C voltage.

A similar comparison can be made by observing the FFT analysis shown in Figures 4.13 and 4.14. Figure 4.13 show displays the FFT results of the converter sinusoidal three-phase current when the grid voltage is unbalanced. In figure 4.13, the THD is shown to range from 7.45% to 7.56%. The magnitude of the 3rd order harmonic is around 180 V which is comparatively extremely large compared to the magnitude of the 3rd order harmonic in figure 4.14 which does not exceed 2 V. The THD is also small, ranging from 0.13% to 0.15% validating that the harmonics caused by the negative-sequence current have been eliminated through the use of the auxiliary controller.

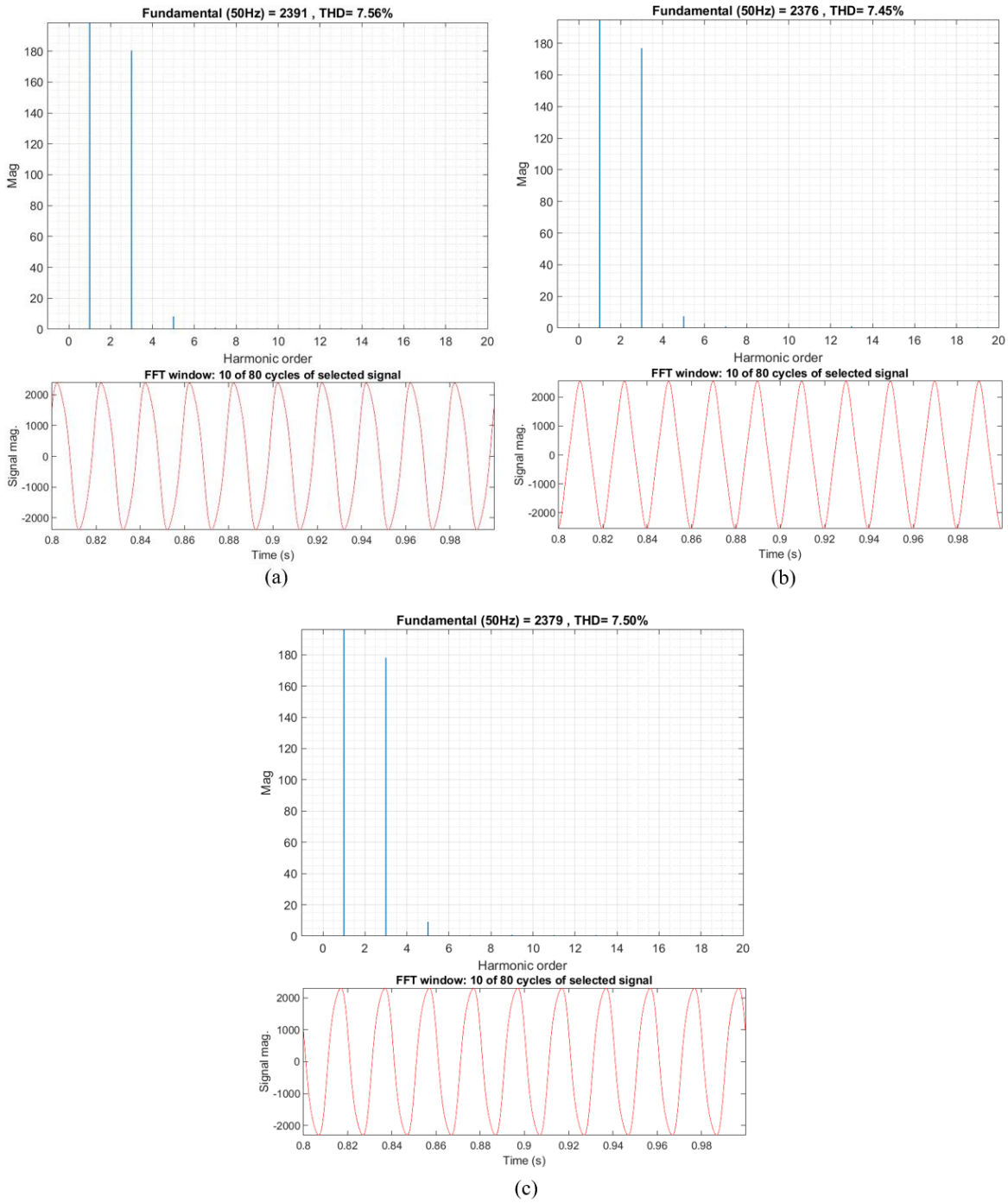

Figure 4.13 FFT analysis of converter sinusoidal three-phase current during grid voltage unbalance case. (a) Phase-A current. (b) Phase-B current. (c) Phase-C current.

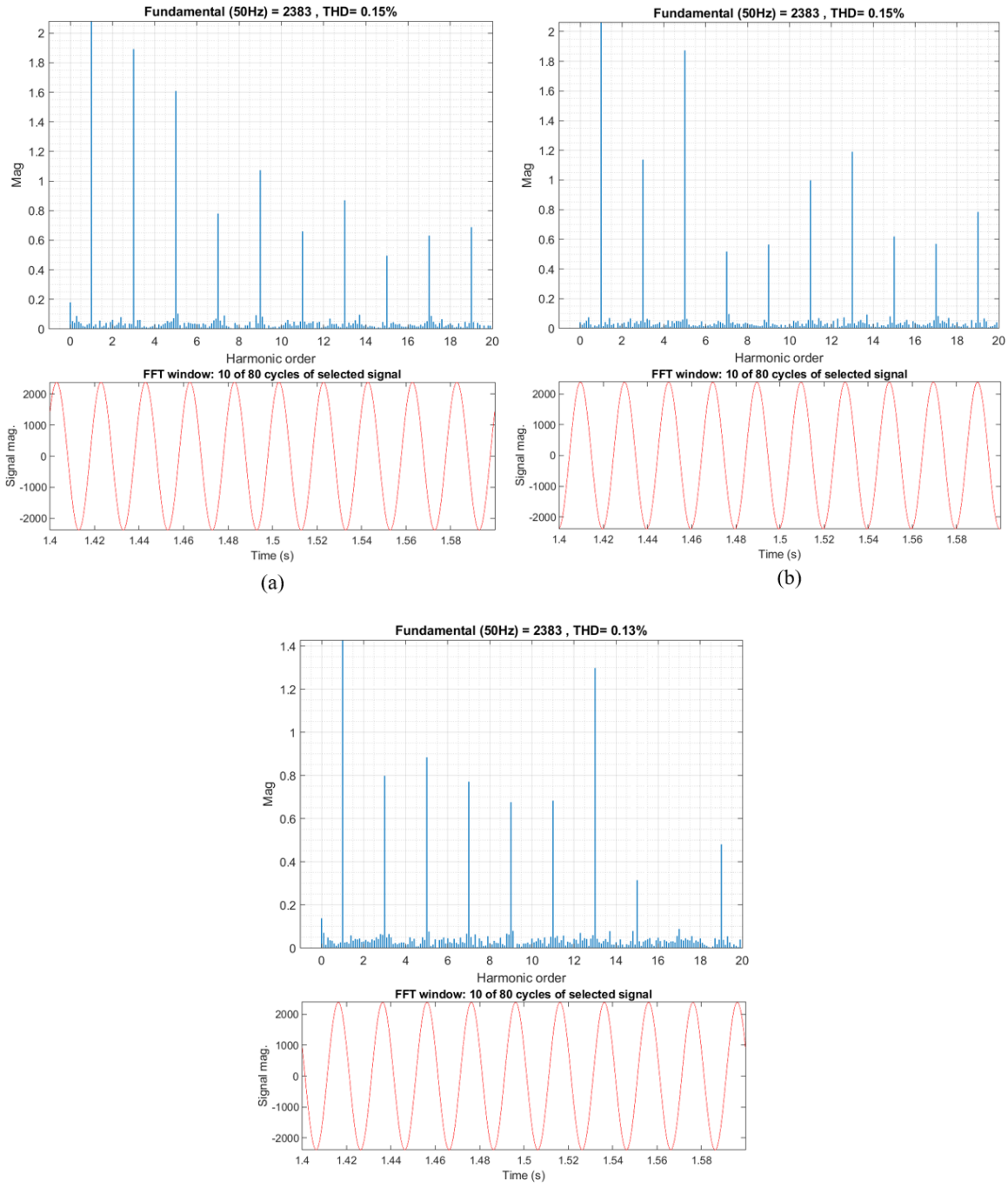

Figure 4.14 FFT analysis of converter sinusoidal three-phase current after the auxiliary controller is employed. (a) Phase-A current. (b) Phase-B current. (c) Phase-C current.

4.2 Conclusion/Summary

To summarize, the auxiliary controller, when the H3LC enters unbalanced mode, suppresses the negative-sequence current that flows from the AC grid. As the converter voltage is decreased from the imbalance, the current, in turn, is increased. With the negative-sequence controller, the three-phase current waveform is balanced, however. The power measurements show that there is significantly less oscillation in the case of the auxiliary controller than without. Also, the FBSM voltages are shown to be well balanced with negative-sequence suppression controller which demonstrates that the energy balancing discussed in Chapter 3 is working as intended. Lastly, the double-line frequency components that were present during the voltage unbalance case are seen to be suppressed after the use of the auxiliary controller when observing the FFT analysis of the waveforms.

Chapter 5: Conclusion

Due to the increasing demand in energy distribution and generation, there is a rapid increase in research and development activities in the field of grid connected high power electronic converters, e.g., HVDC and FACTS systems. While there are several novel power electronic converter circuit topologies and control methods being unveiled, challenges in control development of the power electronic converters during abnormal or faulted grid operating conditions are also being discovered. Grid voltage sagging is an example of an issue that needs to be taken into consideration for safe and reliable system operation [46]. Grid voltage sags produce negative-sequence components that can greatly affect the performance of the power electronic converter system if the power converter controls are not designed properly. Negative-sequence grid voltage at the PCC results in an uncontrolled negative-sequence current flowing from the converter to power grid which may destabilize the power injected into the AC grid and, in turn, produces DC bus voltage ripples of the power electronic converter. There are different mitigation strategies proposed in the literature for different power converter types. The negative-sequence current suppression controller proposed in this thesis, offers a control method that has been designed for the H3LC, an emergent cascaded hybrid multilevel converter, and has been verified by the detailed simulation model of a H3LC in Simulink/Simscape Electrical/Specialized Power System environment. The method can be applied to other cascaded hybrid multilevel converters, e.g., thyristor-based hybrid 3-level converter [30] and hybrid 5-level converter [54] with a similar circuit topology to the H3LC.

5.1 Thesis Summary

This thesis analyzed negative-sequence current suppression control methods used in various power electronic converters. An existing symmetrical-component-based negative-sequence

control method is formulated in the dq converter reference frame for the H3LC. This thesis discussed the theory behind the development of the negative-sequence suppression control and evaluated its performance through simulations for multiple case studies. The theoretical and evaluation sections in this thesis offered a different perspective in developing a working negative-sequence suppression controller for the emerging hybrid multilevel converters for HVDC and FACTS applications. These new hybrid converters including the H2LC, H3LC and AAC can be viable alternatives to the state-of-the-art MMCs, applied to various applications that are accompanied by grid voltage unbalance issues.

5.2 Future Work

An improvement to compensating the unbalanced voltages would be to mitigate the effects of zero-sequence current on the grid. Due to the decoupling transformer in the H3LC and the lack of a neutral wire, creating a zero-sequence current controller is not viable using the same methods outlined in this thesis. Another topic of research that could be expanded upon would be the simulations. Doing more stringent simulations based on industrial codes and standards for stricter performance evaluation and points of failure would help add to the feasibility of a negative-sequence controller used for the H3LC and similar topologies. Lastly, according to [45], simply using the negated version of the positive-sequence phase angle from the PLL for the negative-sequence creates a small steady-state error in the output power. As creating a separate PLL tracker for the negative-sequence was determined to be beyond the scope of this thesis, it would be a method of further optimization to the H3LC negative-sequence current suppression controller.

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