Tampere University

Arttu Ruusila

MODULATION METHODS FOR CONVERTERS USED AS STATIC SYNCHRONOUS COMPENSATORS

Master of Science Thesis
Faculty of Engineering and Natural Sciences
Examiners: Associate Professor Petros Karamanakos
Assistant Professor Antonios Antonopoulos
May 2023

ABSTRACT

Arttu Ruusila: Modulation methods for converters used as static synchronous compensators
Master of Science Thesis
Tampere University
Master's Degree Programme in Automation Engineering
May 2023

A static synchronous compensator (STATCOM) is a device that is capable of compensating reactive power from the grid or supplying active power into the grid if connected to energy storage. The main component of the STATCOM is a voltage source converter, in this thesis a multilevel modular converter (MMC) in a double-star configuration.

The MMC consists of submodules that can be inserted or bypassed. Two main types of MMC submodules exist. A half-bridge (HB) submodule (SM) consists of 2 semiconductor switches and is capable of producing 2 voltage levels. A full-bridge (FB) SM on the other hand consists of 4 semiconductor switches and is capable of producing 3 voltage levels which allows a much broader range of operation.

The modulation methods for the HB-MMC are well-known. Although FB SM has significant advantages and is widely used, the available modulation methods for the FB-MMC include only phase-shifted carriers pulse width modulation (PS-PWM), optimized pulse patterns, space vector modulation, and hybrid nearest level modulation (NLM). Out of these methods, only PS-PWM enables the use of a variable dc-link voltage and boosting the dc-link voltage. Based on the modulating signals of PS-PWM phase disposition (PD) PWM and NLM for FB-MMC are developed. All these methods can produce 2N+1 voltage levels and boost the dc-link voltage.

In addition to choosing the number of SMs to be inserted at any given time step, the SM capacitor voltage balancing has to be considered. The balancing can be done with a sorting algorithm or the modulation can have inherent natural balancing ability. In this thesis, two sorting algorithms are examined. The natural balancing ability of PS-PWM for HB-MMC and FB-MMC is also addressed.

The performance of the modulation methods is evaluated with simulations based on their current quality, device switching frequency, apparent switching frequency, and peak-to-peak amplitude of the circulating currents. For a fair and meaningful comparison, all methods have effectively the same device switching frequency. The performance of PS-PWM and PD-PWM is identical when 2N+1 modulation is used and almost identical with N+1 modulation. These carrier-based methods outperform NLM in all performance metrics.

Keywords: modular multilevel converter, mmc, modulation, voltage balancing

The originality of this thesis has been checked using the Turnitin OriginalityCheck service.

TIIVISTELMÄ

Arttu Ruusila: Modulaatiomenetelmät staattisena synkronikompensaattorina toimiville konverttereille
Diplomityö
Tampereen yliopisto
Automaatiotekniikan DI-ohjelma
Toukokuu 2023

Staattinen synkronikompensaattori (STATCOM) on laite, joka kykenee kompensoimaan loistehoa sähköverkosta tai syöttämään pätötehoa verkkoon, mikäli se on kytketty energiavarastoon. STATCOMin pääkomponentti on jännitelähdekonvertteri, joka on tässä työssä modulaarinen monitasoinen konvertteri (MMC) kaksoistähtikytkennässä.

MMC koostuu moduuleista, jotka voidaan ohittaa tai kytkeä konvertteriin. MMC:llä on kaksi yleisesti käytettyä moduulityyppiä. Puolisiltamoduuli (HB) koostuu kahdesta puolijohdekytkimestä ja pystyy tuottamaan 2 jännitetasoa. Kokosiltamoduuli (FB) puolestaan koostuu neljästä puolijohdekytkimestä ja kykenee tuottamaan 3 jännitetasoa, mikä mahdollistaa laajemman toiminta-alueen.

Modulointimenetelmät puolisiltamoduuleista koostuvalle mmc:lle

Modulointimenetelmät puolisiltamoduuleista koostuvalle MMC:lle (HB-MMC) ovat hyvin tunnettuja. Vaikka kokosiltamoduulilla on huomattavia etuja ja se on laajasti käytössä, tunnetut modulointimenetelmät kokosiltamoduuleista koostuvalle MMC:lle (FB-MMC) sisältävät ainoastaan PS-PWM- (eng. phase-shifted carriers pulse width modulation), OPPs- (eng. optimized pulse patterns), SVM- (eng. space vector modulation) ja hybridi NLM- (eng. nearest level modulation) menetelmät. Näistä menetelmistä vain PS-PWM mahdollistaa muuttuvan jännitteen dc-linkissä sekä boost-moodissa toimimisen. PS-PWM-menetelmän modulaatiosignaaleihin perustuen kehitetään PD-PWM (eng. phase disposition PWM) ja NLM menetelmät kokosiltamoduuleille. Kaikki nämä menetelmät voivat tuottaa 2N+1 jännitetasoa ja toimia boost-moodissa.

Moduulien määrän valitsemisen lisäksi jokaisella ajan hetkellä on otettava huomioon moduulien kondensaattoreiden jännitteiden tasapainotus. Tasapainotus voidaan tehdä lajittelualgoritmilla tai modulointimenetelmä voi pystyä itse pitämään jännitteet tasapainossa. Tässä työssä tutkitaan kahta lajittelualgoritmia. Lisäksi käsitellään PS-PWM-menetelmän tasapainotuskykyä HB-MMC:lle ja FB-MMC:lle.

Modulaatiomenetelmien suorituskykyä arvioidaan simuloinneilla niiden tuottaman virran laadun, kytkimien ja konvertterin kytkentätaajuuden sekä kiertävien virtojen huipusta huippuun -arvon avulla. Jotta vertailua voidaan tehdä, kaikilla menetelmillä on lähes sama kytkimien kytkentätaajuus. PS-PWM:n ja PD-PWM:n suorituskyky on identtinen, kun käytetään 2N+1 modulointia ja lähes identtinen N+1 moduloinnilla. Näiden menetelmien suorituskyky on kaikilla suorituskyvymittareilla parempi kuin NLM:llä.

Avainsanat: modular multilevel converter, mmc, modulation, voltage balancing

Tämän julkaisun alkuperäisyys on tarkastettu Turnitin OriginalityCheck -ohjelmalla.

PREFACE

I would like to express my gratitude to Dr. Petros Karamanakos for providing me with this topic and trusting me, although my previous knowledge of the topic was limited. Thank you for your supervision, time, and support during the project. I would also like to thank Dr. Antonios Antonopoulos for his valuable feedback and advice.

Thanks to my family and friends for their support, encouragement, and shared interest through the years, starting from the very first school day. Last, thank you Jutta for supporting and pushing me in the right direction every day.

I am glad that this does not end here.

Tampere, 11th May 2023

Arttu Ruusila

CONTENTS

LIST OF ACRONYMS

APOD-PWM	alternating phase opposite disposition pulse width modulation
FACTS	flexible ac transmission system
FB	full bridge
HB	half bridge
HVDC	high voltage direct current
IGBT	insulated gate bipolar transistor
LB	left bridge
MMC	modular multilevel converter
NLM	nearest level modulation
OPPs	optimized pulse patterns
p.u.	per unit
PCC	point of common coupling
PD-PWM	phase disposition pulse width modulation
POD-PWM	phase opposite disposition pulse width modulation
PS-PWM	phase-shifted carriers pulse width modulation
PWM	pulse width modulation
RB	right bridge
SHE	selective harmonic elimination
SM	submodule
STATCOM	static synchronous compensator
SVM	space vector modulation
TDD	total demand distortion
THD	total harmonic distortion
VSC	voltage source converter

LIST OF SYMBOLS

c	correction factor
C_{SM}	submodule capacitance
D_i	the ith bypass diode in a submodule
f_1	modulating signal frequency
f_c	carrier frequency
f_g	grid frequency
$f_{\mathrm{sw,app}}$	apparent switching frequency
$f_{\mathrm{sw,dev}}$	device switching frequency
$\boldsymbol{g}$	gating vector
h	number of semiconductor devices
I_{arm}	arm current
$i_{\mathrm{circ},x}$	circulating current in phase x
i_{dc}	dc-link current
i_{jx}	arm current in arm jx
$\hat{I}_n$	amplitude of nth current harmonic
I_R	rated current
I_{TDD}	current total demand distortion
I_{THD}	current total harmonic distortion
i_x	current of phase x
L_{arm}	arm inductance
L_g	grid inductance
m	modulation index
m_0	dc offset
m_f	carrier-to-fundamental frequency ratio
N	number of submodules in an arm
n_{jx}	inserted SMs in arm jx

$n_{jx,\mathrm{diff}}$	difference of the inserted SMs between two consecutive steps in arm jx
$n_{jx,\mathrm{old}}$	inserted SMs on previous time step in arm jx
n_{low}	number of inserted submodules in lower arm
n_{out}	phase output pattern
n_{up}	number of inserted submodules in upper arm
R_{arm}	arm resistance
R_g	grid resistance
s	switching state of a submodule
S_i	the ith switch in a submodule
t	time
T_s	sampling interval
$\hat{v}_1$	peak amplitude of phase output voltage
V_c^{Σ}	sum of submodule capacitor voltages in arm
V_c	nominal submodule capacitor voltage
v_c	submodule capacitor voltage
V_{dc}	dc-link voltage
v_g	grid voltage
v_{jx}	arm voltage of arm jx
V_R	rated voltage
V_{ref}	phase voltage reference amplitude
$w^l_{\mathrm{LB},x}$	modulating signal for left bridges of lower arm of phase x
$w^l_{\mathrm{RB},x}$	modulating signal for right bridges of lower arm of phase x
$w_{\mathrm{low},x}$	modulating signal for lower arm of phase x
$w^u_{\mathrm{LB},x}$	modulating signal for left bridges of upper arm of phase x
$w^u_{\mathrm{RB},x}$	modulating signal for right bridges of upper arm of phase x
$w_{\mathrm{up},x}$	modulating signal for upper arm of phase x
ω_g	grid angular frequency
ϕ_c	carrier phase shift
θ_x	inital phase shift of phase x

1. INTRODUCTION

A static synchronous compensator (STATCOM) is a shunt-connected flexible ac transmission system (FACTS). Its main function is to control reactive power in a transmission or a distribution grid. It can also provide active power to the grid if connected to energy storage [1]. The main component of the STATCOM is a voltage source converter (VSC). This thesis examines a STATCOM where the VSC is a modular multilevel converter (MMC).

The MMC was first presented in 2003 [2]. Since that, it has been a topic of continuous research. The MMC consists of a varying number of submodules (SMs), which makes it modular, efficient, and able to achieve all voltage-level requirements. It has a superior harmonic performance and the size of passive filters can be reduced or they can be removed, especially if the number of SMs is high [3].

To achieve the functional requirements of the STATCOM, the MMC must be able to produce a desired output voltage by inserting and bypassing SMs. This is done by modulating the MMC. The modulation of the MMC consists of two parts: determining how many SMs are needed at a time instant and which SMs should be inserted or bypassed. The latter part presents a secondary control objective about keeping the SM voltages balanced.

Numerous modulation methods have been presented in the literature in the last two decades. A widely used category of modulation methods is carrier-based methods. Generally, these methods have one carrier signal per voltage level and the carrier is compared with a modulating signal to determine the state of the SM. The carrier-based pulse width modulation (PWM) methods include phase-shifted PWM (PS-PWM), phase-disposition (PD-PWM), phase opposition disposition (POD-PWM), and alternative phase opposition disposition (APOD-PWM) methods [4].

The MMC can also be modulated with methods that do not require carriers and allow modulation at the fundamental frequency [3]. These methods include nearest level modulation (NLM), selective harmonic elimination (SHE), and optimized pulse patterns (OPPs). The NLM produces the desired voltage by rounding the number of SMs that should be inserted to achieve a reference voltage. It can be also combined with PWM, creating hybrid NLM modulation [5]. SHE eliminates selected harmonics from the harmonic spectrum. OPPs is a modulation method that optimizes the harmonic spectrum rather than eliminat-

ing certain harmonics. It produces the lowest current total harmonic distortion (THD) by default.

All the previously mentioned modulation methods are phase-voltage modulation techniques. Space vector modulation (SVM) is a modulation method that is based on synthesizing the reference voltage vector by combining a finite number of voltage vectors scaled by defined duty cycles. SVM tries to provide desired line-to-line voltages and can add flexibility to modulation via redundant switching states and adjustable duty cycles [6].

In addition to selecting the number of SMs to be inserted, an SM capacitor voltage balance needs to be considered. An unbalance among the capacitor voltages increases circulating currents and affects the output voltage of the MMC. The capacitor voltages can be naturally balanced in the modulation stage, or the balance can be achieved by dedicated voltage balancing control. The most widely used method to control the capacitor voltages is a sorting method that is based on sorting the capacitor voltages and choosing inserted SMs depending on the SM voltage and the current direction [3].

In this thesis modulation methods and capacitor voltage balancing solutions suitable for the MMC used as a STATCOM are evaluated. The MMC is in a double-star configuration and consists of full-bridge SMs. Different modulation methods are evaluated based on current quality, an apparent switching frequency, and circulating currents.

The structure of the thesis is as follows: Chapter 2 presents the structure and operation principle of the MMC with both half-bridge and full-bridge SMs. In Chapter 3 an overview of different modulation methods for MMC is presented. The carrier-based methods and NLM for the full-bridge MMC are analyzed in depth. The different voltage balancing methods are also discussed. Chapter 4 compares chosen modulation methods based on their performance, while Chapter 5 concludes the thesis and presents future research subjects.

2. MODULAR MULTILEVEL CONVERTER

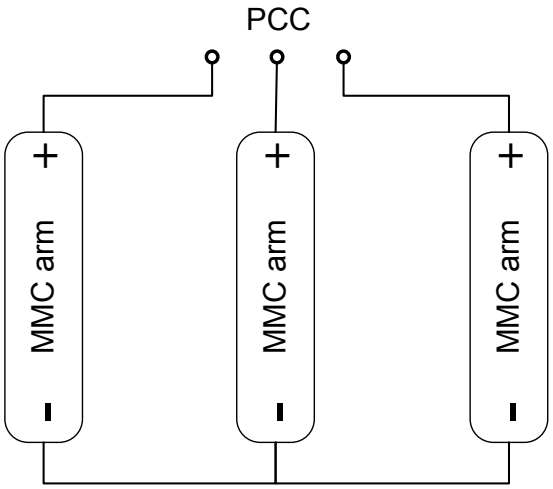
The MMC is part of the multilevel converter family, which, in addition to the MMC includes neutral point clamped converters, flying capacitor converters, and cascade H-bridge converters [7]. It has gained a lot of popularity due to its fundamental features, such as modularity and the ability to achieve any number of voltage levels. As increasing the number of voltage levels only requires adding more SMs, it can be done without increasing the complexity of the converter [8, p. 23].

Although the MMC was initially proposed for high-voltage direct current (HVDC) systems, it also has other significant applications. For example, the converter can be used to control medium-voltage variable-speed drives, as a VSC in FACTS, or to connect energy storage to a grid [3]. In this thesis, the MMC is the VSC of a STATCOM.

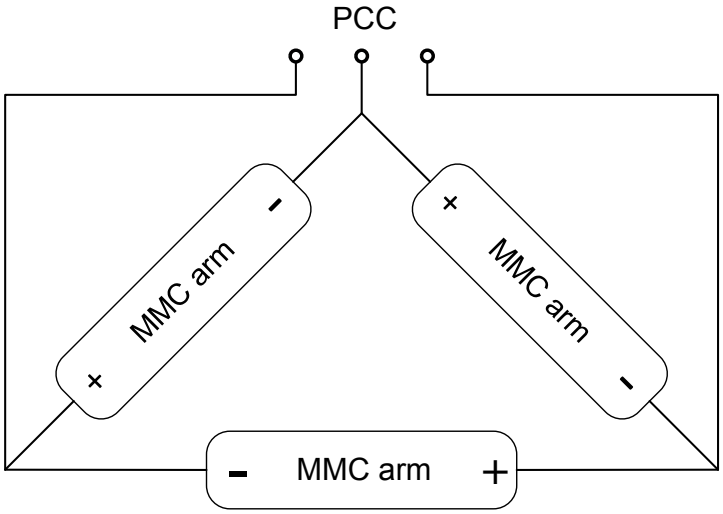
2.1 Structure of MMC

The MMC can have various configurations, such as a single-star MMC, presented in Fig. 2.1a and a delta-connected MMC, presented in Fig. 2.1b. Both converter types consist of three MMC arms, described in Fig. 2.1c. Each arm consists of N series-connected SMs, an arm inductor L_{arm}, and an arm resistor R_{arm}. These configurations do not have a common dc link and thus cannot perform a dc to ac or an ac to dc conversion. The MMC must be in a double-star configuration to achieve said conversions, presented in Fig. 2.2.

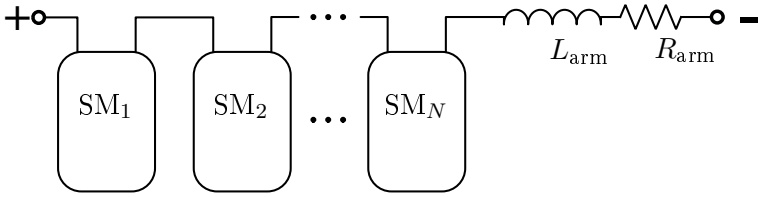
The MMC in the double-star configuration has three phase legs $x \in \{a, b, c\}$, each divided into an upper and a lower arm, $j \in \{u, l\}$, respectively. The arm inductors limit current peaks due to instantaneous voltage differences between the upper and lower arm and filter out high-frequency current components [3],[7]. In Fig. 2.2, the converter is connected to a dc-voltage source V_{dc}, but the dc link of the converter can be also connected to a capacitor or short-circuited. The converter is connected to the grid at the point of common coupling (PCC). Each phase of the grid is modeled with an inductance L_g, a resistance R_g, and a voltage source v_g.



(a) *Single-star configuration.*



(b) *Delta configuration.*



(c) *MMC arm consisting of submodules, arm inductor, and arm resistor.*

Figure 2.1. *Single-star and delta configuration.*

2.2 MMC submodules

The MMC SMs can have various configurations, out of which the most commonly used are half-bridge (HB) or full-bridge (FB) configurations [7], presented in Fig. 2.3. The HB SM consists of the capacitor C_{SM} and two insulated gate bipolar transistor (IGBT) switches S_1 and S_2 with antiparallel diodes D_1 and D_2, as illustrated in Fig. 2.3a. It can

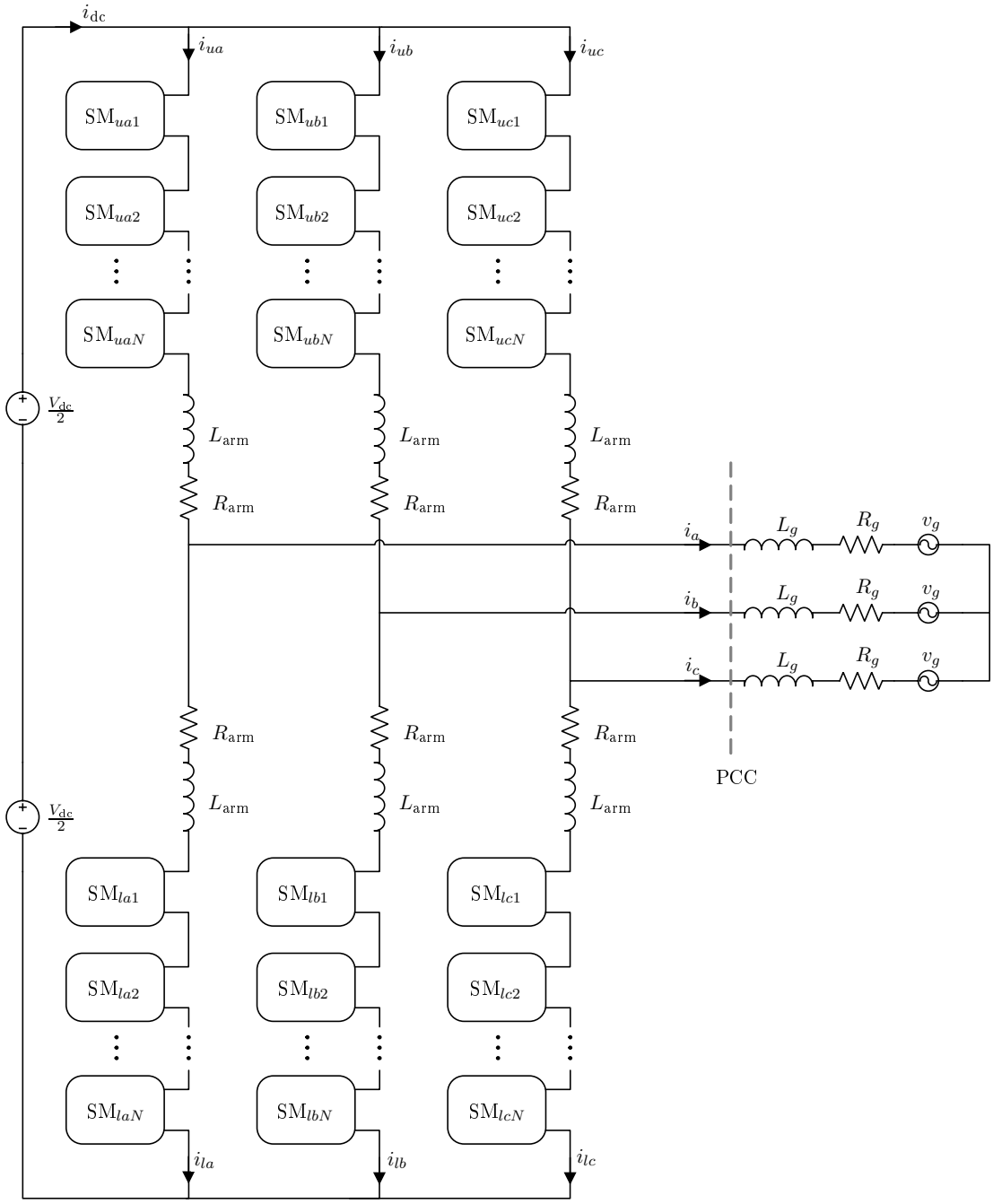
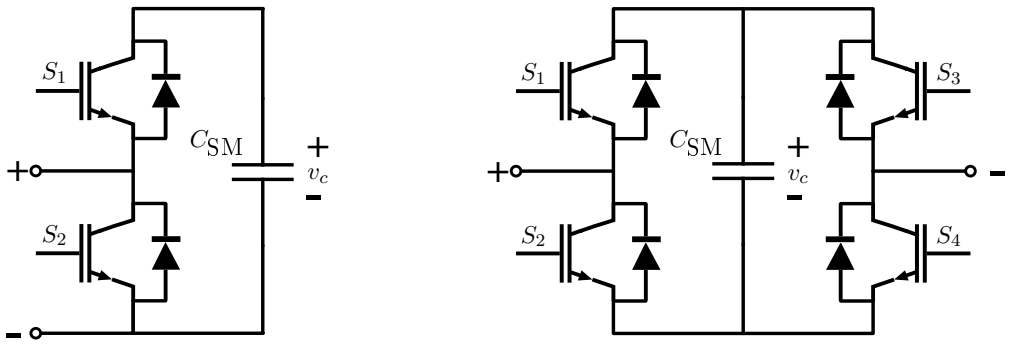


Figure 2.2. *MMC in double-star configuration.*

produce two voltage levels, 0 V or its capacitor voltage v_c. An MMC consisting of only HB SMs is known as a half-bridge MMC (HB-MMC).

As the HB SM can produce only two voltage levels, a dc component will result in the phase output voltage and thus the converter needs to be connected to a dc system to compensate for the dc component. The HB-MMC is capable of producing an arm voltage up to a sum of the capacitor voltages



(a) *Half-bridge SM.* ***(b)*** *Full-bridge SM.*

Figure 2.3. *MMC SM configurations.*

$$V_c^{\Sigma} = \sum_{i=1}^{N} v_{c,i} \,, \tag{2.1}$$

in the range of $[0, V_c^{\Sigma}]$ [8, p. 27]. With the dc component of $V_{\mathrm{dc}}/2$, the HB-MMC can produce the phase output voltage with a peak amplitude $\hat{v}_1$ of

$$\hat{v}_1 = \frac{1}{2}(V_c^{\Sigma} - |V_{\mathrm{dc}} - V_c^{\Sigma}|) \,. \tag{2.2}$$

The operating regions of the HB-MMC and the FB-MMC are presented in Fig. 2.4. It can be observed at HB-MMC is not able to produce voltage higher than V_{dc}, and thus it operates always in the buck mode.

The FB SM consists of four IGBT switches S_i and four antiparallel diodes D_i, where $i \in \{1, 2, 3, 4\}$. The switches S_1, S_2 and the diodes D_1 and D_2 form the left bridge (LB), and switches S_3, S_4 and diodes D_3 and D_4 the right bridge (RB) of the SM as presented in Fig. 2.3b. The FB SM can produce three voltage levels, 0 V or $\pm v_c$. In this thesis, an MMC consisting of full-bridge SMs (FB-MMC) is analyzed.

FB-MMC can produce the phase output voltage without the dc component even if the dc link is short-circuited. It is capable of producing the arm voltage in the range of $[-V_c^{\Sigma}, V_c^{\Sigma}]$ [8, p. 27], and peak phase output voltage of

$$\hat{v}_1 = V_c^{\Sigma} - |V_{\mathrm{dc}}| \,. \tag{2.3}$$

From Fig. 2.4 it can be observed that the FB-MMC is capable of producing twice as high output phase voltage as the HB-MMC. It can also produce a peak output voltage higher than V_{dc} and thus operate in the boost mode. The ability to operate in boost mode means that the FB-MMC can be connected to a dc link with a variable voltage and keep a

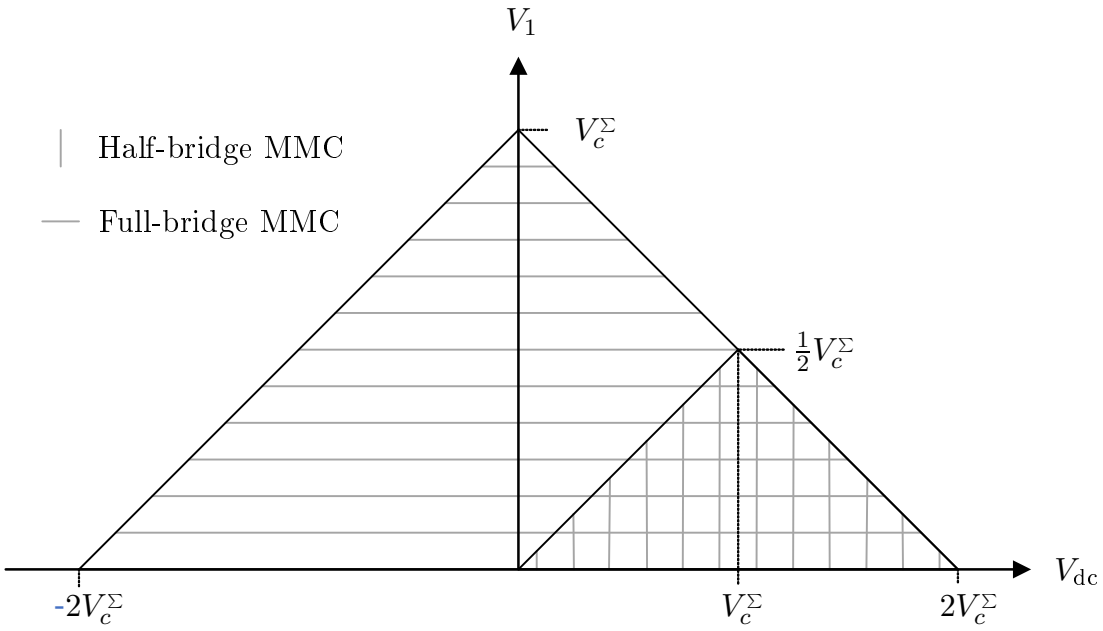


Figure 2.4. *Operation regions of HB-MMC and FB-MMC. Adopted from [8, p. 48].*

constant output voltage, even if the dc link voltage decreases. This makes it an attractive option for a grid-connected inverter connected to a renewable energy source with great voltage variations [9]. The FB-MMC is also capable of fully disconnecting the dc and the ac side by turning all the switches off, which is not possible with HB SMs.

The downside of the FB SM compared with the HB SM is the increasing number of semiconductor devices and increased power losses [3]. Semiconductor conduction losses are doubled as the current passes through two switching devices instead of one [8, p. 49]. The switching losses can on the other hand be the same for both SM configurations in some operating points. This is achieved by switching only one bridge of the FB SM and keeping the other bridge in the same state. For example, in buck mode, voltage 0 and v_c can be produced by keeping switch S_3 off, S_4 on, and changing the states of switches S_1 and S_2.

2.3 Operation principle of FB-MMC

The operation of the FB-MMC is based on inserting or bypassing SMs in the arms. The arm voltage v_{jx} can be represented as

$$v_{jx} = \sum_{i=1}^{N} s_{jxi} v_{c,jxi}, \tag{2.4}$$

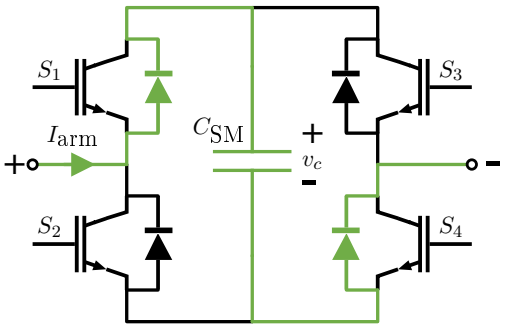
where $s_{jxi} \in \{-1, 0, 1\}$ denotes the switching state of each individual SM. Each inserted SM capacitor is charged or discharged depending on the arm current I_{arm} direction. The

Table 2.1. *SM states.*

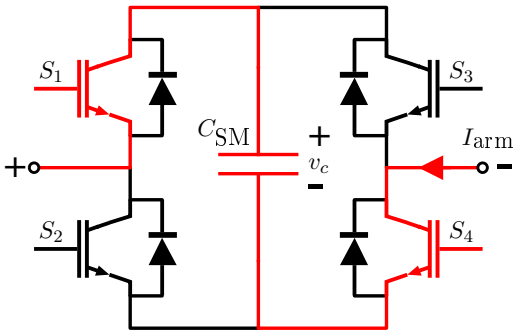
Switch position				Switching state	Voltage	SM state	
S_1	S_2	S_3	S_4			$I_{\mathrm{arm}} > 0$	$I_{\mathrm{arm}} < 0$
1	0	0	1	1	v_c	Charge	Discharge
1	0	1	0	0	0	Bypass	Bypass
0	1	0	1	0	0	Bypass	Bypass
0	1	1	0	-1	$-v_c$	Discharge	Charge

SM switching state, the output voltage, and the state of the charging are presented in Table 2.1 along with the switch positions. The switch positions 1 and 0 represent switch states on and off respectively. In addition to the switch positions presented in Table 2.1, if all the switches in one SM are turned off, the SM is in a blocking state, separating the ac from the dc side of the converter. If both switches in the LB or the RB, S_1 and S_2 or S_3 and S_4, respectively, are turned on at the same time, the SM capacitor will be short-circuited.

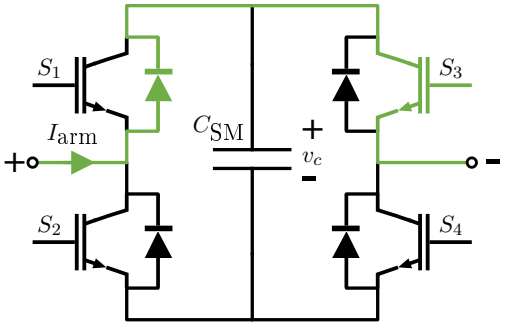
Fig. 2.5 presents the current paths in different switching states. For example, switching state 1 is presented in figures 2.5a and 2.5b, where the switches S_1 and S_4 are in on-state and the switches S_2 and S_3 are in off-state. In Fig. 2.5a a positive current flows through the antiparallel diodes of the IGBTs that are turned on and charges the capacitor. In Fig. 2.5b a negative current flows through the switches S_1 and S_4 and discharges the capacitor.



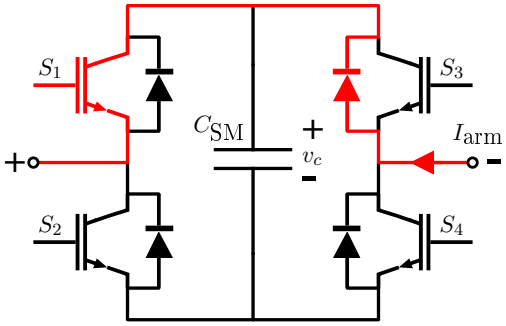
(a) *Switching state 1, switches S_1 and S_4 on, $I_{arm} > 0$.*



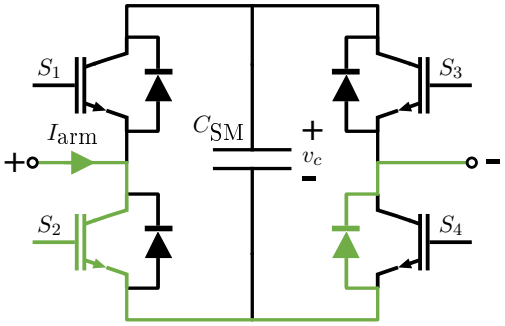
(b) *Switching state 1, switches S_1 and S_4 on, $I_{arm} < 0$.*



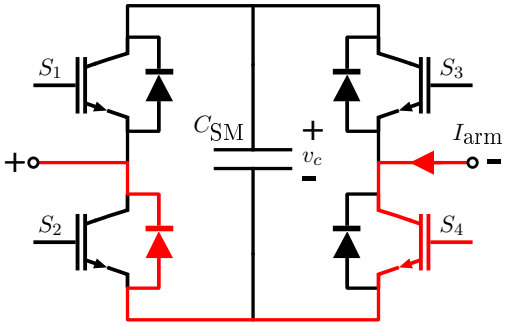
(c) *Switching state 0, switches S_1 and S_3 on, $I_{arm} > 0$*



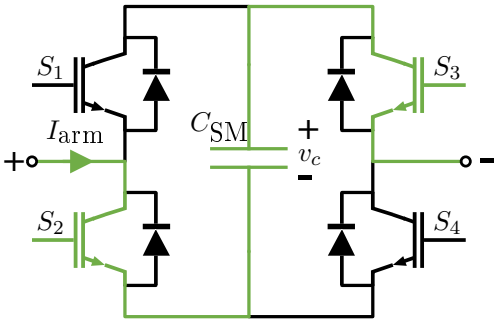
(d) *Switching state 0, switches S_1 and S_3 on, $I_{arm} < 0$*



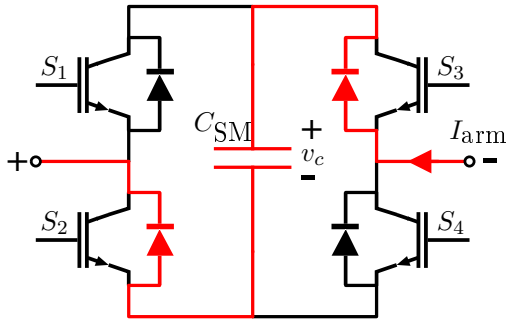
(e) *Switching state 0, switches S_2 and S_4 on, $I_{arm} > 0$*



(f) *Switching state 0, switches S_2 and S_4 on, $I_{arm} < 0$*



(g) *Switching state -1, switches S_2 and S_3 on, $I_{arm} > 0$*



(h) *Switching state -1, switches S_2 and S_3 on, $I_{arm} < 0$*

Figure 2.5. *Switching states and currents paths for FB SM*

3. MMC MODULATION

Producing the desired phase voltage requires inserting an appropriate amount of SMs in the arm. The modulation of the MMC consists of two parts: selecting the number of SMs to be inserted in the arm and selecting which SMs should be inserted. The first produces desired output voltage and the latter keeps the SM capacitor voltages balanced. In this chapter, an overview of different modulation methods for the double-star MMC is presented first. Subsequently, the operation principles of PS-PWM, PD-PWM, and NLM are introduced for HB- and FB-MMC. Last the balancing of the SM capacitor voltages is addressed.

3.1 Overview of modulation methods for MMC

Characteristics of the different modulation methods are presented in Table 3.1. These characteristics are stated for HB-MMC, but in many cases apply to FB-MMC.

The implementation effort for carrier-based methods and NLM is low, as they can easily be implemented with digital logic circuits. Implementing SVM is possible, even for a higher number of SMs, but will require complex algorithms [10]. SHE and OPPs are very hard to implement, as OPPs require solving an optimization problem and SHE a set of non-linear equations. The complexity of the problems is high and will increase as the number of SMs increases [7]. When the FB-MMC is used, there is also a great number of redundant states, that make solving the problem more complicated. This limits the suitability of these methods for a higher number of SMs. Based on implementation effort and suitability for a high number of SMs, PS-PWM, PD-PWM, and NLM are evaluated in this thesis, as the FB-MMC in STATCOM application can have tens of SMs per arm.

PS-PWM, SHE, and OPPs possess the ability for distributed modulation. This means, that the switching commands do not need to be sent from a central controller, but they can be generated in the SMs [11].

Almost all modulation methods have the ability to balance the SM voltages in the modulation stage, without voltage measurements and a dedicated voltage balancing control. PS-PWM for HB-MMC has an inherent voltage balancing ability [12]. In PD-PWM, voltage balance can be achieved by rotating carriers attached to SMs [13]. The same principle

	Implementation effort	Distributed modulation	Natural balancing	Fundamental switching frequency	Suited for a high number of SMs
PS-PWM	Low	Yes	Inherent	No	Yes
PD-WPM	Low	No	Achievable	No	Yes
NLM	Low	No	Achiavable[1]	Yes	Yes
Hybrid NLM	Low	No	No	No	Yes
SVM	High	No	Achievable	No	Yes
SHE	Very high	Yes	Achiavable[1]	Yes	No
OPPs	Very high	Yes	Achiavable[1]	Yes	No

[1] On fundamental frequency.

Table 3.1. *Characteristics of MMC modulation methods.*

can be used with SHE [14], and probably be extended to NLM and OPPs operating at the fundamental frequency. Balancing in the modulation stage can be achieved also with SVM [15].

3.2 PS-PWM

PS-PWM is a modulation technique that consists of N carriers per arm that have the same amplitude but are phase-shifted relative to each other. The carriers are compared to modulating signals, and the comparison produces switching states of the SMs and eventually the number of SMs that need to be inserted per arm. In this chapter PS-PWM for HB-MMC is first introduced and then modified to work with FB-MMC.

3.2.1 PS-PWM for HB-MMC

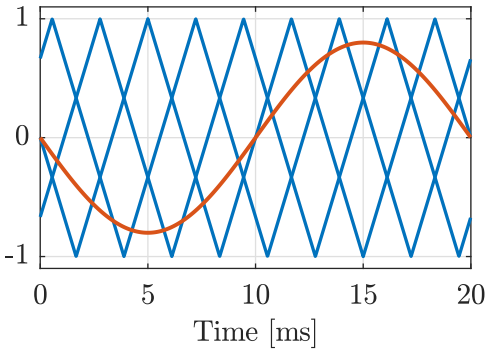
When PS-PWM is applied to the HB-MMC, the carriers are in the range of $[-1, 1]$, and phase-shifted by π/N, as presented in Figs. 3.1a and 3.1b with 3 SMs. The modulating signals for the upper and lower arms in phase x are

$$w_{\mathrm{up},x} = m \sin(\omega_g t + \pi + \theta_x) \tag{3.1a}$$

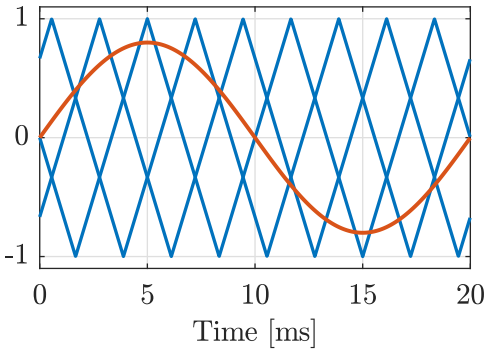
$$w_{\mathrm{low},x} = m \sin(\omega_g t + \theta_x)\,, \tag{3.1b}$$

where ω_g is is the grid angular frequency, t is the time and θ_x is the initial phase of phase x. m is a modulation index, defined as

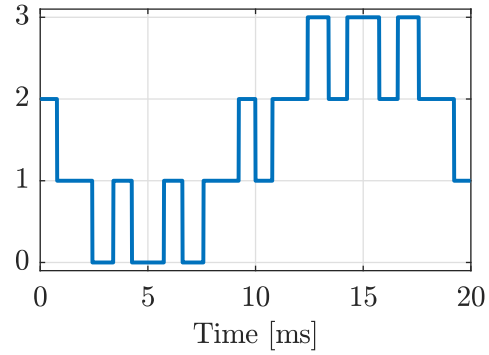
$$m = \frac{2V_{\mathrm{ref}}}{NV_c}\,, \tag{3.2}$$



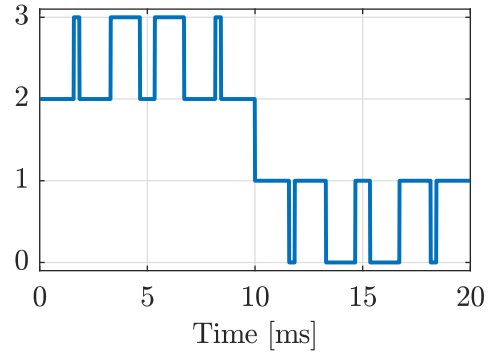
(a) *Carriers (blue) and modulating signal (red) of the upper arm.*



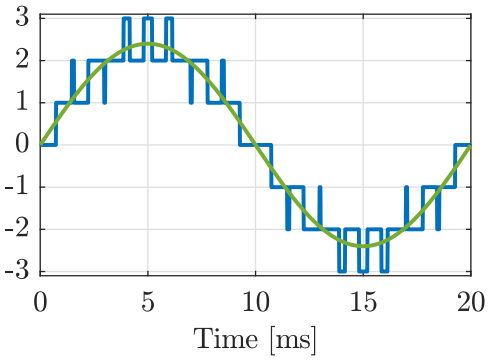
(b) *Carriers (blue) and modulating signal (red) of the lower arm.*



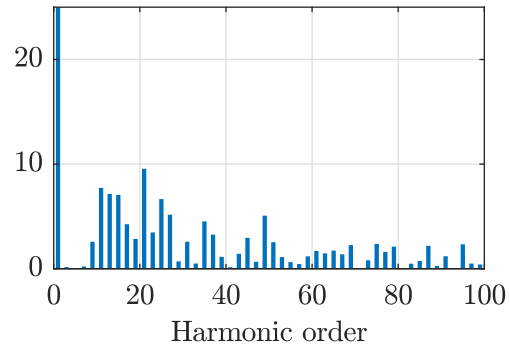
(c) *Inserted SMs in the upper arm,* n_{up}.



(d) *Inserted SMs in the lower arm* n_{low}.



(e) *Output of the PWM* n_{out} *(blue) and reference signal (green).*



(f) *Harmonic spectrum of* n_{out} *as a percentage of the fundamental component. The THD is 23.5%.*

Figure 3.1. *Operating principle of PS-PWM for HB-MMC in phase* a. $N = 3$, $m_f = 3$, $m = 0.8$, $2N + 1$ *modulation.*

where V_{ref} is the reference amplitude for the MMC phase voltage and V_c is the nominal voltage of the SM capacitor. These modulation signals can be used when the SM capacitors are charged to a voltage of V_{dc}/N. The ratio between a carrier frequency f_c and a modulating signal frequency f_1 is a carrier-to-fundamental frequency ratio

$$m_f = \frac{f_c}{f_1}\,. \tag{3.3}$$

PS-PWM can produce $N+1$ or $2N+1$ voltage levels. Increasing the number of voltage levels will decrease the output voltage harmonics and increase the apparent switching frequency of the MMC without changing the device switching frequency by much. Small changes are possible due to the phase shift of the carriers between complementary arms. To minimize the voltage harmonics [16], and achieve $2N+1$ voltage levels, the phase shift between the upper and lower arm carriers is

$$\phi_c = \begin{cases} 0, & N \text{ is odd} \\ \frac{\pi}{2N}, & N \text{ is even}\,. \end{cases} \tag{3.4}$$

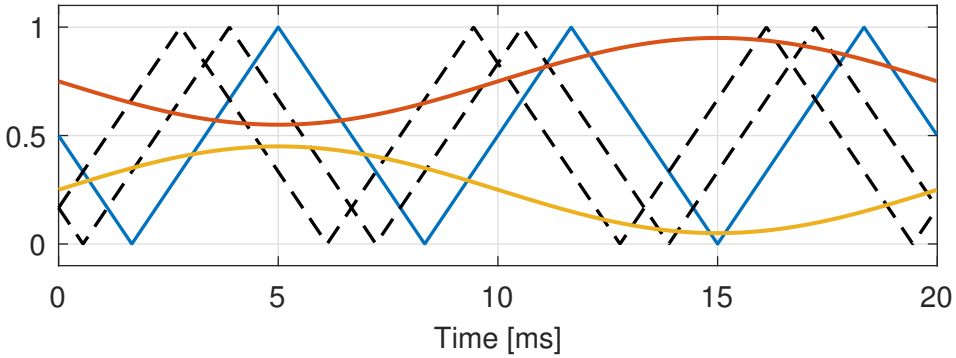
The $2N+1$ modulation is achieved by interleaving the upper and lower arm so that the pulses in the arms do not happen simultaneously. The downside of this practice is an increase in the circulating currents, due to the voltage difference between the complementary arms.

PS-PWM for the HB-MMC in phase a is depicted in Fig. 3.1, where $N=3$, $m_f=3$, and $m=0.8$. $2N+1$ modulation is used, and thus the carriers of the arms are in the same phase, as given by (3.4). Figs. 3.1a and 3.1b present the carriers and the modulating signals for the upper and lower arm, respectively. Each SM is assigned to one carrier. If the modulating signal is greater than the carrier, the SM assigned to it is inserted into the arm. When all the carriers are compared to the modulating signal, the number of inserted SMs in the arm is produced. The number of inserted SMs in the upper arm, n_{up}, and in the lower arm, n_{low}, are presented in 3.1c and 3.1d, respectively. Finally, when the pulse patterns of the arms are combined, the phase output pulse pattern can be formed by calculating $n_{\mathrm{out}} = n_{\mathrm{low}} - n_{\mathrm{up}}$. Fig. 3.1e presents the output pulse pattern with the reference signal. As $2N+1$ modulation is used, only one SM is inserted or bypassed at a time.

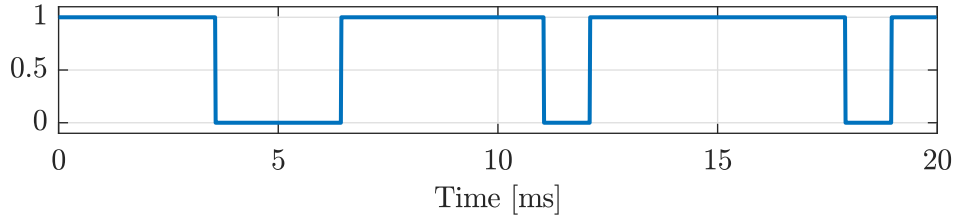
The harmonic spectrum of n_{out} is presented in Fig. 3.1f. The first carrier group can be observed around the 18th harmonic, corresponding to $2Nm_f$. The THD is 23.53%.

3.2.2 PS-PWM for a FB-MMC

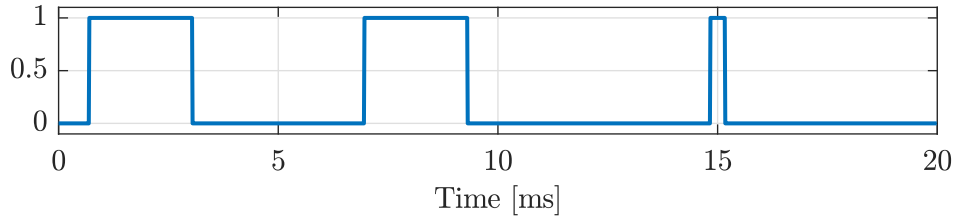
Using PS-PWM for FB-MMC requires some modifications, as the FB SM can have 3 states instead of 2, and the converter can operate in the boost mode. The number of the carriers is the same, but their value is in the range of $[0,1]$. The phase shift among the carriers in one arm is $\pi/(2N)$, as presented in Fig. 3.2a for 3 submodules in the upper arm of phase a. Instead of one modulating signal per arm, two modulating signals are needed, one for the LB and one for the RB of the FB SM. Modulating signals for the FB-MMC with a variable dc-link voltage based on a dc offset m_0 and modulation index m are presented in [17]. The dc offset is defined as



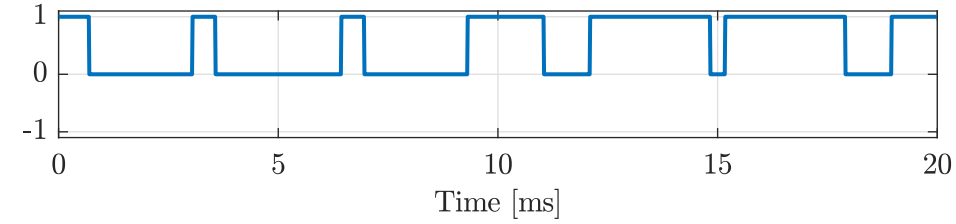
(a) *Carriers and modulating signals of the upper arm. The red modulating signal modulates the LB of the SM, and the yellow modulates the RB of the SM when they are compared to the blue carrier. Dashed carriers are assigned to other SMs.*



(b) *State of the LB.*



(c) *State of the RB.*



(d) *State of the SM.*

Figure 3.2. *Inserting and bypassing SM in the upper arm of phase a using PS-PWM for a FB-MMC. $N = 3$, $m_f = 3$, $m_0 = 1$, $m = 0.8$.*

$$m_0 = \frac{V_{\mathrm{dc}}}{NV_c}\,. \tag{3.5}$$

The converter will operate in the boost mode when $m > m_0$. If $m_0 + m > 2$, the converter operates in overmodulation. The modulating signals for the upper and lower arm SMs in

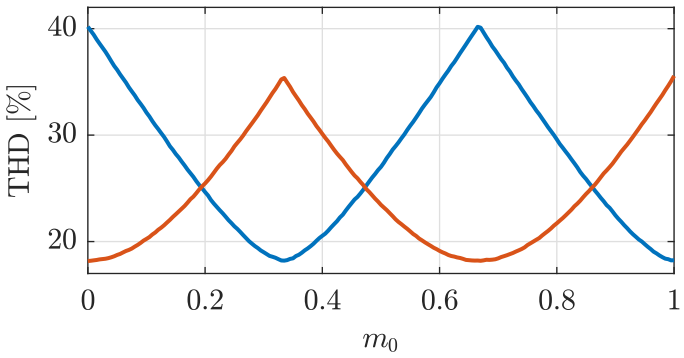


Figure 3.3. *THD of the output of PS-PWM for FB-MMC as a function of dc-offset m_0 with a phase shift of 0 (blue) and $\pi/(2N)$ (red). $N = 3$, $m = 1$.*

phase x are given by

$$w^u_{\mathrm{LB},x} = \frac{1}{2} + \frac{m_0}{4} - \frac{m}{4}\sin(\omega_g t + \theta_x) \tag{3.6a}$$

$$w^u_{\mathrm{RB},x} = \frac{1}{2} - \frac{m_0}{4} + \frac{m}{4}\sin(\omega_g t + \theta_x) \tag{3.6b}$$

$$w^l_{\mathrm{LB},x} = \frac{1}{2} + \frac{m_0}{4} + \frac{m}{4}\sin(\omega_g t + \theta_x) \tag{3.6c}$$

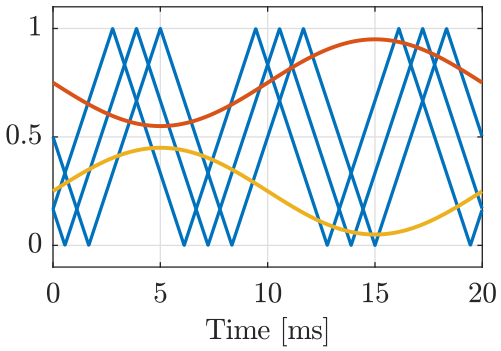
$$w^l_{\mathrm{RB},x} = \frac{1}{2} - \frac{m_0}{4} - \frac{m}{4}\sin(\omega_g t + \theta_x)\,. \tag{3.6d}$$

As with the PS-PWM for HB-MMC, the output voltage harmonics of PS-PWM for FB-MMC can be decreased by adjusting the phase shift between the carriers of the upper and lower arm. The dc-link voltage affects the THD of the PWM output when the system operates in boost mode. The effect is presented in Fig 3.3, where $N = 3$, and $m = 1$. The THD varies depending on the dc offset m_0. The blue line describes a case where the phase shift between the carriers of the complementary arms is 0 and the red one a case where it is $\pi/(2N$. [18] proposes that a phase shift of

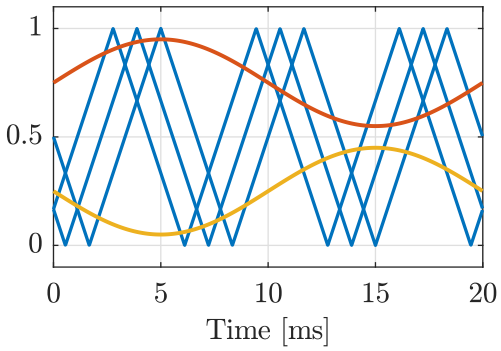
$$\phi_c = \begin{cases} 0, & \mathrm{round}(Nm_0) \text{ is odd} \\ \frac{\pi}{2N}, & \mathrm{round}(Nm_0) \text{ is even} \end{cases} \tag{3.7}$$

should be used to minimize the harmonics around the carrier frequency. This does not optimize the whole harmonic spectrum but decreases the need for harmonic filters. In buck mode ($m_0 = 1$), the phase shift given by (3.7) correspond to $2N + 1$ modulation.

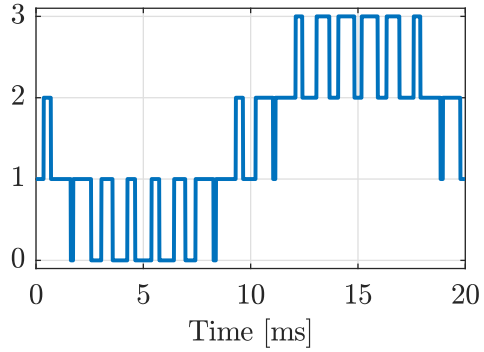
The behavior of one SM in the upper arm uf phase a is presented in Fig. 3.2, where



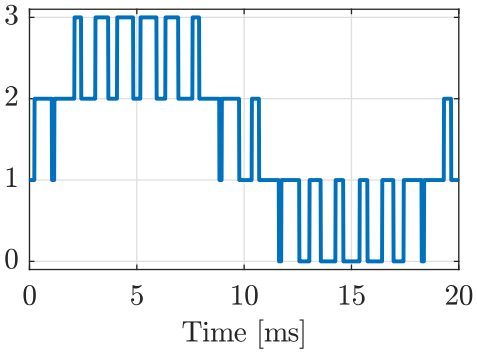
(a) *Carriers (blue) and modulating signals of the upper arm..*



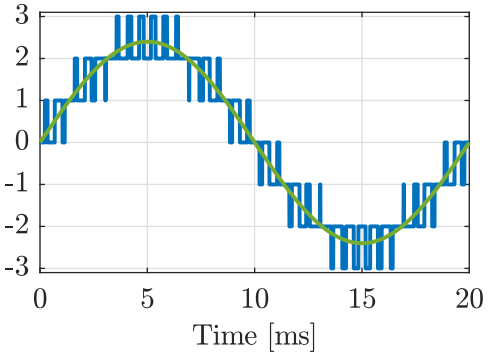
(b) *Carriers (blue) and modulating signals of the lower arm.*



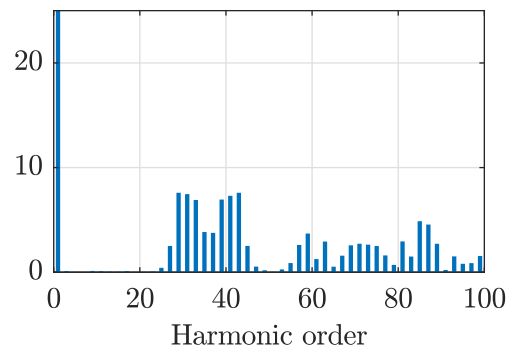
(c) *Inserted SMs in the upper arm,* n_{up}.



(d) *Inserted SMs in the lower arm,* n_{low}.



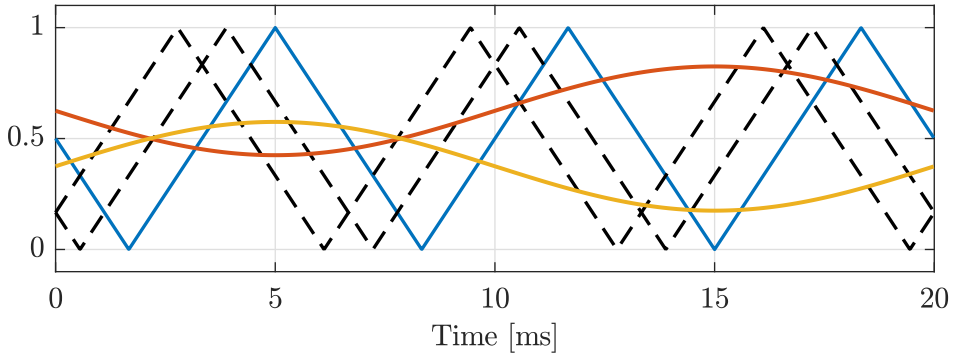
(e) *Output of the PWM* n_{out} *(blue) and reference signal (green).*



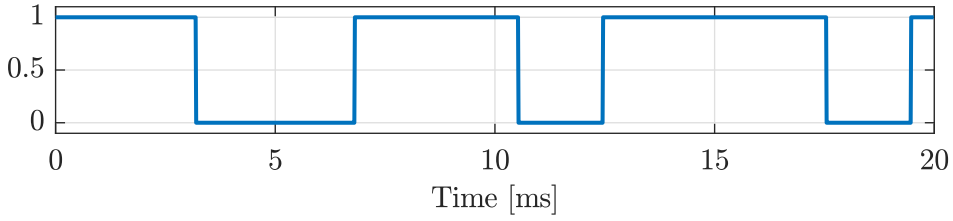
(f) *Harmonic spectrum of* n_{out} *as a percentage of the fundamental component. The THD is 24.7%.*

Figure 3.4. *Operating principle of PS-PWM for FB-MMC in phase* a. $N = 3$, $m_f = 3$, $m_0 = 1$, $m = 0.8$, $2N + 1$ *modulation.*

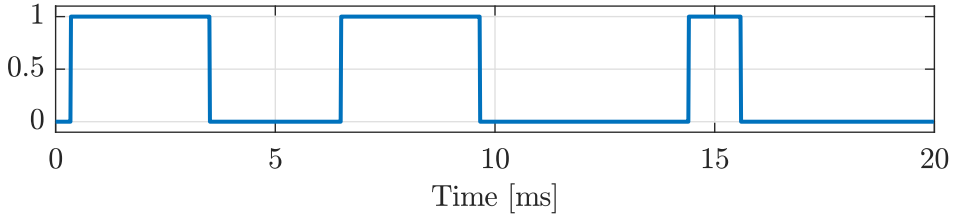
$N = 3$, $m_f = 3$, $m_0 = 1$ and $m = 0.8$. The modulating signals and the carriers for the arm of the FB-MMC are presented in Fig. 3.2a, where the blue carrier and the red modulating signal produce the state of LB of the SM assigned to the blue carrier. The state of the LB is presented in Fig. 3.2b. If the modulating signal is greater than the carrier, the state of the LB is 1, switch S_1 is on, and S_2 is off, see Fig. 2.3b. If the carrier is greater than the modulating signal, the switch positions are reversed. The same carrier and the yellow modulating signal produce the state of RB of the same SM similarly, which



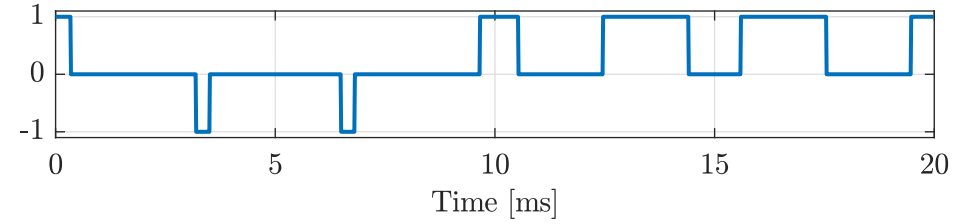
(a) *Carriers and modulating signals of the upper arm. The red modulating signal modulates the LB of the SM, and the yellow modulates the RB of the SM when they are compared to the blue carrier. Dashed carriers are assigned to other SMs.*



(b) *State of the LB.*



(c) *State of the RB.*

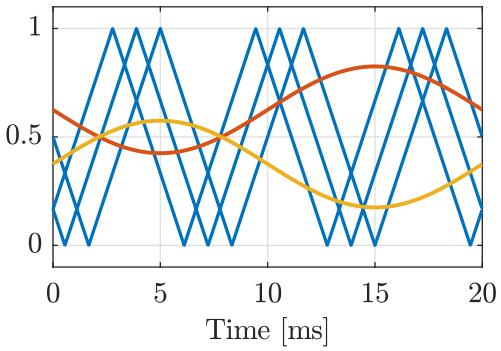


(d) *State of the SM.*

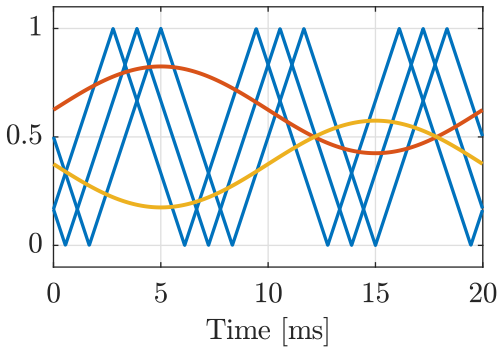
Figure 3.5. *Inserting and bypassing SM in phase a using PS-PWM for FB-MMC in boost mode. The SM is assigned to the blue carrier. $N = 3$, $m_f = 3$, $m_0 = 0.5$, $m = 0.8$.*

is presented in Fig. 3.2c. State 1 corresponds to the switch S_3 being on and S_4 off, and state 0 to switch S_3 being off and S_4 on, see Fig. 2.3b. The states of the switches form the state of the SM in Fig. 3.2d, based on Table 2.1. Gating signals for the switches can be produced directly from the modulation.

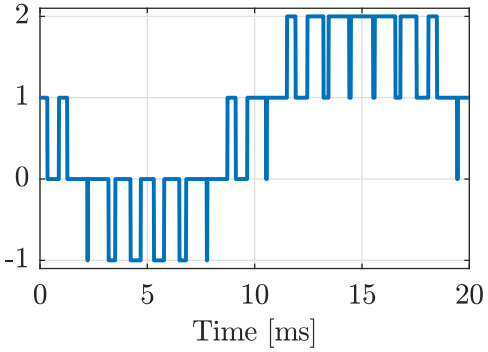
Similarly to PS-PWM for the HB-MMC, multiple carriers compared to the modulating signals will form the number of inserted submodules in the arms and the phase output pulse pattern, as presented for phase a in Fig. 3.4, where $N = 3$, $m_f = 3$, $m_0 = 1$ and



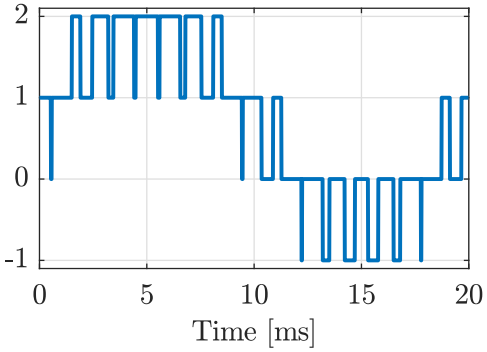
(a) *Carriers (blue) and modulating signals of the upper arm.*



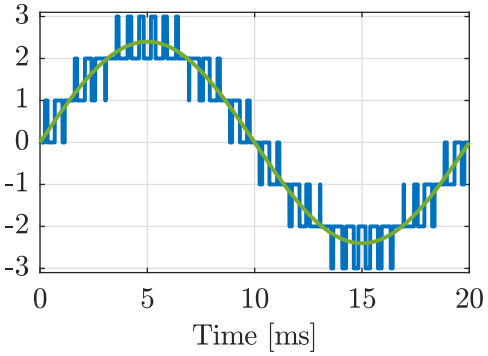
(b) *Carriers (blue) and modulating signals of the lower arm.*



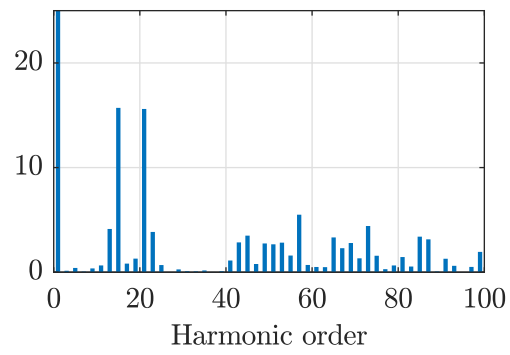
(c) *Inserted SMs in the upper arm,* n_{up}.



(d) *Inserted SMs in the lower arm,* n_{low}.



(e) *Output of the PWM* n_{out} *(blue) and reference signal (green).*



(f) *Harmonic spectrum of* n_{out} *as a percentage of the fundamental component. The THD is 28.35%.*

Figure 3.6. *Operation of PS-PWM for FB-MMC in phase* a *in boost mode.* $N = 3$, $m_f = 3$, $m_0 = 0.5$, $m = 0.8$. *Voltage harmonics minimized with* (3.7).

$m = 0.8$. The modulating signals and the carriers for the upper and lower arm are presented in Figs. 3.4a and 3.4b, respectively. The carriers in the arms are in the same phase, as the carrier phase shift is chosen based on (3.7).

The harmonic spectrum of PS-PWM output is presented in Fig. 3.4f. The first harmonic group appears close around the 36th harmonic, corresponding to $4Nm_f$. The THD is 24.7%.

The modulating signals that enable the boost mode can be calculated with (3.6). The operation of one SM in the boost mode is presented in Fig. 3.5, where $N = 3$, $m_f = 3$, $m_0 = 0.5$ and $m = 0.8$. The state of the SM can now be -1, meaning that it produces a voltage of $-v_c$. For switching states, see Table 2.1.

The operation of the converter arms of phase a in the boost mode is presented in Fig. 3.6, where $N = 3$, $m_f = 3$, $m_0 = 0.5$ and $m = 0.8$. The number of inserted SMs in the arm can be negative, as at some time instants one SM is connected in switching state -1. The SM produces the voltage of $-v_c$ and boosts the output phase voltage.

The harmonic spectrum of n_{out} is presented in 3.6f. The THD is 28.35%. The first harmonic group is now around the 18th harmonic, corresponding to $2Nm_f$.

3.3 PD-PWM

PD-PWM is a modulation method where N carriers have the same phase and amplitude, but are distributed evenly between 0 and 1. The carriers are not assigned to certain SMs.

3.3.1 PD-PWM for HB-MMC

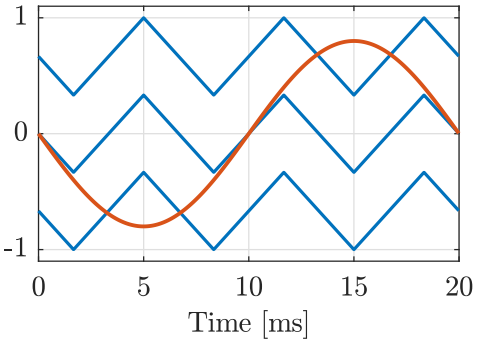
As in PS-PWM for HB-MMC, PD-PWM for HB-MMC has also two modulating signals given by (3.1). N carriers are evenly spread between -1 and 1, as presented in Figs. 3.7a and 3.7b for the upper and lower arm of phase a, respectively. The number of submodules is 3, $m_f = 3$ and $m = 0.8$.

The number of SMs inserted in the arm is resolved by comparing the modulating signal to the carriers. Each carrier that the modulating signal exceeds corresponds to an inserted SM. In Figs. 3.7a and 3.7b the blue carriers and the red modulating signal are compared and the number of inserted SMs in the upper and lower arm are produced, as presented in Figs. 3.7c and 3.7d, respectively. Combining the arms, the output of the PWM can be resolved, as presented in Fig. 3.7e. To produce $2N + 1$ voltage levels, the phase shift between the upper and lower arm should be π.

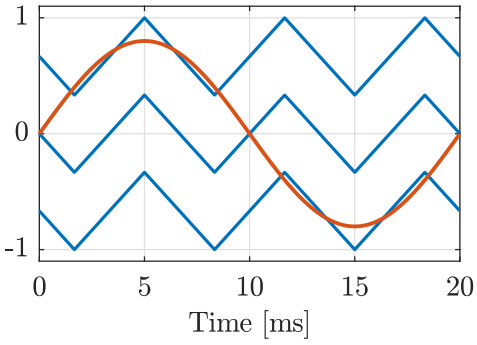
The harmonic spectrum of PD-PWM for HB-MMC is presented in Fig. 3.7f. The THD is 27.7%. The harmonics are concentrated to low frequencies because the carrier frequency is only 150 Hz, which results in a low apparent switching frequency.

3.3.2 PD-PWM for FB-MMC

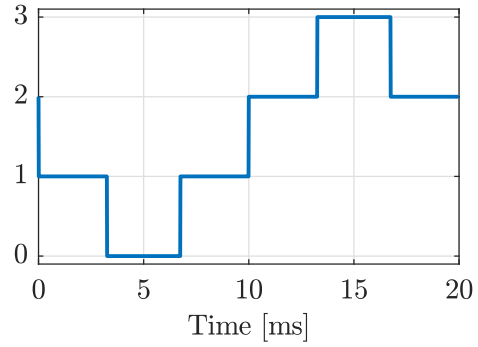
When HB SMs are changed to FB SMs the modulating signals given by (3.6) are used to allow variations in the dc link and enable the boost mode. The dc-offset m_0 will affect the phase shift between the carriers in the upper and lower arm that should be chosen.



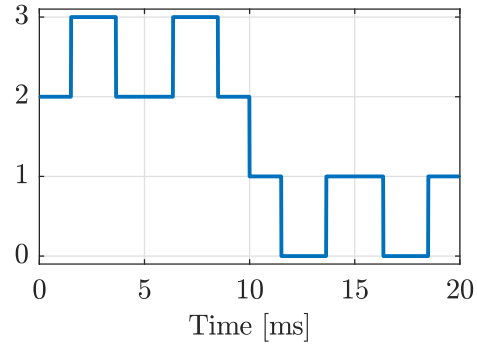
(a) *Carriers (blue) and modulating signal of the upper arm.*



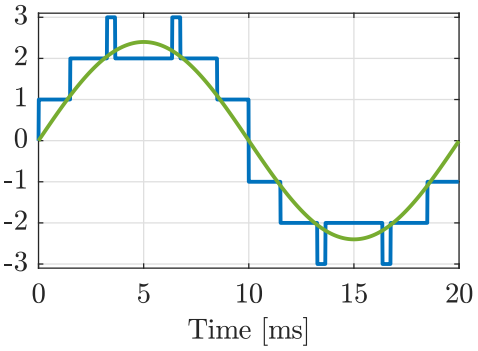
(b) *Carriers (blue) and modulating signal of the lower arm.*



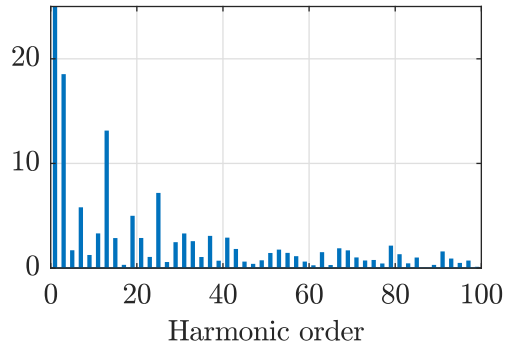
(c) *Inserted SMs in the upper arm,* n_{up}.



(d) *Inserted SMs in the lower arm,* n_{low}.



(e) *Output of the PWM* n_{out} *(blue) and reference signal (green).*



(f) *Harmonic spectrum of* n_{out} *as a percentage of the fundamental component. The THD is 27.7%.*

Figure 3.7. *Operation of PD-PWM for HB-MMC in phase* a. $N = 3$, $m_f = 3$, $m = 0.8$, $2N + 1$ *modulation.*

This is presented in Fig. 3.8, where $N = 3$, and $m = 1$. In the case of PS-PWM, when moving from HB- to FB-MMC, the phase shift was halved. The same can be applied here to FB operation. The blue line describes a case where the phase shift between arms is 0 and the red one a case where it is $\pi/2$.

As the Fig. 3.8 is similar to Fig. 3.3, (3.7) can be modified for PD-PWM to

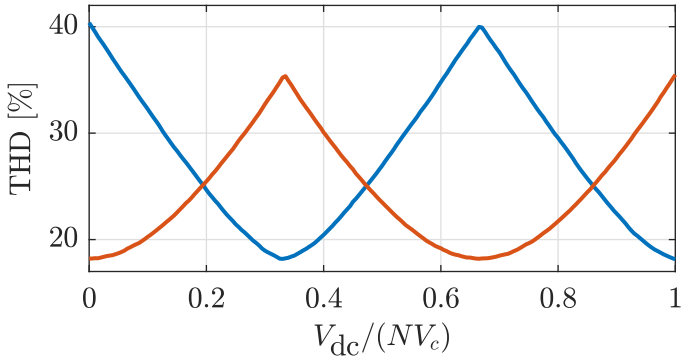
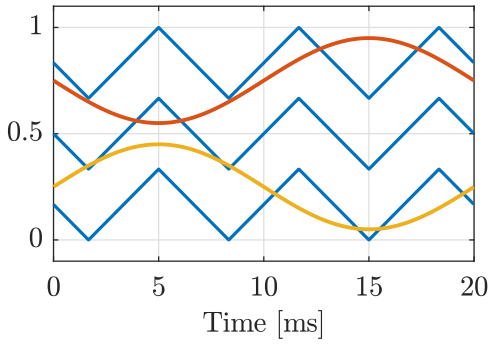


Figure 3.8. *THD of the PD-PWM output as a function of dc link voltage with a phase shift of 0 (blue) and* $\pi/2$ *(red).* $N = 3$*, and* $m = 1$*. The THD varies depending on the dc offset* m_0*.*

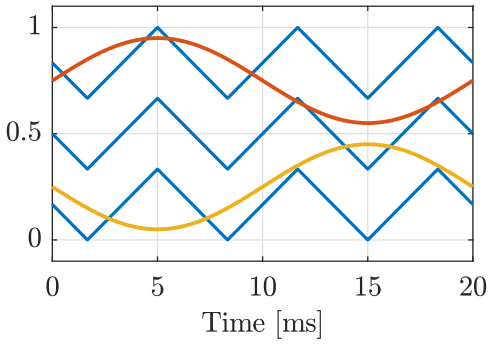
$$\phi_c = \begin{cases} 0, & \mathrm{round}(Nm_0) \text{ is odd} \\ \frac{\pi}{2}, & \mathrm{round}(Nm_0) \text{ is even}\,. \end{cases} \tag{3.8}$$

The principle of PD-PWM for FB-MMC is presented in Fig. 3.9. Figs. 3.9a and 3.9b present the modulating signals and the carriers for the upper and lower arm of phase a, respectively. The red modulating signal modulates the LBs of the arm and the yellow modulating signal modulates the RBs of the arm. The carriers in both arms are in the same phase, based on (3.8). The number of LBs and RBs is determined by counting how many carriers are below the respective modulating signal. The number of inserted LBs and RBs are presented in Figs. 3.9c and 3.9e for the upper arm and in Figs. 3.9c and 3.9e for the lower arm, respectively. The number of inserted SMs in the arm can be resolved by subtracting the number of the RBs from the number of LBs. The number of inserted SMs in the arms is presented in figures 3.9g and 3.9h. Finally, the number of inserted SMs in the phase is presented in 3.9i.

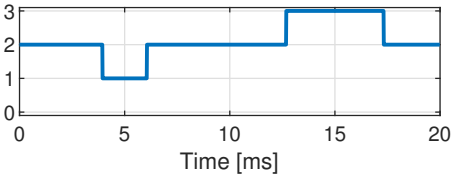
The harmonic spectrum of PD-PWM for PD-PWM is presented in Fig. 3.9j. The THD is 26.0%. The harmonics remain in the low frequencies.



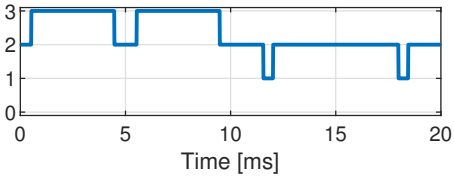
(a) *Carriers (blue) and modulating signals of the upper arm. The red modulating signal modulates the LBs and the yellow the RBs.*



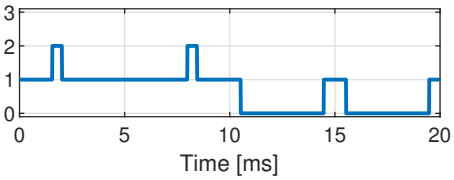
(b) *Carriers (blue) and modulating signals of the lower arm. The red modulating signal modulates the LBs and the yellow the RBs.*



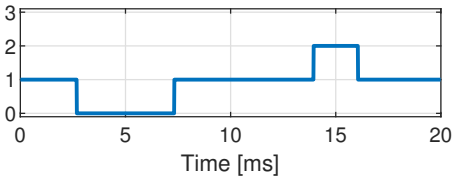
(c) *Number of inserted LBs in the upper arm.*



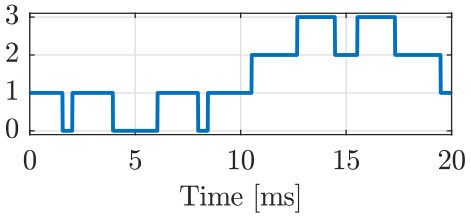
(d) *Number of inserted LBs in the lower arm.*



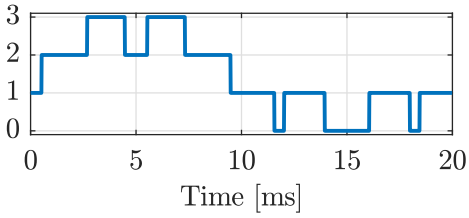
(e) *Number of inserted RBs in the upper arm.*



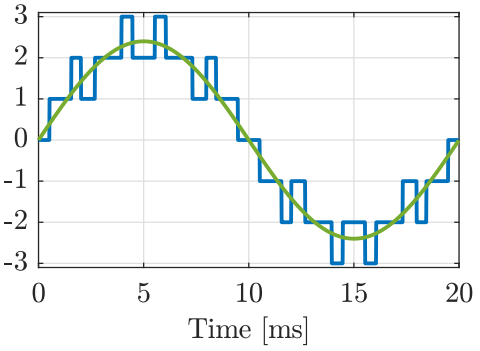
(f) *Number of inserted RBs in the lower arm.*



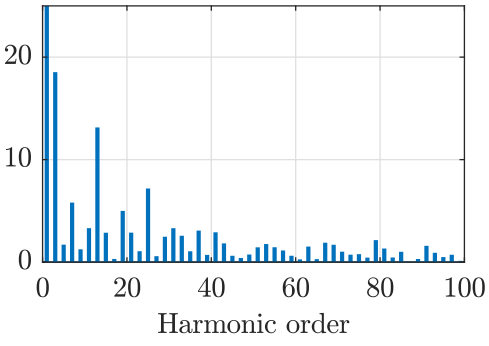
(g) *Inserted SMs in the upper arm,* n_{up}.



(h) *Inserted SMs in the lower arm,* n_{low}.



(i) *Output of the PWM* n_{out} *(blue) and reference signal (green).*



(j) *Harmonic spectrum of* n_{out} *as a percentage of the fundamental component. The THD is 26.0%.*

Figure 3.9. *Operation of PD-PWM for FB-MMC in phase* a. $N = 3$, $m_f = 3$, $m_0 = 1$, $m = 0.8$, $2N + 1$ *modulation.*

3.4 Other PD-PWM methods

By modifying the carriers in PD-PWM, different variants result. In this thesis, POD-PWM and APOD-PWM are examined. These methods adopt the principle of PD-PWM with regards to the dispositioned carriers, but with the difference that they are not in the same phase.

3.4.1 POD- and APOD-PWM for HB-MMC

The operation principle of POD- and APOD-PWM for HB-MMC, presented in Figs. 3.10 and 3.11, is the same as with PD-PWM for HB-MMC. In both examples, $N = 4$, $m_f = 3$ and $m = 0.8$. In POD-PWM, the negative carriers are phase shifted by π. In APOD-PWM every second carrier is phase shifted by π. An even number of SMs is considered, as the carriers cannot be equally divided if N is odd. The upper and lower arm carriers are phase shifted by π to create $2N + 1$ voltage levels.

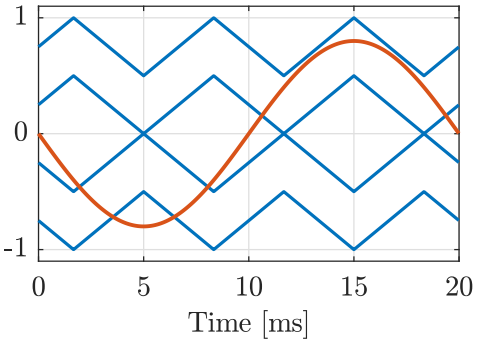
The harmonic spectra of POD- and APOD-PWM are presented in Figs. 3.10f and 3.11f, respectively. The converter output is the same for both methods and thus the spectra are the same. THD is 15%.

3.4.2 POD- and APOD-PWM for FB-MMC

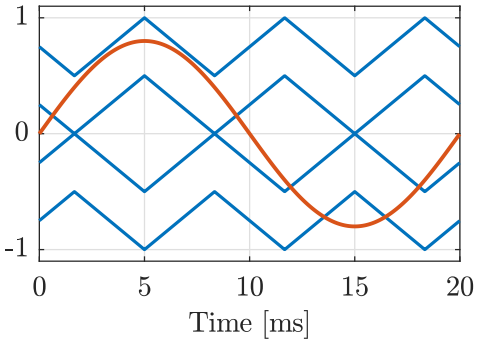
In order to modulate FB-MMC with POD- or APOD-PWM, 4 modulating signals as given by (3.6) are needed. Similar to PD-PWM, the number of LBs and RBs to be inserted is calculated based on carriers that the modulating signals exceed. This is described in Section 3.3.2. The operating principle of POD- and APOD-PWM is presented in Figs. 3.12 and 3.13 respectively, where $N = 4$, $m_f = 3$, and $m = 0.8$. An even number of SMs are used to evenly distribute the carriers between 0 and 1. The upper and lower arm carriers are phase shifted by π as with PD-PWM.

From Figs. 3.12 and 3.13 a symmetry with respect to a horizontal line crossing y-axis at 0.5 can be observed with the carriers and the modulating signals. In the figures $N = 4$, $m_f = 3$, $m_0 = 1$, and $m = 0.8$. This symmetry causes a switching event to the LB and RB simultaneously, resulting in 2 SMs being inserted or bypassed in the arm at the same time. This characteristic does not allow for the generation of $2N + 1$ voltage levels. In addition, when POD-PWM is used, the switching events in both arms happen simultaneously, resulting in four SMs being inserted or bypassed at once in a phase. Because of these characteristics, POD-PWM and APOD-PWM are not suitable options for modulating FB-MMC.

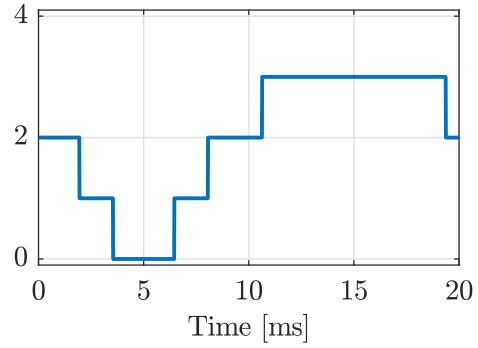
Figs. 3.12j and 3.13j present the harmonic spectra of POD- and APOD-PWM for FB-MMC, respectively. The THD of POD-PWM is 74.7% and the THD of APOD-PWM is



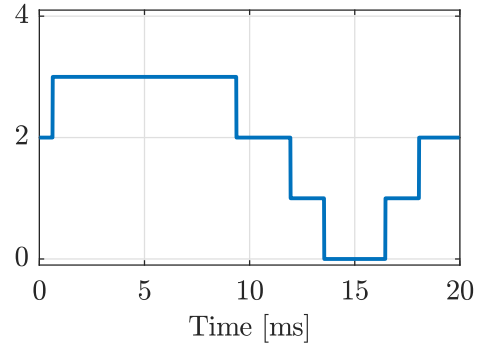
(a) *Carriers (blue) and modulating signal of the upper arm.*



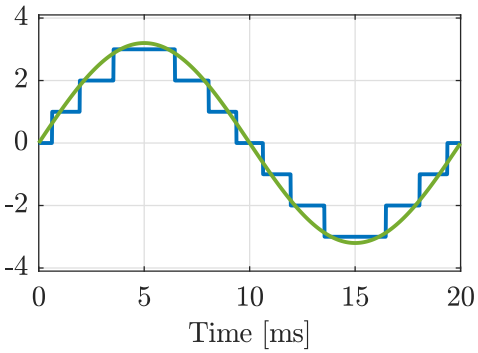
(b) *Carriers (blue) and modulating signal of the lower arm.*



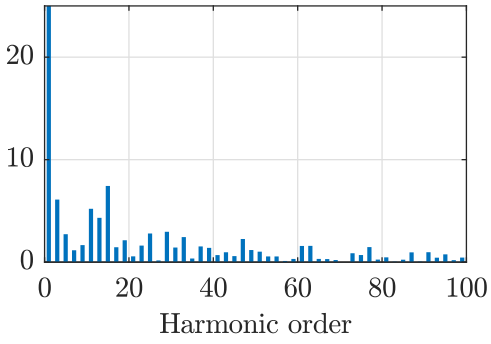
(c) *Inserted SMs in the upper arm,* n_{up}.



(d) *Inserted SMs in the lower arm,* n_{low}.



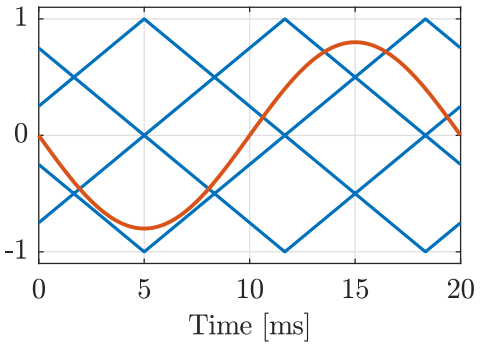
(e) *Output of the PWM* n_{out} *(blue) and reference signal (green).*



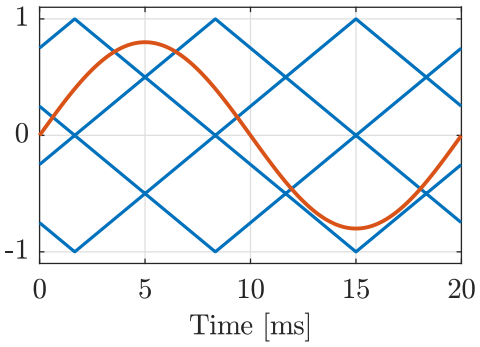
(f) *Harmonic spectrum of* n_{out} *as a percentage of the fundamental component. The THD is 15.0%.*

Figure 3.10. *Operation of POD-PWM for HB-MMC in phase* a. $N = 4$, $m_f = 3$, $m_0 = 1$, $m = 0.8$.

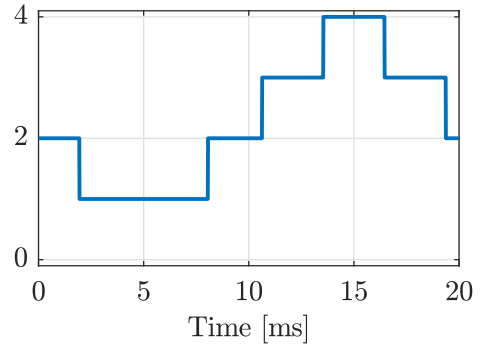
34.6%.



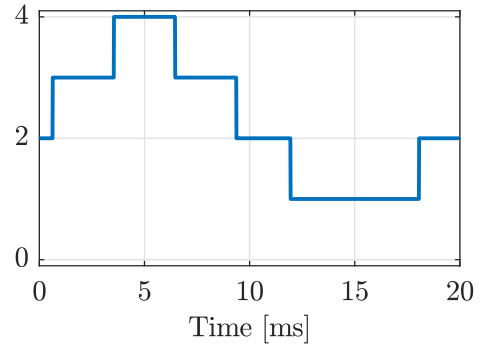
(a) *Carriers (blue) and modulating signals of the upper arm.*



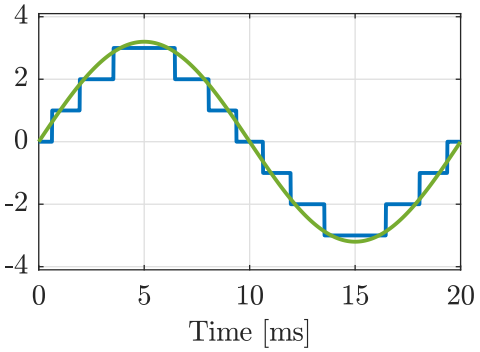
(b) *Carriers (blue) and modulating signals of the lower arm.*



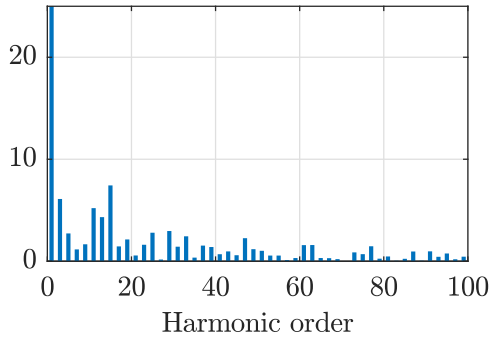
(c) *Inserted SMs in the upper arm,* n_{up}.



(d) *Inserted SMs in the lower arm,* n_{low}.

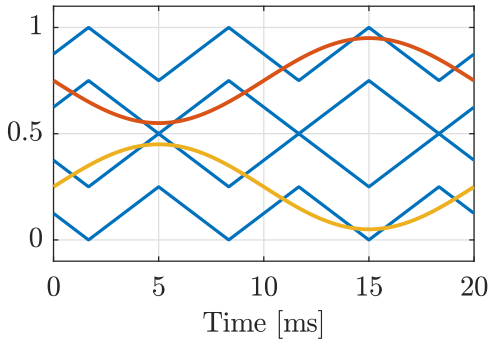


(e) *Output of the PWM* n_{out} *(blue) and reference signal (green).*

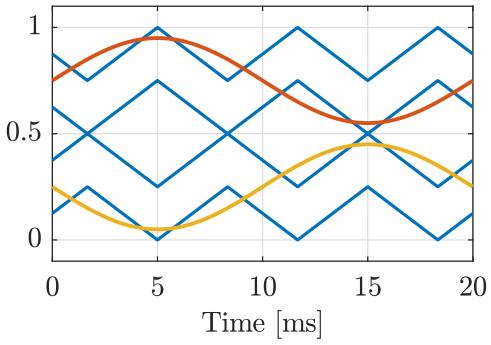


(f) *Harmonic spectrum of* n_{out} *as a percentage of the fundamental component. THD is 15.0%.*

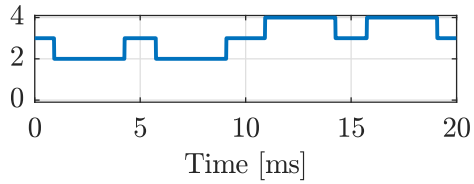
Figure 3.11. *Operation of APOD-PWM for HB-MMC in phase* a. $N = 4$, $m_f = 3$, $m = 0.8$, $2N + 1$ *modulation.*



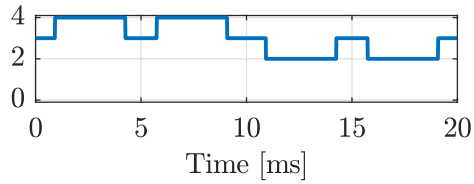
(a) *Carriers (blue) and modulating signals of the upper arm. The red modulating signal modulates the LBs and the yellow the RBs.*



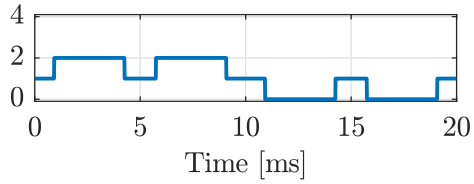
(b) *Carriers (blue) and modulating signals of the lower arm. The red modulating signal modulates the LBs and the yellow the RBs.*



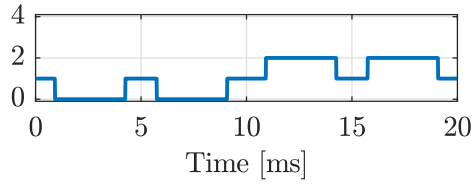
(c) *Number of inserted LBs in the upper arm.*



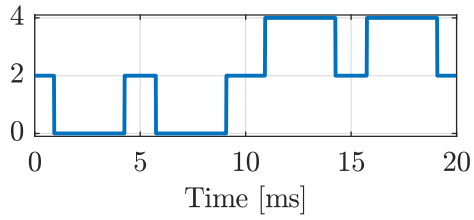
(d) *Number of inserted LBs in the lower arm.*



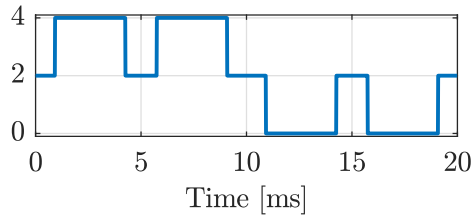
(e) *Number of inserted RBs in the upper arm.*



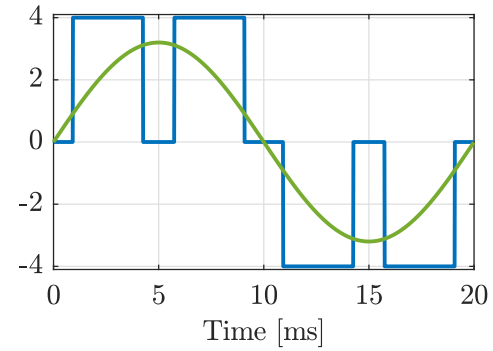
(f) *Number of inserted RBs in the lower arm.*



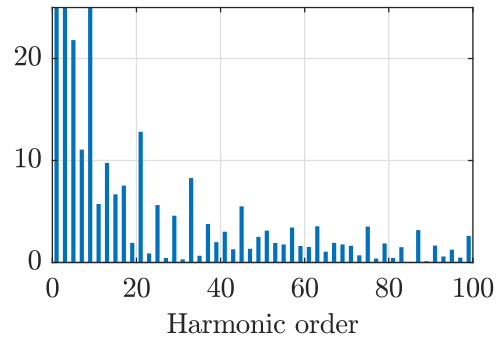
(g) *Inserted SMs in the upper arm, n_{up}.*



(h) *Inserted SMs in the lower arm, n_{low}.*

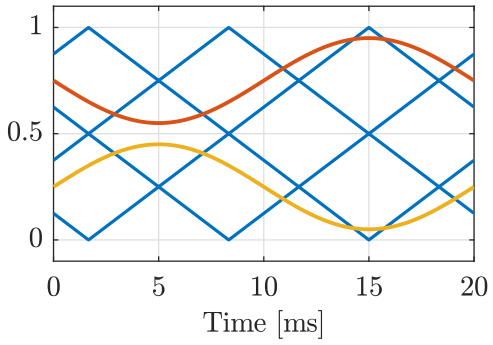


(i) *Output of the PWM n_{out} (blue) and reference signal (green).*

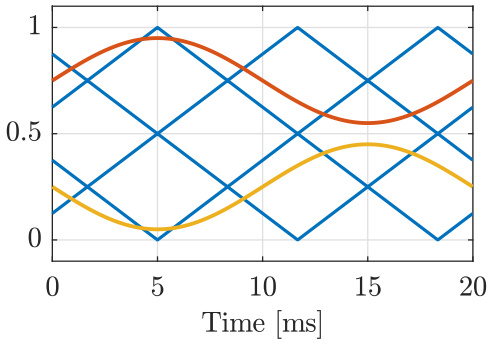


(j) *Harmonic spectrum of n_{out} as a percentage of the fundamental component. THD is 74.7%.*

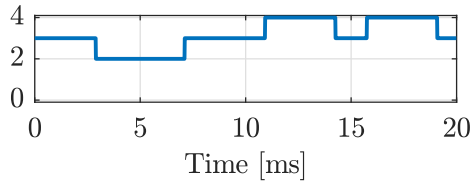
Figure 3.12. *Operation of POD-PWM for FB-MMC in phase a. $N = 4$, $m_f = 3$, $m_0 = 1$, $m = 0.8$.*



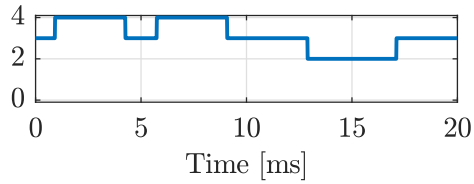
(a) *Carriers (blue) and modulating signals of the upper arm. The red modulating signal modulates the LBs and the yellow the RBs.*



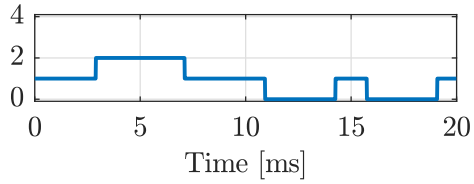
(b) *Carriers (blue) and modulating signals of the lower arm. The red modulating signal modulates the LBs and the yellow the RBs.*



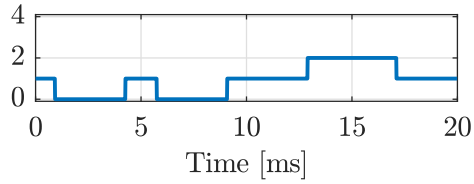
(c) *Number of inserted LBs in the upper arm.*



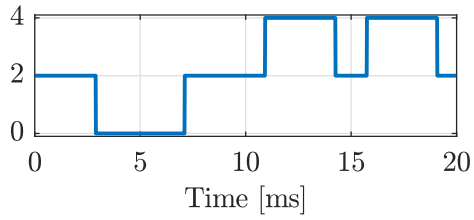
(d) *Number of inserted LBs in the lower arm.*



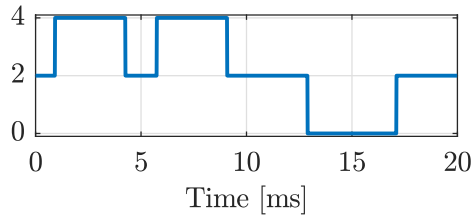
(e) *Number of inserted RBs in the upper arm.*



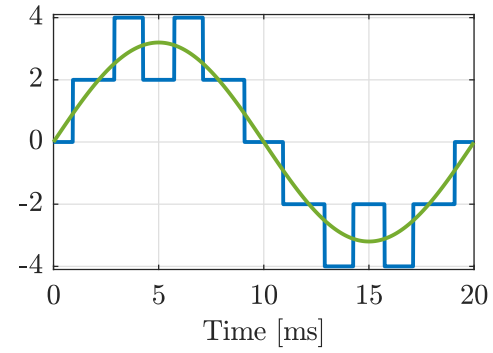
(f) *Number of inserted RBs in the lower arm.*



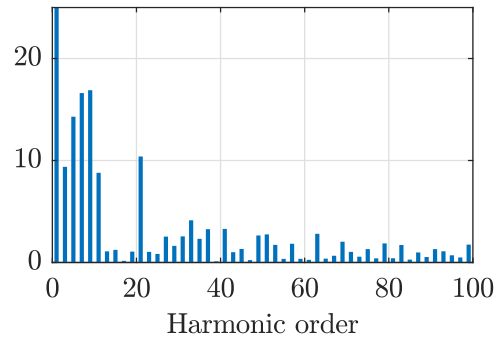
(g) *Inserted SMs in the upper arm, n_{up}.*



(h) *Inserted SMs in the lower arm, n_{low}.*



(i) *Output of the PWM n_{out} (blue) and reference signal (green).*



(j) *Harmonic spectrum of n_{out} as a percentage of the fundamental component. THD is 34.6%.*

Figure 3.13. *Operation of APOD-PWM for FB-MMC in phase a. $N = 4$, $m_f = 3$, $m_0 = 1$, $m = 0.8$.*

3.5 NLM

NLM is a modulation method that produces a staircase waveform by rounding the modulating signal. It is particularly useful for MMCs with a large number of SMs. As the current quality depends only on the SM number, it is not a suitable method for a low SM number. A downside of NLM is that it results in a tracking error due to the difference between the fundamental component of the generated waveform and the reference [8, p. 255]. The error gets smaller with a higher SM number.

3.5.1 NLM for HB-MMC

The modulating signals for NLM for HB-MMC in phase x can be presented as

$$w_{\mathrm{up},x} = \frac{1}{2}(1 - m\sin(\omega t + \theta_x))N \tag{3.9a}$$

$$w_{\mathrm{low},x} = \frac{1}{2}(1 + m\sin(\omega t + \theta_x))N\,. \tag{3.9b}$$

Using the modulation signals, the number of submodules to be inserted in the upper and lower arm of phase x can be solved as

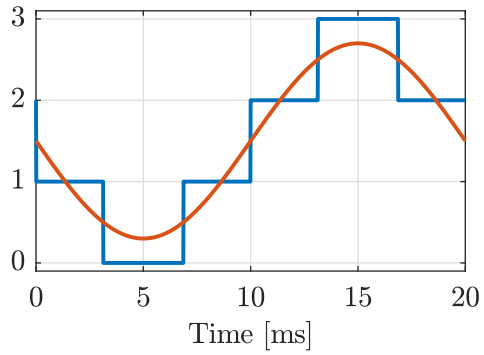
$$n_{\mathrm{up},x} = \mathrm{round}\,(w_{\mathrm{up},x}) \tag{3.10a}$$

$$n_{\mathrm{low},x} = \mathrm{round}\,(w_{\mathrm{low},x})\ . \tag{3.10b}$$

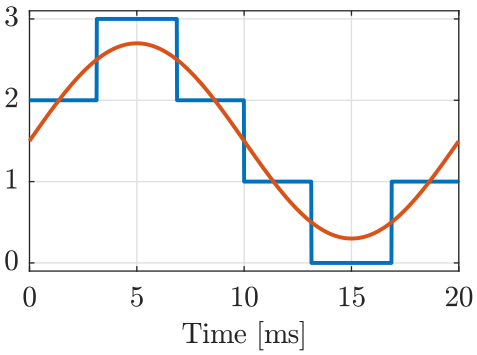
The operation of NLM with $N + 1$ voltage levels for phase a of HB-MMC is presented in Fig. 3.14, where $N = 3$ and $m = 0.8$. Red modulation signals are rounded in Figs. 3.14a and 3.14b to the nearest integer to form the number of inserted SMs in the upper and lower arm, respectively. When combined, they form the NLM output, illustrated in Fig. 3.14c. The harmonic spectrum of NLM is presented in Fig. 3.14d. No clear harmonics groups can be observed. The THD is 31.8%.

Rounding to the nearest integer will produce a maximum $N + 1$ voltage levels, as the switching events in the upper and lower arm happen simultaneously. The maximum number of voltage levels can be increased to $2N + 1$ by changing the rounding procedure [19]. The number of SMs to be inserted in the arms of phase x is now

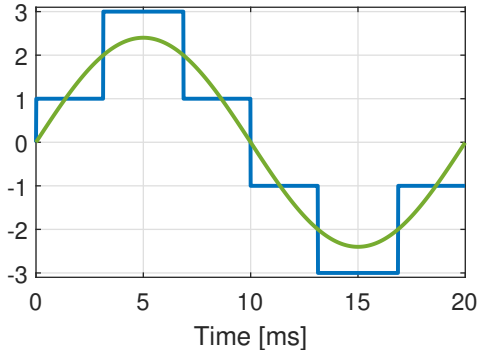
$$n_{\mathrm{up},x} = \mathrm{round}_{0.25}\,(w_{\mathrm{up},x}) \tag{3.11a}$$



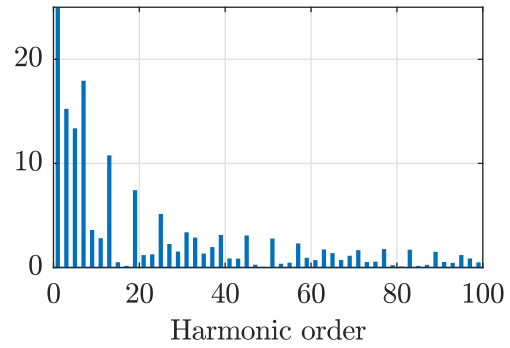
(a) *Inserted SMs in the upper arm, n_{up} (blue) and modulating signal (red).*



(b) *Inserted SMs in the lower arm, n_{low} and modulating signal (red).*



(c) *Output of NLM n_{out} (blue) and reference signal (green).*



(d) *Harmonic spectrum of n_{out} as a percentage of the fundamental component. The THD is 31.8%.*

Figure 3.14. *NLM for phase a of HB-MMC. $N = 3$, $m = 0.8$, $N + 1$ modulation.*

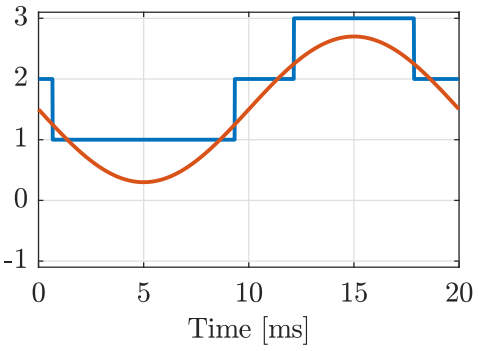
$$n_{\text{low},x} = \text{round}_{0.25}\left(w_{\text{low},x}\right) \ , \tag{3.11b}$$

where the operation $\text{round}_{0.25}()$ is defined as

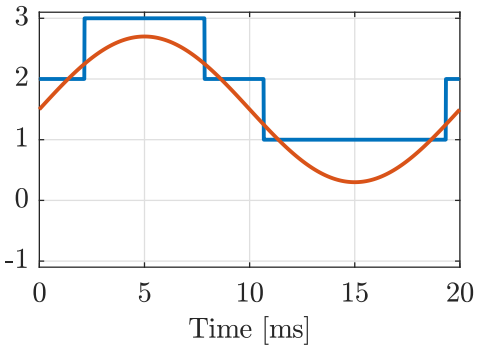
$$\text{round}_{0.25}(v) = \begin{cases} \text{floor}(v), & x < \text{floor}(v) + 0.25 \\ \text{ceil}(v), & x \geq \text{floor}(v) + 0.25 \, , \end{cases} \tag{3.12}$$

where v is the input of the function, given by (3.9). The input of the rounding function is rounded down to the nearest integer if the absolute value of the decimal fraction of the input is lower than 0.25, otherwise, it is rounded up to the nearest integer. This will cause the switching events in the complementary arms to happen at different times, increasing the voltage levels of the phase output. The operation with $2N+1$ modulation is presented in Fig. 3.15 with 3 SMs and $m = 0.8$ for phase a. The pulses in the arms do not happen simultaneously, and the NLM output has $2N + 1$ voltage levels.

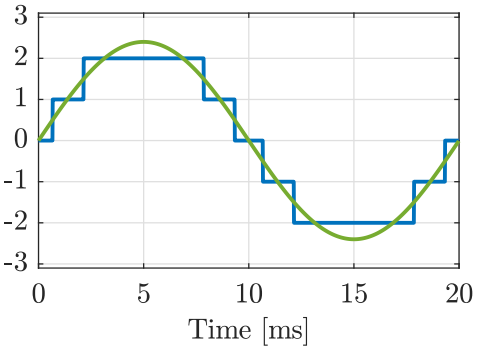
The harmonic spectrum of $2N + 1$ NLM operation is presented in Fig. 3.15d. Similar to



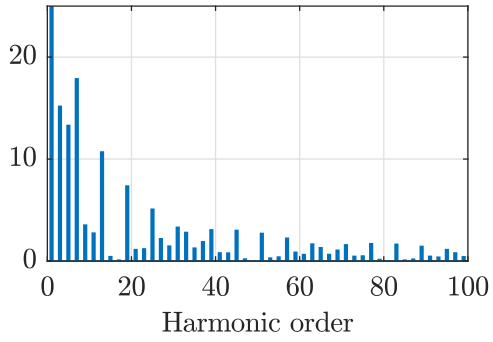
(a) *Inserted SMs in the upper arm, n_{up} and modulating signal (red).*



(b) *Inserted SMs in the lower arm, n_{low} and modulating signal (red).*



(c) *Output of NLM n_{out} (blue) and reference signal (green).*



(d) *Harmonic spectrum of n_{out} as a percentage of the fundamental component. The THD is 16.7%.*

Figure 3.15. *NLM for phase a of HB-MMC. $N = 3$, $m = 0.8$, $2N + 1$ modulation.*

$N + 1$ modulation in Fig. 3.14d, clear harmonic groups cannot be observed. The THD is 16.7%, which is a clear improvement from $N + 1$ modulation.

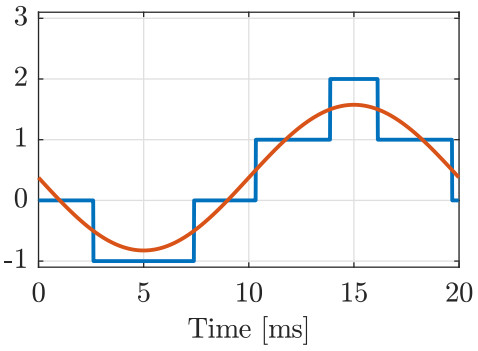
3.5.2 NLM for FB-MMC

The reference signals (3.6) can be utilized for NLM and FB-MMC. The number of inserted SMs in the upper and lower arm of phase x can be obtained by

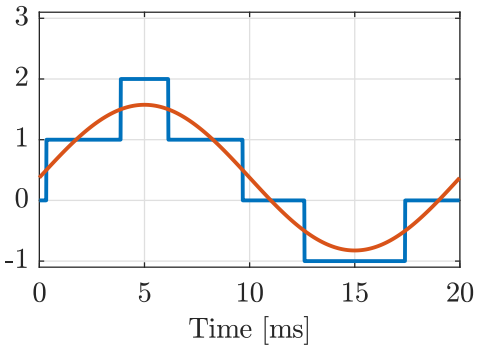
$$n_{\text{up},x} = \text{round}((w^u_{\text{LB},x} - w^u_{\text{RB},x})N) \tag{3.13a}$$

$$n_{\text{low},x} = \text{round}((w^l_{\text{LB},x} - w^l_{\text{RB},x})N)\,. \tag{3.13b}$$

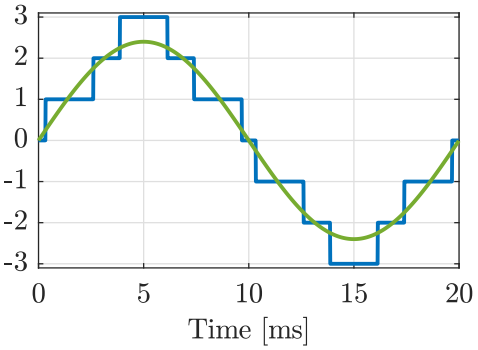
If the number of SMs to be inserted into the arm is positive, the SMs have to be in switching state 1 and produce positive voltage. If it is negative, the SMs should be inserted in switching state -1, producing a negative voltage. In the first case, the converter will operate as an HB-MMC in buck mode, producing the output presented in Fig 3.14, when



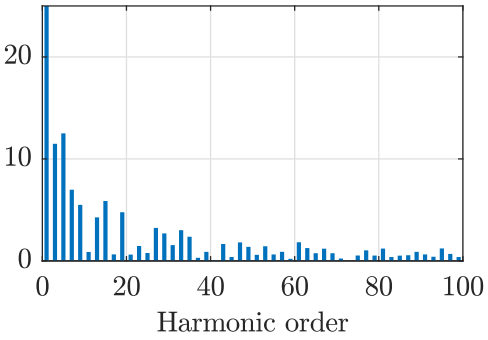
(a) *Inserted SMs in the upper arm, n_{up}.*



(b) *Inserted SMs in the lower arm, n_{low}.*



(c) *Output of NLM n_{out} (blue) and reference signal (green).*



(d) *Harmonic spectrum of n_{out} as a percentage of the fundamental component. The THD is 23.0%.*

Figure 3.16. *NLM for FB-MMC operating in phase a in boost mode with* (3.13)*. $N = 3$, $m_0 = 0.25$, $m = 0.8$.*

$N = 3$, $m_0 = 1$, and $m = 0.8$. In the latter case, the converter will operate in the boost mode.

In buck mode, $2N+1$ voltage levels can be achieved by modifying the rounding procedure. The number of inserted SMs in the arms is

$$n_{\mathrm{up},x} = \mathrm{round}_{0.25}((w^u_{\mathrm{LB},x} - w^u_{\mathrm{RB},x})N) \tag{3.14a}$$

$$n_{\mathrm{low},x} = \mathrm{round}_{0.25}((w^l_{\mathrm{LB},x} - w^l_{\mathrm{RB},x})N)\,. \tag{3.14b}$$

The output of the NLM for FB-MMC is the same as in Fig. 3.15, when $N = 3$, $m_0 = 1$, and $m = 0.8$.

The operation of NLM in phase a in the boost mode is presented in Fig. 3.16. NLM is operating with (3.13), $N = 3$, $m_0 = 0.25$ and $m = 0.8$. Although (3.13) produced $N + 1$ voltage levels in the buck mode, with given parameters in the boost mode it produces $2N + 1$ voltage levels. The dc component of the modulating signals is changed in the

boost mode, which will result in different switching waveforms in the complementary arms. In Fig. 3.16c, it can be observed that the rounding does not happen when the decimal fraction of the reference signal is 0.5, which results in an inaccurate staircase waveform. The FB-MMC can operate in boost mode with NLM, but the rounding procedure should be investigated further.

3.6 Capacitor voltage balancing

The SM capacitor voltages should be kept balanced to ensure stable operation and reduce circulating currents. The balancing can be done in two ways: the modulation stage can keep the voltages naturally balanced, or there is a dedicated voltage balancing algorithm after the modulation stage.

3.6.1 Natural balance

Some modulation methods have an inherent ability to keep the capacitor voltages balanced. The natural balancing ability of PS-PWM for HB-MMC is well known. [12] shows that the capacitor voltages stay balanced if the carrier-to-fundamental frequency ratio is chosen based on Table 3.2. The product Nm_f should be an odd or even integer depending on if N is odd or even and the used voltage levels. In addition, m_f cannot be an integer in order to achieve natural balancing.

Choosing m_f based on Table 3.2 will result in ac quantities of the converter having only odd-order harmonics. The dc side quantities will contain only even-order harmonics. Although the carrier-to-fundamental frequency ratio is not an integer, no subharmonics appear in the spectrum of the modulation output.

Voltage levels	Odd N	Even N
$N+1$	$Nm_f = \text{Odd}$	$Nm_f = \text{Even}$
$2N+1$	$Nm_f = \text{Even}$	$Nm_f = \text{Odd}$

Table 3.2. *m_f for naturally balanced HB-MMC with PS-PWM for a different number of SMs and voltage levels.*

For example, if N is 3, $2N+1$ modulation is used, and m_f should be as close to 3 as possible, the suitable m_f to achieve natural balance would be 3.333 of 2.666. The harmonic spectrum of PS-PWM with $m_f = 3.333$ is presented in Fig. 3.17. Only odd harmonics appear in the spectrum.

These results apply to HB-MMC. Simulation results of the natural balancing ability of an FB-MMC are presented in Chapter 4.

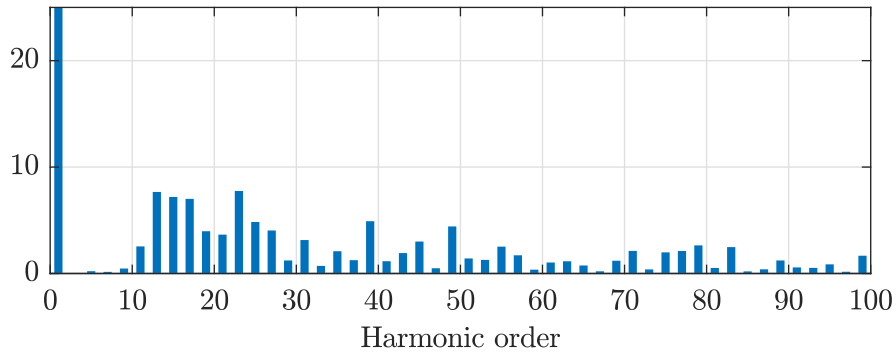


Figure 3.17. *Harmonic spectrum of PS-PWM for HB-MMC with non-integer m_f as percentage of fundamental component. The THD is 22.2%. $N = 3$, $m_f = 3.333$, $m = 0.8$, $2N + 1$ modulation.*

3.6.2 Balancing control

The balancing of the SM voltages can be achieved by using a voltage-balancing controller. Numerous types of controllers exist. The most widely used technique is a sorting algorithm. The algorithm has many variations. The first and the simplest version was introduced at the same publication as the MMC [2]. After that, the performance of the algorithm has been subject to improvement. For example, [20] divides the traditional sorting algorithm into two parts and modifies their sampling intervals in order to reduce the device switching frequency. In [21] a tolerance band method for the sorting algorithm was introduced, and [22] introduces a predictive sorting algorithm. Other balancing control techniques, for example, alter the reference signals in PS-PWM [16], estimate the arm energy [23], or rotate the carriers [13]. In this thesis, the conventional sorting algorithm, presented in [2], and a revised sorting algorithm to decrease the device switching frequency from [24] are examined.

The conventional sorting algorithm sorts the SMs based on their capacitor voltages and inserts SMs with the lowest or the highest voltage, depending on the current direction and the switching state of the SMs. The algorithm is presented in Fig. 3.18 and executed for each arm separately. The first step of the process is to compute the difference of the inserted SMs between two consecutive steps, denoted by $n_{jx,\text{diff}}$. In other words, given the number of SMs inserted in the previous step, $n_{jx,\text{old}}$, and the number of SMs require to be inserted in the current step, n_{jx}, the algorithm first computes

$$n_{jx,\text{diff}} = n_{jx} - n_{jx,\text{old}} \,. \tag{3.15}$$

If the number of SMs does not change, i.e. $n_{jx,\text{diff}} = 0$, no changes are made to the inserted SMs. Otherwise, the SMs are sorted based on their capacitor voltages.

The choice between inserting the SMs with the highest or lowest voltages is made based

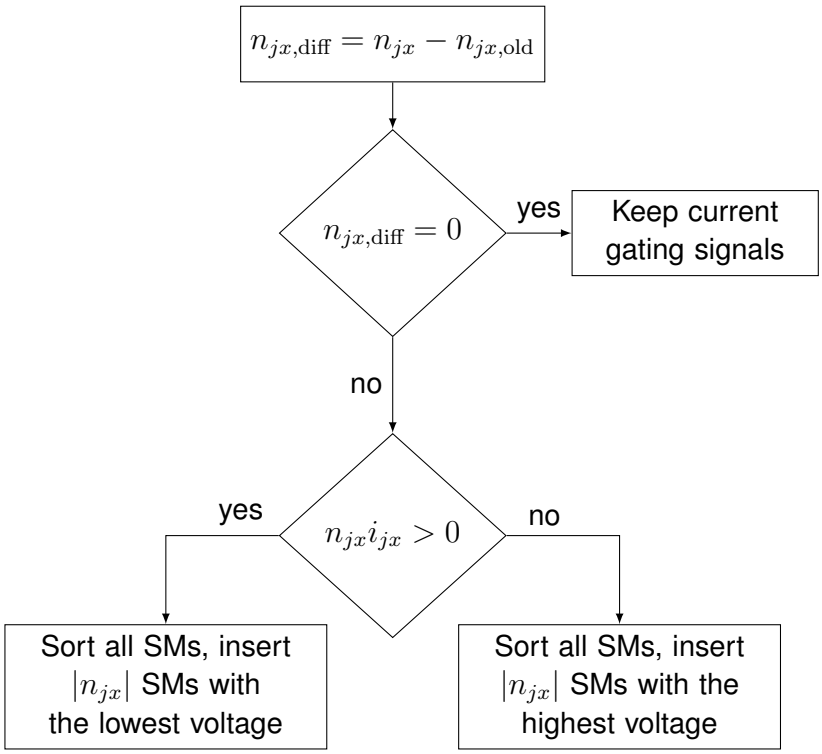


Figure 3.18. *A conventional sorting algorithm.*

on the arm current i_{jx} direction and the switching state of the inserted SMs. If n_{jx} is positive, the SMs will be in the switching state 1. Then, a positive current will charge them and therefore the SMs with the lowest voltage should be inserted. If the current is negative, SMs with the highest voltage should be discharged. In boost mode, when n_{jx} is negative and the SMs are in the switching state -1, the actions are reversed.

Although the conventional sorting algorithm will keep the voltages well balanced, it may cause unnecessary changes in SM states and increase the device switching frequency, causing more switching losses. If the modulator makes switching events repeatedly and passes them to the sorting algorithm, the algorithm will be executed at a high sampling interval. The algorithm will sort all the SMs and change the state of multiple SMs, even if it would not be strictly needed.

The modifications to the conventional sorting algorithm presented in [24] try to reduce the device switching frequency of the converter. This is achieved by making only necessary changes to the SM states. $|n_{jx,\text{diff}}|$ SMs are inserted or bypassed at a time, which reduces the device switching frequency. The revised sorting algorithm is presented in Fig. 3.19. If $n_{jx,\text{diff}}$ is positive, $|n_{jx,\text{diff}}|$ SMs need to be inserted, if it is negative, $|n_{jx,\text{diff}}|$ SMs need to be bypassed. As in the conventional sorting algorithm, the arm current i_{jx} direction and the sign of the SMs to be inserted decide if the SMs to be inserted or bypassed should be the ones with the lowest or the highest voltage. The device switching frequency will decrease, but the capacitor voltage ripple may increase as fewer SM states are changed per execution.

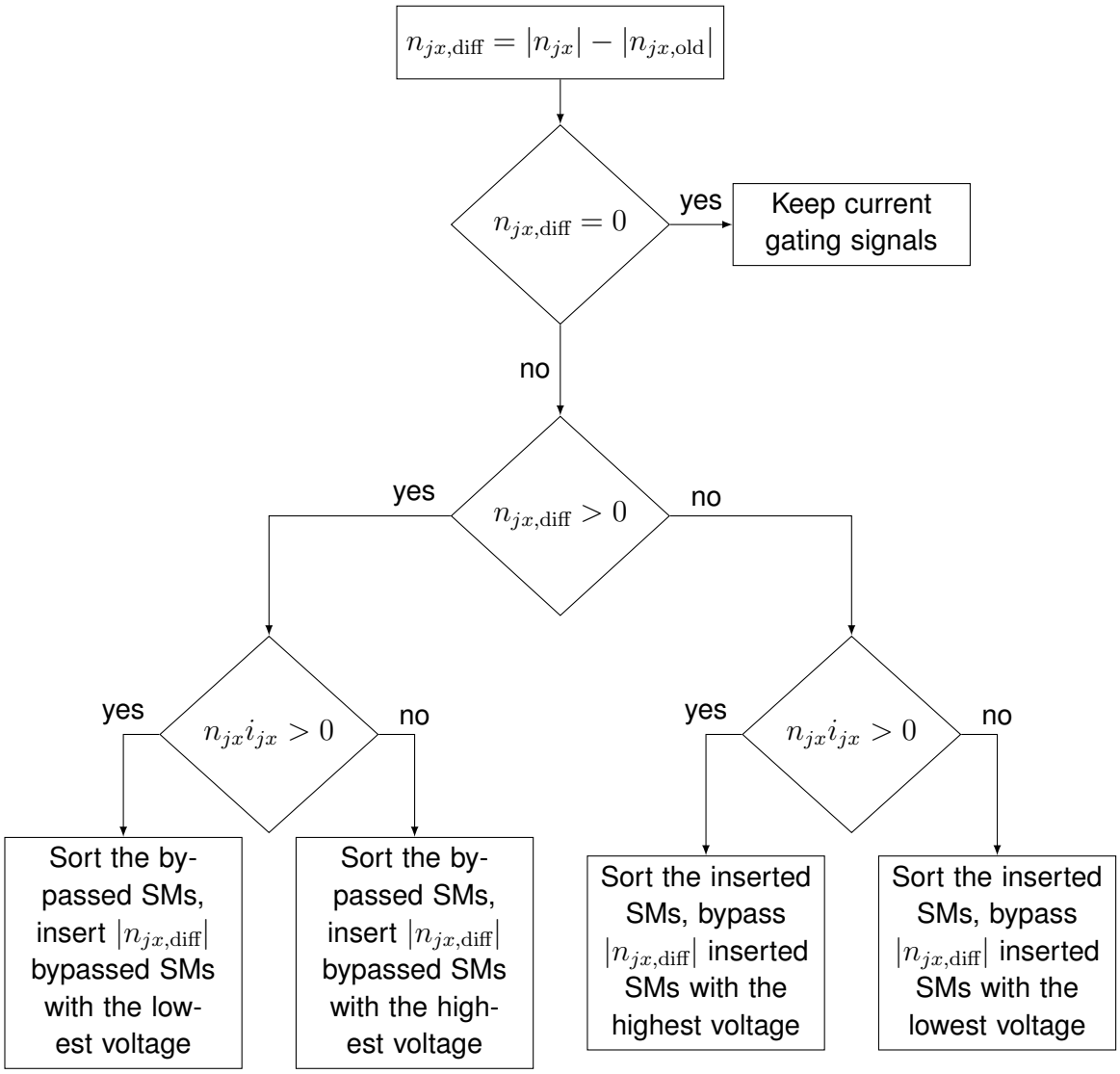
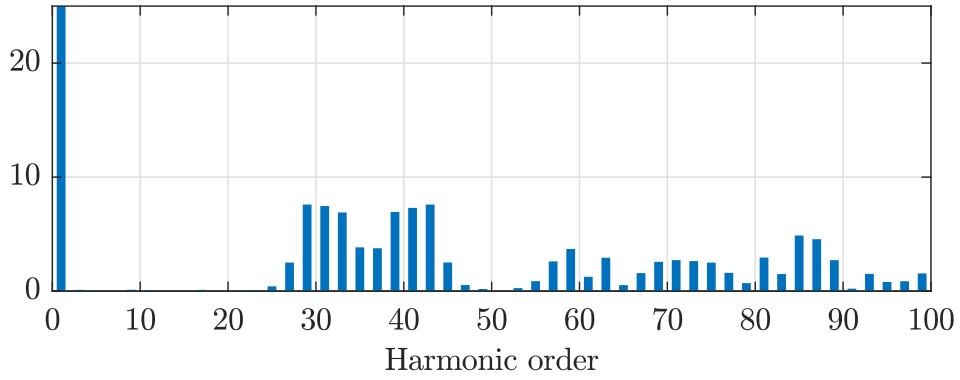
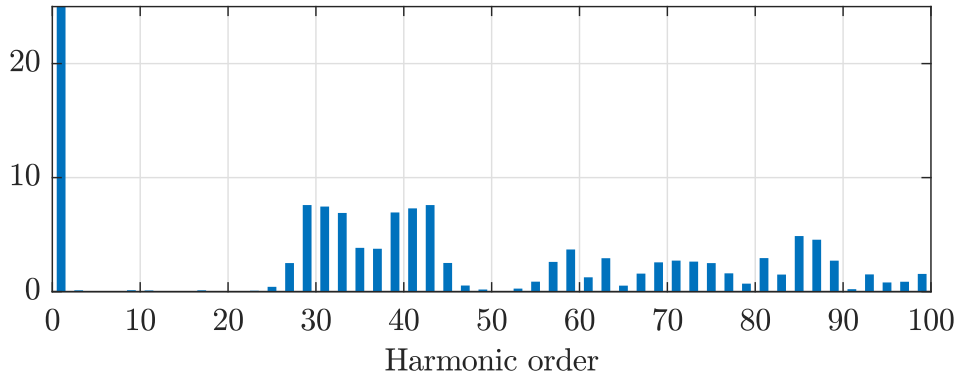


Figure 3.19. *A revised sorting algorithm to reduce the device switching frequency.*

The harmonic spectra of sorting algorithms are presented in Fig. 3.20. PS-PWM with 3 SMs and m_f of 3 is used. $m = 0 = 1$, $m = 0.8$ and $2N + 1$ modulation is used. The spectrum of both algorithms is the same as the spectra of the PS-PWM output in Fig. 3.4f. The sorting algorithm does not change the switching events in the phase output.



(a) *Conventional sorting algorithm.*



(b) *Revised sorting algorithm.*

Figure 3.20. *Harmonic spectra of PS-PWM FB-MMC with a sorting algorithm as a percentage of fundamental component. THD is 24.7%.* $N = 3$, $m_f = 3$, $m_0 = 1$, $m = 0.8$, $2N + 1$ *modulation.*

4. PERFORMANCE ASSESMENT

The performance of the different modulation methods is evaluated based on their output current quality, apparent switching frequency, device switching frequency, and circulating currents. The evaluation is done using Mathworks' Matlab and Simulink softwares. First, the evaluation metrics are presented. Subsequently, the simulation model is described more in detail. Last, the performance of the modulation methods is presented and evaluated.

4.1 Evaluation metrics

The MMC should produce a current as close to sinusoidal as possible. The quality of the produced current can be evaluated by calculating the THD or the total demand distortion (TDD) of the current. The THD is defined as

$$I_{\mathrm{THD}} = \frac{1}{\hat{I}_1}\sqrt{\sum_{k\neq 1}^{K} \hat{I_n}^2}, \tag{4.1}$$

where $\hat{I}_1$ is the amplitude of the fundamental component of the current. $\hat{I}_n$ is the amplitude of nth harmonic. The TDD is defined as

$$I_{\mathrm{TDD}} = \frac{1}{I_R}\sqrt{\sum_{k\neq 1}^{K} \hat{I_n}^2}, \tag{4.2}$$

where $\hat{I}_R$ is the rated current of the converter. Using the TDD is recommended, as THD can produce a high I_{THD} value if $\hat{I}_1$ is small when operating on a light load [25]. This makes I_{THD} appear to approach infinity, although the harmonic currents can be relatively small.

The limits for the harmonic content of the current at the PCC are set by the IEEE-519 standard [26]. The standard sets limits for the odd and even current harmonics separately. Subharmonics should be limited to sufficiently low levels. The harmonic limits for a system rated from 120 V to 69 kV are presented in Table 4.1. The limits depend on the short circuit

Table 4.1. *IEEE-519-2014 current distortion limits as a percentage of rated current for a system rated 120 V to 69 kV.*

harmonic order		Distortion limit [%]
$2 \leq h < 11$	odd	4
	even	1
$11 \leq h < 17$	odd	2
	even	0.5
$17 \leq h < 23$	odd	1.5
	even	0.38
$23 \leq h < 35$	odd	0.6
	even	0.15
$35 \leq$	odd	0.3
	even	0.08

current at the point of common coupling. The tightest limits are presented, as the short circuit current is not determined in this thesis.

A ripple in the SM voltages causes a voltage difference between the upper and lower phase leg, which leads to circulating currents. The voltage difference can result also from $2N + 1$ modulation, as the upper and lower arm do not have the same number of SMs connected at all times. The circulating currents do not affect the phase output voltage or the current, but increase the currents in the converter arms, resulting in increased power losses [3]. The circulating current i_{circ} in phase x can be calculated as

$$i_{\mathrm{circ},x} = \frac{i_{ux} - i_{lx}}{2} - \frac{i_{\mathrm{dc}}}{3}\,, \tag{4.3}$$

where i_{ux} and i_{lx} are the current in the upper and lower arm of the phase x, respectively. i_{dc} is the dc-link current, see Fig. 2.2. The modulation methods are evaluated based on the peak-to-peak circulating current in steady-state operation.

Two switching frequencies can be defined for the converter. The device switching frequency $f_{\mathrm{sw,dev}}$ describes the frequency at which a single switching device is operating. The device switching frequency can be calculated as

$$f_{\mathrm{sw,dev}} = \lim_{K\to\infty} \frac{1}{hKT_s} \sum_{l=0}^{K-1} ||\Delta \boldsymbol{g}(l)||_1\,, \tag{4.4}$$

where T_s is the sampling interval, h is the number of semiconductor devices in the converter. $\Delta \boldsymbol{g}(l) = \boldsymbol{g}(l) - \boldsymbol{g}(l-1)$, where $\boldsymbol{g}$ is the gating signals of the converter. Two consecutive switching events form a pulse and thus the sum of the switching events has

Parameter	Symbol	Definition	Base value
Voltage	V_B	$\sqrt{\frac{2}{3}}V_R$	12.25 kV
Current	I_B	$\sqrt{2}I_R$	1.41 kA
Frequency	ω_B	$2\pi f_g$	314.16 $1/\text{s}$
Impedance	Z_B	$\frac{V_B}{I_B}$	8.66 Ω
Capacitance	C_B	$\frac{1}{\omega_B Z_B}$	367.55 µF
Inductance	L_B	$\frac{Z_B}{\omega_B}$	27.60 mH

Table 4.2. *Per unit system.*

to be divided by 2.

The apparent switching frequency presents the switching frequency of the converter output in one phase. It can be presented as

$$f_{\text{sw,app}} = \lim_{K\to\infty} \frac{1}{6cKT_s} \sum_{l=0}^{K-1} ||\Delta \boldsymbol{n}_{\text{out}}(l)||_1 \,, \tag{4.5}$$

where $\Delta \boldsymbol{n}_{\text{out}}(l) = \boldsymbol{n}_{\text{out}}(l) - \boldsymbol{n}_{\text{out}}(l-1)$. $\boldsymbol{n}_{\text{out}}$ is $\begin{bmatrix} n_{\text{out,a}} & n_{\text{out,b}} & n_{\text{out,c}} \end{bmatrix}^T$. c is a correction factor that is 2 when $N+1$ modulation is used and 1 when $2N+1$ modulation is used. As with device switching frequency, to count the pulses, the sum of switching events has to be divided by three. Additionally, as all 3 phases are taken into account, the sum has to be divided by 3.

4.2 Simulation enviroment

The performance of modulation methods is evaluated based on simulations in steady-state operation. The system operates in an open loop, meaning that no controllers are used. All simulations are done with a constant V_{ref} of 0.9 per unit (p.u.), which is fed straight to the modulator. The modulator produces the number of SMs to be inserted, which is forwarded to the voltage balancing algorithm, using one of the algorithms presented in Section 3.6.2. When PS-PWM is used, the balancing can be bypassed and the switching commands produced directly in the modulator. The MMC is connected to a dc voltage source with a constant voltage.

The simulation results are stated in per unit system, presented in Table 4.2. The base values are denoted with the subscript B and the rated values with the subscript R. The values of the system parameters are presented in Table 4.3.

Parameter	Symbol	SI value	Per unit value
Rated voltage	V_R	15 kV	1.22
Rated current	I_R	1000 A	$7.07 \cdot 10^{-1}$
Grid frequency	f_g	50 Hz	$1.59 \cdot 10^{-1}$
Dc link voltage	V_{dc}	26.4 kV	2.16
Arm resistance	R_{arm}	0.1 Ω	$1.15 \cdot 10^{-2}$
Arm inductance	L_{arm}	4.8 mH	$1.74 \cdot 10^{-1}$
SM capacitance	C_{SM}	22.7 mF	$6.18 \cdot 10^{1}$
SM number	N	12	

Table 4.3. *Simulation parameters.*

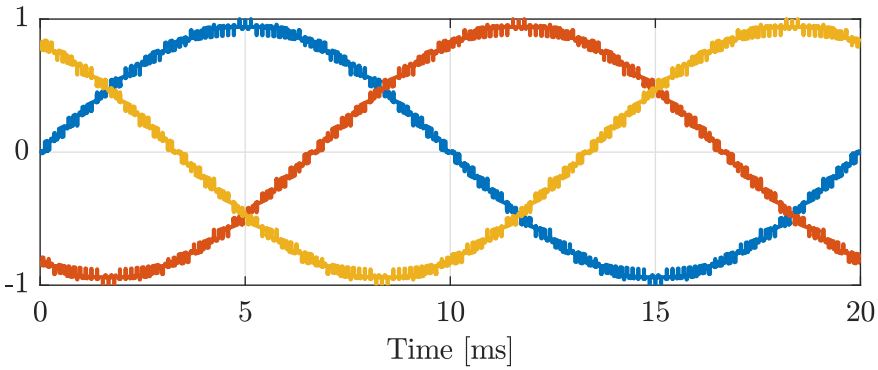


Figure 4.1. *Three-phase grid voltages in steady-state PS-PWM operation. Blue, red, and yellow colors correspond the phases a, b, and c respectively.* $N = 12$, $m_f = 3$, $V_{ref} = 0.9$ *p.u.,* $2N + 1$ *modulation.*

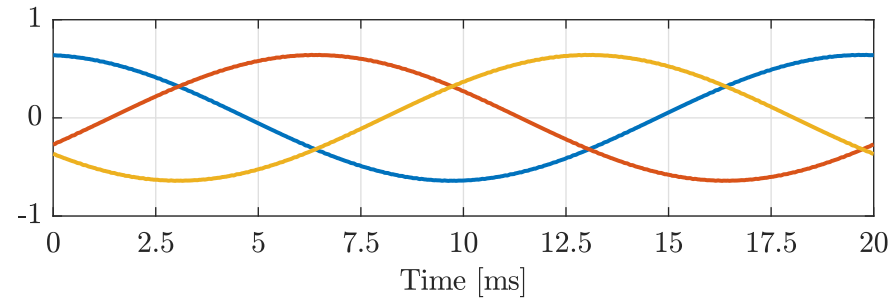
4.3 Performance of PS-PWM

The FB-MMC is modulated with PS-PWM. V_{ref} is 0.9 p.u. and m_f is 3. The converter operates in buck mode with $2N + 1$ modulation. The modulator is connected to the revised sorting algorithm, presented in Fig. 3.19. The grid voltages are presented in Fig. 4.1. The apparent switching frequency of the converter is 7100 Hz and the device switching frequency is 148 Hz.

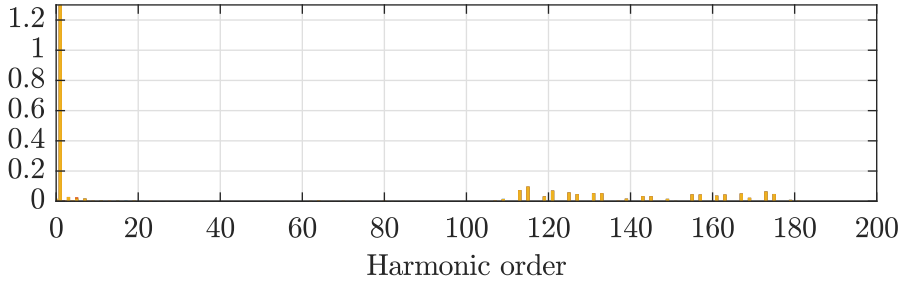
The phase currents and their harmonic spectra are presented in Fig. 4.2, and are almost identical among all the 3 phases. The small differences in the spectra are due to a limited sampling frequency of the simulation. This causes also the triplen harmonics to the spectra. The current harmonics fulfill the limits set by the IEEE-519 standard, described in Table 4.1. The TDD of the current is 0.15%.

The circulating current in phase x is presented in Fig. 4.3. The peak-to-peak value of the circulating current is $16 \cdot 10^{-3}$ p.u.

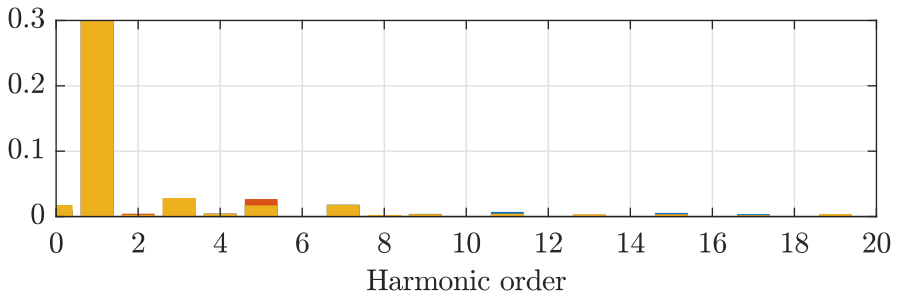
The capacitor voltages in the arms of phase x for different sorting methods are presented



(a) *Grid currents.*



(b) *Harmonic spectra of grid currents as a percentage of the rated current. The TDD is 0.15%.*



(c) *Harmonic spectra of first 20 harmonics of the grid currents as a percentage of the rated current.*

Figure 4.2. *Three-phase grid currents and harmonic spectra of the currents in steady-state PS-PWM operation. Blue, red, and yellow colors correspond to phases a, b, and c respectively.* $N = 12$, $m_f = 3$, $V_{ref} = 0.9$ *p.u.,* $2N + 1$ *modulation.*

in Fig. 4.4. Both algorithms keep the capacitor voltages balanced. In terms of the capacitor voltage ripple, there is no significant difference. The device switching frequency of the conventional sorting algorithm is 635 Hz. The revised sorting algorithm produces a device switching frequency of $f_{\mathrm{sw,dev}}$ 148 Hz. The decrease in $f_{\mathrm{sw,dev}}$ is significant, highlighting the benefits of the revised sorting algorithm when used with PS-PWM.

When the converter operates with the same parameters and $N + 1$ voltage levels, the apparent switching frequency is 3500 Hz. The device switching frequency is similar to $2N+1$ modulation, 146 Hz. The peak-to-peak circulating current is decreased to $0.21 \cdot 10^{-3}$ p.u.

The harmonic spectra of the currents are presented in Fig. 4.5. The TDD is 0.49%. While the harmonics over the 100th harmonic are similar in $N + 1$ and $2N + 1$ modulation, a new group of harmonics appears around the 72nd harmonic. The spectra of the $N + 1$

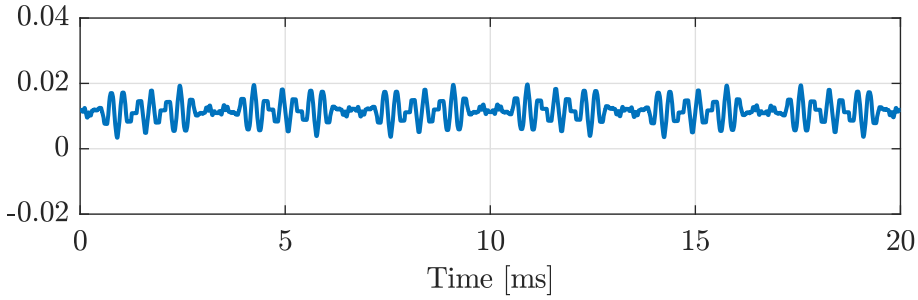
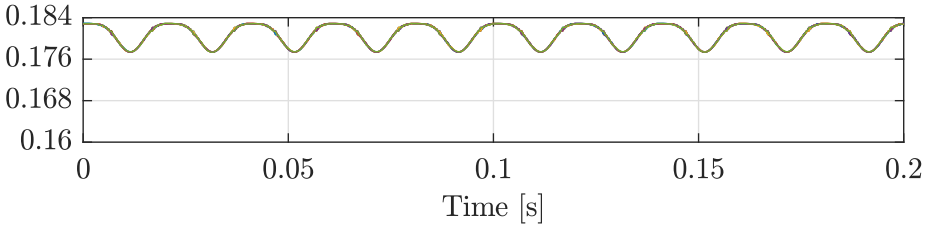
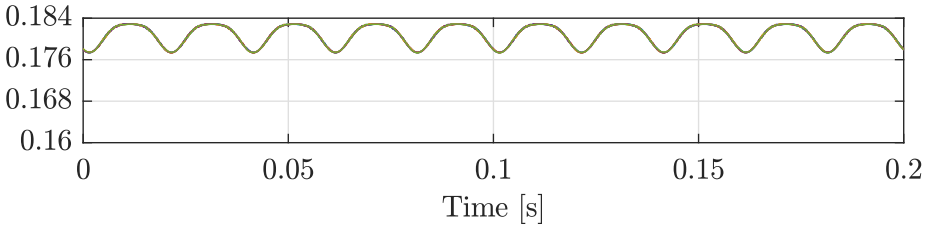


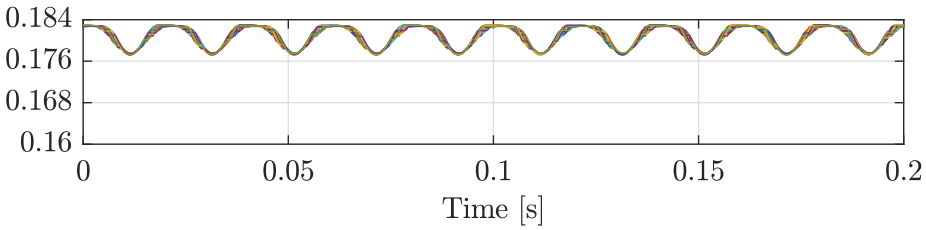
Figure 4.3. *Circulating current in phase x of FB-MMC in steady-state PS-PWM operation. $N = 12$, $m_f = 3$, $V_{ref} = 0.9$ p.u., $2N + 1$ modulation.*



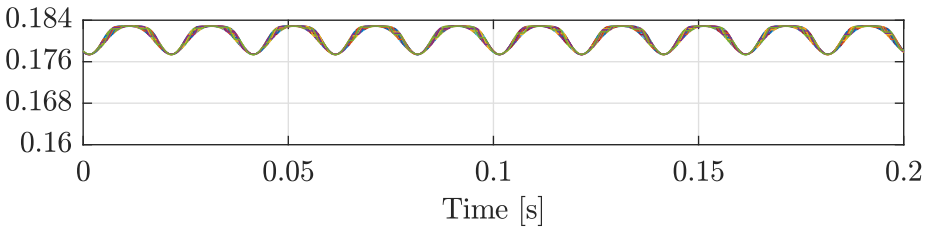
(a) *Conventional sorting algorithm, upper arm.*



(b) *Conventional sorting algorithm, lower arm.*



(c) *Revised sorting algorithm, upper arm.*



(d) *Revised sorting algorithm, lower arm.*

Figure 4.4. *Individual capacitor voltages for the upper and lower arm in phase x in steady-state PS-PWM operation with conventional and revised sorting algorithm. $N = 12$, $m_f = 3$, $V_{ref} = 0.9$ p.u., $2N + 1$ modulation.*

modulation do not fulfill the limits set by the IEEE-519 standard.

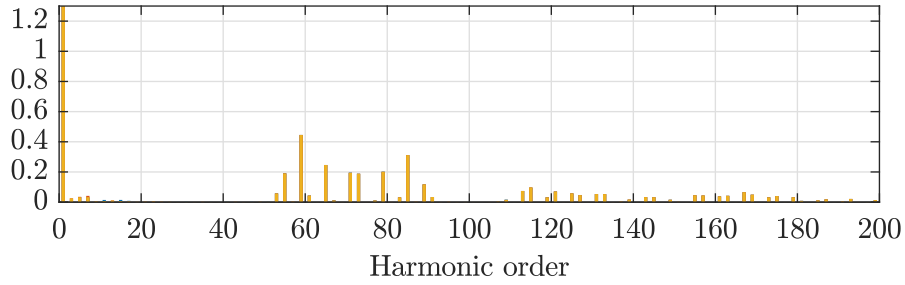
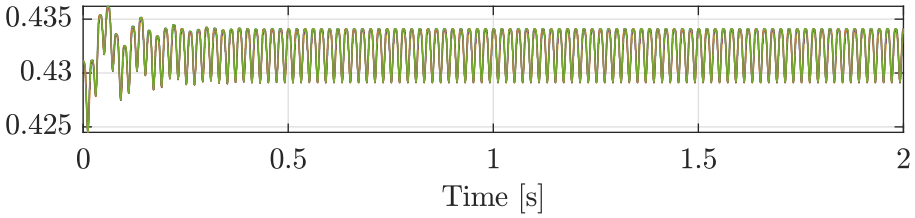
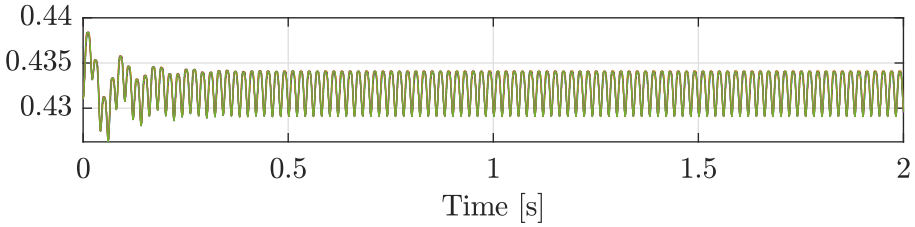


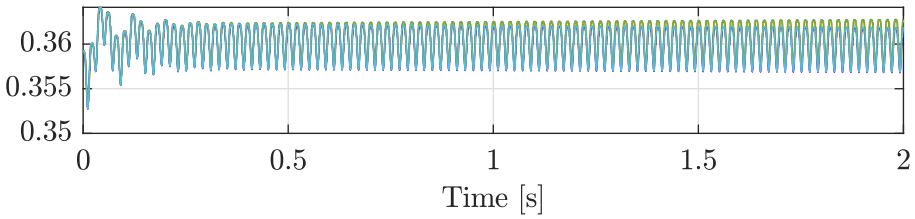
Figure 4.5. *Harmonic spectra of the grid currents as a percentage of the rated current in steady-state PS-PWM operation. The TDD is 0.49%. Blue, red, and yellow colors are phases a, b, and c respectively.* $N = 12$, $m_f = 3$, $V_{ref} = 0.9$ *p.u.,* $N + 1$ *modulation.*



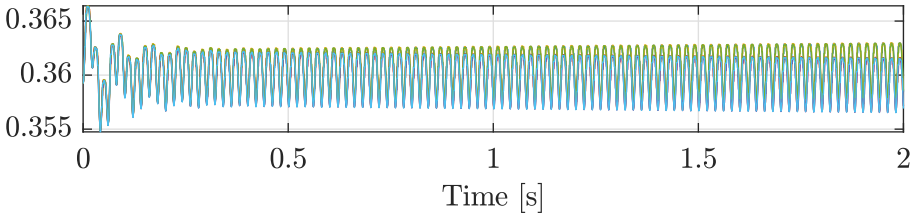
(a) *Upper arm,* $N = 5$, $m_f = 3.2$.



(b) *Lower arm,* $N = 5$, $m_f = 3.2$.



(c) *Upper arm,* $N = 6$, $m_f = 3.1667$.



(d) *Lower arm,* $N = 6$, $m_f = 3.1667$.

Figure 4.6. *Individual capacitor voltages in the upper and lower arm in phase* x *for 5 and 6 SMs with non-integer* m_f *in PS-PWM operation.* $V_{ref} = 0.9$ *p.u.,* $2N + 1$ *modulation.*

4.3.1 Natural balancing ability of PS-PWM for FB-MMC

The HB-MMC is able to achieve natural balance when m_f is a non-integer number chosen based on Table 3.2. Suitable carrier-to-fundamental frequency ratios for FB-MMC have

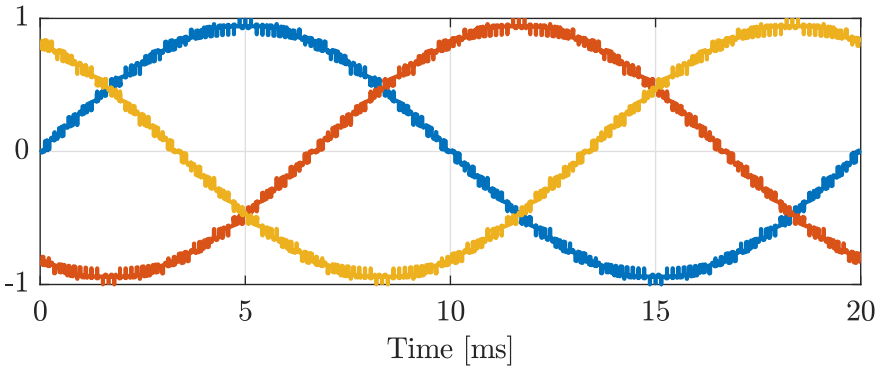


Figure 4.7. *Three-phase grid voltages in steady-state PD-PWM operation. Blue, red, and yellow colors correspond to phases a, b, and c respectively.* $N = 12$, $m_f = 36$, $V_{ref} = 0.9$ *p.u.,* $2N + 1$ *modulation.*

not been proposed. In Fig 4.6 operation of FB-MMC is presented with non-integer m_f for 5 and 6 SMs. The initial capacitor voltages are now $V_{\mathrm{dc}}/5$ and $V_{\mathrm{dc}}/6$, respectively. For 5 and 6 SMs m_f is 3.2 and 3.1667, respectively, when $2N + 1$ modulation is used, chosen based on Table 3.2. The FB-MMC with 5 SMs achieves natural balance. When 6 SMs are used, the capacitor voltages start to diverge from the nominal voltage. It is clear that the carrier-to-fundamental frequency ratios for HB-MMC cannot necessarily be applied directly to FB-MMC, but with some values of m_f, the natural balance is achievable. This behavior will be investigated further in the future.

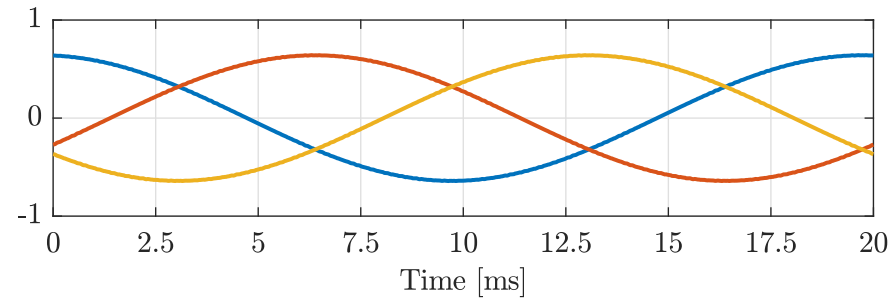
4.4 Performance of PD-PWM

The FB-MMC is modulated with PD-PWM. As previously, V_{ref} is 0.9 p.u., and the revised sorting algorithm is employed along with the modulator. m_f is increased to 36 to achieve a similar device switching frequency as with PS-PWM. When the converter operates in the buck mode with $2N+1$ modulation, the apparent switching frequency of the converter is 7100 Hz and the device switching frequency is 148 Hz. The grid voltages are presented in Fig. 4.7.

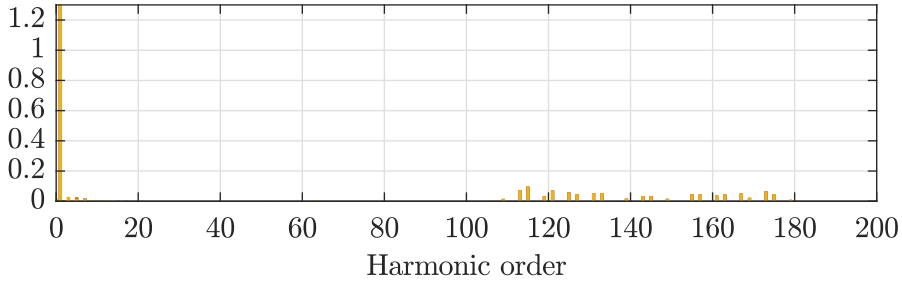
Fig 4.8 presents the phase currents and their harmonic spectra. Similarly to PS-PWM, the currents are almost identical, and the small differences between the phases are due to the sampling frequency. The current harmonics fulfill the limits set by the IEEE-519 standard. The current TDD is 0.15%.

Fig. 4.9 presents the circulating current in phase x. The peak-to-peak amplitude of the circulating current is $16{\cdot}10^{-3}$ p.u.

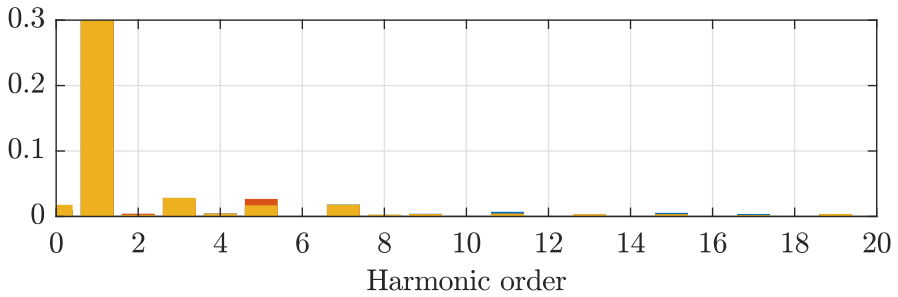
The capacitor voltages in the arms of phase x for different sorting methods are presented in Fig. 4.10. The results are similar to PS-PWM and both algorithms keep the capacitor voltages balanced. The device switching frequency of the conventional sorting algorithm



(a) *Grid currents.*



(b) *Harmonic spectra of grid currents as a percentage of the rated current. The TDD is 0.15%.*



(c) *Harmonic spectra of first 20 harmonics of grid currents as a percentage of the rated current.*

Figure 4.8. *Three-phase grid currents and harmonic spectra of the currents in steady-state PD-PWM operation. Blue, red, and yellow colors correspond to phases a, b, and c respectively.* $N = 12$, $m_f = 36$, $V_{ref} = 0.9$ *p.u.,* $2N + 1$ *modulation.*

is 635 Hz, while the revised sorting algorithm has a device switching frequency of $f_{\mathrm{sw,dev}}$ 148 Hz. Based on the results, the revised sorting algorithm outperforms the conventional sorting algorithm when used with PD-PWM.

PD-PWM can be operated also with $N+1$ voltage levels. Similarly to PS-PWM, the apparent switching frequency decreases and is 3600 Hz when $N + 1$ modulation is used. The device switching frequency is 150 Hz, and the circulating currents decrease to $0.17 \cdot 10^{-3}$ p.u. The current TDD is 0.49%. Fig. 4.11 presents the harmonic spectra of the currents, and as previously with PS-PWM, PD-PWM produces a new group of harmonics around the 72nd harmonic. Because of the new harmonics, the EEE-519 standard limits are not fulfilled.

The performance of PS-PWM and PD-PWM is really similar with both $N + 1$ and $2N + 1$ modulation. The similarities and differences between these methods are further dis-

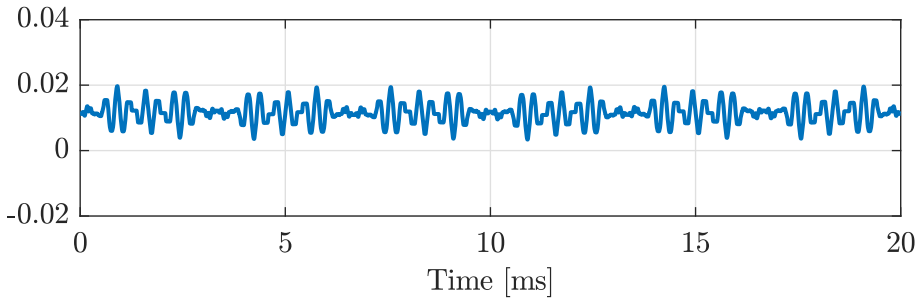
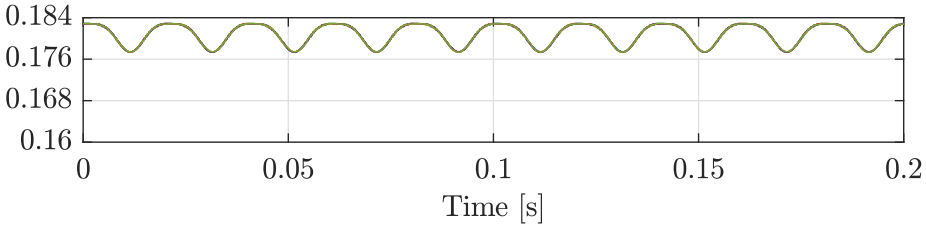
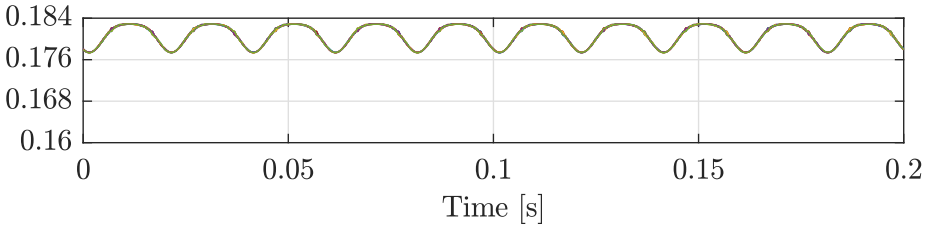


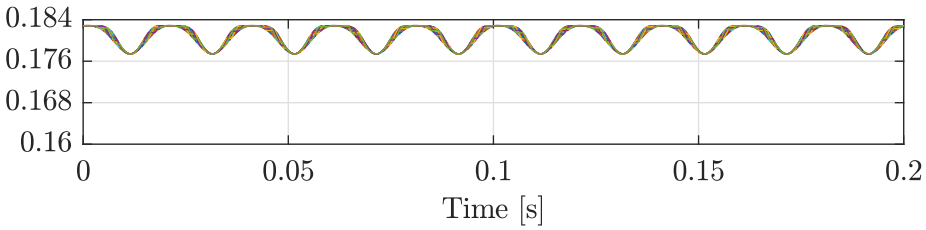
Figure 4.9. *Circulating current in phase x of FB-MMC in steady-state PD-PWM operation. $N = 12$, $m_f = 36$, $V_{ref} = 0.9$ p.u., $2N + 1$ modulation.*



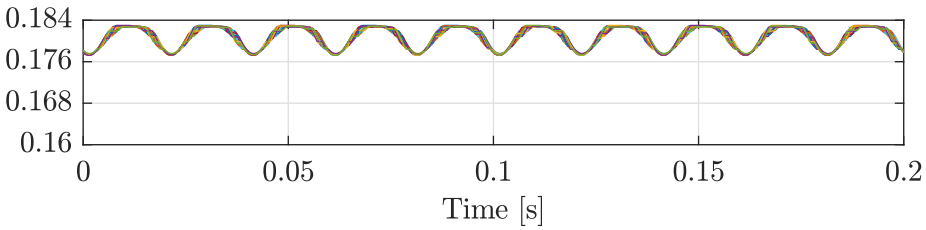
(a) *Conventional sorting algorithm, upper arm.*



(b) *Conventional sorting algorithm, lower arm.*



(c) *Revised sorting algorithm, upper arm.*



(d) *Revised sorting algorithm, lower arm.*

Figure 4.10. *Individual capacitor voltages for the upper and lower arm in phase x in steady-state PD-PWM operation with conventional and revised sorting algorithm. $N = 12$, $m_f = 36$, $V_{ref} = 0.9$ p.u., $2N + 1$ modulation.*

cussed in Section 4.6.

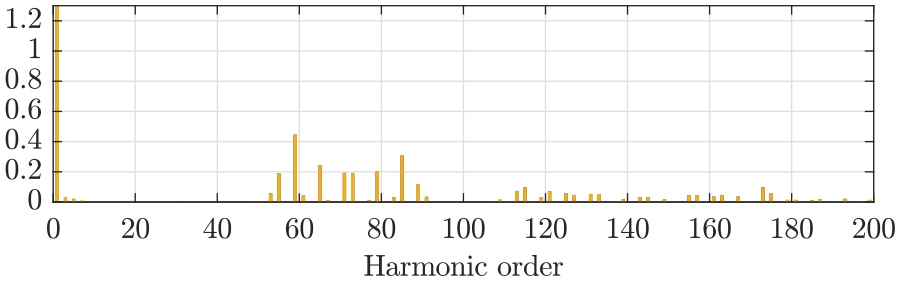


Figure 4.11. *Harmonic spectra of the grid currents as a percentage of the rated current in steady-state PD-PWM operation. The TDD is 0.49%. Blue, red, and yellow colors correspond to phases a, b, and c respectively.* $N = 12$, $m_f = 36$, $V_{ref} = 0.9$ *p.u.,* $N + 1$ *modulation.*

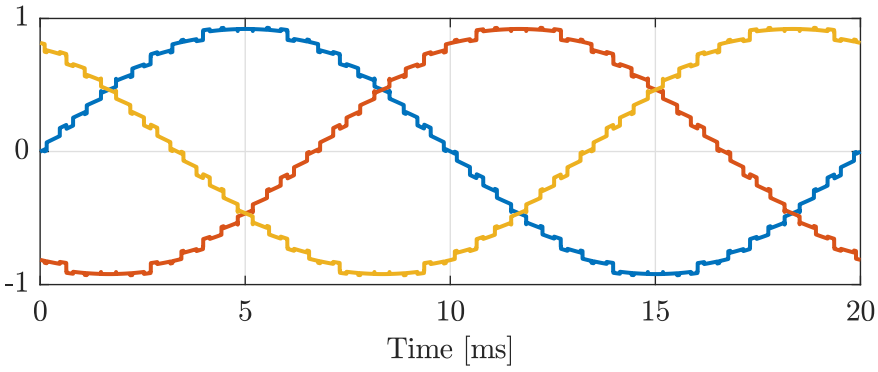


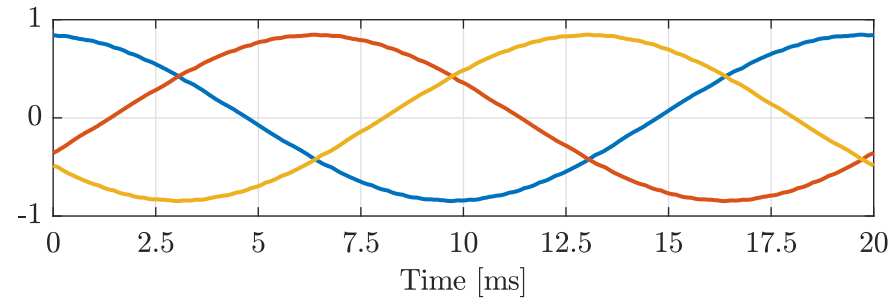
Figure 4.12. *Three-phase grid voltages in steady-state NLM operation. Blue, red, and yellow colors are phases a, b, and c respectively.* $N = 12$, $V_{ref} = 0.9$ *p.u.,* $2N + 1$ *modulation.*

4.5 Performance of NLM

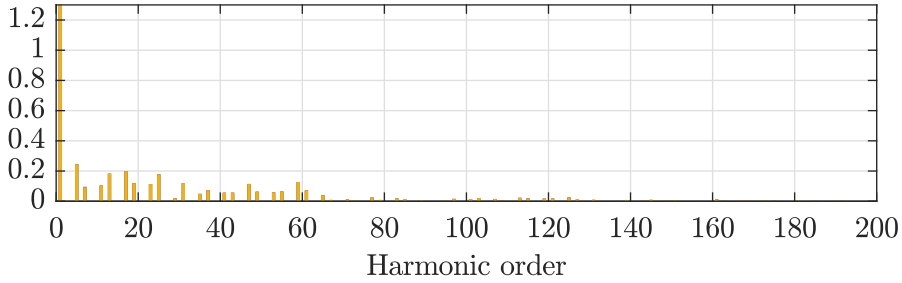
The FB-MMC is modulated with NLM. As previously, V_{ref} is 0.9 p.u. $2N + 1$ modulation is used based on (3.11). The modulator is used with the conventional sorting algorithm. The reason for this is that since the apparent switching frequency of NLM is low, the revised sorting algorithm may not be able to keep SM voltages balanced. The grid voltages are presented in Fig. 4.12. NLM produces an apparent switching frequency of 1000 Hz and a device switching frequency of 144 Hz.

The phase currents and their harmonic spectra are presented in Fig. 4.13. Clear harmonic groups cannot be observed and the harmonics are concentrated at the low frequencies. The TDD of the current is 0.46% and the current harmonics fulfill the limits set by the IEEE-519 standard.

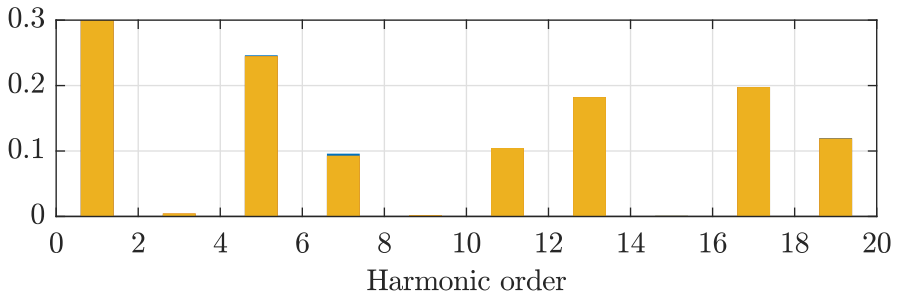
The circulating current in phase x is presented in Fig. 4.14. The peak-to-peak value of the circulating current is $37.9 \cdot 10^{-3}$ p.u. The circulating current is much higher than with the carrier-based methods because the upper and lower arm have a different number of submodules inserted into them for a longer period.



(a) *Grid currents.*



(b) *Harmonic spectra of grid currents as a percentage of the rated current. The TDD is 0.46%.*



(c) *Harmonic spectra of first 20 harmonics of grid currents as a percentage of the rated current.*

Figure 4.13. *Three-phase grid currents and harmonic spectra of the currents in steady-state NLM operation. Blue, red, and yellow colors are phases a, b, and c respectively.* $N = 12$, $V_{ref} = 0.9$ *p.u.,* $2N + 1$ *modulation.*

The individual capacitor voltages with the conventional sorting algorithm and the revised sorting algorithm are presented in Fig. 4.15. $f_{\mathrm{sw,dev}}$ is 144 Hz and 21 Hz respectively. The average capacitor voltages are lower than with the carrier-based modulation methods. The voltage drop is due to the increased circulating currents. The same observation was made in [19] for HB-MMC.

Using the conventional sorting algorithm reduces the voltage ripple. When the revised sorting algorithm is used, one SM in both arms is constantly bypassed in the steady state. This results from the periodicity of the NLM, and circulating current and will lead to uneven losses and wearing in the switching devices among the SMs. The performance of the revised sorting algorithm could be improved by allowing the algorithm to make a limited number of unnecessary switching events, i.e. inserting and bypassing SMs whose state does not need to change.

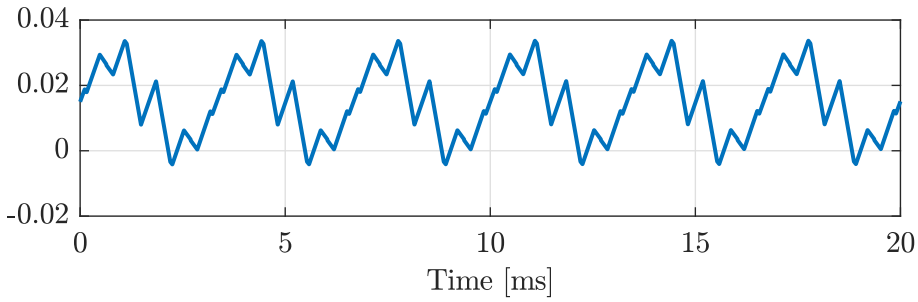
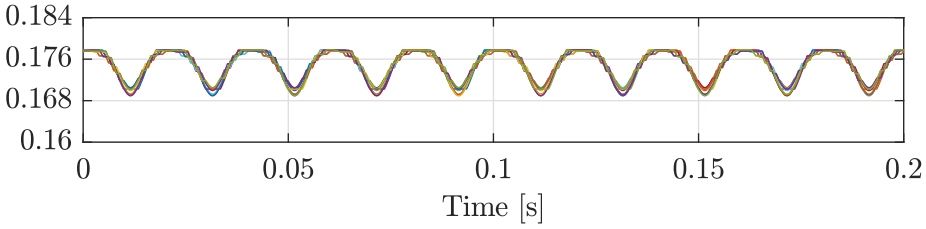
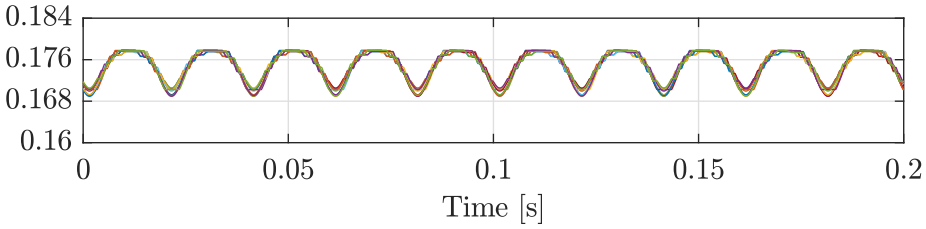


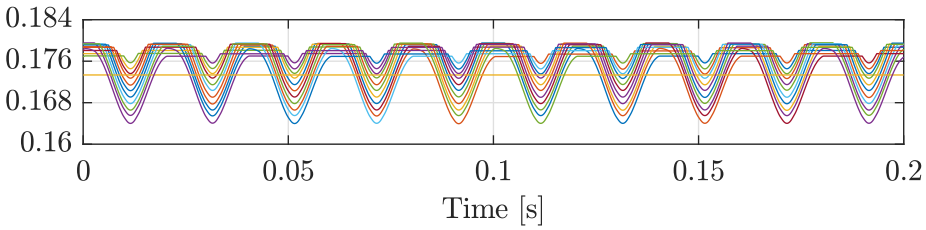
Figure 4.14. *Circulating current in phase x of FB-MMC in steady-state NLM operation. $N = 12$, $V_{ref} = 0.9$ p.u., $2N + 1$ modulation.*



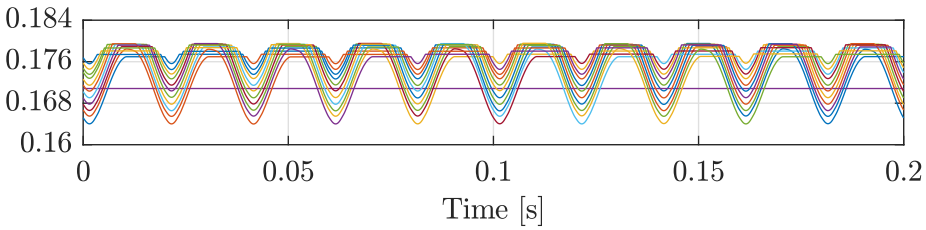
(a) *Conventional sorting algorithm, upper arm.*



(b) *Conventional sorting algorithm, lower arm.*



(c) *Revised sorting algorithm, upper arm.*



(d) *Revised sorting algorithm, lower arm.*

Figure 4.15. *Individual capacitor voltages for the upper and lower arm in phase x in steady-state NLM operation with conventional and revised sorting algorithm. $N = 12$, $V_{ref} = 0.9$ p.u., $2N + 1$ modulation.*

When NLM is used with $N+1$ voltage levels, the apparent switching frequency decreases to 500 Hz. The device switching frequency remains similar, 141 Hz. The current harmonic

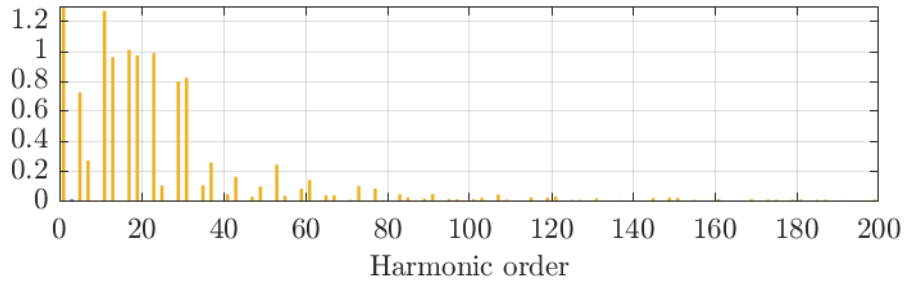
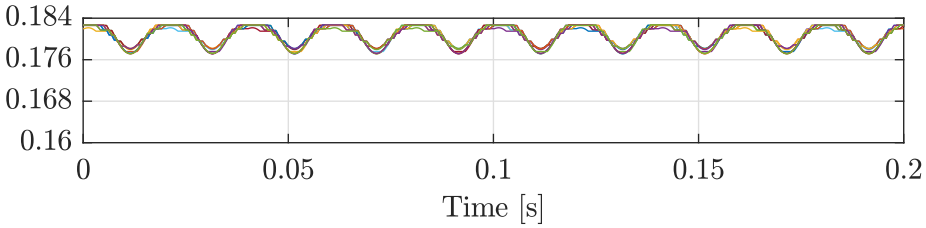
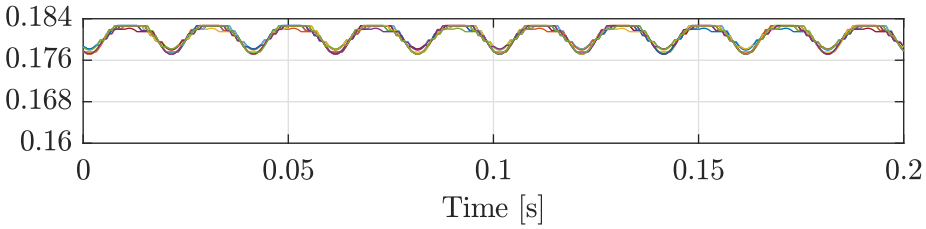


Figure 4.16. *Harmonic spectra of the grid current as a percentage of the rated current in steady-state NLM operation. The TDD is 1.63%. Blue, red, and yellow colors correspond to phases a, b, and c respectively.* $N = 12$, $V_{ref} = 0.9$ *p.u.,* $N + 1$ *modulation.*



(a) *Upper arm.*



(b) *Lower arm.*

Figure 4.17. *Individual capacitor voltages for the upper and lower arm in phase* x *in steady-state NLM operation with a conventional sorting algorithm.* $N = 12$, $V_{ref} = 0.9$ *p.u.,* $N + 1$ *modulation.*

spectrum is depicted in Fig. 4.16. The current TDD is 1.63%. The harmonic spectra of the $N + 1$ and $2N + 1$ modulation differ a lot, as NLM does not produce deterministic harmonic spectra. The harmonic limits set by IEEE-519 standard are not fulfilled.

The circulating currents decrease when $N + 1$ modulation is used, as the same amount of submodules is always inserted in the complementary arms. The peak-to-peak value of circulating current is now $0.55 \cdot 10^{-3}$ p.u. The average capacitor voltages are close to their nominal value, as presented in Fig. 4.17.

4.6 Summary of results

The summary of the results is presented in Table 4.4. The carrier-based methods produce the same PWM output when $2N+1$ modulation is used, which explains the same results. The PWM outputs of PS-PWM and PD-PWM with $2N + 1$ voltage levels are presented

	Voltage levels	PS-PWM	PD-PWM	NLM
Sorting algorithm	$N+1$	Revised	Revised	Conventional
	$2N+1$	Revised	Revised	Conventional
Current TDD [%]	$N+1$	0.49	0.49	1.63
	$2N+1$	0.15	0.15	0.46
$f_{\mathrm{sw,app}}$ [Hz]	$N+1$	3500	3600	500
	$2N+1$	7100	7100	1000
$f_{\mathrm{sw,dev}}$ [Hz]	$N+1$	146	150	141
	$2N+1$	148	148	144
Peak-to-peak circulating current [p.u.]	$N+1$	$21 \cdot 10^{-5}$	$17 \cdot 10^{-5}$	$55 \cdot 10^{-5}$
	$2N+1$	$16 \cdot 10^{-3}$	$16 \cdot 10^{-3}$	$30 \cdot 10^{-3}$

Table 4.4. *Simulation results.*

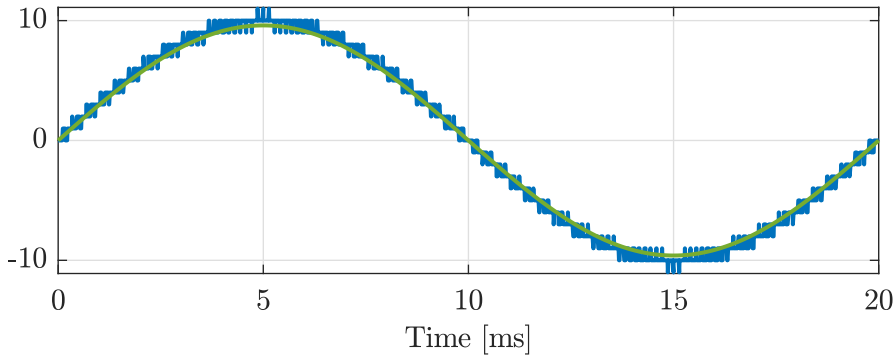
in Fig. 4.18. When $N+1$ modulation is used, small differences between PS-PWM and PD-PWM appear, but the overall performance is still virtually the same.

All the methods have effectively the same device switching frequency regardless of the used voltage levels. The carrier-based methods have an output current TDD of 0.15%, while NLM has a TDD of 0.46% when $2N+1$ modulation is used. NLM produces almost twice as high peak-to-peak value of the circulating current as the carrier-based methods, which leads to a decrease in the capacitor voltages.

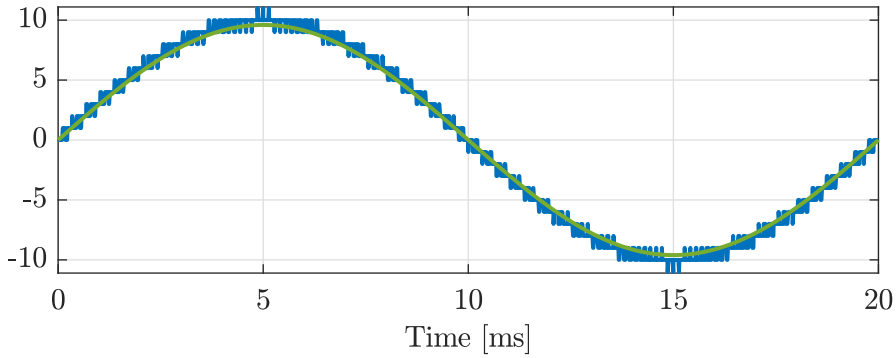
When $N+1$ modulation is used, the current quality of all the methods decreases as expected. On the other hand, the circulating currents decrease, as the switching events in the upper and lower arm happen simultaneously. Similarly to $2N+1$ modulation, the performance of NLM is considerably weaker on all metrics compared to the carrier-based methods.

In the end, implementation wise PD-PWM has an advantage over PS-PWM, as the switching frequencies can be decreased by decreasing the carrier-to-fundamental frequency ratio. In these results, m_f for PS-PWM was 3 and m_f for PD-PWM was 36. The carrier frequency of PD-PWM was 12, i.e., N times higher than PS-PWM. If the number of SMs increases, the carrier frequency can be decreased in order to lower the device switching frequency while maintaining the same current quality. PD-PWM is therefore capable of achieving lower device switching frequencies than PS-PWM.

When the SM number increases, NLM is a good option as a modulation method due to its easy implementation. Also, the absence of carriers makes the design process simpler, as parameters for the carriers do not have to be chosen. Improving the revised sorting algorithm to meet the needs of NLM would decrease the device switching frequency and the switching losses of the converter while maintaining the same current TDD and $f_{\mathrm{sw,app}}$.



(a) *PS-PWM.*



(b) *PD-PWM.*

Figure 4.18. $n_{out,x}$ *(blue) and reference (green) of PS-PWM and PD-PWM.*

The current TDD could be decreased by adding more SMs to the system or by introducing more switching events by combining NLM with a carrier-based method.

The downsides of the NLM cannot be overlooked. When compared to the carrier-based methods, NLM produced the greatest circulating currents. With $2N + 1$ modulation, the circulating currents lead to a voltage drop in the SM capacitor voltages. Also, as stated in Section 3.5, NLM will result in a difference between the fundamental component of the generated waveform and the reference, when the number of SM is low. The error gets smaller as N increases.

5. CONCLUSIONS

In this thesis, modulation methods for FB-MMCs in a double-star configuration were examined. The modulation methods for HB-MMC are well known, but information about methods for FB-MMC is not widely available. First, an overview of modulation methods was presented. PS-PWM for the FB-MMC with a variable dc-link voltage existed. PD-PWM and NLM for FB-MMC were developed based on modulating signals of PS-PWM. All three methods are able to produce both $N + 1$ and $2N + 1$ voltage levels and operate in the boost mode when the dc-link voltage is below the nominal value. POD- and APOD-PWM were also investigated. The output of said methods was not suitable as $2N + 1$ modulation could not be achieved due to symmetry in the modulating signals and the carriers.

Two voltage balancing algorithms were implemented for the FB-MMC. The conventional sorting algorithm sorts all capacitors at each execution. The revised sorting algorithm sorts and switches only a minimum amount of SMs, decreasing the device switching frequency.

The modulation and sorting methods were tested by simulating the converter in Matlab and Simulink. An FB-MMC in the double-star configuration was connected to a grid and modulated with different modulator and voltage balancing combinations in an open-loop setting. The performance of the modulation methods was evaluated based on their current quality, apparent and device switching frequency, and circulating currents.

All the methods had effectively the same device switching frequency regardless of whether $N+1$ or $2N+1$ modulation was used. It was observed that PS-PWM and PD-PWM produced the same switching instant when $2N + 1$ modulation was used and thus their performance was identical. When $N + 1$ modulation was used, their performance did not have notable differences. In terms of the current quality, the performance of carrier-based methods was better than NLM. The apparent switching frequency was higher and the peak-to-peak value of circulating currents was lower with the carrier-based methods than with NLM.

For carrier-based methods, the performance of sorting algorithms was very similar. As expected, the conventional sorting algorithm kept the SM capacitor voltages a bit better balanced but resulted in a much higher device switching frequency. For NLM, the con-

ventional sorting algorithm was a better choice, as the revised sorting algorithm resulted in uneven usage of the SMs.

Finally, the natural balancing ability of FB-MMC in PS-PWM operation was analyzed with simulations. The balancing ability seems to exist with some carrier-to-fundamental frequency ratios. Known ratios exist for HB-MMC but are not applicable to FB-MMC in all cases.

5.1 Future research

In this thesis, it was observed that the FB-MMC with PS-PWM has a natural balancing ability with some carrier-to-fundamental frequency ratios. This behavior should be analyzed further to allow for meaningful conclusions.

The performance of NLM leaves room for improvement in the modulating and SM voltage balancing stages. The current quality could be increased by creating a hybrid NLM. [27] presents a hybrid method but does not address the effect of variable dc-link voltage and boost mode. The voltage balancing of NLM could be improved by using the revised sorting algorithm but allowing more switching events per execution.

The sorting algorithms should be investigated further to take the redundant states of the FB-MMC into account when SMs are inserted or bypassed. Loss analysis should be performed to evaluate loss distribution among switches in one SM.

The performance of the modulation and capacitor voltage balancing methods should be analyzed also in the boost mode. Additionally, more performance metrics should be introduced, for example, power losses, modularity, and robustness to faults.

REFERENCES

[1] Y. Cheng, C. Qian, M. Crow, S. Pekarek, and S. Atcitty, “A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage”, *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1512–1521, Oct. 2006.

[2] A. Lesnicar and R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range”, in *2003 IEEE Bologna Power Tech Conference Proceedings*, vol. 3, Bologa, Italy, Jun. 2003, pp. 1–6.

[3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, “Operation, control, and applications of the modular multilevel converter: A review”, *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[4] A. Hassanpoor, S. Norrga, H.-P. Nee, and L. Ängquist, “Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application”, in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Montreal, Canada, Oct. 2012, pp. 388–393.

[5] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, “An improved pulse width modulation method for chopper-cell-based modular multilevel converters”, *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3472–3481, Aug. 2012.

[6] Y. Deng and R. G. Harley, “Space-vector versus nearest-level pulse width modulation for multilevel converters”, *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 2962–2974, Jun. 2015.

[7] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, “Circuit topologies, modeling, control schemes, and applications of modular multilevel converters”, *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, Jan. 2015.

[8] K. Sharifabadi, R. Teodorescu, L. Harnefors, *et al.*, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems: A Guide to Employability and Professional Development*. New York: John Wiley & Sons, Incorporated, 2016.

[9] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi, “Experimental verification of a modular multilevel cascade inverter based on double-star bridge cells”, *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 509–519, Jan. 2014.

[10] Y. Deng, K. H. Teo, C. Duan, T. G. Habetler, and R. G. Harley, “A fast and generalized space vector modulation scheme for multilevel inverters”, *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5204–5217, Oct. 2014.

[11] J. E. Huber and A. J. Korn, “Optimized pulse pattern modulation for modular multilevel converter high-speed drive”, in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, Novi Sad, Serbia, Sep. 2012, LS1a–1.4–1–LS1a–1.4–7.

[12] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, “Analysis and operation of modular multilevel converters with phase-shifted carrier PWM”, *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 268–283, Jan. 2015.

[13] A. O. Arslan, F. Eroğlu, M. Kurtoğlu, and A. M. Vural, “Optimal carrier frequency swapping for PD-PWM in modular multilevel converter”, in *2019 3rd International Symposium on Multidisciplinary Studies and Innovative Technologies (ISMSIT)*, Ankara, Turkey, Oct. 2019, pp. 1–6.

[14] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, “A new modulation method for the modular multilevel converter allowing fundamental switching frequency”, *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3482–3494, Aug. 2012.

[15] O. J. K. Oghorada, L. Zhang, I. B. Efika, and C. J. Nwobu, “Control of modular multilevel converters using an overlapping multihexagon space vector modulation scheme”, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 381–391, Mar. 2019.

[16] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, “Analysis of the phase-shifted carrier modulation for modular multilevel converters”, *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 297–310, Jan. 2015.

[17] A. Allu, M. Odavic, and K. Atallah, “Design considerations of a full bridge modular multilevel converter under variable DC link voltage”, in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, USA, Oct. 2017, pp. 504–510.

[18] S. Thakur, M. Odavic, A. Allu, Z. Q. Zhu, and K. Atallah, “Analytical modelling and optimization of output voltage harmonic spectra of full-bridge modular multilevel converters in boost mode”, *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3403–3420, Mar. 2022.

[19] P. Hu and D. Jiang, “A level-increased nearest level modulation method for modular multilevel converters”, *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1836–1842, Apr. 2015.

[20] J. Qin and M. Saeedifard, “Reduced switching-frequency voltage-balancing strategies for modular multilevel HVDC converters”, *IEEE Transactions on Power Delivery*, vol. 28, no. 4, pp. 2403–2410, Oct. 2013.

[21] A. Hassanpoor, L. Ängquist, S. Norrga, K. Ilves, and H.-P. Nee, “Tolerance band modulation methods for modular multilevel converters”, *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 311–326, Jan. 2015.

[22] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, “Predictive sorting algorithm for modular multilevel converters minimizing the spread in the submodule capacitor

voltages", *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 440–449, Jan. 2015.

[23] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H.-P. Nee, "Open-loop control of modular multilevel converters using estimation of stored energy", *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2516–2524, Nov. 2011.

[24] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters", *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[25] T. Blooming and D. Carnovale, "Application of IEEE STD 519-1992 harmonic limits", in *Conference Record of 2006 Annual Pulp and Paper Industry Technical Conference*, Appleton, USA, Jun. 2006, pp. 1–9.

[26] "IEEE recommended practice and requirements for harmonic control in electric power systems", *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, Jun. 2014.

[27] J. He, L. Lin, and C. Xu, "A self-adapted compositive modulation method for full-bridge modular multilevel converter", in *2019 4th IEEE Workshop on the Electronic Grid (eGRID)*, Xiamen, China, Nov. 2019, pp. 1–5.