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Analysis and design of high gain DC-DC converter for renewable energy applications

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ABSTRACT

The paper proposes an efficient DC-DC converter for renewable energy applications. The proposed high-gain converter is designed with switched inductor cell and voltage multiplier cell. In the proposed converter, the continuous source current is obtained by switched inductor cells, and high-voltage gain is achieved using voltage multiplier cells. The proposed converter provides a voltage gain of 10 when operated with a duty ratio of 27.3%, whereas a voltage gain of 39 is obtained for an 80% duty ratio. The efficiency of 96.54% is achieved in simulation for the rated condition of 24 V/240 V, 120W. The converter operation under steady-state, state-space modelling, and voltage and current stress of the power semiconductor components are analyzed. In addition to that, loss distribution and efficiency analysis are made. The performance of the converter is analyzed using the Matlab Simulink tool. Also, the experimental hardware prototype model is developed to validate the simulated and theoretical analysis.

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KEYWORDS
Voltage stress; voltage multiplier cell; renewable energy applications; high efficiency; gain cell

1. Introduction

The power conversion systems require high-gain DC-DC boost converters. This requirement has increased due to applications of higher efficiency and power density. DC-DC boost converters are used in various applications, including battery charging in uninterruptible power supplies, electric vehicles, and DC distribution systems, since these applications require high-voltage gain converters. The source voltage is increased to match the load's requirements using a DC-DC boost converter. High-performance DC-DC converters have gained significant popularity due to their use in photovoltaic (PV) applications. For DC distributed generation systems, solar photovoltaic is one of the essential energy sources. Based on the system requirement, the converter topologies have been chosen. The selection criteria include switching mechanisms, directions of power flow, type of isolation, voltage/current supplied and system stability. In [1], the converter is designed using passive switched capacitors. Although using a large number of switched capacitors increases gain, it also increases the input current's ripple. In paper [2], the authors focus on a hybrid converter with one switch, one inductor, and several capacitors. The boost structure of the converter provides regulating capability, while the voltage multiplier structure provides gain improvement. In [3], a boost converter with an active switched inductor is proposed. The circuit has low voltage stress across the diode, constant input current and a lower rating of voltages for passive components. It has a gain of 4/(1-D). The main reason for the variations in the theoretical and experimental gain is the parasitic internal resistance of several circuit components. It causes a decline in the converter's efficiency. In [4], the author briefs about a high-gain converter that uses regenerative boost configuration. The gain obtained is (2-D) / (1-D)⊃2. A non-isolated non-coupled inductor-based topology for DC microgrids is suggested in [5]. This converter provides a gain of (D2-3D + 3)/(1-D)⊃2. The main downside of converter architecture is pulsating output current and relatively high switch current stress. A converter consisting of a high-conversion-ratio interleaved boost stage and multiplier circuit is proposed in [6]. The voltage multiplier cell present in the converter provides a high conversion ratio. It provides a gain of 4/(1-D). In the paper [7], the authors describe a transformerless boost-based DC-DC converter. The components' normalized peak voltage stress can also be greatly lowered by increasing the number of interleaving stages. The gain of this converter is (2 + 4D)/(1-D). A unique quadratic buck–boost converter is presented in [8]. An interleaved boost type converter is presented in [9]. A coupled inductor with switching capacitors provides a very high-gain. This type of converter is better suited to boost low output voltages. The paper [10] suggests a high step-up transformerless DC-DC converter. The efficiency of this topology is 93% and provides a voltage gain of up to 10 times the input voltage. Various VMCs are used in [11] to improve the gain of interleaved

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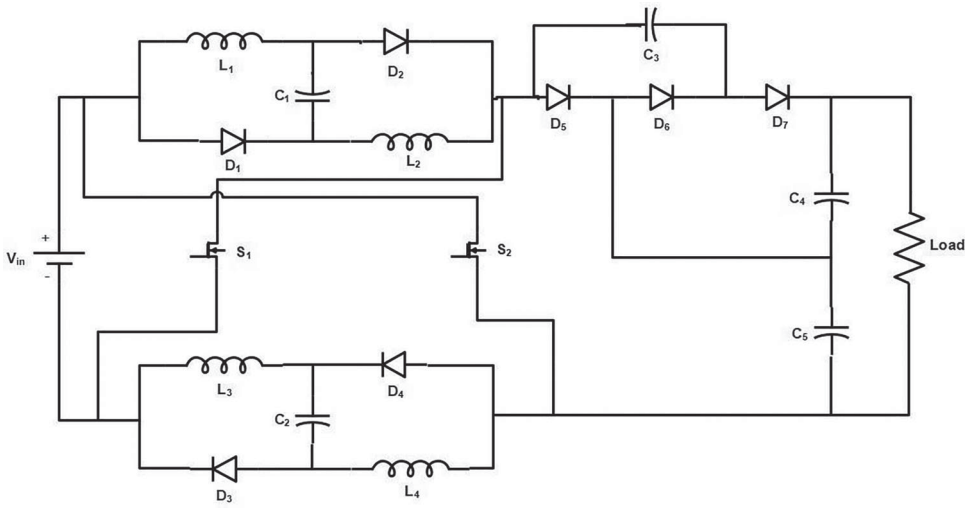

Figure 1. Proposed high-gain DC-DC converter.

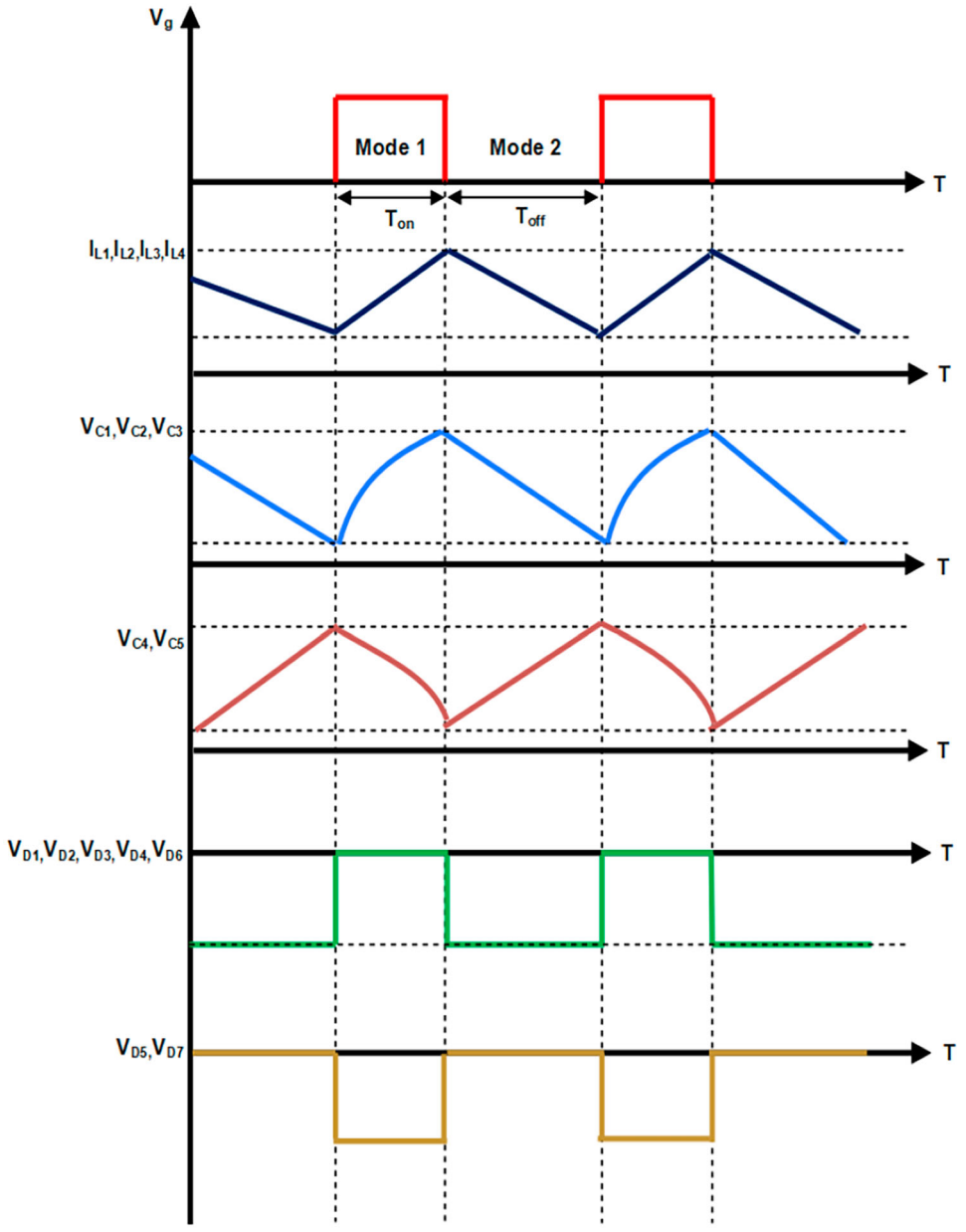

Figure 2. Switching waveform.

converters. Using more switched capacitors boosts the converter's gain and increases the incoming current's ripple. In the paper [12], the authors describe a non-isolated topology. This design, however, necessitates a larger number of inductors. In [13], a switched capacitor structure is used. However, this structure must be utilized with other DC-DC converters to regulate variable voltage. In [14], the author discusses the DC-DC buck–boost converter. This converter has many switches, which would lead to high switching losses. In [15], authors suggest that increasing the cascaded conventional boost converters can enhance gain. However, the components are subjected to a tremendous amount of voltage stress. Quadratic gain converters can also enhance the output voltage at lower duty cycles. In addition, as the duty cycle increases, the current increases, resulting in larger converter losses. There is a large voltage gain and less component voltage stress [16]; however, the input and output of these circuits are not connected to the same ground. Voltage sampling will become more difficult as a result of this. These issues hamper the implementation of topology. In [17], the authors categorize the topologies into two groups depending on whether or not a transformer is employed. In general, isolation transformers significantly benefit from obtaining a high-gain. The disadvantage is that using such transformers increases the converter's cost and size. At lower duty cycles, quadratic gain converters can increase the output voltage. In [18], a quadratic buck–boost converter is proposed. These converters employ many switching capacitors cells to achieve high-gain without using coupled inductors and transformers. The disadvantage is that there will be high converter losses when the duty cycle increases. A transformerless DC-DC converter is discussed in [19]. This converter has lesser gain and more stress when compared to the converter proposed. In [20], the authors present a non-inverting DC-DC converter. It generates a bigger voltage gain while putting less strain on the switches. The suggested converter has a symmetrical configuration, so choosing the components is easier. The gain of the converter is (3 + D)/(1-D). In paper [21], active switched inductor based boost converter topology is developed. Three power switches operated with two duty ratio is used to achieve high-voltage gain. The switched inductor and switched capacitor based boost converter topology is developed and its operating strategies are explained in [22]. The coupled inductor and diode capacitor multiplier cell based boost converter structure is presented in [23]. This study presents a new high-gain converter to solve these shortcomings. It has two symmetrical voltage multiplier cells and a three-diode gain cell. Compared to other existing converters, it has a better gain and efficiency. The components are easier to choose because the proposed converter has a symmetrical structure.

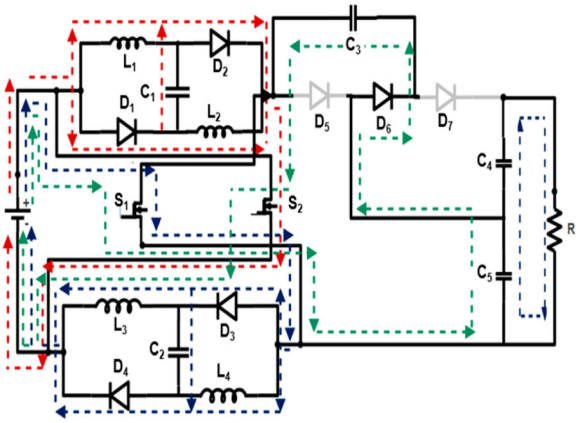

Figure 3. First mode of operation.

2. Proposed converter

Figure 1 provides the circuit schematic for the proposed high-gain DC-DC converter. The converter's gain is increased by using two identical switched-inductor-based VMCs. Seven diodes D_1 to D_7, switches S_1 and S_2, five capacitors C_1 to C_5, and four inductors L_1 to L_4 make up the converter topology. S_1 and S_2 are operated using the same signal and simultaneously turned on and off. The converter operates in two modes based on the gating signal and is shown in Figure 2.

2.1. First mode of operation

During T_{on} period, S_1 and S_2, diodes D_1 to D_4 and D_6 are in forward bias while diodes D_5 and D_7 are in reverse bias. Also, capacitors C_1, C_2 and C_3 are charging while other capacitors C_4 and C_5, are discharging. The diagram corresponding to the mode one operation is given in Figure 3.

The voltage expression for the inductors and capacitor current expression in first mode is obtained by applying KVL & KCL in Figure 3, and the Equations are represented as (1) to (8).

$$V_{L1} = V_{L2} = V_{L3} = V_{L4} = V_{in}. \quad (1)$$

$$V_{in} = V_{C1} = V_{C2}. \quad (2)$$

$$V_{in} + V_{C5} = V_{C3}. \quad (3)$$

$$i_{C1} = I_{in} - I_{L1} - I_{L2}. \quad (4)$$

$$i_{C2} = I_{in} - I_{L3} - I_{L4}. \quad (5)$$

$$i_{C3} = I_{in}. \quad (6)$$

$$i_{C4} = I_0. \quad (7)$$

$$i_{C5} = I_{in} + I_0. \quad (8)$$

2.2. Second mode of operation

During T_{off} period, S_1 and S_2, diodes D_1 to D_4 and D_6 are in reverse bias, diodes D_5 and D_7 operate and capacitors C_4 and C_5 are charging while other capacitors C_1,

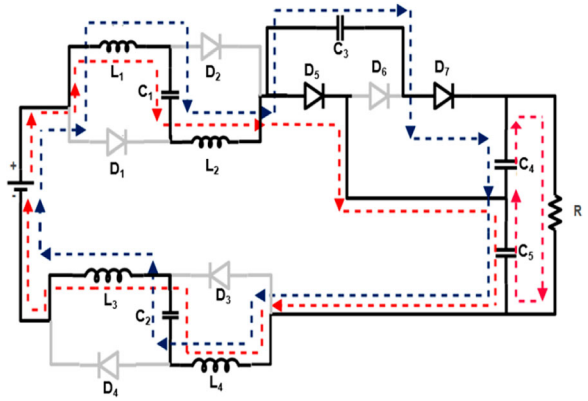

Figure 4. Second mode of operation.

C_2, and C_3 are discharging. The diagram corresponding to the second mode of operation is provided in Figure 4.

The inductor voltage and capacitor current expression during second mode of operation is obtained from Figure 4, after applying KVL & KCL, the Equations are given as (9) and (14)

$$V_{in} - 4V_{L1} + V_{C1} + V_{C3} - V_0 - V_{C2} = 0. \quad (9)$$

$$V_{C5} + V_{C4} = V_0. \quad (10)$$

$$i_{C1} = I_{L1}. \quad (11)$$

$$i_{C2} = I_{L3}. \quad (12)$$

$$i_{C3} = i_{C4} = \frac{I_{L2} - I_{L3}}{2}. \quad (13)$$

$$i_{C5} = I_0 - I_{L3}. \quad (14)$$

2.3. Voltage gain

By applying the volt–sec balance principle to Equations (1), (2), (9) and (10) the steady-state voltage gain expression of the proposed converter is given in Equation (18).

$$\int_0^{T_{on}} V_{in}dt + \int_{T_{on}}^{T} \left(\frac{7V_{in} - V_0}{8}\right) dt = 0 \quad (15)$$

$$V_{in}(d) = -\left[\frac{7V_{in}(1-d) - V_0(1-d)}{8}\right]. \quad (16)$$

$$\frac{8V_{in}d}{(1-d)} = -7V_{in} + V_0. \quad (17)$$

$$\frac{V_0}{V_{in}} = \frac{7+d}{1-d}. \quad (18)$$

2.4. State space modelling

The generalized state space average behaviour of DC-DC converter over a period can be expressed as

$$\dot{x}(t) = Ax(t) + Bu(t). \quad (19)$$

$$y(t) = Cx(t) + Du(t). \quad (20)$$

where $A = A_1d + A_2(1\text{-}d)$, $B = B_1d + B_2(1\text{-}d)$, $C = C_1d + C_2(1\text{-}d)$, $D = D_1d + D_2(1\text{-}d)$ and d is duty cycle.

From Equations (1–8), the state space matrix for first mode of operation is given in Equations (21 & 22).

$$\begin{pmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \dot{i}_{L4} \\ \dot{v}_{C1} \\ \dot{v}_{C2} \\ \dot{v}_{C3} \\ \dot{v}_{C4} \\ \dot{v}_{C5} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{-d}{C_1} & \frac{-d}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-d}{C_2} & \frac{-d}{C_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}$$

$$\times \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{d}{RC_4} & \frac{d}{RC_4} \\ 0 & \frac{d}{RC_5} & \frac{d}{RC_5} \end{pmatrix} \begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{pmatrix}$$

$$+ \begin{pmatrix} \frac{d}{L_1} & 0 \\ \frac{d}{L_2} & 0 \\ \frac{d}{L_2} & 0 \\ \frac{d}{L_4} & 0 \\ 0 & \frac{d}{C_1} \\ 0 & \frac{d}{C_2} \\ 0 & \frac{d}{C_3} \\ 0 & \frac{d}{C_4} \\ 0 & \frac{d}{C_5} \end{pmatrix} \begin{pmatrix} V_{in} & I_{in} \end{pmatrix} \quad (21)$$

$$y = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{pmatrix} \begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{pmatrix} \quad (22)$$

Similarly, the state space equations for the second mode of operation are obtained from Equations (9–14) and are given in Equations (23 and 24). The averaged state space equations of the proposed converter are derived from Equations (21–24) is expressed in Equations (25 and 26).

$$\begin{pmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \dot{i}_{L4} \\ \dot{v}_{C1} \\ \dot{v}_{C2} \\ \dot{v}_{C3} \\ \dot{v}_{C4} \\ \dot{v}_{c5} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & \frac{2(1-d)}{4L_1} \\ 0 & 0 & 0 & 0 & \frac{2(1-d)}{4L_2} \\ 0 & 0 & 0 & 0 & \frac{2(1-d)}{4L_3} \\ 0 & 0 & 0 & 0 & \frac{2(1-d)}{4L_4} \\ \frac{1-d}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1-d}{C_2} & 0 & 0 \\ 0 & \frac{1-d}{2C_3} & \frac{d-1}{2C_3} & 0 & 0 \\ 0 & \frac{1-d}{2C_4} & \frac{d-1}{2C_4} & 0 & 0 \\ 0 & 0 & \frac{d-1}{C_5} & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{pmatrix} + \begin{pmatrix} 0 & 0 & 0 & \frac{-(1-d)}{4L_1} \\ 0 & 0 & 0 & \frac{-(1-d)}{4L_2} \\ 0 & 0 & 0 & \frac{-(1-d)}{4L_3} \\ 0 & 0 & 0 & \frac{-(1-d)}{4L_4} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1-d}{RC_5} & \frac{1-d}{RC_5} \end{pmatrix} + \begin{pmatrix} \frac{1-d}{4L_1} & 0 \\ \frac{1-d}{4L_2} & 0 \\ \frac{1-d}{4L_3} & 0 \\ \frac{1-d}{4L_4} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} V_{in} & I_{in} \end{pmatrix} \tag{23}$$

$$y = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{pmatrix} \begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{pmatrix} \tag{24}$$

$$\begin{pmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \dot{i}_{L4} \\ \dot{v}_{C1} \\ \dot{v}_{C2} \\ \dot{v}_{C3} \\ \dot{v}_{C4} \\ \dot{v}_{c5} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1-2d}{C_1} & \frac{1-2d}{C_1} & 0 & 0 \\ 0 & 0 & \frac{1-2d}{C_2} & \frac{1-2d}{C_2} \\ 0 & \frac{1-d}{2C_3} & 0 & 0 \\ 0 & \frac{1-d}{2C_4} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} \frac{2(1-d)}{4L_1} & 0 & 0 & 0 & \frac{-(1-d)}{4L_1} \\ \frac{2(1-d)}{4L_2} & 0 & 0 & 0 & \frac{-(1-d)}{4L_2} \\ \frac{2(1-d)}{4L_3} & 0 & 0 & 0 & \frac{-(1-d)}{4L_3} \\ 0 & 0 & 0 & 0 & \frac{-(1-d)}{4L_4} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{d}{RC_4} & \frac{d}{RC_4} \\ 0 & 0 & 0 & \frac{d}{RC_5} & \frac{d}{RC_5} \end{pmatrix} \begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{pmatrix} + \begin{pmatrix} \frac{1+3d}{4L_1} & 0 \\ \frac{1+3d}{4L_2} & 0 \\ \frac{1+3d}{4L_3} & 0 \\ \frac{1+3d}{4L_4} & 0 \\ 0 & \frac{d}{C_1} \\ 0 & \frac{d}{C_2} \\ 0 & \frac{d}{C_3} \\ 0 & \frac{d}{C_4} \\ 0 & \frac{d}{C_5} \end{pmatrix} \begin{pmatrix} V_{in} & I_{in} \end{pmatrix} \tag{25}$$

$$y = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{pmatrix} \begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{pmatrix} \tag{26}$$

3. Design of passive component

3.1. Design of inductor

The inductor design of proposed converter is depends on input current ripple (Δi_L), switching frequency (f_s)

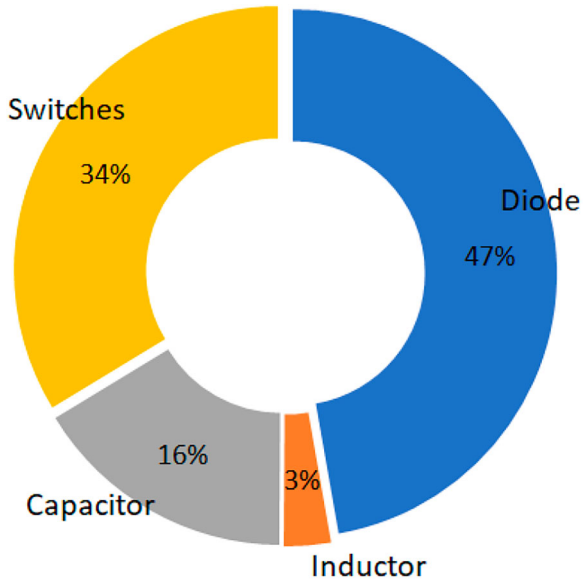

Figure 5. Power loss distribution curve.

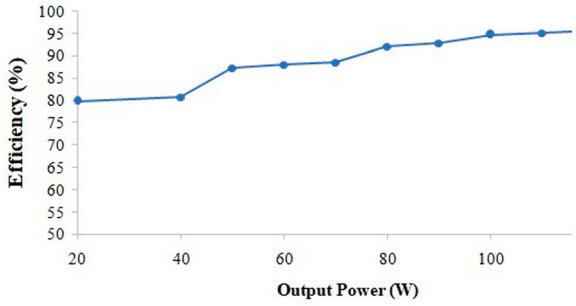

Figure 6. Efficiency against output power.

and duty ratio. The values for the inductors are designed from the Equations (27–31).

$$V_{L1} = V_{L2} = V_{L3} = V_{L4} = V_{in}. \tag{27}$$

$$V_{in} = L_1 \frac{di_{L1}}{t_1}. \tag{28}$$

$$V_{in} = L_1 \frac{\Delta I_{L1}}{DT}. \tag{29}$$

$$L_1 = \frac{V_{in} \times DT}{\Delta I_{L1}}. \tag{30}$$

$$L_2 = \frac{V_{in} \times D}{f \Delta I_{L2}}. \tag{31}$$

3.2. Selection of capacitor

The capacitor selection is based on switching frequency (f_s), duty ratio (d), output current (I_0), voltage ripple (ΔV_C). The output capacitors C_4 & C_5 and capacitors C_1, C_2 and C_3 are selected based on the equations (32–36)

$$C_1 = \frac{\text{Vin}((3 + \text{D})}{\text{R}\, f_s (1 - \text{D}) \Delta V_{C1}}. \tag{32}$$

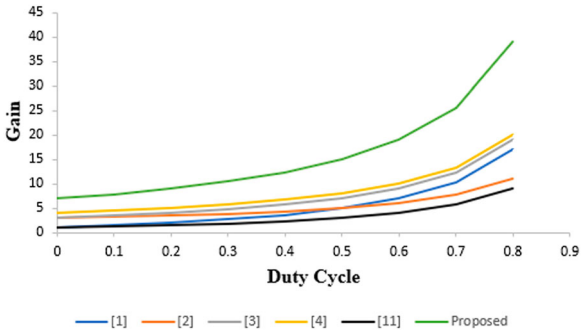

Figure 7. Gain comparison with a duty cycle.

$$C_2 = \frac{\text{Vin}(3 + \text{D})}{\text{R}\, f_s (1 - \text{D}) \Delta V_{C2}}. \tag{33}$$

$$C_3 = \frac{I_0}{\text{f} \Delta V_{C3}}. \tag{34}$$

$$C_4 = \frac{I_0 D}{\text{f} \Delta V_{C4}}. \tag{35}$$

$$C_5 = \frac{(1 + \text{D})}{\text{f} \Delta V_{C5}}. \tag{36}$$

3.3. Stress across the power semiconductor devices

Voltage stress and current stress of the power switches S_1 and S_2 in terms of output voltage and current during the first and second mode of operation is obtained and given in the equations (37 and 38).

$$V_{s1,s2} = \frac{(1 + d) V_0)}{3 + 5d}. \tag{37}$$

$$I_{S1,S2} = \frac{I_0 (1 + d)}{(1 - d)\sqrt{d}}. \tag{38}$$

The voltage across the power diodes and the average diode current in the converter is obtained from Figures 3 and 4 and given in equations (39–41)

$$V_{d1,d2,d3,d4} = \frac{V_{in}}{1 - d}. \tag{39}$$

$$V_{d5} = V_{d6} = V_{d7} = \frac{4V_0}{7 + d}. \tag{40}$$

$$I_d = I_0. \tag{41}$$

The inductor current of the proposed converter is obtained by using the Equation (42).

$$I_L = \left(\frac{3 - d}{1 - d}\right) I_0. \tag{42}$$

3.4. Power loss calculation

The non-idealities of semiconductor devices are considered as a reason for power loss. The converter performance is verified by doing power loss manipulations. The inductor ripple current and capacitor ripple voltage is neglected to simplify the analysis. The losses in

Table 1. Proposed converter comparison with the converters.

Topology	Number of components N_s	N_d	N_l	N_c	$\%\Delta I_{in}$	Max. current stress on switch	Max. voltage stress on switch	Voltage stress on diode	Max. efficiency (%)	Voltage gain
Ref. [1]	2	2	3	3	Medium	$\frac{2P_0\sqrt{d}}{V_{in}(1+3d)}$	$\frac{V_{in}}{1-d}$	$\frac{2V_{in}}{1-d}$	95.5%	$\frac{1+3d}{1-d}$
Ref. [2]	1	4	1	4	Medium	$\frac{2I_0}{1-d}\sqrt{d}$	$\frac{V_{in}}{1-d}$	$\frac{I_0}{\sqrt{d}}$	95.44%	$\frac{3-d}{1-d}$
Ref. [3]	2	5	4	3	Medium	$\frac{I_0(1+d)}{(1-d)\sqrt{d}}$	$\frac{2V_{in}}{1-d}$	$\frac{V_0}{R\sqrt{1-d}}$	96.53%	$\frac{3+d}{1-d}$
Ref. [4]	2	4	2	4	Max	$\frac{I_{in}}{2}$	$\frac{V_{in}}{d}$	$\frac{V_0}{2}$	95.60%	$\frac{4}{1-d}$
Ref. [11]	2	3	2	2	Medium	$\frac{I_{in}}{2}$	$\frac{V_0-V_{in}}{2}$	$\frac{V_0+V_{in}}{2}, V_0$	93%	$\frac{1+d}{1-d}$
Proposed Converter	2	7	4	5	Max	$\frac{I_0(1+d)}{(1-d)\sqrt{d}}$	V_{in}	$V_{d1-4}=\frac{V_{in}}{1-d}$ $V_{d5-7}=\frac{4V_0}{7+d}$	96.54%	$\frac{7+d}{1-d}$

Table 2. Simulated parameters of proposed converter.

Parameters	Values
Input voltage	24 V
Output voltage	240 V
Output power	120 W
Switching frequency	20 kHz
Inductor	$L_1 = L_2 = L_3 = L_4 = 330\,\mu H$
Capacitor	$C_1 = C_2 = C_3 = 220\,\mu F C_4 = C_5 = 470\,\mu F$

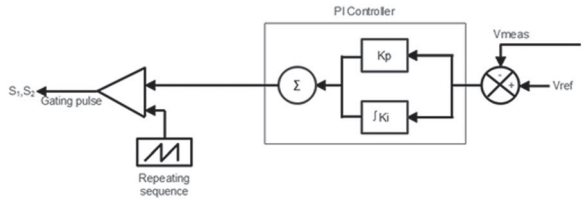

Figure 8. Block diagram of PI controller.

Table 3. Voltage, current and power values under line voltage variation.

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency (%)
20	6.5	139.96	240	0.5	120	92.24
24	5.236	123.288	240	0.5	120	95.495
28	4.464	158.144	240	0.5	120	96.01

diodes, capacitors, switches, inductors are considered as power losses in DC-DC converters. The parasitic resistance in the inductors (r_L), capacitors (r_C), ON resistance of the diode (r_d) and forward cut-in voltages (V_f) are considered for the power loss calculations. The power losses are calculated for the output power of 120 W, output voltage of 240 V, $r_d = 0.1\Omega$, $r_C = 0.08\Omega$, $r_{C0} = 0.13\Omega$,$V_f = 0.8$V

3.4.1. Power loss in diode

In the proposed converter, power losses due to diodes is due to ON state resistance and forward cut-in voltage and are determined by using the equations (43–45).

$$i_{d1,d2,d3,d4}^{rms} = \frac{V_0}{R\sqrt{d}}. \tag{43}$$

$$i_{d5,d6,d7}^{rms} = \frac{V_0}{R\sqrt{(1-d)}}. \tag{44}$$

$$P_d^{Loss} = \sum_{n=1}^{7} V_{fn} i_{dn}^{avg} + r_{dn} i_{dn}^2. \tag{45}$$

$$P_d^{Loss} = 2.65W. \tag{46}$$

3.4.2. Power loss in inductor

The power loss in the inductor is calculated by neglecting the ripple current and can be obtained by using the equations (47–49).

$$i_L^{rms} = \frac{V_0}{R(1-d)}. \tag{47}$$

$$P_L^{loss} = \sum_{n=1}^{4} i_{Ln}^2 r_{Ln}. \tag{48}$$

$$P_L^{loss} = 1.61\text{W} \tag{49}$$

3.4.3. Power loss in capacitor

Neglecting the ripple voltage, the power loss in the capacitor is computed by using the equations (50–53).

$$i_{C1,c2}^{rms} = \frac{V_0}{R\sqrt{d(1-d)}}. \tag{50}$$

$$i_{C3,c4,c5}^{rms} = \frac{V_0\sqrt{(1-d)}}{R\sqrt{d}}. \tag{51}$$

$$P_C^{loss} = \sum_{n=1}^{5} i_{Cn}^2 r_{cn}. \tag{52}$$

$$P_C^{loss} = 0.91\text{W}. \tag{53}$$

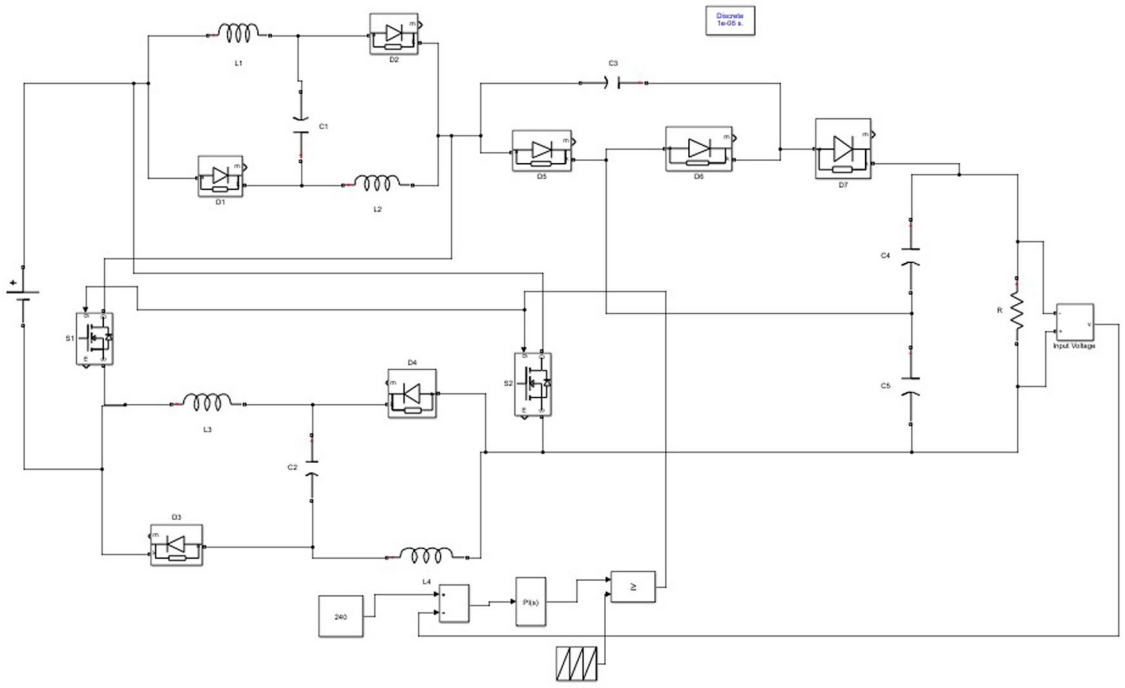

Figure 9. Closed Loop simulink model of proposed converter.

3.4.4. Power loss in switch

The power losses in semiconductor switches are mainly due to conduction loss and switching loss. The switching loss is mainly due to turn on and turn off time. The ON-state resistance of the switch is responsible for conduction loss. The total loss in the switch is calculated by considering d = 0.273, $r_{sw-on} = 0.1\Omega$, $t_{on} = 23$ ns, $t_{off} = 150$ ns, $f_s = 20$ kHz. The total power loss due to switches is obtained from the equation (54–56).

$$P_{sw}^{loss} = P_{sw}^{Cond.loss} + P_{sw}^{switchloss}. \tag{54}$$

$$P_{sw}^{loss} = \frac{2V_0{}^2(1+d)^2 V_{sw-on}}{d(1-d)^2R^2} + \frac{2V_0{}^2(1-d)(t_{on}+t_{off})f_s}{R(d+3)(1-d)d}. \tag{55}$$

$$P_{sw}^{loss} = 1.89\text{W}. \tag{56}$$

The total power loss of the proposed converter is given in Equation (57) and efficiency of the converter for the output power of 120W is calculated by using the Equation (59).

$$P_{loss}^{total} = P_{sw}^{loss} + P_C^{loss} + P_L^{loss} + P_d^{Loss}. \tag{57}$$

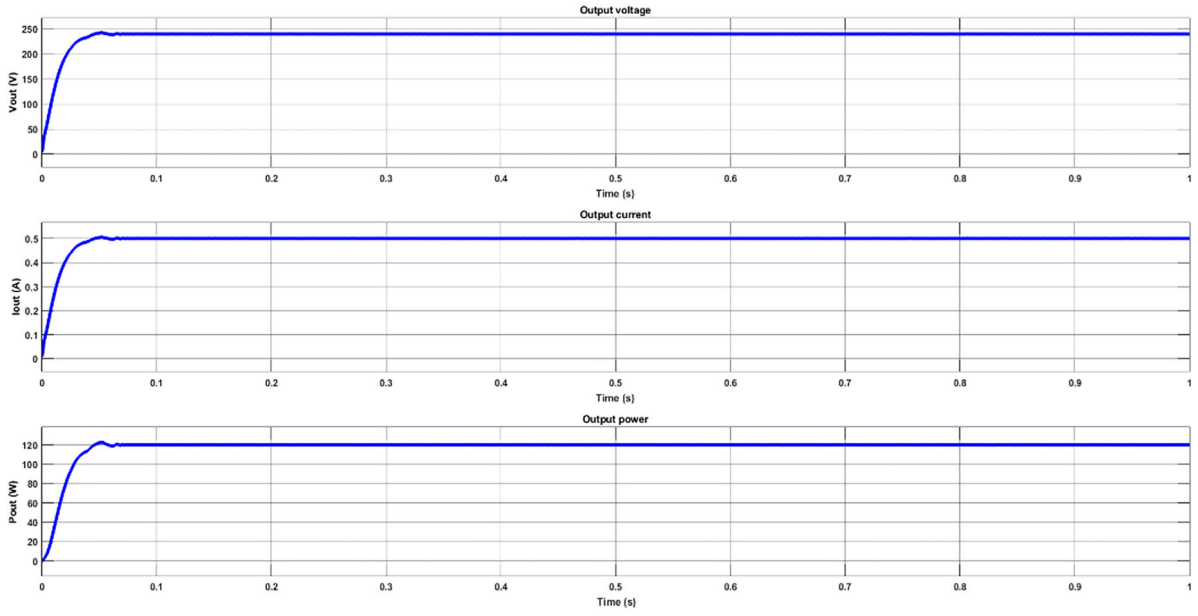

Figure 10. Closed loop simulated output voltage, current and power waveforms.

$$P_{loss}^{total} = 5.61\text{W}. \quad (58)$$

$$\eta = \frac{P_0}{P_0 + P_{loss}^{total}} = \frac{100}{100 + 5.61} = 94.68\%. \quad (59)$$

The distribution of power loss of the semiconductor devices are presented in the Figure 5. The maximum power loss occurs in power diodes followed by switches, capacitors and inductors. The efficiency of the proposed converter using the voltage gain and the total power loss is pictured in Figure 6. The converter attains the maximum of efficiency of 95.53% at the rated load power condition.

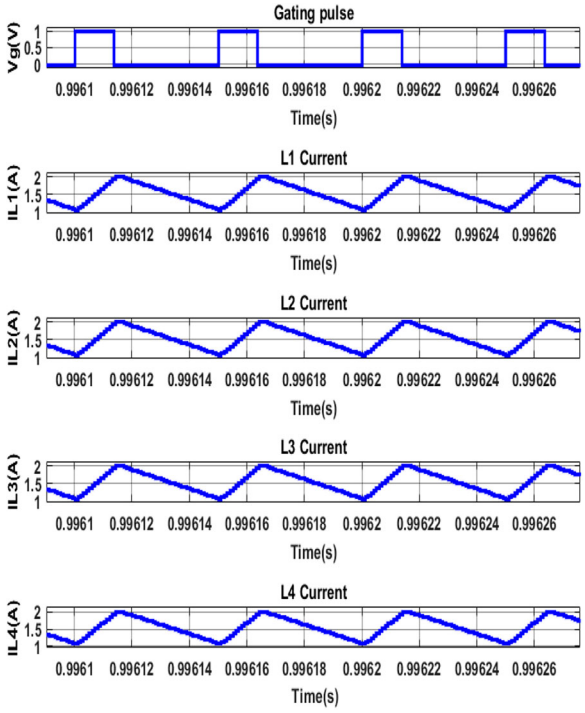

Figure 11. Simulated Inductor current waveforms.

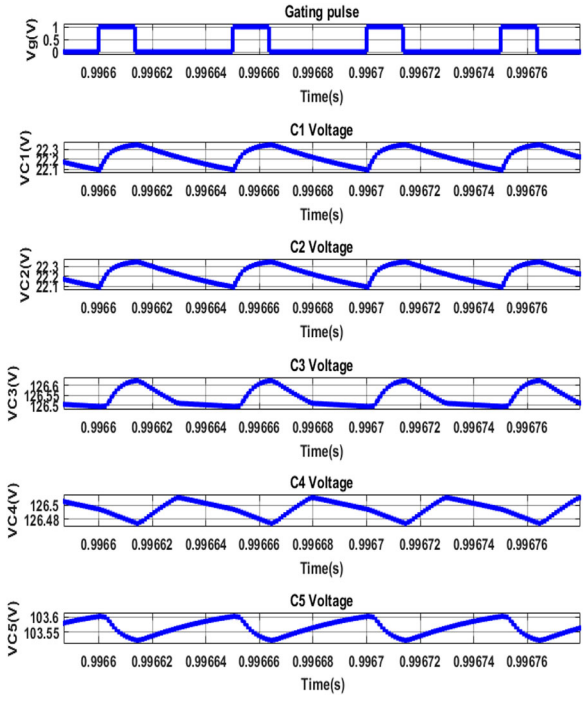

Figure 12. Simulated Capacitor Voltage waveforms.

Table 4. Voltage, current and power values under the variation of reference voltage.

V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{ref} (V)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency (%)
24	3.557	85.368	200	200	0.4175	120	96.77
24	5.128	123.288	240	240	0.5	120	97.495
24	6.923	188.016	280	280	0.5829	120	98.22

Table 5. Voltage, current and power values under load power variations.

Load (%)	V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	Efficiency (%)
40	24	2.282	54.762	240	0.2	48	87.642
60	24	3.288	78.912	240	0.3	72	91.24
100	24	5.137	123.288	240	0.5	120	97.495

Table 6. Hardware specifications.

Parameters	Values
Input voltage	24 V
Output voltage	240 V
Output power	120 W
Inductors L_1–L_4	330 µH, 10 A
Capacitors	$C_1 = C_2 = 220$ µF, 50 V $C_3 = 220$ µF, 250 V $C_4 = C_5 = 470$ µF, 200 V
Diodes D_1–D_7	MUR3060, 10 A, 200 V
Power switch	IRFP460, 200 V, 40 A

4. Comparative analysis

The comparative analysis of the proposed converter with the existing converter topology is discussed in this section. The voltage gain, voltage stress, current stresses of the devices, input ripple current are considered as a comparative metrics and are tabulated in Table 1. Figure 7 depicts a voltage gain comparison of proposed converter with the other converters in the literature. The voltage gain of the proposed converter is 43.59% more than the gain obtained in [1] for the duty ratio of 0.8. Though the number of components in the proposed converter is more when compared with the other converters, the duty ratio of 0.273 is sufficient to get the voltage gain of 10. The voltage stress of the proposed converter is 27% less than the converter in [11]. One of the downside of the proposed converter is the high input current ripple.

5. Simulation results of the proposed converter

The performance of the proposed converter is simulated using MATLAB simulink environment. The converter circuit parameters are calculated using the equations (30–36) and the values are tabulated in

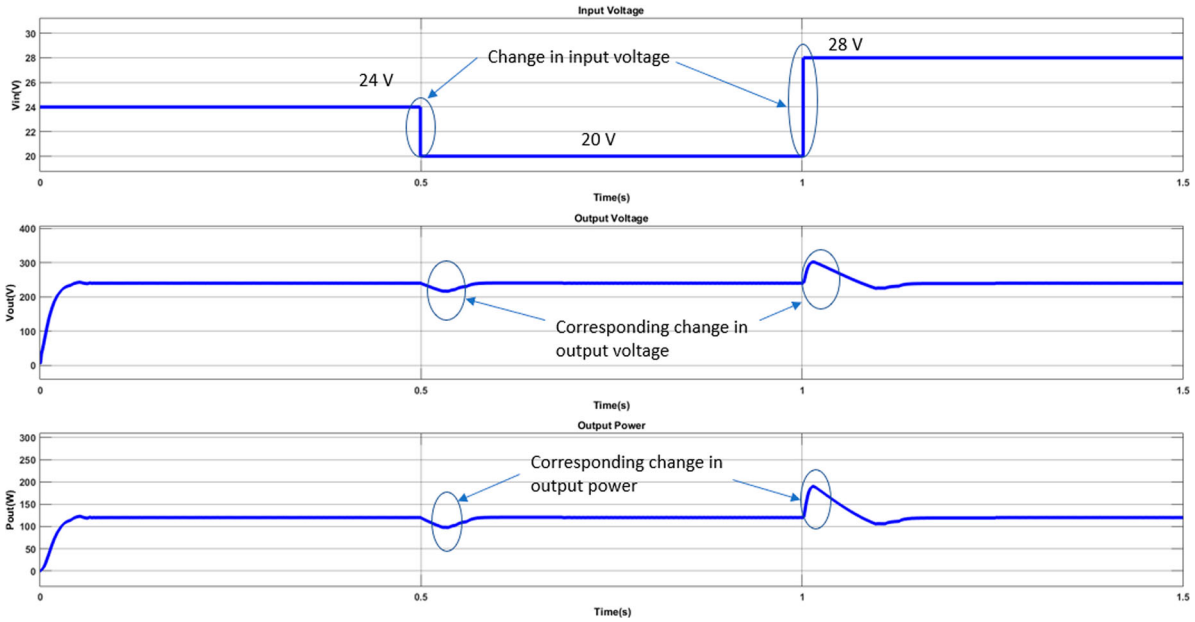

Figure 13. Simulated Line voltage regulation waveforms.

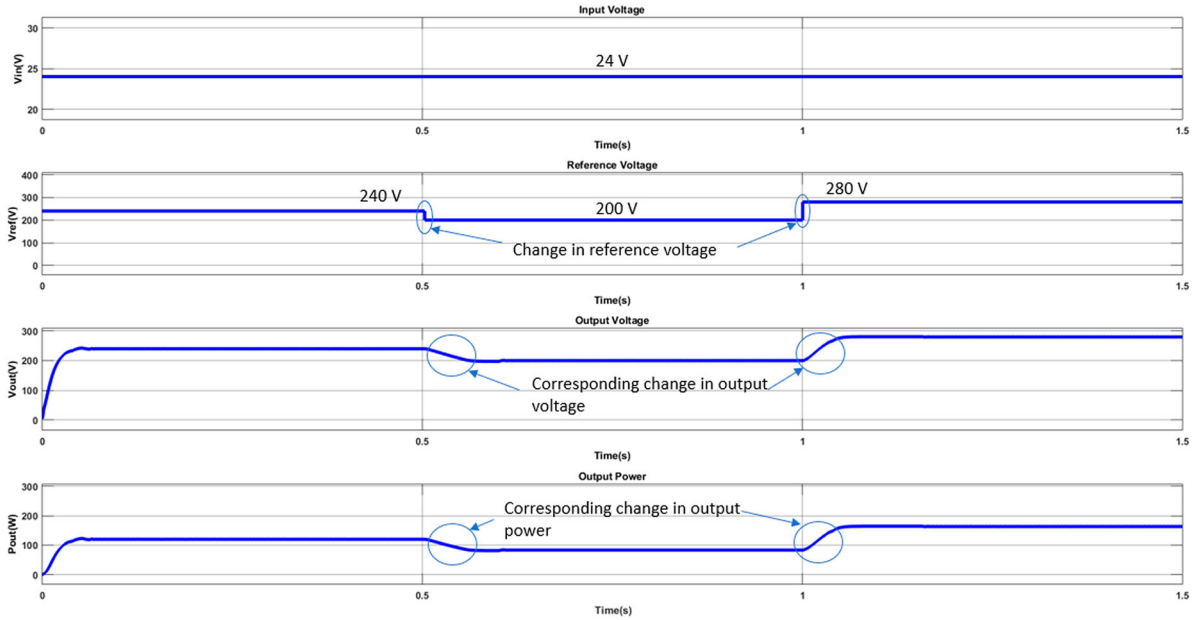

Figure 14. Simulated Reference voltage variation waveforms.

Table 2. The proposed converter is designed to maintain the output voltage of 240 V for the input voltage of 24 V. To maintain the constant output voltage, PI controller is employed. The controller parameters are tuned using Z-N method. The values of K_p and K_i are 0.01, 235 and 0.7687. The block diagram of PI controller is presented in Figure 8. The closed loop simulink model of proposed converter is shown in Figure 9.

The resistive load is considered for converter performance analysis. The simulated voltage, current and power waveforms at the output of converter is shown in Figure 10. The PI controller employed in the converter regulates the output voltage and maintain at 240 V. Likewise, the inductor current waveforms are shown in Figure 11. When the switch is on, the inductors (L_1, L2, L3, & L_4) in the switched inductor cell get charged and dissipate its stored energy when the switch is off. The voltage waveforms of the capacitors in the switched inductor cell (C_1, C_2) and voltage multiplier cell (C_3, C_4, C_5) are pictured in Figure 12.

The performance of the converter with the controller under transient condition is also be analyzed by varying the reference voltage, source voltage and load power.

5.1. Performance analysis of converter under line voltage variation

The line voltage of the converter is varied from 4 V above than the designed input voltage range and 4 V

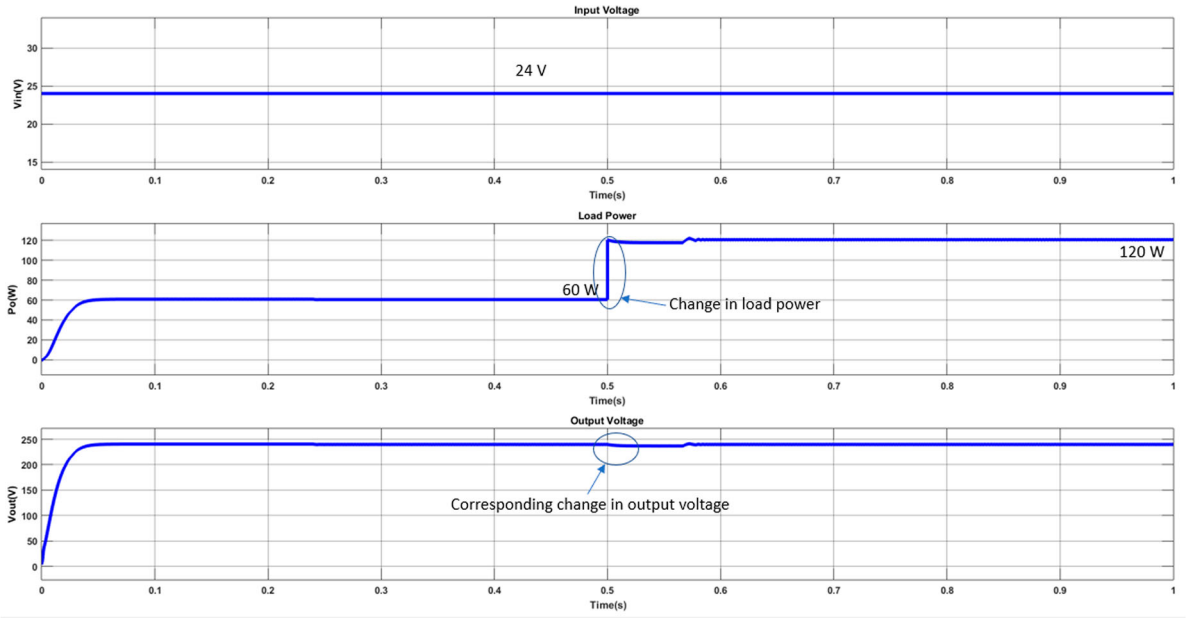

Figure 15. Simulated Load Power variation waveforms.

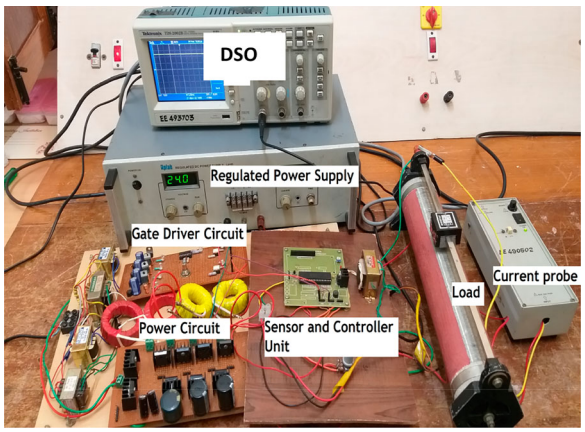

Figure 16. Hardware setup.

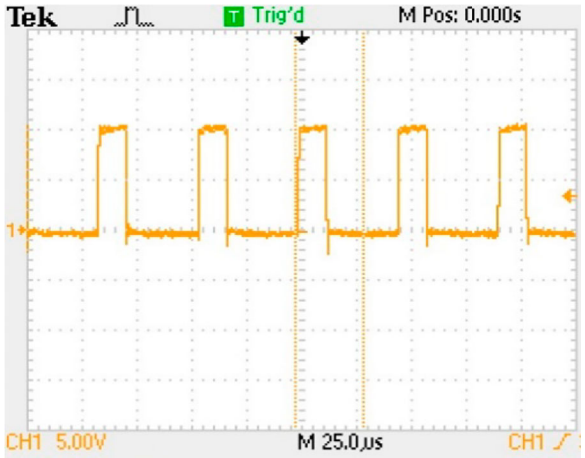

Figure 17. Gating pulse waveform.

below the designed value. The line voltage is varied at different time intervals. At time t = 0, the line voltage is kept as 24 V, the converter maintains the load voltage of 240 V. At time t = 0.5s, the line voltage is reduced from 24 V to 20 V. The controller has to tracks the change

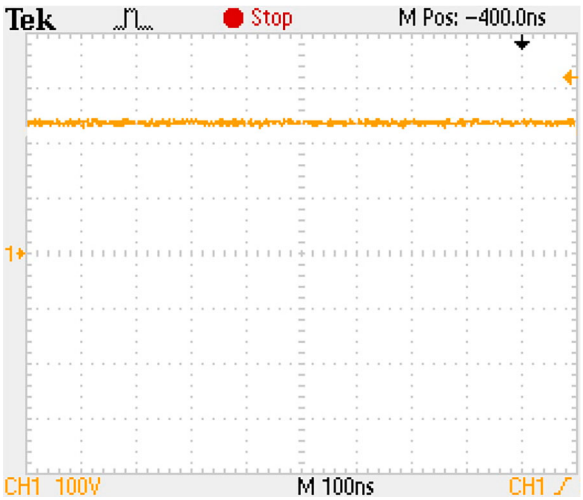

Figure 18. Output voltage Waveform for the source voltage of 24V.

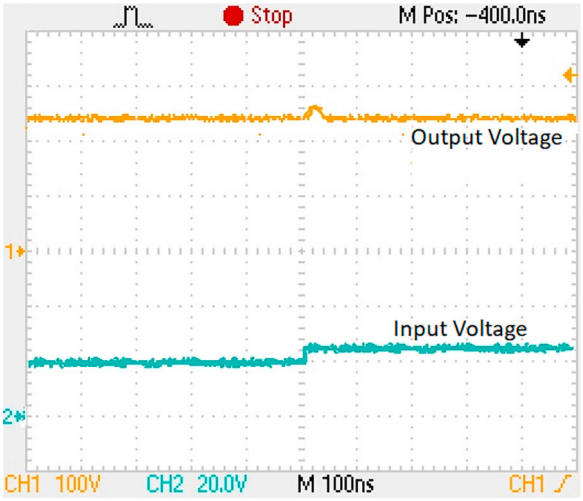

Figure 19. Line Voltage Regulation waveform under dynamic change in Input voltage from 20 V to 24V.

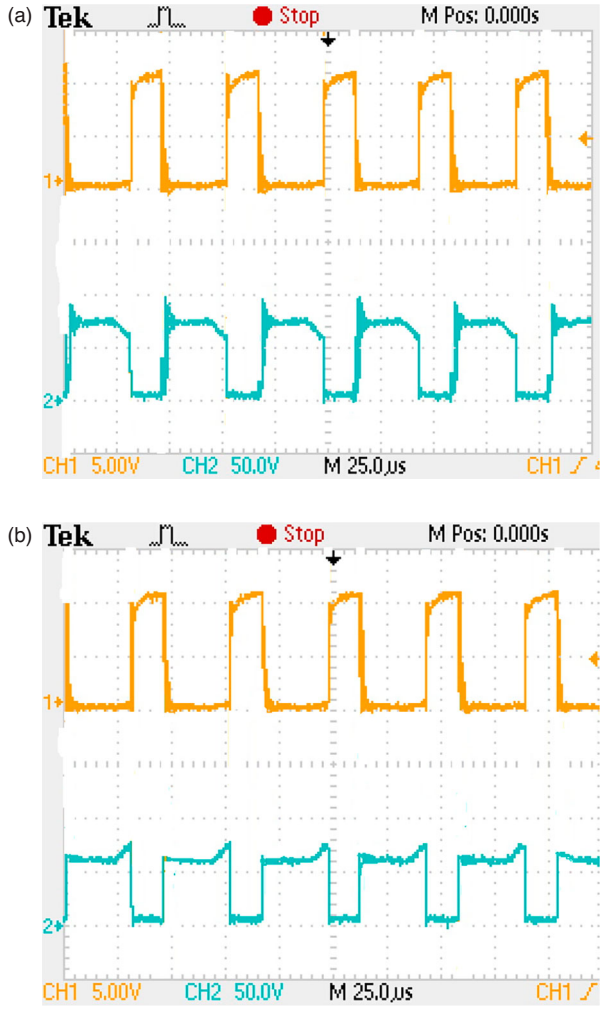

Figure 20. (a): Switch S_1 Voltage Waveform. (b): Switch S_2 voltage waveform.

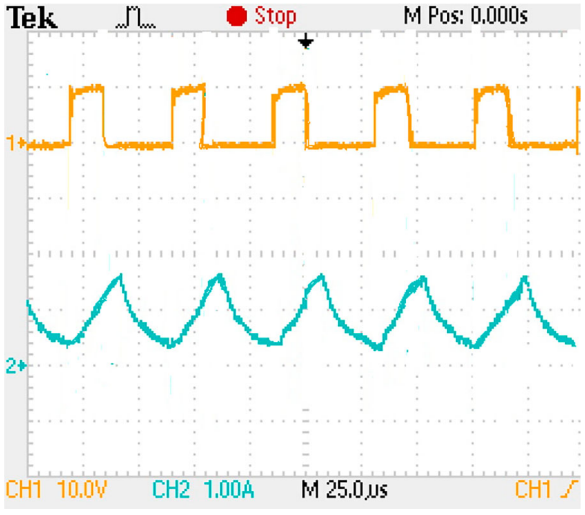

Figure 21. Inductor Current (I_{L1}, I_{L2}, I_{L3}, I_{L4}) Waveforms.

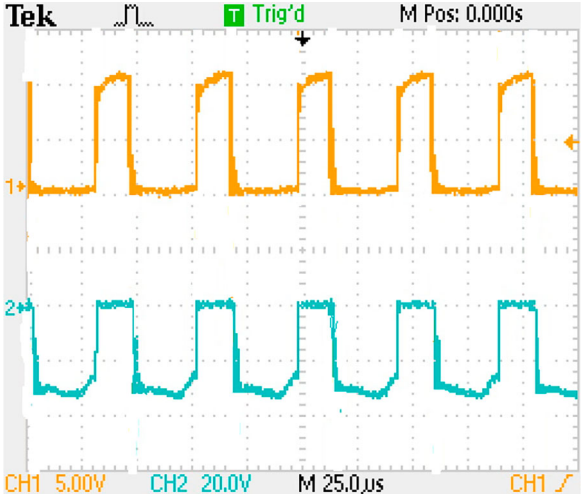

Figure 22. Diodes D_1, D_2, D_3 voltage waveform.

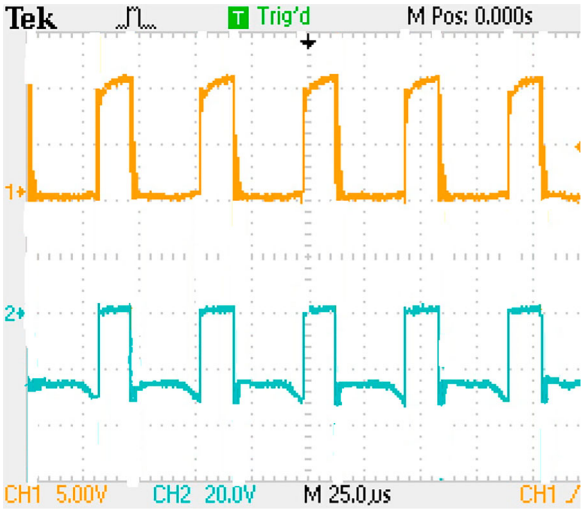

Figure 23. Diode D_4, D_5 voltage waveform.

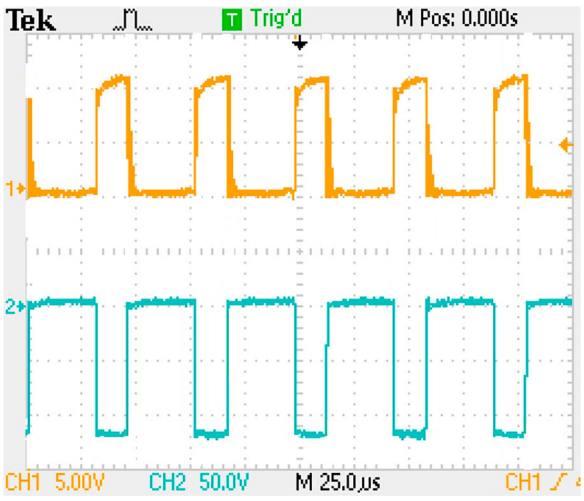

Figure 24. Diode D_6 voltage waveform.

in line voltage and generates the required gate signal to regulate the output voltage to 240 V. The controller takes less than .02s to regulate the output voltage. Likewise, at time t = 1s, the line voltage is varied from 20 V to 24 V. The controller takes the increase in line voltage variation and generates the gating pulse to maintain the output voltage. The voltage, current and power values at both input and output of the converter is noted during these variations and are tabulated in Table

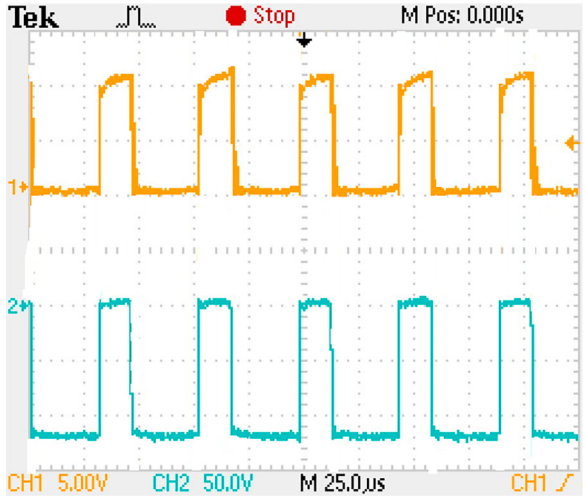

Figure 25. Diode D_7 voltage waveform.

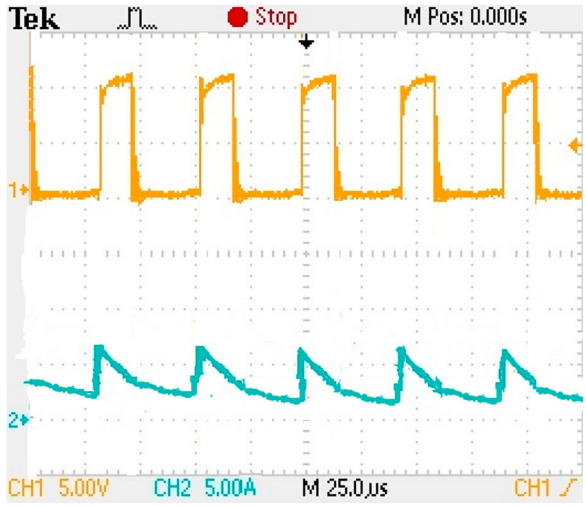

Figure 26. Source current waveform.

3 and the corresponding waveforms are depicted in Figure 13.

5.2. Performance analysis of converter under reference voltage variation

The converter is designed to maintain the output voltage of 240 V. In this case, the controller's ability is analyzed by varying the reference voltage of the converter. The reference voltage is varied at regular interval of time between 200 V to 280 V. At time t = 0s, the reference voltage is maintained at 240 V, the converter maintains this voltage at the output side. At time t = 0.5s, the reference voltage is made 40 V less that the initial value. The PI controller employed in the converter identifies the change in reference voltage and generates the gating signal to maintain the output voltage of 200 V. The change in reference voltage variations and the corresponding variations in output voltage and power are shown in Figure 14 and the values are tabulated in Table 4.

5.3. Performance analysis of converter under load power variation

In this case, the load power of the converter is varied from 40%, 60% and 100% of rated load condition. These variations are made at constant time intervals. The controller effectively tracks the change in load power variations and maintains the output voltage. The variation in change in load power and the corresponding variations in output voltage is given in Figure 15 and the corresponding voltage, current and power values are tabulated in Table 5.

6. Hardware implementation

In section 5, the converter performance is analysed in simulation environment. To validate the simulated results, hardware prototype type model is developed. The experimental model of the proposed converter is developed by considering the parameter values tabulated in Table 6. The hardware prototype model of the proposed converter is shown in Figure 16. The gate driver circuit generates the required gating signal for the converter switches. The prototype model is developed for the input voltage of 24 V, output voltage of 240 V and the power rating of 120W.

Based on the Equation (18), the output voltage of 240 V is attained for the source volatge of 24 V, duty ratio of 0.273. The gating signal required to achieve the required output voltage is generated using PIC microcontroller and the gate driver IC TL494. The gating pulse waveform is shown in Figure 17. The theoritical output voltage of 240 V is attained for the duty ratio of 0.273 while the output voltage of about 240 V is generated experimentally and shown in Figure 18. The result validaes the proposed converter attains the voltage gain of 10 at 0.273 duty ratio. Likewise, the transient behaviour of the converter with the controller is anlaysed experimentally by applying change in source voltage. Initially, the source voltage of 20 V is applied to the converter, the output voltage of 240 V is maintained and the source voltage is varied from from 20 V to 24 V, the controller tracks the change in voltage and ragulates the output voltage of 240 V and shown in Figure 19. In Figure 20(a,b) shows the voltage across the switches, S_1 and S_2. The theoritical value of voltage across the switch is about 61 V. The experimental result validates the same. The inductor current waveforms of the proposed converter is shown in Figure 21. The diode voltages waveforms are given in Figure 22, Figure 23, Figure 24 and Figure 25. The theoritical diode voltage across the diodes D_6 and D_7 are 112 V, whereas the experimental values are around 110 V. The source current waveform of proposed converter is depicts in Figure 26. In Figure 26, the These experimental results validates the simulated and theoritically calculated values. Thus the operation of the converter has been experimentally validated.

7. Conclusion

The non-isolated DC-DC high-gain converter suitable for renewable energy applications is proposed in this work. The power switches in the converter turned ON simultaneously make the inductor in the switched inductor cell charge the inductor with the source voltage. During turn OFF condition, the energy stored in the inductor is delivered to the load. The voltage multiplier cell in the converter is used to increase the output voltage and improves the voltage gain. The operating modes, steady-state analysis, voltage and current stress analysis and efficiency analysis are made. The converter's performance under closed-loop conditions is analyzed for varying source voltage, reference voltage and load power variations. The simulated and experimental efficiency of 96.54% and 95.2%, respectively, is achieved with a duty ratio of 27.3% under rated conditions. The continuous source current at the input side makes the converter suitable for renewable energy applications such as electric vehicles, UPS, light emitting diode and DC distribution systems.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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