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A new frequency control method to enhance fault ride-through capability of VSC-HVDC systems supplying industrial plants

Mahmudreza Changizian, Amirreza Mizani, Abbas Shoulaie *

Department of Electrical Engineering, Iran University of Science and Technology (IUST), Heidarkhani St., Narmak, 16844, Tehran, Iran

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ABSTRACT

Voltage sags is one of the most important issue of power quality, which can disrupt industrial process and impose huge costs on industrial plants. For improving disturbance ride-through capability of voltage source converter based on high voltage direct current (VSC-HVDC) supplying industrial plant, an auxiliary frequency controller is proposed to control output voltage frequency at inverter station. Since industrial loads are more sensitive to voltage drops compared to frequency deviations, output voltage frequency is slightly deceased based on DC-link voltage changes during disturbances in proposed control scheme in order to prevent voltage collapse and provide desirable voltage quality for industrial plants; hence, the continuity of industrial process will be ensured. The case study is a part of a real industrial plant and variations of DC-link voltage, AC buses voltages, induction motors speed, and performance of adjustable speed drive are investigated when the proposed method is used during faults. In proposed method, voltage drop across industrial plant during a severe fault is less than other methods and dynamic performance of system is improved. The case study is simulated under balanced three-phase fault, double line-to-ground fault, and single line-to-ground fault in PSCAD/EMTDC, and results verify the validity of the proposed control scheme.

1. Introduction

Generally, voltage sag constitutes around 65% of power quality disturbances in the utility system [1]. Also, it occurs in industrial plants resulting in a number of problems because of the high sensitivity of industrial equipment to voltage sags. Hence, voltage sag is the most important issue of power quality in industrial plants [2, 3]. As reported in literatures, motor contactors will be tripped at 30% voltage drop or even less than that causing a motor stalling [4] as well as the only 15% voltage drop is the critical point in adjustable speed drives (ASDs) [1]. Programmable logic controller, personal computer and High-Intensity Discharge Lamps are the other most sensitive devices to voltage sag in industrial plants [3, 5–7]. Therefore, voltage sag can cause an interruption in industrial process and impose huge costs on industrial plants [2, 8].

Nowadays, the usage of voltage source converter based on high voltage direct current (VSC-HVDC) in utility system is expanding due to its benefits, namely the ability to flexibly control power flows [9], connecting capability to weak grid and passive network [10], and improving power quality [11, 12].

Although the transmission power to DC-link get limited in VSC-HVDC system in the sending side at the time of fault occurrence, it could play important role in power quality improvement due to the high ability to flexibly control power flows. It is just necessary to be improved control structure in order to prevent voltage collapse during fault occurrence. Therefore, the frequency controller at the receiving side converter in VSC-HVDC transmission system have been proposed in the several researches [12–17] in order to reduce voltage drop and prevent voltage collapse. Since industrial plants are more sensitive to voltage drops as opposed to frequency deviations, this approach will be realized by slightly decreasing the VSC output voltage frequency[12]. In [12], it is proposed the frequency controller based on electrical energy fluctuation in the DC capacitors. The complex determination of the controller coefficient is the main problems of this method. Also, the controller has not set the frequency at the receiving side in steady-state operation, so the system cannot be started reliably. In [14], the frequency controller based on AC output voltage variations is presented. The problem with this method is the high voltage drop during the fault, which is more than the acceptable value mentioned for industrial equipment, which are sensitive to voltage. Furthermore, this control strategy may not make

* Corresponding author.
E-mail address: shoulaie@iust.ac.ir (A. Shoulaie).

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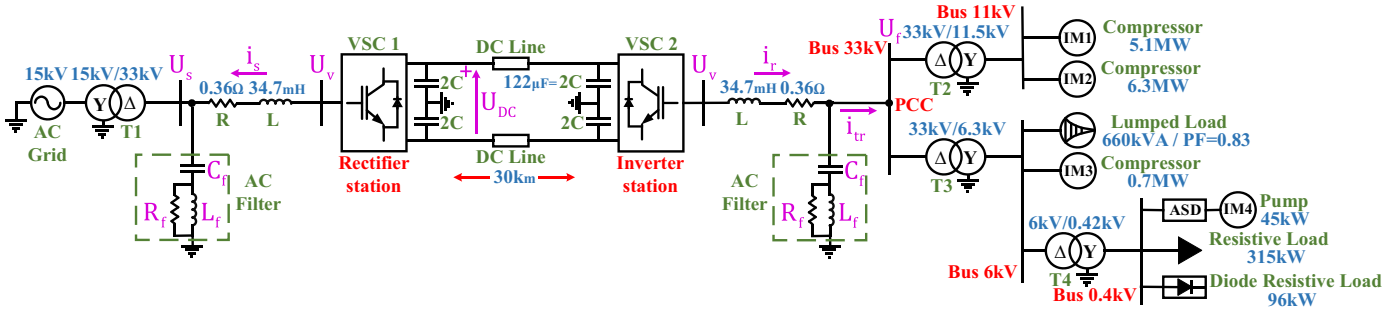

Fig. 1. The case study.

industrial plants ride through severe faults and the occurrence of voltage collapse is possible. In [13, 15–17], AC voltage and frequency controllers are proposed at receiving side converter. The main idea of this strategy is based on power-frequency characteristic known as the droop of the system in an interconnected system. An active power reference is required to generate the current reference. Hence, the exact value of the active power reference is required, while this value may change in different operating modes of industrial plants and has no fixed values. In addition to the mentioned methods, a feed-forward controller with a nonlinearity compensation is proposed in [18] so as to improve the waveform quality of the output voltage. Although this method can mitigate voltage fluctuation caused by sudden changes of load current, it cannot be suitable for severe disturbances due to the current system limitation during fault occurrence, which are not considered in this strategy. In [19], a new method is developed for the optimal PI controller parameters tuning of VSC-HVDC system with offshore wind farm integration as well. This method could improve restoration system after disturbances and effectively suppress the oscillations of DC-link voltage. But during severe disturbances, this method cannot provide desired voltage quality for industrial loads and voltage collapse is more possible due to imbalance between transmitted power and consumption power in the DC-link. The introduced methods in [12–19] have not been investigated under double line-to-ground fault (DLGF). However, the probability of this fault type is around 17% – 21% in network [8, 20, 21] as well as the phase asymmetry created in this state is relatively higher than single line-to-ground fault (SLGF).

In this paper, it is proposed a new frequency control method for the VSC-HVDC in order to improve the fault ride–through capability and voltage stability in industrial plants. Proposed method controls the output voltage frequency at the receiving side based on DC-link voltage variations. In this paper, the performance of the proposed method is studied under SLGF, DLGF, and balanced three phase fault (3LGF) at the sending side.

The main contributions of this paper are summarized as follows:

(1) Different methods of voltage disturbance ride-through capability of the system are discussed according to the VSC-HVDC characteristics.
(2) The impact of frequency decline on induction motor behavior is analyzed as the dominated load in industrial plant.
(3) A new frequency control method is proposed for the VSC-HVDC in order to improve the voltage stability in industrial plants during voltage sag.
(4) The performance of the proposed method is investigated under 3LGF, DLGF, and SLGF conditions and it is compared to methods in [12] and [14]. The proposed method has better performance in comparison with other methods in terms of different parameters such as minimum AC voltage at industrial plants, minimum DC voltage at DC-link, minimum DC voltage and maximum current at ASD, and maximum speed deviation in induction motors during voltage sag.
(5) The proposed method maintains the minimum AC voltage at an acceptable value for very sensitive loads, when voltage drop occurs under severe faults; hence, the continuity of the industrial process will be ensured and the cost of interruption in industrial process will reduce effectively.
(6) Finally, the proposed scheme is verified by the simulation results in an industrial plant, which is supplying through a bipolar two-level VSC-HVDC system.

2. Case study

2.1. System topology

The case study is shown in Fig. 1. The industrial plant is an offshore gas platform supplied through a bipolar two-level VSC-HVDC transmission system. The industrial plant consists of four induction motors (IMs), ASD, lumped load, diode rectifier load, and resistive load, which are based on a real plant. The voltage sag is one of the most important power quality problems in offshore platform [22, 23]. The voltage sag may cause to stop gas platform production. When the compressor shut down, the restart process is complex and it takes a long time to start-up

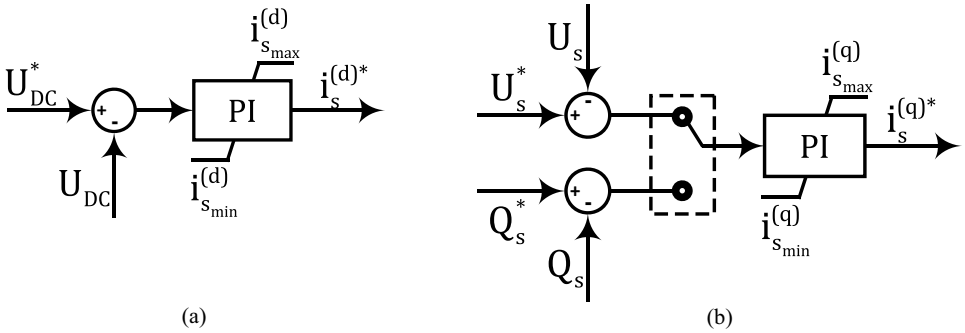

Fig. 2. Outer control loop at rectifier station, (a) DC voltage controller, (b) AC voltage or reactive power controller.

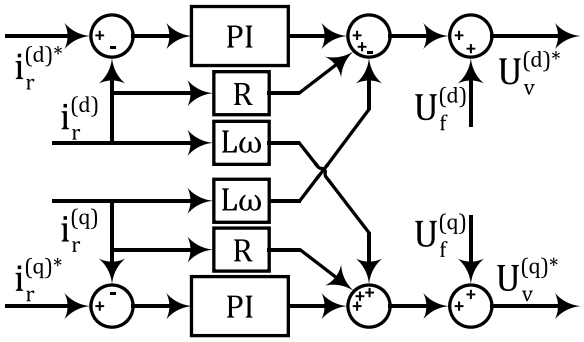

Fig. 3. Inner current control loop at inverter stations.

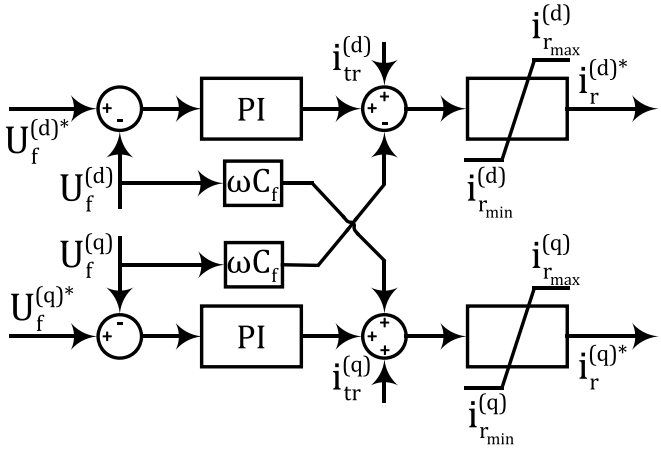

Fig. 4. Outer control loop at inverter station.

again [22]. Hence, voltage sag can cause great economic loss [22]. The specific parameters of IMs are listed in Table 8 in the appendix.

2.2. Control system

The VSC control systems at rectifier and inverter stations include a similar inner current controller and two different outer controllers. The outer control loop at rectifier station includes DC voltage controller and AC voltage or reactive power controller, which is shown in Fig. 2. At inverter station in Fig. 1, the current through the phase reactor and the voltage of the VSC side can be expressed as follow.

$$u_v^{(abc)}(t) = u_f^{(abc)}(t) + Ri_r^{(abc)}(t) + L\frac{d}{dt}i_r^{(abc)}(t) \tag{1}$$

$$i_r^{(abc)}(t) = i_{tr}^{(abc)}(t) + C_f\frac{d}{dt}u_f^{(abc)}(t) \tag{2}$$

Based on [13], the AC filter is purely capacitive at low frequencies, so R_f and L_f are neglected in the vector controller equations. After transforming from three-phase reference frame to rotating reference frame by using Clarke and Park transformations, the Eqs. (3) and (4) can be obtained.

$$u_v^{(dq)}(t) = u_f^{(dq)}(t) + Ri_r^{(dq)}(t) + j\omega Li_r^{(dq)}(t) + L\frac{d}{dt}i_r^{(dq)}(t) \tag{3}$$

$$i_r^{(dq)}(t) = i_{tr}^{(dq)}(t) + j\omega C_f u_f^{(dq)}(t) + C_f\frac{d}{dt}u_f^{(dq)}(t) \tag{4}$$

Based on (3), the block diagram of inner current control loop at inverter stations is shown in Fig. 3. Also based on (4), the block diagram of outer control loop at inverter station is shown in Fig. 4. The dq-axis voltage reference values in Fig. 4 are selected as follows.

$$u_f^{(d)*} = 1\ pu,\ u_f^{(q)*} = 0 \tag{5}$$

When the current exceeds the limit of VSCs current, it is considered two conditions. (I) If the VSC is connected to a strong grid, it will be given high priority to the active reference current so as to keep up the DC voltage. (II) If the VSC is connected to a weak grid or used to supply an industrial plant, it will be given high priority to the reactive reference current so as to keep up the AC voltage [24]. So the current limitation in VSC1 and VSC2 are implemented as follows.

$$for\ VSC1\begin{cases} i_{s_{max}}^{(d)} = I_{lim},\ i_{s_{min}}^{(d)} = -I_{lim} \\ i_{s_{max}}^{(q)} = \sqrt{I_{lim}^2 - \left(i_s^{(d)*}\right)^2},\ i_{s_{min}}^{(q)} = -i_{s_{max}}^{(q)} \end{cases} \tag{6}$$

$$for\ VSC2\begin{cases} i_{r_{max}}^{(q)} = I_{lim},\ i_{r_{min}}^{(q)} = -I_{lim} \\ i_{r_{max}}^{(d)} = \sqrt{I_{lim}^2 - \left(i_r^{(q)*}\right)^2},\ i_{r_{min}}^{(d)} = -i_{r_{max}}^{(d)} \end{cases} \tag{7}$$

Where I_{lim} is the IGBTs current limit, which typically set 1.2 times the total load current. In this paper, an additional outer controller will be proposed at control system of VSC2 in order to improve voltage stability of industrial plant.

3. Enhancement voltage stability in VSC-HVDC system during disturbances

According to the VSC-HVDC characteristics, the voltage disturbance ride-through capability of the system could be improved in different ways, which are discussed as follows.

3.1. Increase of DC-link capacitor size

In VSC-HVDC system, a time constant (τ) is defined as the ratio between the stored energy at rated DC voltage (U_{DCN}) and the rated apparent power of the converter (S_N) [12]. So DC-link capacitor size is obtained as follows.

$$C = \frac{2\tau S_N}{U_{DCN}^2} \tag{8}$$

By increasing DC capacitor size, the stored energy is increased in DC-link and voltage stability is improved during fault and disturbances. On the other hand, the increase in DC capacitor size results in high cost, the VSC station footprint increase, reducing the dynamics of the system and increasing current after fault occurring. Therefore, this method is not appropriate.

3.2. Increase of the converter current limit

Transferred active power to the DC-link is increased during fault by increasing the current limit and rated power of the VSC [13]. So, voltage collapse may be prevented at the inverter station. As the current limit of the converter increases, the cost of the converter valves will rise and its footprint will also become larger. Therefore, this method is not appropriate.

3.3. Decreasing output voltage frequency at inverter station

As mentioned, industrial installations are more sensitive to voltage drops compared to frequency deviations. In order to investigate the effect of frequency reduction on motor behavior, the Thevenin equivalent of the IEEE-recommended circuit for induction motor is considered. It is assumed that the load torque is proportional to square of speed and motor is in steady-state. The supply voltage frequency is reduced as much as 2 Hz in 0.25 s by using a ramp function. It is assumed that the electrical system is in a quasi-steady-state condition at each frequency.

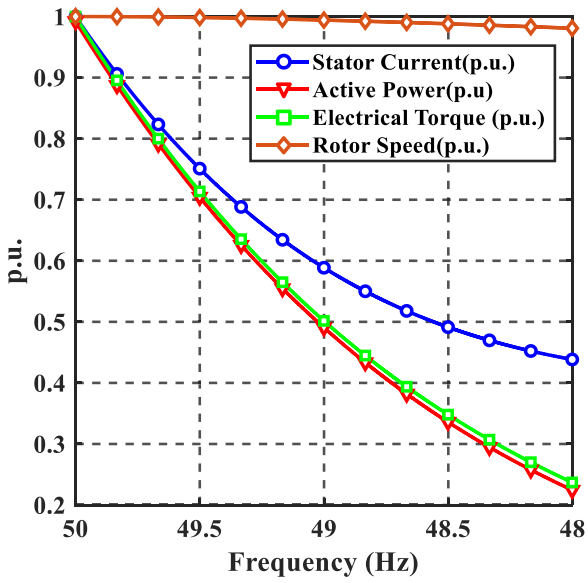

Fig. 5. The variations in stator current, absorbed active power, electrical torque, and motor speed relative to the frequency reduction.

So, the curve variations of absorbed active power, motor speed, and stator current based on frequency changes are shown in Fig. 5. As much as the speed of frequency reduction is faster, the momentary reduction of absorbed active power, electrical torque and stator current are greater in IM.

As a consequent, if the VSC output voltage frequency is slightly decreased during fault intervals in industrial plant including IMs, electrical torque, mechanical torque and absorbed active power of IMs will be reduced. By using this method, a momentary surplus energy is created in IMs according to the inertia of the rotating masses, which can be used to ride through disturbances as well [12]. Drastic drop in electrical torque for a very short period of time in a motor with a large inertia only causes a limited decrease in speed and a reduction in rotational stored kinetic energy, so there is no concern about motor stalling.

4. Proposed control method

As discussed, the appropriate method for improving voltage stability in VSC-HVDC system during fault is to decrease output voltage frequency at inverter station. Hence, a frequency controller is added to the inverter station control system as an outer controller in this paper.

The control of output voltage frequency based on DC-link voltage changes is the main idea of the proposed controller. When a fault occurs at the sending side, DC voltage decreases due to the active power reduction transferred to the DC-link at the rectifier station. The proposed method reduces the output voltage frequency based on the voltage drop at DC-link. Hence, the DC voltage will increase and the voltage stability will improve at the point of common coupling (PCC), because the power consumed from DC-link decreases at the inverter station by reducing frequency. The proposed function for frequency controller is as follows:

$$f_{new} = f^* - \Delta f \tag{9}$$

$$\Delta f = K\gamma\zeta \tag{10}$$

Where f^* is the output voltage reference frequency (50 Hz), f_{new} is the new frequency, which sets the VSC outer controller frequency and K, γ and ζ are defined as follows:

$$\begin{cases} if\ U_{DC} < U_{DCmin} \rightarrow K = 1 \\ if\ U_{DC} > U_{DCmax} \rightarrow K = 0 \end{cases} \tag{11}$$

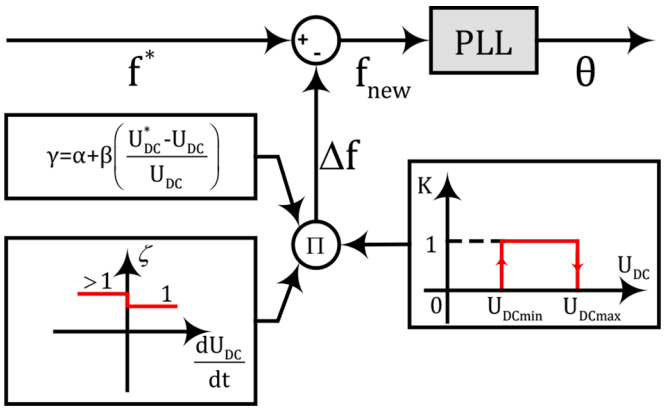

Fig. 6. The proposed frequency controller.

$$\gamma = \alpha + \beta\left(\frac{U^*_{DC} - U_{DC}}{U^*_{DC}}\right) \tag{12}$$

$$\begin{cases} if\ \frac{dU_{DC}}{dt} \langle 0 \rightarrow \zeta \rangle 1 \\ if\ \frac{dU_{DC}}{dt} > 0 \rightarrow \zeta = 1 \end{cases} \tag{13}$$

K factor activates the frequency controller. If the DC voltage is less than U_{DCmin}, the controller will be activated and the frequency is reduced, if the voltage is higher than U_{DCmax}, the frequency controller will be deactivated and the frequency will be set on 50 Hz. U_{DCmin} is determined based on relation between DC voltage and output AC voltage in the inverter:

$$U^*_{Lrms} = \frac{\sqrt{3}}{2\sqrt{2}} m_a U_{DC} \tag{14}$$

Where m_a is modulation index and U^*_{Lrms} is the reference value of the AC voltage at PCC. The maximum value of m_a is equal to 1. So, the minimum value of DC voltage is obtained as follows in order to avoid decreasing the output voltage in PCC;

$$U_{DCmin} = \frac{2\sqrt{2}}{\sqrt{3}} U^*_{Lrms} \tag{15}$$

When DC voltage drops more than U_{DCmin}, the voltage drop occurs on PCC. Therefore, U_{DCmin} is considered to activate the proposed frequency controller.

γ is a variable factor consisting of a fixed term, which is equal to α and a variable term dependent on fluctuation of DC voltage and β. As shown in the previous section, the reduction of momentary absorbed active power in IM gets faster by an abrupt reduction of frequency. For this reason, the γ in proposed method includes a constant value (α) so that the certain value of the reference frequency is quickly reduced, when the frequency controller is activated. Thereby, it improves system dynamics and achieves faster stability. In addition, if the reduction of frequency is not sufficient, γ could surge based on DC voltage decline relative to the reference value and β. Therefore, the output voltage frequency decreases further. α and β are adjustable based on the sensitivity of the industrial load to frequency deviations.

When U_{DC} variations rate is negative ($dU_{DC}/dt < 0$), it means the output power is still greater than the input power in DC-link, ζ is set on greater than 1.0 to further reduce the output frequency. When U_{DC} variations rate is positive, it means the DC voltage is increasing, so ζ set on 1.0. The block diagram of the proposed frequency controller is shown in Fig. 6.

Table 1
Case study parameters.

Symbol	Parameter	Value
S_{rated}	Rated apparent Power	15 MVA
I_{lim} /I_n	VSCs current limit/ total load current	1.2
U_s	Rated AC Voltage at grid side	33 kV
U_f	Rated AC Voltage at PCC	33 kV
U_{DC}	Rated DC Voltage	70 kV
2C	DC Capacitors	122 μF
F	AC frequency	50 Hz
f_s	PWM frequency	1650 Hz
L	AC Reactor inductance	34.7 mH
R	AC Reactor resistance	0.36 Ω

5. Simulation study

The case study shown in Fig. 1 is simulated in PSCAD/EMTDC to verify the proposed control method. The main circuit parameters are presented in Table 1. In this section, the performance of the proposed method is investigated and compared with methods in [12] and [14] to enhance voltage quality of an industrial plant, when a balanced AC fault (3LGF) and unbalanced AC faults (DLGF and SLGF) occur on the sending side. The control parameters of the proposed method set on $U_{DCmin} = 0.77p.u.$, $U_{DCmax} = 0.95p.u.$, $\alpha = 0.5$, $\beta = 2$ and $\zeta = 1.5$ (for $dU_{DC}/dt < 0$), based on system parameters and supposed that industrial load are not sensitive to frequency deviations.

5.1. Balanced three phase fault (3LGF) at the sending side

A balanced three-phase fault with 50% voltage sag is applied at the grid side. The fault is occurred at 0.6 s and cleared 15 cycles later. This duration of temporary fault is enough long to challenge the proposed method. It is shown the dynamic performances of the DC voltage, AC voltage and tracked frequency at the PCC under 3LGF in Fig. 7, when three different frequency control methods are used. As shown in Fig. 7 (a), the DC voltage decreases during the fault interval due to the reduced transmission power to DC link, which is not enough to supply the total load. When the introduced frequency controller in [14] is used, the DC voltage drops to 0.5 p.u. during fault interval and the AC voltage at PCC does not return to its pre-fault level after the fault clearance. Consequently, voltage collapse occurs at industrial plant. By using the proposed frequency controller and the introduced frequency controller in [12], DC voltage drops to 0.75 p.u. and 0.6 p.u. respectively. Hence, the decrease of DC voltage is smaller in these methods than that with the frequency controller method in [14]. In addition, AC voltage at PCC returns to its nominal value after fault clearance, which validates the effectiveness of these methods to prevent voltage collapse.

The voltage drop is more than 20% at PCC by using the introduced controller in [12]; however, this value is less than 8.5% by using the proposed controller. Therefore, the performance of the proposed method is better than the method in [12], which can prevent tripping and malfunctioning very sensitive loads to voltage drop at industrial plant. Rotor speed of IM1, IM2, and IM3 during the 3LGF with the proposed method is shown in Fig. 7(d). As is clear, the speed of motors decline by reducing frequency. The drop in speed of the IMs is around 3%, which is acceptable in that speed-sensitive processes typically are not powered directly by IMs. Minimum voltages at different buses by using the proposed method, methods in [12] and [14] are presented in Table 2.

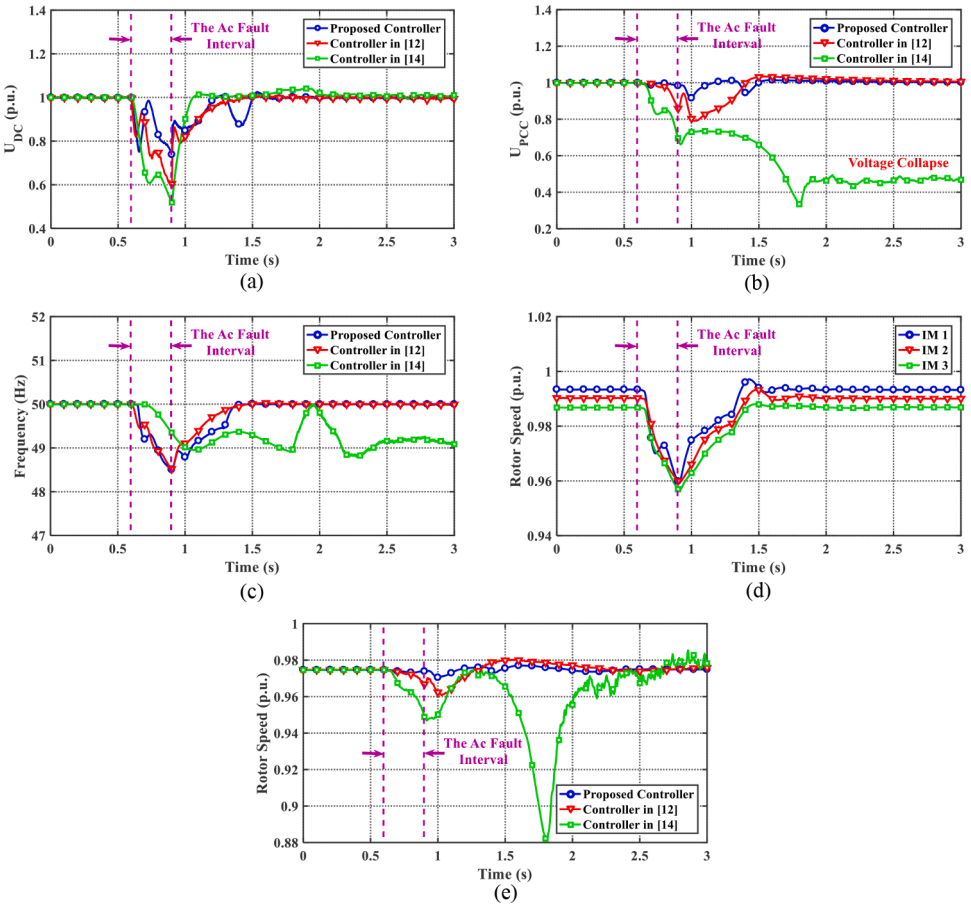

Fig. 7. Results of 3LGF simulation, (a) DC voltage, (b) AC voltage at PCC, (c) tracked frequency at the PCC, (d) the angular mechanical velocity of IM1, IM2, and IM3 by using the proposed method, (e) the angular mechanical velocity of IM4 by using three different methods.

Table 2
Minimum voltage at different buses during 3LGF in p.u.

Bus	33 kV	11 kV	6 kV	0.4 kV
Proposed method	0.916	0.934	0.921	0.917
Method in [12]	0.791	0.812	0.8	0.798
Method in [14]	×	×	×	×

Table 3
The measured parameters of ADS in different frequency controller during 3LGF in p.u.

Parameter	Minimum DC-bus voltage	Maximum switch current	Maximum speed deviation
Proposed method	0.92 p.u.	1.28 p.u.	0.37%
Method in [12]	0.77 p.u.	1.98 p.u.	1.4%
Method in [14]	×	×	×

Based on [25], ASD should be protected against overcurrent and undervoltage/overvoltage (DC/AC). In the speed-sensitive processes, the minimum drop in speed can disrupt the production process [25]. Therefore, tripping of the ASD is possible during the voltage sag due to occurring DC-bus undervoltage, overcurrent and speed drop [26]. Fig. 7 (e) shows the speed of IM4 in three different methods. By using method in [14], IM4 should be stalled due to voltage collapse. As is clear, the deviation of speed in IM4 is almost zero with proposed method. However, The speed variations in IM4 is more than 1.4% by using method in [12]. The minimum voltage at ASD DC-bus, maximum current of ASD's rectifier switches and maximum deviation of motor speed with different frequency control methods are compared in Table 3. In method [12], the ASD will be most probably tripped due to the operation of overcurrent and DC undervoltage protection; hence, the production process is disrupted. According to the Table 3, the minimum DC/AC voltage and maximum current are maintained at the desired value by using the proposed method in the event of the severe fault; consequently, ASD goes on operating as well as maintaining the speed of IM4.

5.2. *Unbalanced fault (DLGF) at the sending side*

In this section, a DLGF with 50% voltage sag is applied in phase A and phase B at the grid side. The fault is occurred at 0.6 s and is cleared 15 cycles later. The responses of the system during DLGF by using three different frequency controllers are shown in Fig. 8. As shown in Fig. 8(a), the DC voltage drops to 0.7 p.u., 0.6 p.u. and 0.6 p.u. by using the proposed frequency controller, the frequency controller methods in [12] and [14] respectively. The AC voltage at PCC returns to its nominal value after fault clearance, which verifies the effectiveness of all three methods to prevent voltage collapse. The voltage drop at PCC is more than 28% when controller in [14] is used; however, this value is 13.8% by using the proposed controller. So, the performance of the proposed method is better than method in [14] under DLGF and it can prevent tripping and malfunctioning very sensitive load to voltage sag at industrial plant. The voltage drop at PCC is 14% by using the controller method in [12], which has not a distinct difference with proposed method. After fault clearance, the AC voltage at PCC returns to steady state in the proposed method much faster than method in [12], which

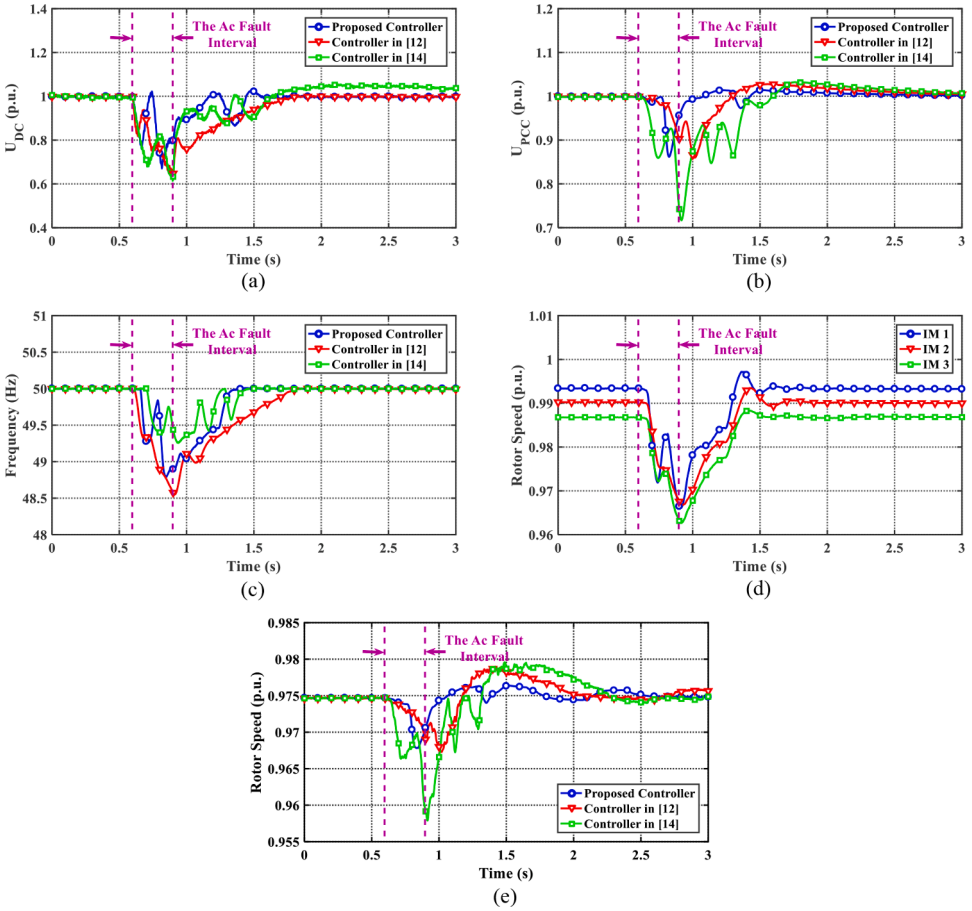

Fig. 8. Results of DLGF simulation, (a) DC voltage, (b) AC voltage at PCC, (c) tracked frequency at the PCC, (d) the angular mechanical velocity of IM1, IM2, and IM3 by using the proposed method, (e) the angular mechanical velocity of IM4 by using three different methods.

Table 4
Minimum voltage at different buses during DLGF in p.u.

Bus	33 kV	11 kV	6 kV	0.4 kV
Proposed method	0.862	0.89	0.87	0.857
Method in [12]	0.858	0.88	0.87	0.85
Method in [14]	0.717	0.754	0.73	0.72

Table 5
The measured parameters of ADS in different frequency controller during DLGF in p.u.

Parameter	Minimum DC-bus voltage	Maximum switch current	Maximum speed deviation
Proposed method	0.85 p.u.	1.5 p.u.	0.67%
Method in [12]	0.8 p.u.	1.56 p.u.	0.89%
Method in [14]	0.65 p.u.	2 p.u.	1.76%

can improve the dynamic performance of the system. Mechanical speed of IM1, IM2, and IM3 during DLGF with the proposed method are shown in Fig. 8(d). Minimum voltage at different buses are presented in Table 4. The speed of IM4 by using three different methods is shown in Fig. 8(e). By using the proposed method, the deviation of speed in IM4 is less than other methods, which becomes stable faster. However, the motor speed deviations is still high by using method in [14]. It is shown the measured parameters of ASD in Table 5. In method [14], the ASD will be most likely to be tripped due to the operation of overcurrent and undervoltage protection system. According to the results, the proposed method has better performances in this fault type.

5.3. Unbalanced fault (SLGF) at the sending side

A SLGF with 50% voltage sag is applied in phase A at the grid side. The fault is occurred at 0.6 s and is cleared 15 cycles later. The dynamic performances of the DC voltage, AC voltage and tracked frequency at the PCC during SLGF are shown in Fig. 9 when three different frequency control methods are used. As shown in Fig. 9(a), the DC voltage drops to 0.67 p.u., 0.85 p.u., and 0.79 p.u. by using the introduced frequency controller in [12, 14], and the proposed frequency controller, respectively. The AC voltage at PCC returns to its pre-fault level after fault clearance shown the effectiveness of all three methods to prevent voltage collapse. The voltage drop at PCC is more than 13% by using controller in [14]; however, this value is less than 4% and 3% when method in [12] and proposed controller are used respectively.

So, the performance of the proposed method and method in [12] is better than method in [14] in terms of voltage sag. In [12], the frequency controller reduces the frequency of the inverter output voltage as soon as fault occurs. However, the proposed method avoids unnecessary frequency deviation due to the activation of that for reducing the frequency based on U_{DCmin}. Therefore, the frequency variations interval is much less in the proposed method than the method in [12], which will improve the dynamic performance of IMs. It is shown the mechanical speed of IM1, IM2, and IM3 during the SLGF with the proposed method in Fig. 9(d). Minimum voltage at different buses are presented in Table 6. It is shown the speed of IM4 in three different methods in Fig. 9 (e). As is clear, the deviation of speed in IM4 by using proposed method

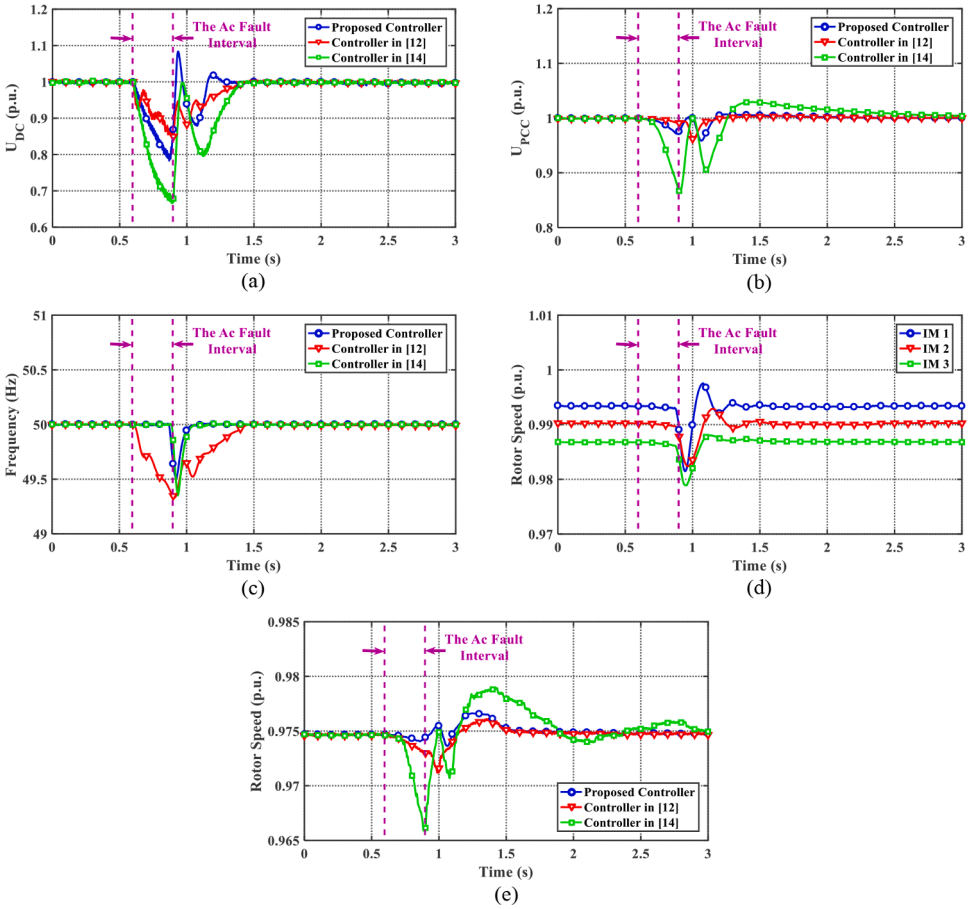

Fig. 9. Results of SLGF simulation, (a) DC voltage, (b) AC voltage at PCC, (c) tracked frequency at the PCC, (d) the angular mechanical velocity of IM1, IM2, and IM3 by using the proposed method, (e) the angular mechanical velocity of IM4 by using three different methods.

Table 6
Minimum voltage at different buses during SLGF in p.u.

Bus	33 kV	11 kV	6 kV	0.4 kV
Proposed method	0.972	0.97	0.97	0.973
Method in [12]	0.96	0.965	0.95	0.96
Method in [14]	0.865	0.88	0.87	0.87

Table 7
The measured parameters of ADS in different frequency controller during SLGF in p.u.

Parameter	Minimum DC-bus voltage	Maximum switch current	Maximum speed deviation
Proposed method	0.96 p.u.	1.18 p.u.	0.19%
Method in [12]	0.92 p.u.	1.2 p.u.	0.4%
Method in [14]	0.82 p.u.	1.8 p.u.	0.95%

and method in [12] is less than that by using method in [14]. The measured parameters of ASD during SLGF is shown in Table 7. Based on Table 7, ASD is very likely to be tripped due to the operation of overcurrent protection by using method in [14]. In this state, the proposed method has better performances compared to methods in [12] and [14].

Based on simulation results in three-phase-to-ground fault, the frequency at PCC is reduced by 1.5 Hz (3%) for a short period of time when the proposed frequency controller is used. The AC voltage at PCC has dropped 8.3% during this period. Therefore, V/Hz ratio not only is not increased but also is reduced. So there is no concern about saturation of transformers and other machines. Other faults are similar to this and there are no saturation problems.

6. Conclusion

According to the VSC-HVDC characteristics, voltage stability during disturbances could be improved in different ways, which are discussed in this paper. The decrease of output voltage frequency at inverter station is more favorable than other methods. The impact of frequency decline on IM behavior is investigated, which shows that momentary absorbed active power will be drastically reduced, if the VSC output voltage frequency is slightly decreased during fault interval. In this paper, a new frequency control method is proposed for improving the disturbance ride-through capability of VSC-HVDC link supplying industrial plant. The case study is a part of a real industrial plant, which is supplying through VSC-HVDC link. The proposed method decreases output voltage frequency based on DC-link voltage variation.

Performances of the proposed method is investigated in the case study under 3LGF, DLGF, and SLGF conditions and compared with other methods. Dynamic performances of the DC voltage, AC voltage and tracked frequency at the PCC during voltage sag are analyzed. According to the simulation results, the proposed method has better performance than other methods in terms of minimum voltage at different AC buses, DC-bus undervoltage and overcurrent in ASD, and variations of speed in IM connected to ASD, during voltage sag. The proposed method maintains the minimum AC voltage at an acceptable value for very sensitive loads to voltage drop under severe faults; hence, the continuity of the industrial process will be ensured. Not only does the proposed method lead to ride through severe faults, but also it provides the desirable voltage quality for industrial plant.

For future work, the effect of frequency reduction in an industrial system with VSC-HVDC and internal multilevel DC network for enhancement voltage stability during disturbances can be studied. In this case, the output voltage frequency of some inverters that they are connected to the motor slightly decreases. So the energy of the rotating masses is delivered to the common DC-bus, which all loads are connected to it. There is a higher flexibility in this case because the frequency reduction can be selectively applied only to machines, which are not sensitive to frequency deviations. –

Table 8
Induction motor data.

Motor	IM1	IM2	IM3	IM4
Rated power (MW)	5.1	6.3	0.7	0.045
Rated voltage (kV)	11	11	6	0.4
Rated phase current (A)	331.4	375	78	64
Power factor at rated load	0.89	0.91	0.89	0.88
Efficiency at rated load (%)	96.6	96.8	97.1	92.2
Split at full load (p.u.)	0.006	0.0053	0.005	0.0013
Starting current at full volt (p.u.)	6	4.5	5.5	8.6
Locked rotor torque (p.u.)	0.5	0.4	0.7	2.13
Break down torque (p.u.)	1.7	2	2.5	3.38
Number of poles	4	4	2	2
Polar moment of inertia ($kg.m^2$)	447	854	24.7	0.36
Torque load	$k_1\omega_{m1}^2$	$k_2\omega_{m2}^2$	$k_3\omega_{m3}$	$k_4\omega_{m4}^2$

CRediT authorship contribution statement

Mahmudreza Changizian: Conceptualization, Methodology, Software, Validation, Writing – original draft. **Amirreza Mizani:** Formal analysis, Software, Validation, Data curation, Writing – original draft. **Abbas Shoulaie:** Writing – review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data Availability

Data will be made available on request.

Appendix

Note that IMs are the dominated loads in industrial plant. Parameters of each motor are normalized based on its rating listed in Table 8.

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