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Fault-Tolerant Model-Free Predictive Controller for Multilevel Cascaded H-bridge Inverters with Faulty Cells

Paul Gistain Ipoum-Ngome, *Member, IEEE*, Daniel Legrand Mon-Nzongo, *Member,* Rodolfo, C. C. Flesch, *Member,* Jinquan Tang, Tao Jin, *Senior Member,* Mengqi Wang, *Member.*

Abstract- **In this paper, a fault-tolerant model-free predictive controller (FT-MFPC) for cascaded H-bridge multilevel inverters (CHMLIs) is proposed. FT-MFPC is based on an association of model-free predictive controller (MFPC) and a PI-like structure known as current variation controller (CVC). As in MFPC, the dynamic structure (DS) which is used for prediction of the system output is obtained from past measurements of current variations, but CVC modifies the dynamics before they are stored for prediction. As a consequence, even if the converter operates with bypassed modules, FT-MFPC adapts its DS to represent the real dynamics of the system and enables a closed-loop response with balanced load currents in unbalanced CHMLIs. Simulation and experimental results validate the adaptability of the proposed strategy to operate a seven-level inverter under various configurations of bypassed H-bridge modules. The experimental results show that, for different post-fault operations, the maximal current THD and imbalance factor at steady state in the worst-case scenario are below 5% and 2%, respectively.**

***Index Terms*—Data-driven control, model predictive control (MPC), dynamic structure, multilevel cascaded H-bridge inverters.**

I. INTRODUCTION

Despite the recent achievements in high-power switching devices based on silicon carbide with high blocking voltage [1], topologies based on silicon devices are still the most widely used alternatives [2]. In this case, multilevel converters are required for high-voltage applications, particularly series-connected cascaded H-bridge multilevel inverters (CHMLIs), which are modular, thus allowing an easy extension for very high voltage values [3]-[4]. CHMLIs contain a large number of switching devices, so the reliability of the overall system is decreased when compared with classic converters, since the failure of one module can compromise the functionality of the whole converter [4]-[5]. In this regard, fault-tolerant controllers (FTCs) have been adopted for extending the life service of CHMLIs by providing them a post-fault operation (PFO) [4],[6].

An FTC is often divided into two parts: a fault detection and location (FDL) scheme and a fault tolerant (FT) strategy. FDL schemes are active during the fault and crucial for isolating the affected H-bridge cell(s) [7], while FT strategies are used to achieve a balanced current during PFO, in which faults are modeled as bypassed H-bridges. For FDL methods, hardware and software schemes have been proposed for short and open-circuit faults [7]-[11]. For short-circuit faults, hardware methods are implemented at the gate driver stage to avoid the fast-acting damage of the opposite switch in an H-bridge cell. On the other hand, software schemes are preferred for open-circuit faults because they are not a direct threat to the system safety in a short run [10]-[11].

In the same manner, FT strategies which ensure balanced currents and line-to-line voltages are divided into hardware and software solutions [12]-[13]. Among hardware-based methods [13]-[15], hot-swap method requires extra cascaded H-bridges to replace the damaged cells and allows to operate at the same rated power. However, it increases both the size and cost of the converter [15]. An alternative solution to achieve a symmetric CHMLI is to bypass the same number of cells in each phase, but this approach reduces the power capability of the system. To extract the maximum possible power during PFO, only damaged H-bridge cells need to be bypassed and then software FT solutions are used to keep the system balanced.

Software-based approaches exploit the large number of state voltages with redundancies in CHMLI to balance load currents and line-to-line voltages during PFO. In this case, the switching states being synthesized by the PWM, neutral shift, and fundamental phase-shift compensation (FPSC) methods are derived by adjusting magnitude and phase of either voltage references or carrier signals [16]-[19]. Other methods based on unbalanced space vector and selective harmonic elimination are also proposed [20]-[21]. Moreover, for PFO with uneven power generation, a zero-sequence voltage injection (ZSVI) has been proposed in [4], and [22]. Even though significant progress has been made with regard to these fault-tolerant methods based on PWM (FT-PWM), they are valid only for PFO modes with solutions pre-calculated. For instance, in a case of an 11-level CHMLI, 30 fault events are possible [18] and only 23 have solutions by using FPSC. To design an effective PFC for all PFO modes, the 30 solutions to upload in FTC are pre-calculated based on extended FPSC. When these FT-PWM are in closed loop, the voltage references are usually generated by linear controllers which are designed to operate with nominal load parameters and DC-link voltages. Therefore, unless additional control schemes are added, the closed-loop responses of these FTCs are not as good as in the nominal case when additional uncertainties, such as load resistance increases and capacitor voltages unbalance, affect the system [23]-[24].

An alternative approach for designing FDL and FT schemes is the use of model predictive control (MPC) [25]-[27]. MPC is a discrete-time strategy with a straightforward implementation and which enables an easier inclusion of constraints [28]-[30]. In power electronics, MPC can be divided in continuous-control-set MPC (CCS-MPC) and finite-control-set MPC (FCS-MPC). A modulator that transforms a real-valued output into switching states is needed in CCS-MPC. On the other hand, FCS-MPC exploits the switching states of the converter to predict and solve the optimization problem, so the resulting control action is directly the switching state [28]. To limit the computational burden, which exponentially increases with the prediction horizon and the number of switching states to evaluate, the prediction horizon is often limited to two samples in FCS-MPC [29]. With the focus on CHMLI, various FCS-MPCs are proposed for controlling the current, performing capacitor voltage balancing, and solving additional issues, such as reduction of common-mode voltage (CMV) [31]-[36].

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However, in FTC research field, the study is still more focused on FDL schemes and the literature on FT strategies is limited, particularly for application with CHMLI. Several FDL schemes based on MPC have been proposed and the most recent one, described in [26], uses only the AC current measurement. In [27], a fault ride-through strategy based on MPC is proposed for single-phase modular multilevel converters. This approach uses several control objectives in the cost function and requires building a look-up table (LUT) of switching states related to the fault condition, which increases the complexity of the controller.

The need for defining the switching set which characterizes each PFO and extending the cost function makes it challenging to design an FT strategy based on MPC (FT-MPC) and to the best of the authors' knowledge such FT-MPC has not yet been proposed for CHMLI. Moreover, it is relevant to obtain an FT-MPC able to adapt its response under load parameter changes. Model-free predictive control (MFPC) is known to provide a robust response, since in this case the prediction relies on the measured current and current variations (CVs) [37]-[39].

An extended MFPC has been proposed for CHMLI in [40]. The method uses the classic MFPC principle described in [37] and a current variation controller (CVC) to generate control signals and compensate for the simplification in the MFPC method. The CVC is based on PI-like controller to generate the control signal related to each applied state. Unlike the classic PI current controller, which considers as input the error between the reference and the measured current, the CVC uses as input the variation between two consecutive measured currents. Since in this case the prediction is made based on data measured in the process after being modified by CVC, the expression data-driven predictive controller (DDPC) is used as a substitute for this extended MFPC. Reference [40] focused only on DDPC adaptability under different time-varying load parameters. Since the prediction model is also independent of the inverter model, it has potential to adapt to changes in the inverter configuration and enable operation under unbalanced MLCHB.

In this paper, the DDPC proposed in [40] is analyzed with the focus on operation with unbalanced CHMLI due to bypassed H-bridge cells, and the algorithm is extended so that the controller can adapt its closed-loop action and provide a balanced PFO under a wide range of faulty-cell cases. This behavior is obtained using only a current control objective, so no information about the specific fault condition is needed. In the rest of this paper, a background of classic MPC for CHMLI connected to a load is presented and various FT-PWMs are discussed in section II. The proposed FT-MFPC is detailed in section III. Sections IV and V summarize the simulation and experimental results. Conclusions are discussed in section VI.

II. System Description and Review of FT-PWMs

A. System under investigation

The system under investigation is presented in Fig. 1 and it is constituted by an *RL*-load fed by an ℓ-level CHMLI, $\ell = (2C + 1)$, where C is the number of cells connected in series per phase. Each cell has a DC source E_o, an H-bridge noted CHB$_j$, and its related switches $\bar{k}_{jx}$ and k_{jx} to isolate a cell$_j$ in case of a fault event. The output voltage per cell is given by

$$v_{jx} = \lambda_{jx} v_{o,jx} \quad \text{and} \quad v_{o,jx} = E_o u_{jx} \quad , \tag{1}$$

where $u_{jx} \in \{-1,0,1\}$ is the switching level for a cell$_j$ in a phase

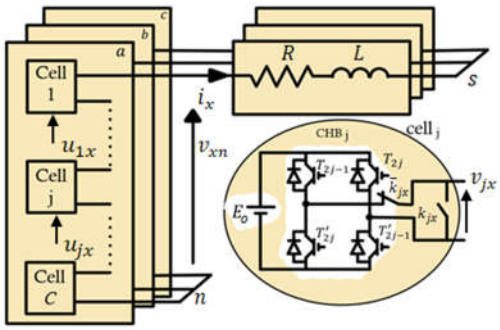

Fig. 1. CHMLI connected to RL-load

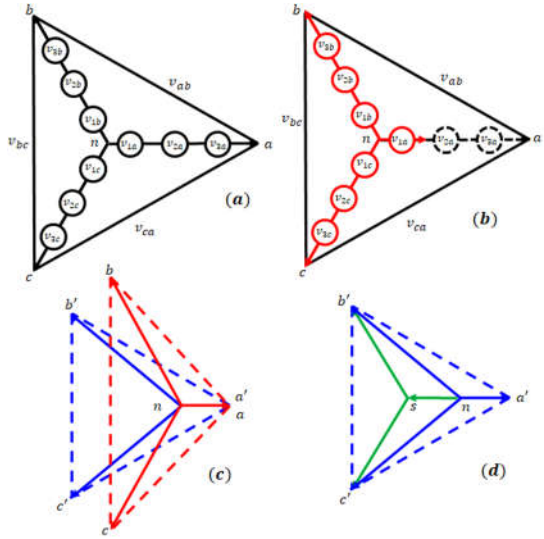

Fig. 2. Vector representation of CHMLI at different operating conditions: (a) balanced mode; (b) unbalanced mode due to faulty cells; (c) balanced mode by neutral shift; (d) equivalent balanced mode by zero-sequence voltage injection.

x, v_{jx} is the output voltage per cell, and $\lambda_{jx} \epsilon [0;1]$ is the inter-bridge voltage unbalance ratio. In case of PFO, only two cases of λ_{jx} are considered: zero for a bypassed cell and one for a healthy cell. Thus, the output voltage per phase v_{xn} is given by

$$v_{xn} = \sum_{j=1}^{C} v_{jx} \quad . \tag{2}$$

Applying v_{xn} to a load at k results in a current response $i_x(k+1)$ that is given by

$$i_x(k+1) = i_x(k) - T_s \frac{R}{L} i_x(k) + \frac{T_s}{L} v_{xn}(k) \quad . \tag{3}$$

Considering $i_x(k)$ is balanced, the current response $i_x(k+1)$ is either balanced or imbalanced, depending on the operating condition of the CHMLI. The operating condition of CHMLI can be characterized by the inter-phase voltage imbalance as

$$\lambda_x = \sum_{j=1}^{C} \lambda_{jx} \Big/ C \, . \tag{4}$$

In normal operation, $\lambda_{x\epsilon\{a,b,c\}} = 1$, CHMLI generates balanced output voltages, as illustrated in Fig. 2(a), and the current in (3) is balanced. However, in case of PFO, affected H-bridge cells are bypassed. For example, with $\lambda_{2a} = \lambda_{3a} = 0$, the resulting $\lambda_{x\epsilon\{a,b,c\}}$ are unequal, meaning that the CHMLI is unbalanced, as illustrated in Fig. 2(b). In this scenario the current response is unbalanced unless an FT strategy is used.

B. FTC based on PWM schemes (FT-PWM)

In FTs based on neutral shift methods, the balancing of the line-to-line voltage is achieved by modification of the PWM

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stage. For example, by shifting the angles of the other two heathy phases, the resulting line-to-line voltages are balanced, as shown in blue in Fig. 2(c). This approach is also known as vector-based method and has been proven effective for both motors and grid-connected applications [16]-[18]. Seen from the load side, FT-PWM can be derived as phase shift added with a CMV (v_{ns}), as illustrated in Fig. 2 (d). Thus, other FT-PWM are waveform-based methods which propose a ZSVI so that the load voltage remains balanced [4], [22]. However, given the significant complexity to obtain the parameters to reconfigure the modulator, all faulty H-bridge scenarios have to be solved offline and uploaded in FTC for closed-loop control [18].

C. Challenges in tuning FTC based on MPC (FT-MPC)

Classic FCS-MPC does not have a modulator, so including the unbalanced CHMLI in the optimization problem solved at each iteration is the only option to balance the system during PFO. This option is challenging because MPC relies on the model of an CHMLI at normal condition to synthesize the candidate voltages used in the prediction model. For example, in a current loop, the prediction model in MPC is given by (1)-(3) with $\lambda_{x\epsilon\{a,b,c\}} = 1$. With the unbalanced CHMLI not considered in the prediction model and the cost function limited to a current control objective, the resulting current response is unbalanced, as illustrated in Fig. 3 for the simulation parameters in Table I. Unbalanced currents not only reduce the overall system performances, but also put its safety at risk. For example, in motor drives, they generate pulsating torques on motor shaft, which can result in loosening of the mechanical transmissions or worse failure of the shaft due to mechanical resonances [6]. To balance the load voltages and currents, the prediction model of the inverter has to be modified or additional control objectives must be used to readjust the path of the applied state voltages. The modification of the model requires the update of the switching set according to the specific PFO condition, and if done online [27] it requires high execution effort, which will exacerbate in a three-phase CHMLI. To reduce the computation time, offline tuning of switching set approach can be considered. However, it will require a large memory for storing all switching set configurations, which is less attractive than storing the parameters of neutral shift with FT-PWM methods.

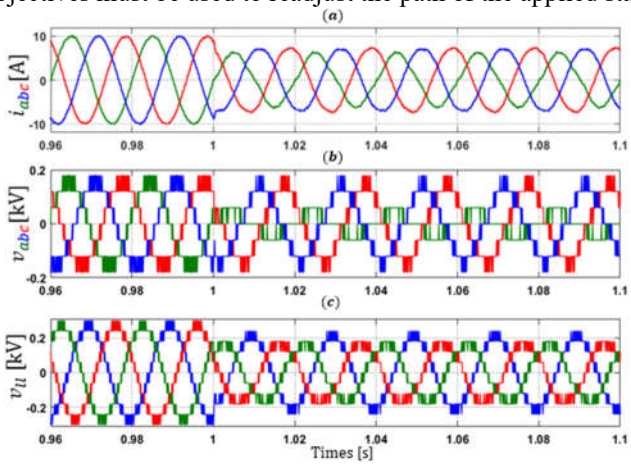

Fig. 3. Simulation results under MPC from pre-fault to post-fault condition with two cells bypassed: (a) currents; (b) line voltages; (c) line-to-line voltages.

TABLE I
SYSTEM NOMINAL PARAMETERS

Variable	Description	Simulation	Experimentation
E_o	DC-link voltage per cell	60 V	40 V
R	Nominal resistor	15 Ω	12 Ω
L	Nominal inductance	10 mH	10 mH
I_n	Nominal current	10 A	9 A
T_s	Sampling time	200 μs	167 μs
ℓ	Number of levels	7	7
k_p	Proportional gain	1	1
k_i	Integral gain	30×50	30×50
G	Attenuation gain	0.75	0.66

III. PROPOSED FTC BASED ON EXTENDED MFPC (FT-DDPC)

To avoid the need for the model of the inverter for each PFO condition, MFPC is associated with a PI-like controller to define the load control signal driving the prediction. A simplified description of the prediction model during PFO is presented in Fig. 4. For a three-phase CHMLI, there are $m = (2C+1)^3$ candidate state voltages. For each voltage, v_{xn}^p, $p \in \{1,..,m\}$, applied at k, it is possible to obtain a current prediction for phase x, i_x^p, at $k+1$ as

$$i_x^p(k+1) = i_x(k) - T_s\frac{R}{L}i_x(k) + \frac{T_s}{L}v_{xn}^p(k) \ . \tag{5}$$

At nominal load parameters, this current prediction depends on the measured current and dynamics function as

$$i_x^p(k+1) = i_x(k) + F_x^p\left(i_x(k), v_{xn}^p(k)\right) \ , \tag{6}$$

where $F_x^p(\cdot)$ is a function that represents the dynamics of the system related to an applied voltage v_{xn}^p. In a case where the post-fault model of CHMLI is available, it is possible to write a family of functions F_x as

$$\begin{cases} F_x = \begin{bmatrix} F_x^1 & F_x^2 & .... & F_x^p & .... & F_x^{m-1} & F_x^m \end{bmatrix}^T \\ F_x^p = -T_s\dfrac{R}{L}i_x(k) + \dfrac{T_s}{L}\displaystyle\sum_{j=1}^{C}\lambda_{jx}(k)v_{o,jx}^p(k) \end{cases} \tag{7}$$

Unfortunately, it is challenging to evaluate F_x considering all possible state voltages affected by the bypass of cells without increasing the algorithm computational burden [27]. Instead of searching for the post-fault model of the CHMLI to build F_x, a model-free prediction approach is used to approximate F_x.

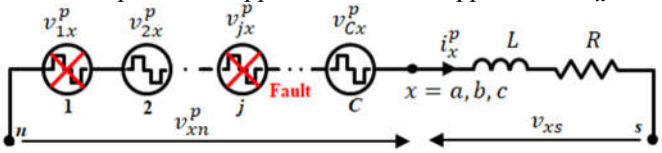

Fig. 4. Prediction model with CHMLI for any operating condition.

A. Model-free prediction approach

In MFPC, the prediction in (6) relies on the history of the system CV to approximate the dynamics F_x^p associated to each applied state v_{xn}^p. Fig. 5(a) illustrates a current response of a single-phase 3-level CHMLI connected to a load with $v_{xn}^p \in \{-E, 0, E\}$, $p\epsilon\{1,2,3\}$. Each colored dot represents the time instant at which the current is measured before the new optimum voltage is applied. The cylinder characterizes a LUT storing approximated dynamics of the system, $\hat{F}_x$, v_{xn}^{op} is the optimum applied state voltage, and i_x^{op} is the current response due to v_{xn}^{op}. Note that each applied v_{xn}^{op} results in a current response i_x^{op}, which is measured at the next sample. For instance, the optimum state applied at $k-1$ is v_{xn}^3, which results in a current $i_x(k)$, measured at k, given by i_x^3.

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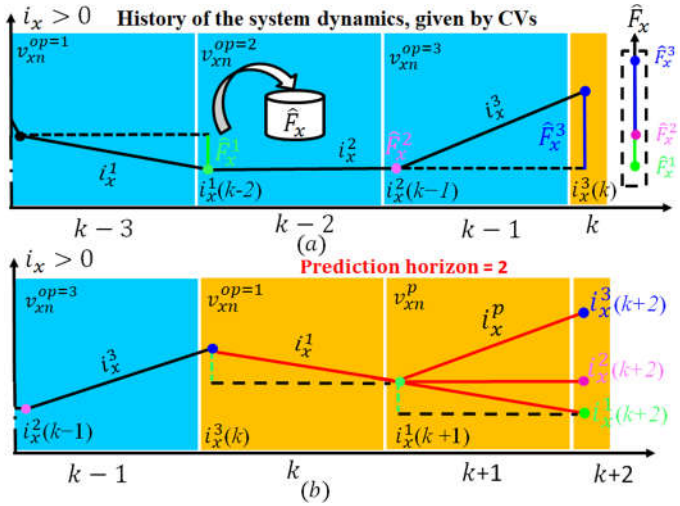

Fig. 5. Illustration of current prediction: (a) approximation of the dynamic structure; (b) current prediction for a horizon of two samples.

Considering i_x^2 (or $i_x\,(k-1)$) was stored at $(k-1)$, the approximated dynamics $\hat{F}_x^3$ due to v_{xn}^3 is evaluated at k and it is equal to the CV between $i_x(k)$ and $i_x(k-1)$, i.e. $\hat{F}_x^3 = i_x^3 - i_x^2$, as illustrated by the blue segment in Fig. 5(a). Using the same principle during $k-3$ and $k-2$, all optimum dynamics for $op\epsilon\{1,2,3\}$ are stored in $\hat{F}_x$, as shown in Fig. 5(a).

As a generalization, $\hat{F}_x^{op}$ due to an optimum voltage v_{xn}^{op} applied at $(k-q-1)$ is equal to the CV observed at $(k-q)$ as

$$\hat{F}_x^{op} = \Delta i_x = i_x(k-q) - i_x(k-q-1)\ . \tag{8}$$

At sample k, $q\epsilon\mathbb{N}$ is the aging of the dynamic data, thus $\hat{F}_x^{op}$ is q-sample old for $q \neq 0$ and actual if $q = 0$. At each sample, only one current variation is computed, thus at k-th sample, for instance, $\hat{F}_x$ is updated only at the previous optimal position, by replacing an older value for the same voltage position by the new measured current variation as

$$\begin{cases} \hat{F}_x\big|_{p=op} = \hat{F}_x^{op} \quad \text{where} \quad \hat{F}_x\big|_{p} = \hat{F}_x^{p} \in \hat{F}_x \\ \hat{F}_x = \left[\hat{F}_x^1 \quad \hat{F}_x^2 \quad \ldots \quad \hat{F}_x^p \quad \ldots \quad \hat{F}_x^{m-1} \quad \hat{F}_x^m\right]^T \end{cases} \tag{9}$$

If sampling times are small enough and all state voltages of the converter are applied, $\hat{F}_x$ can be fully obtained in a short period of time after startup, and then used to approximate each F_x^p as

$$F_x^p \cong \hat{F}_x^p \quad \text{with} \quad 1 \le p \le m\ . \tag{10}$$

Since the current response at $k+1$ is the result of v_{xn}^{op} applied at k, $i_x^{op}(k+1)$ can be predicted as the sum of the measured current $i_x(k)$ and $\hat{F}_x^{op}$, as illustrated in Fig. 5(b) with $op = 1$. Thus, the current value can be approximated as

$$i_x^{op}(k+1) \cong i_x(k) + \hat{F}_x^{op}\ . \tag{11}$$

Using the same principle, the current prediction at $k+2$, $i_x^p(k+2)$, due to a candidate state voltage v_{xn}^p is the sum of $i_x^{op}(k+1)$ and $\hat{F}_x^p$, as illustrated in Fig. 5(b) and given by

$$i_x^p(k+2) = i_x^{op}(k+1) + \hat{F}_x^p\ . \tag{12}$$

According to (11)-(12), the prediction model only depends on the actual measured current and $\hat{F}_x$, which are built also from measurements. Thus, the accuracy of the prediction depends on the operating current and the update rate of $\hat{F}_x$. Although the prediction is analytically free from parameters, its accuracy is still indirectly affected by the parameter mismatches that occur in the system. These indirect influences have been illustrated in previous works on case-by-case evaluations [37]-[39], but compared to MPC, MFPC results in a far better accuracy.

B. Current variation controller (CVC) and optimization

To achieve a balanced current response without extending the cost function, a PI-like structure is inserted in the feedback CV loop. This PI does not consider as input the current error, but the measured CV. The compensated dynamics at k is given by

$$\widehat{F'}_x^{op} = k_p \Delta i'_x(k) + k_i T_s \sum_{j=1}^{k} \Delta i'_x(j)\ , \tag{13}$$

where k_p and k_i are the coefficients of the PI controller, and $\Delta i'_x(k)$ is the attenuated CV computed at k and given by

$$\Delta i'_x(k) = i'_x(k) - i'_x(k-1) \ \text{ and } \ i'_x(k) = G i_x(k)\ , \tag{14}$$

with G as the attenuation response gain. Therefore, instead of the CVs used in MFPC, the new prediction model is a function of the output of the PI structure and it is given by

$$i'^{op}_x(k+1) = i'_x(k) + \widehat{F'}_x^{op} \tag{15}$$

$$i'^{p}_x(k+2) = i'^{op}_x(k+1) + \widehat{F'}_x^{p}\ . \tag{16}$$

Similar to (9), $\hat{F}'_x$ is updated at each sample using $\widehat{F'}_x^{op}$ as

$$\widehat{F'}_x\Big|_{p=op} = \widehat{F'}_x^{op}\ . \tag{17}$$

In summary, in the proposed approach CVC modifies the CV before storing it in the LUT of the system dynamics as in (13), while in classic MFPC, CVs generated in (8) are directly stored in the LUT. Thus, in case the system is affected by a fault event, for each CV due to healthy or unhealthy v_{xn}^{op}, an equivalent representation of the dynamics is stored in the LUT after being modified by the PI. Therefore, any change within the load parameter or inverter is gradually considered in the prediction model through $\hat{F}'_x$ generated by the PI structure and then evaluated during the optimization by using only a standard control objective given by

$$g^p = \sum\nolimits_{x\in\{a,b,c\}} \left(i_x^*(k+2) - i'^{p}_x(k+2)\right)^2\ . \tag{18}$$

The current reference $i_x^*(k+2)$ at sample $(k+2)$ is given by

$$i_x^*(k+2) = 6\, i_x^*(k) \ - \ 8\, i_x^*(k-1) \ + \ 3\, i_x^*(k-2)\ , \tag{19}$$

$$i_x^*(k) = I^* \sin\left(\omega\, t + \theta_x + \phi\right)\ , \tag{20}$$

where $\theta_x\epsilon\{0, -2\pi/3, 2\pi/3\}$ and ϕ is the phase angle between voltage and current [22]. Other constraints and objectives can also be considered in the proposed controller as long as they are written as a function of the voltage vectors and the measured quantities in the process. In case the balanced power to extract decreases with the number of bypassed cells, the amplitude of the current reference I^* is defined as a function of the average voltage imbalance ratio and nominal current I_n as

$$I^* = \lambda_{\text{moy}} I_n \quad \text{with } \lambda_{\text{moy}} = \sum\nolimits_x \lambda_x / 3\ . \tag{21}$$

C. Proposed FT-DDPC algorithm

The control diagram of the proposed FT-DDPC is presented in Fig. 6. It consists of the initialization, sub-space prediction, current reference generation, the CVC, and prediction and optimization functions. LUT1, or $\hat{F}'_x$, is the key-point of the FT-

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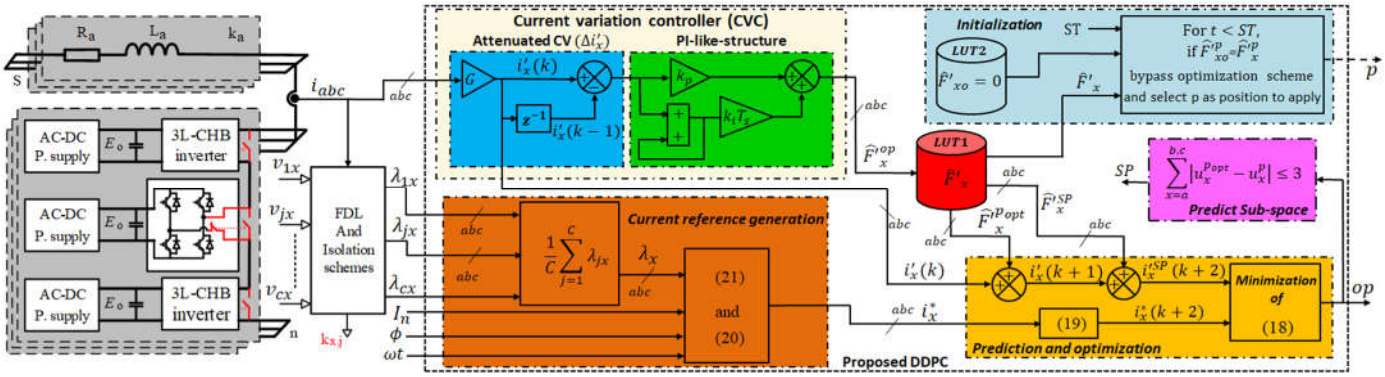

Fig. 6. Proposed fault tolerant data-driven predictive controller for ML-CHBs with faulty cells.

DDPC and has an equivalent role as the model in a regular MPC. The FDL and isolation schemes are not discussed in this paper, but details can be found in [7]-[11] and [25]-[26]. Details about the current reference generation, prediction, and optimization are shown in Fig. 6. The implementation of the FT-DDPC is less straightforward than FT-PWM due to the several added schemes. However, the subspace prediction scheme can be avoided by using all states and the initialization scheme is only a comparison between LUT1 and LUT2 used at the startup.

The evaluation of the whole LUT1 for $p \in \{1,..,m\}$ is the best solution to validate the full potentiality of the proposed FT-DDPC under normal and fault conditions. However, evaluating a LUT1 with higher number of inputs, such as 343 in case of a 7-level CHMLI, raises the issue of the required computational burden, which is critical for implementation. In addition, if a single current control objective is considered, the peak CMV and switching frequency are expected to be higher if a subspace method is not considered. In this work, a subspace method is used to limit the computational burden of the proposed control algorithm and this method is tuned based on CMV limitation [31]-[32] and switching levels restriction, which is given by

$$\left|u_a^{op} - u_a^{p}\right| + \left|u_b^{op} - u_b^{p}\right| + \left|u_c^{op} - u_c^{p}\right| \le h \ , \qquad (22)$$

where h is a relaxation coefficient which defines the maximum number of levels that can be changed from one solution to the next. After several evaluations for different values of h, it was found that $h \ge 3$ is enough to obtain as good transient and steady-state responses as if the whole LUT1 were used.

An accurate LUT1 is crucial for an effective FT-DDPC. To build up LUT1 during the startup time (ST), $\hat{F}_x$ and $\hat{F}_{xo}$ are compared according to the initialization scheme. The key for achieving a good closed-loop performance relies on tuning the PI controller and the attenuation gain. The parameters k_i, k_p, and G are selected based on a grid search that returns a solution with a good tradeoff between the average current error, $\overline{M}$, RMS current error, $\overline{J}$, and total harmonic distortion, $\overline{THD}$, which are respectively given by

$$\overline{M} = \sum\nolimits_{x\in\{a,b,c\}} \frac{M_x}{3}, \quad M_x(G,k_p,k_i,k_d) = \left(\frac{1}{N}\sum_{k=1}^{N}\left|i^*_{x(k)} - i^{'}_{x(k)}\right|\right) \qquad (23)$$

$$\overline{J} = \sum\nolimits_{x\in\{a,b,c\}} \frac{J_x}{3}, \quad J_x(G,k_p,k_i,k_d) = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(i^*_{x(k)} - i^{'}_{x(k)}\right)^2} \qquad (24)$$

$$\overline{THD} = \sum\nolimits_{x\in\{a,b,c\}} \frac{THD_x}{3}, \; THD_x(G,k_p,k_i,k_d) = \frac{1}{\sqrt{2}I_{1x}}\sqrt{\sum_{h\ne 1}\left(\hat{I}_{hx}\right)^2} \qquad (25)$$

where the fundamental component is I_{1x}. The magnitude of a harmonic component is denoted by $\hat{I}_{hx}$ and h is the harmonic order. N is the number of samples for a current cycle.

IV. Numerical Evaluation

The nominal parameters of the load, and level of CHMLI considered in this analysis are given in Table I. The key parameters of the FT-DDPC were selected based on performance indexes values resulting from simulation.

A. Tuning of k_i, k_p, and G parameters of CVC

The critical parameters of CVC were tuned using a grid search with increments given by $\Delta k_i = 50$ and $\Delta G = 0.1$, and $k_p = 1$. The sensitivity of $\overline{M}$, $\overline{J}$, and $\overline{THD}$ versus parameters of the CVC are presented in Fig. 7. Each sub-plot in Fig. 7 presents several colored areas depending on the magnitude value of each performance. Suitable solutions are selected within the green areas and the solutions with the best tradeoff between $\overline{M}$, $\overline{J}$, and $\overline{THD}$ are the ones for which all the indexes assume values in the green region. An example of a solution, which minimizes the three indexes, is $k_i = 1500$ and $G = 0.75$.

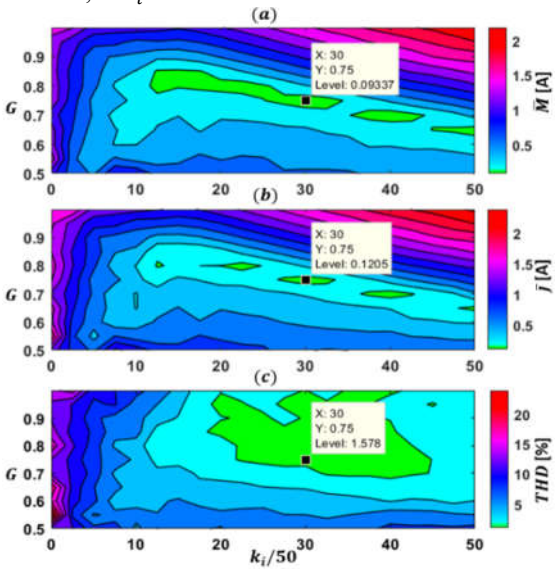

Fig. 7. Analysis of the closed loop performance sensitivities to parameters of CVC for $k_p = 1$: (a) average error $\overline{M}$; (b) RMS current error; (c) current THD.

B. Analysis of the output control signal generated by CVC

1) Waveform-based representation

To analyze $\hat{F}'_x$, numerical results of the proposed controller with the system at normal operation are used. The phase current response, i_a, inverter and load voltages (v_{an} and v_{as}) for phase a are presented in Fig. 8(a)-(c) and validate the proposed FT-DDPC accurancy and fast current response at normal operation. To simplify the analysis of $\hat{F}'_x$, the focus is given on the

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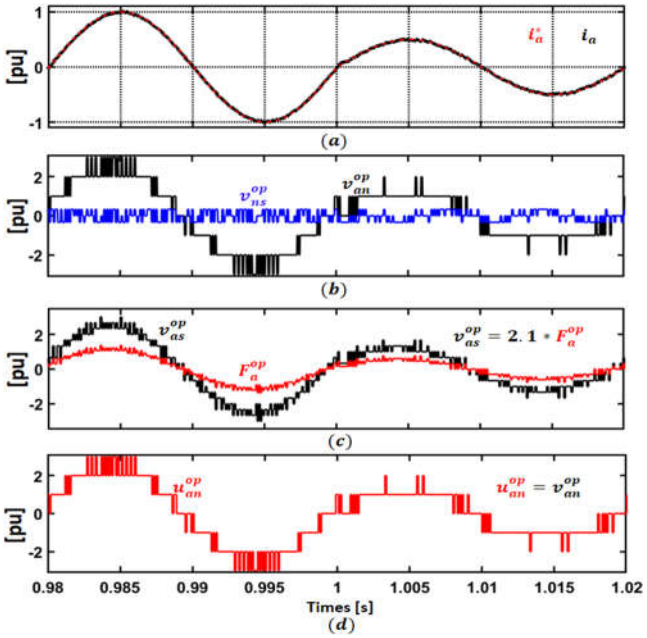

Fig. 8. Numerical evaluation of DDPC at normal operation: (a) load current; (b) inverter output voltage and CMV; (c) load voltage and optimum dynamics; (d) inverter input control signals reconstructed from applied state voltages.

optimum dynamics $\hat{F}_x'^{op}$. A comparative study of $\hat{F}_x'^{op}$ and v_{as}^{op}, plotted in Fig. 8(c), shows that both waveforms are proportional and, for this simulation case, the proportion coefficient is 2.1. This finding means that the dynamic data $\hat{F}_x'$ generated by CVC at each sample is the phase control signal due to the applied inverter voltage which is seen from the load neutral point.

To verify the relation between $\hat{F}_x'^{op}$ and v_{as}^{op} in the time domain, a new variable noted u_{as} is considered equal to $2.1F_a^{op}$. To move from the load to the inverter neutral point, the CMV is injected into u_{as}, and the resulting waveform is noted $u_{an}$and shown in Fig. 8(d), where it is possible to see that it is identic to the inverter voltage levels, v_{an}. From this finding, $\hat{F}_x'^{op}$ can be derived as a function of the control signal due to an applied inverter voltage and its related CMV. For this reason, any healthy or unhealthy state which is applied to the load is directly reconstructed by the CVC and included into the current control objective through the current prediction model. Subsequently, the optimization function evaluates the cost function and searches for the optimum control signal and its CMV to inject so that the load current remains balanced under normal operation or unbalanced CHMLI during PFO.

2) Vector-based representation

To analyze the steady-state representation of $\hat{F}_{abc}'$ for various PFOs, the vector-based representation is used and the current reference is changed so that each $\hat{F}_{abc}'^{op}$ is updated at least once. For easy characterization of $\hat{F}_{abc}'$ and comparison with the space vector (SV) of CHMLI, u_{abc}, which is function of $\hat{F}_{abc}'$, is used and put into $\alpha\beta$-axes. The resulting $u_{\alpha\beta}$ for each operating condition in Table II is shown in Fig. 9, and named dynamic structure (DS) of the system. The DS of case I is equivalent to

TABLE II
EVALUATED CASES OF ML-CHB INVERTER WITH FAULTY CELLS

Failure modes	$[\lambda_{a1}, \lambda_{a2}, \lambda_{a3}]$	$[\lambda_{b1}, \lambda_{b2}, \lambda_{b3}]$	$[\lambda_{c1}, \lambda_{c2}, \lambda_{c3}]$
Case I	[1, 1, 1]	[1, 1, 1]	[1, 1, 1]
Case II	[0, 1, 1]	[1, 1, 1]	[1, 1, 1]
Case III	[0, 0, 1]	[1, 1, 1]	[1, 1, 1]
Case IV	[0, 0, 1]	[0, 1, 1]	[1, 1, 1]

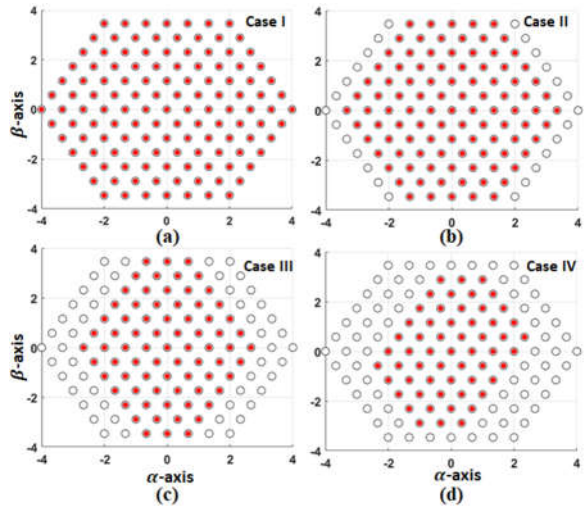

Fig. 9. Dynamic structure of the system for different PFOs: (a) DS at case I; (b) Case II; (c) Case III; (d) Case IV.

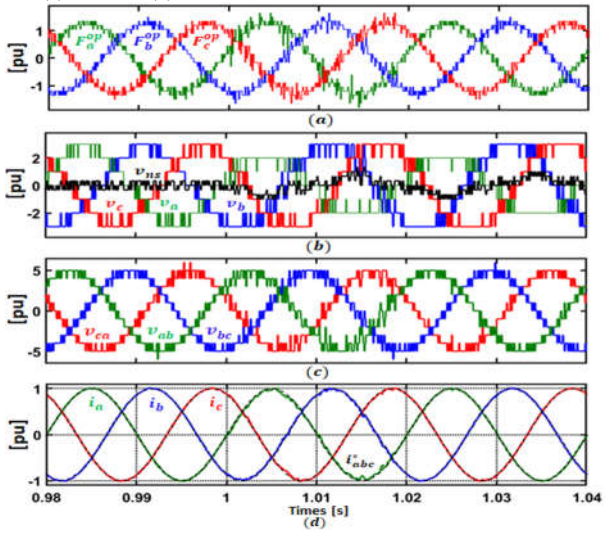

Fig. 10. Simulation results of the proposed method with 1 faulty-cells from case I to case II at nominal current: (a) dynamics related to applied states; (b) inverter output voltages and CMV; (c) line-to-line voltages; (d) load currents.

the SV of a CHMLI at normal condition, while DSs of cases II, III and IV are similar to unbalanced SVs of MLCHB under faulty cells [16]. Since the update of DS only involves one input control state per sample, several samples are required to move from normal DS (case I) to an unbalanced DS. During this period, $\hat{F}_{\alpha\beta}'$ is less reliable; therefore, it has a negative impact on the current prediction and the closed-loop control action. To provide better transients for faults which affect a large number of states, it is important to study a faster update technique [39].

C. Analysis of the adaptability of FT-DDPC

1) FT-DDPC under PFO at rated power:

With an over-design or increase of DC-link voltage during PFO, FT-DDPC has the ability to adapt its closed-loop control and provide a nominal and balanced power to the load, as illustrated in Figs. 10-11. FT-DDPC still provides an accurate response similar to case I under PFO with unequal DC voltages, as illustrated in Fig. 11. Since the number of affected states in case III is higher than in case II, as illustrated in Fig. 9, FTC-MFPC shows a slightly worse transient in case III.

2) FT-DDPC under active fault and PFOs:

Under more than one H-bridge bypassed without increase of the DC-link voltage in the remaining healthy cells, the new current

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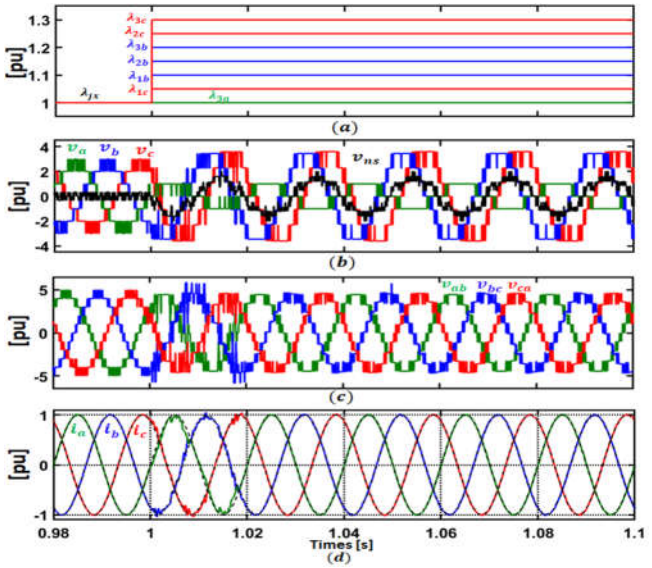

Fig. 11. Simulation results of the proposed method from case I to case III under unequal DC-link voltages and at nominal current: (a) load currents; (b) inverter output voltages and CMV; (c) line-to-line voltages; (d) load currents.

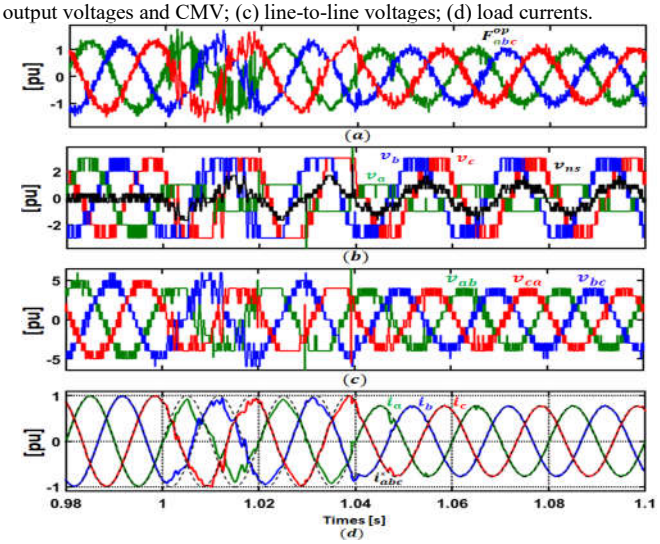

Fig. 12. Simulation results of FTC-MFPC from case I, case III with active fault to case III with affected H-bridges bypassed: (a) DS; (b) inverter output voltages; (c) line-to-line voltages; (d) load currents.

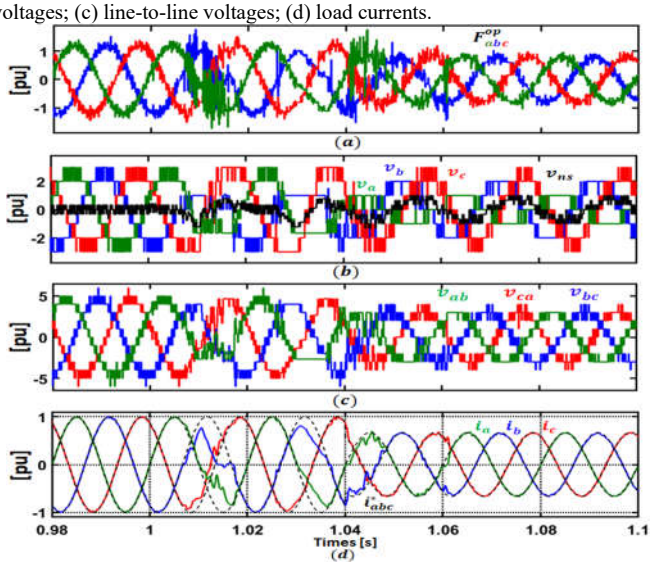

Fig. 13. Simulation results of FTC-MFPC from case I, case IV with active fault to case IV with affected H-bridges bypassed: (a) DS; (b) inverter output voltages; (c) line-to-line voltages; (d) load currents.

reference is obtained through the current reference scheme in Fig. 6. Since the FTC-DDPC is based on adaptive DS, it is important to observe the behavior of DDPC with an active fault and ensure the response is not unstable during the time period where FDI will be active to detect and isolate the affected cells.

For analysis purpose, the faults are assumed to happen at 1 s and the affected cells are bypassed only at 1.04 s. In case III, the fault event affecting CHB.a1 and CHB.a2 are open-circuit capacitors voltages, while in case IV, it is a combination of open- and short-circuit fault devices affecting CHB.a1, CHB.a2, and CHB.b1. While the faults are active but the corresponding cells are not isolated, the closed-loop response shows an imbalance, as shown in Figs. 12-13, which is expected for any controller operating with an active fault. However, the most interesting part from this period with active fault before being bypassed is that the controller is able to provide a good and balanced response after some time. That means that in some cases the proposed controller is able to isolate the fault and provide an accurate response without the need for FDI schemes. After the cells are bypassed, FT-DDPC achieves accurate and balanced current responses. Since the subspaces are tuned based on CMV limitation, the peak CMV is $0.333E_o$ at normal operation, and below $1.7E_o$ for all PFO scenarios.

3) FT-DDPC under parameters mismatches:

The robustness of FT-DDPC is evaluated under resistance and inductance mismatches, as shown in Figs. 14-15. Since the robustness of FT-DPCC is also linked to the modification of the DS, but now due to the load change, DS for each mismatch case is also plotted for load at normal and under parameter change. With a fixed operating current, only the dynamic data around the voltage reference are updated (moved from their initial location according to the load mismatch). Control states with higher amplitude are required to compensate for the resistance step-up than for the inductance change. Thus, except states at the corner, with peak CMV, the control states initially in the outer hexagon are moved and after update they are around the voltage reference in this case, which results in the converter saturation, therefore leading to an increase in the current error and ripples with higher amplitude, as shown in Fig. 14(c).

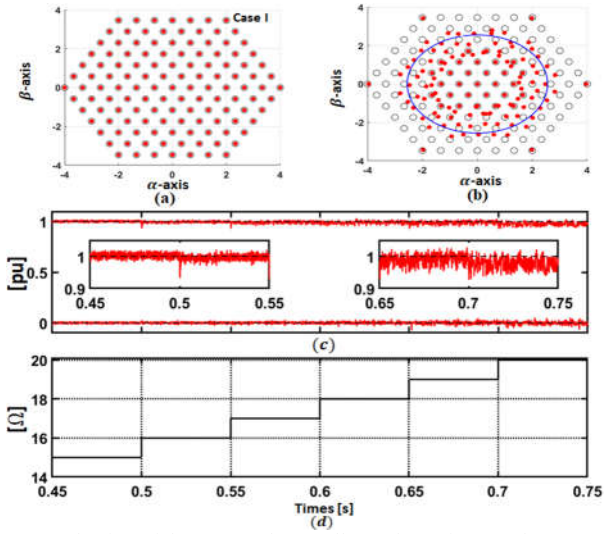

Fig. 14: Evaluation of the proposed controller under resistance change: (a) DS at 15 Ω; (b) DS at 20 Ω; (c) current in dq-axes; (d) resistance variation.

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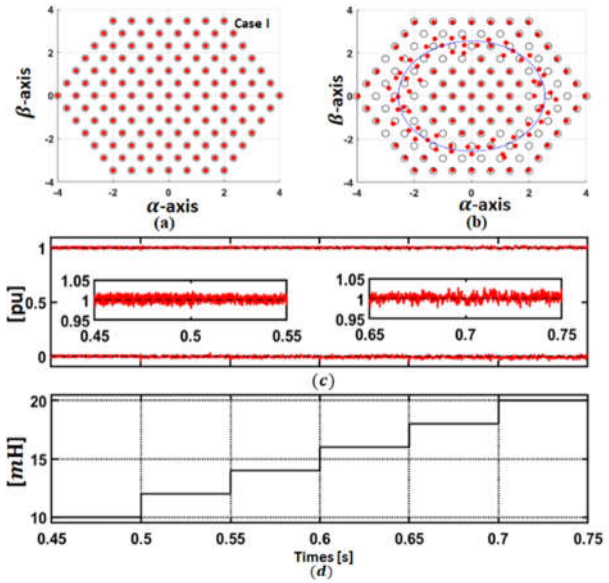

Fig. 15: Evaluation of the proposed controller under inductance change: (a) DS at 10 mH; (b) DS at 20 mH; (c) current in dq-axes; (d) inductance variation.

V. Experimental Validation

The experimental setup used for validation is presented in Fig. 16 and parameters of the system and CVC are given in Table I. The converter used to generate seven voltage levels is constituted of three modules per phase, and each module has an isolated AC-DC power supply and a three-level H-bridge cell, as illustrated in Fig. 6. The experimental tests consisted in bypassing and then restoring H-bridge cells online with the load deviated from the nominal parameters using the rheostat and tap inductance. Since the capacitor voltage balance is not considered in the cost function, the mismatch of DC voltage is another level of the uncertainties faced in the system. This was done to analyze the adaptability of the proposed FT-DDPC in a wide range of PFO scenarios.

Two experimental tests (I and II) have been performed and each test has a duration of 5 s. To evaluate the flexibility of FT-DDPC, each test considers several operation modes, in the following order: normal, PFO, restoring, and back to normal. In test I, up to two cells are bypassed and then restored one after another. In test II, three cells are bypassed and then restored. During each test, the time instants at which the affected modules were bypassed or restored are shown in Table III. To highlight both transient and steady-state responses, reduced windows when commuting from one operating mode to another are plotted, as shown in Figs. 17-18.

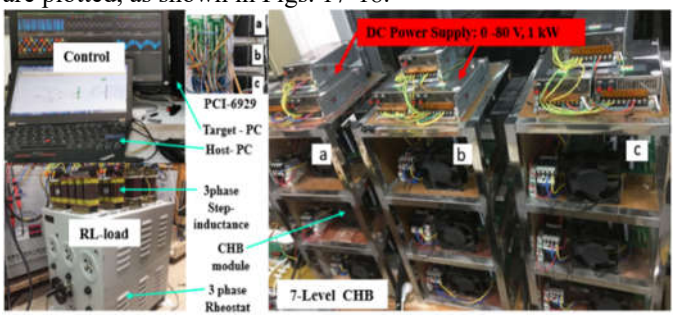

Fig. 16. Overall experimental setup: picture of the hardware interface and power converter connected to a variable RL-load

TABLE III
PERFORMANCES FOR FAULT-TOLERANT OPERATION AT STEADY STATE

	[0 s, 1 s]	[1 s, 2 s]	[2 s, 3 s]	[3 s, 4 s]	[4 s, 5 s]
Test I	Normal	λ_{a1}=0	$\lambda_{a1,a2}$=0	λ_{a1}=0	Normal
THD(%)	< 4	$\cong 4$	$\cong 4$	< 4	< 4
η (%)	< 1	< 1	$\cong 1$	< 1	< 1
$\bar{M}$ (A)	0.14	0.14	0.15	0.15	0.15
$\bar{J}$ (A)	0.18	0.18	0.19	0.19	0.18
Test II	Normal	$\lambda_{a1,a2}$=0	$\lambda_{a1,a2}$= λ_{b1}=0	$\lambda_{a1,a2}$=0	Normal
THD(%)	< 4	$\cong 4$	$\cong 5$	< 5	< 4
η (%)	< 1	< 1	$\cong 1$	< 1	< 1
$\bar{M}$ (A)	0.15	0.15	0.16	0.14	0.15
$\bar{J}$ (A)	0.18	0.19	0.18	0.18	0.18

With experimental results, it is difficult to normalize the DS to the inverter SV since several uncertainties simultaneously affect the system. The geometry of DS is modified according to each operating mode by the update scheme, as shown in Figs. 17(a) and 18(a). It is the opposite of a fixed SV in MPC, which is tuned at normal mode and with nominal parameters. Since DS is a reliable representation of the system under each operating configuration, FT-DDPC does not require a specific design to ensure good and balanced closed-loop response when cells are bypassed or restored. This adaptability is a significant advantage over several FT-PWM, where specific parameters of neutral shift are required for each type of PFO.

The overall performances of tests I and II at steady-state are summarized in Table III. These results validate the ability of FT-DDPC to achieve both balanced currents and line-to-line voltages at different operating conditions even under severe fault operating conditions, such as ($\lambda_{a1,a2}$=0) and ($\lambda_{a1,a2}$=0 and λ_{b1}=0). For all the evaluated cases, the THD and imbalance factor are below 5% and 2%, respectively. In addition, current errors $\bar{M}$ and $\bar{J}$ are both below 0.2 A at steady state.

VI. Conclusion

This paper has proposed an FT-DDPC for CHMLI with faulty cells which is tuned based on a single current control objective. This strategy relies on the model-free prediction approach and the CVC, which is based on a PI-like structure to build up the DS of the system. Considering the load nominal parameters and all states applied, the DS is found to be equivalent to the normal and unbalanced space vectors of the inverter under normal and PFO, respectively. Since, the prediction model is the sum of the measured current and DS, the unbalanced CHMLI problem during PFO mode is included into the current prediction, which enables a fault-tolerant operation by solving only the current control objective. Experimental results under normal, PFO with several bypassed cells and restoring operating modes, and even parameter change have validated the adaptability of FT-DDPC.

The adaptability under various PFO scenarios and parameter mismatches is the main advantage of the proposed controller. However, it requires a longer response time to reach the steady-state in PFO compared to FT-PWM alternatives. To improve the transient response, an effective update technique and learning methods can be investigated in future works. In addition, other works can be focused on the implementation of the proposed controller in other contexts, such as motor drive and grid-connected applications and provide extensive comparative study with the proven FT-PWM strategies.

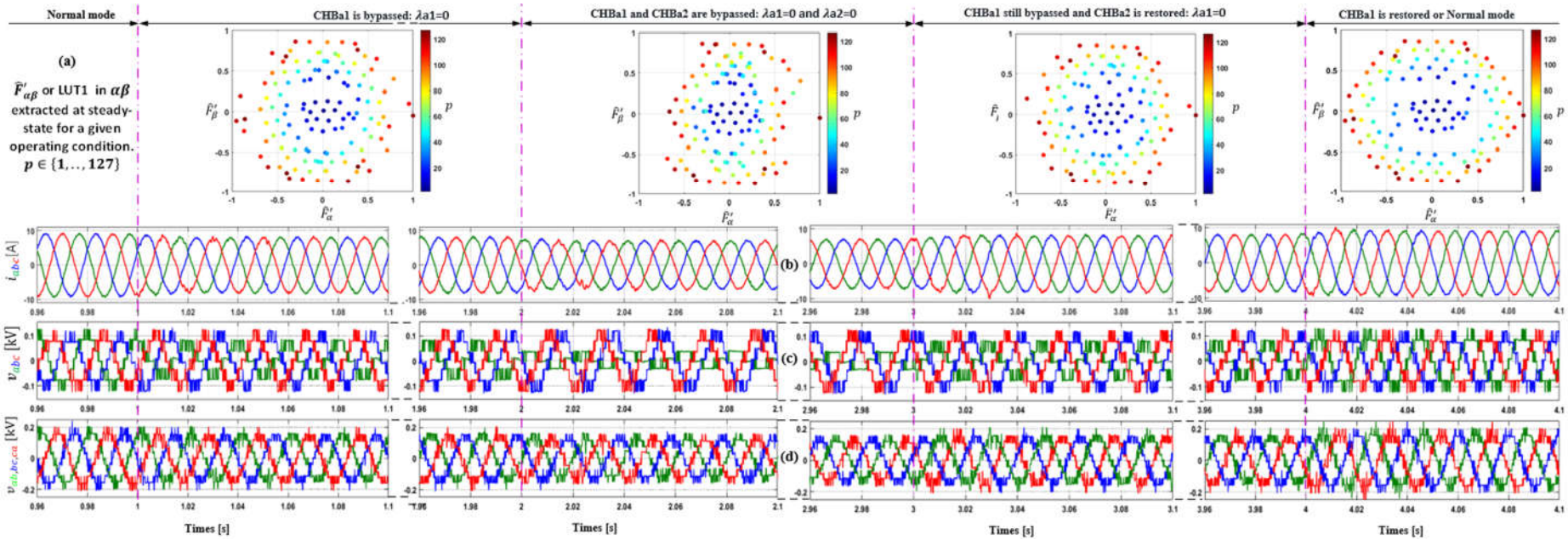

Fig. 17. Experimental results of the proposed controller from normal to fault operation, then from fault to restore phase operation, and finally from restore operation mode back to normal operation (Test I with up to 2 bypassed H-bridge cells) for $k_P = 1$, $k_i = 30 \times 50$, and $G = 0.66$: (a) DS not fully updated and under load parameter mismatches; (b) load current; (c) inverter output voltages; (d) line-to-line voltages.

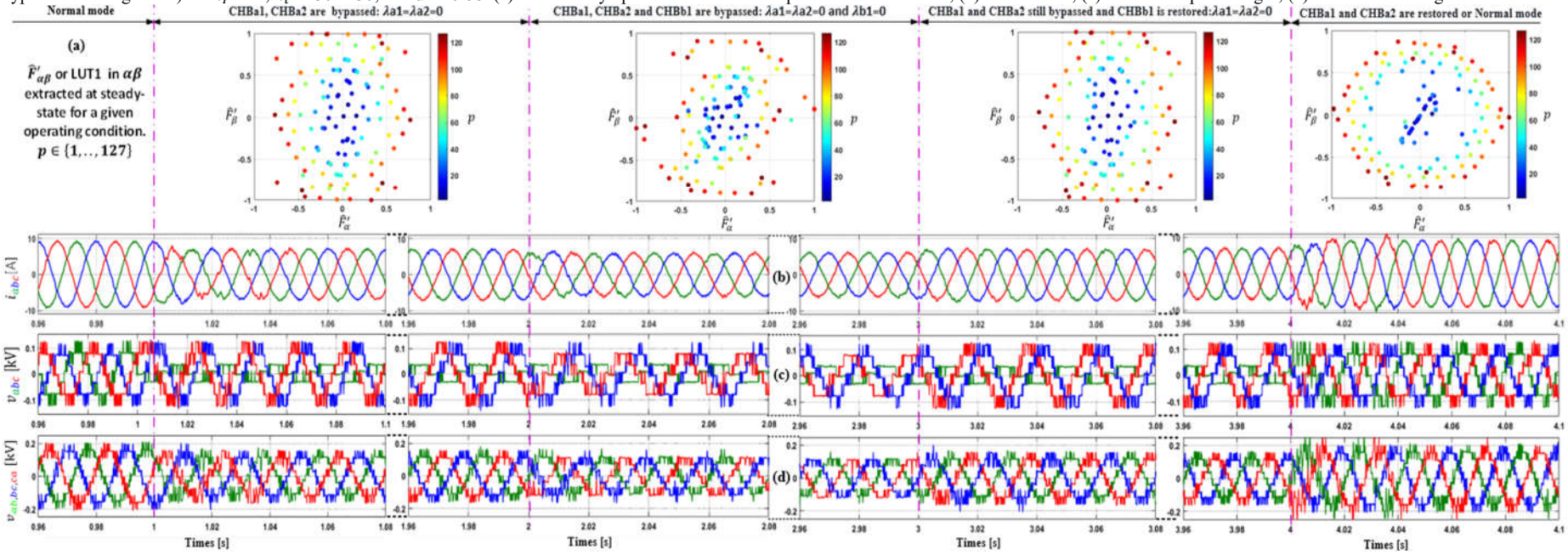

Fig. 18. Experimental results of the proposed controller from normal to fault operation, then from fault to restore phase operation, and finally form restore operation mode back to normal operation (Test II with up to 3 bypassed H-bridge cells) for $k_P = 1$, $k_i = 30 \times 50$, and $G = 0.66$: (a) DS not fully updated and under load parameter mismatches; (b) load currents; (c) inverter output voltages; (d) line-to-line voltages.

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