A Review of Multilevel Inverter Topology and Control Techniques

[1] Gaddafi Sani Shehu, [1] Abdullahi Bala Kunya, [2] Ibrahim Haruna Shanono, and [1] Tankut Yalcinoz
[1] Department of Electrical and Electronics Engineering, Mevlana University, Konya, 42003, Turkey
[2] Department of Electrical and Engineering, Bayero University Kano PMB 3011, Nigeria
Email: sanishehu03@gmail.com, abkunya@abu.edu.ng, ihshanono@buk.edu.ng, tyalcinoz@mevlana.edu.tr

***Abstract*—This paper focused on reviewing the main types of topologies and control strategies employed for the operation of multilevel inverter. Advantages and disadvantages of the topologies and the control techniques in relation to one another are equally reviewed. Recent proposed methods employed to improve the harmonic performance, reduce electromagnetic interference (EMI), lower stress on the power switches, eliminate DC link voltage imbalance and simplify the pulse width modulation control algorithms are fully reviewed. Selective harmonic elimination modulation technique is used in generating the 11-level of output voltage. It is aimed at reducing the total harmonic distortion as low as possible.**

***Index Terms*—harmonic distortion, multilevel inverter, modulation techniques, topology**

I. Introduction

The concept of multilevel inverters (MLI) has been introduced since mid-1970. The term multilevel originated with the three-level inverter. Subsequently, several multilevel inverter topologies continue to emerge, especially in the last two decades. They are power-conversion systems composed by an array of power semiconductors and DC voltage sources that, when appropriately connected and controlled, can generate a multiple-step voltage waveform with variable and controllable frequency, phase and amplitude [1]. The staircase voltage waveform is synthesized by selecting different voltage levels generated by the proper connection of the load to the different DC voltage sources. This connection is performed by proper switching of the power semiconductors [2].

Owing to the increased power rating, improved harmonic performance, reduced electromagnetic interference (EMI), lower stress on the power switches and reduced voltage derivatives (dv/dt) [1], multilevel inverter has continually draws the industrial and academic attention as preferentially one of the leading electronic power conversion mechanism for high power, medium voltage applications [2] and renewable energy interface; such as in photovoltaic (PV) [3], [4], wind [5] and fuel cells [6]. Multilevel inverters have been widely applied to chemical, liquefied natural gas plants, water treatment plants, transportation system (hybrid-plug-in vehicle), power generation, transmission and distribution systems [1]. Intuitively, this is why researchers are spending much efforts trying to improve multilevel inverter through control simplification, reducing the number of DC sources and enhancing the total harmonic distortion (THD) of the output signal [7].

However, for any advantage there usually be a corresponding disadvantage, multilevel inverter is not an exceptional case as it employ higher number of electronic components compared to conventional two-level inverters, introduce complexity in control and DC link capacitor voltage imbalance [8], [9]. Some approaches are developed to reduce the number of switches [8], eliminate DC link voltage imbalance [10], [11] and simplify the pulse width modulation control algorithms [12].

The operations, power ratings, efficiency and of course, applications of multilevel inverter depends majorly on its topology and the type of control algorithm used in its PWM controller [13]. The most commonly known multilevel inverter topology is [2], [7], [14]-[16]:

- Neutral-point-clamped (Diode clamped) MLI
- Flying capacitor (Capacitor clamped) MLI
- Cascaded H-bridge MLI

By combining these topologies with one another, hybrid inverter topologies have been developed. Similarly, by applying different DC voltage levels, an asymmetric hybrid inverter topology has equally been in achieved.

Moreover, MLI control techniques which are based on fundamental and high switching frequency includes [2]:

- Space vector control
- Selective harmonic elimination
- Space vector PWM
- Sinusoidal PWM

As the paper is structured, after this introductory part, Section II and III of this paper give detailed account on the topology and control techniques of MLI. Section IV presents some discussions on the results obtained from the simulation carried out, while the last section concludes the paper.

II. Multilevel Inverter Topology

Generally, these inverters can be classified as voltage source or current source inverters as shown in Fig. 1.

Manuscript received December 8, 2014; revised May 22, 2015.

doi: 10.18178/joace.4.3.233-241

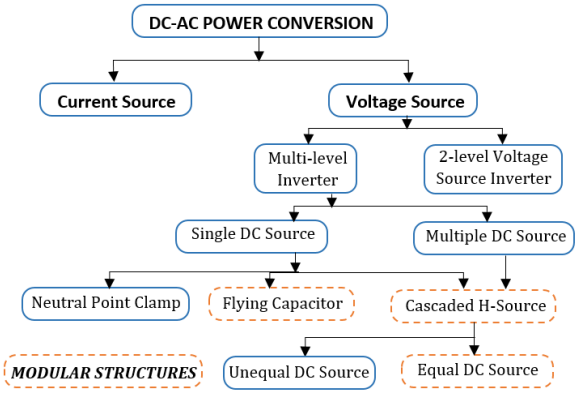

Figure 1. Multilevel inverter topologies [1].

Three major multilevel inverter configurations applied in industrial applications and mentioned in several literatures; cascaded H-bridges inverter with separate DC sources, neutral-point clamped, and flying capacitors used virtually in low, medium and high power applications are briefly discussed. However, there are "hybrid" circuits that are achieved through the combinations of two or more major multilevel topologies or slight reconfigurations to the original one. Some this MLIs has modular structures.

A. *Cascaded H-Bridge Multilevel Inverters(CHBMI)*

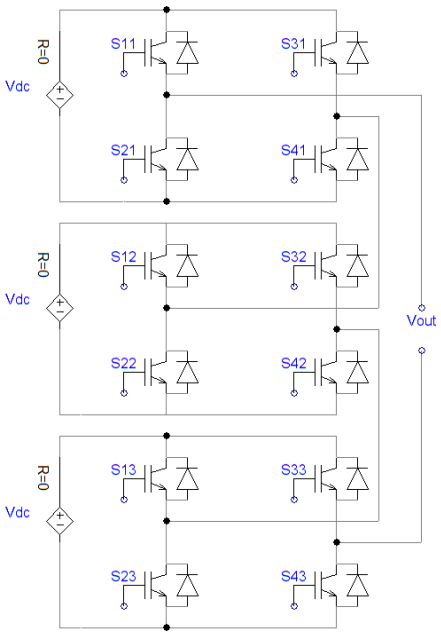

Figure 2. Cascaded bridge multilevel inverter

The CHBMI conventionally requires separate DC sources, but recently a single source is analyzed both are well suited for various renewable energy sources such as photovoltaic [3], [4], fuel cell [6] and biomass. This configuration has recently become very ubiquitous in AC power supply and adjustable speed drive applications [17]. A single-phase *n*-level configuration of such inverter is shown in Fig. 2. Each module consists of a separate DC source associated with a single-phase full-bridge inverter. The terminal voltage of each module is connected in series to form an output voltage V_{out}. The output voltage is synthesized by the sum of each DC source from each module [2]. The number of module (*m*), which is the same as the number of DC sources required, depends on the number of levels (*n*) of the CHBMI. *n* is taken as odd, so as to give an integer-valued number of output phase voltage levels, *m* given by (*n*-1)/2 [18]:

In another literature, the number of output phase voltage levels *m* in a cascade inverter is defined by 2*s*+1, where *s* is the number of separate DC sources [19]. This topology has the advantages of automatic voltage sharing across the switches in a module due to the usage of independent voltage sources. The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be faster, easier and cheaper. The disadvantage of the topology is that separate dc sources are required for each of the bridge [20].

B. *Neutral Point Clamped Multilevel Inverters(NPCMI)*

The NPCMI uses capacitors in series to divide up the DC bus voltage into a set of voltage levels [21]. An example of a single-phase, four-level diode-clamped inverter is shown in Fig. 3. To produce *n*-levels of the phase voltage, an *n*-level NPCMI needs *n*-1 capacitors on the DC bus. Thus, for a four-level inverter, the DC bus consists of three capacitors C_1, C_2 and C_3. For a DC bus voltage of V_{dc}, the voltage across each capacitor is $V_{dc}/3$. Consequently the voltage stress for each power device is limited to one capacitor voltage level $V_{dc}/3$, through the clamping diodes [22].

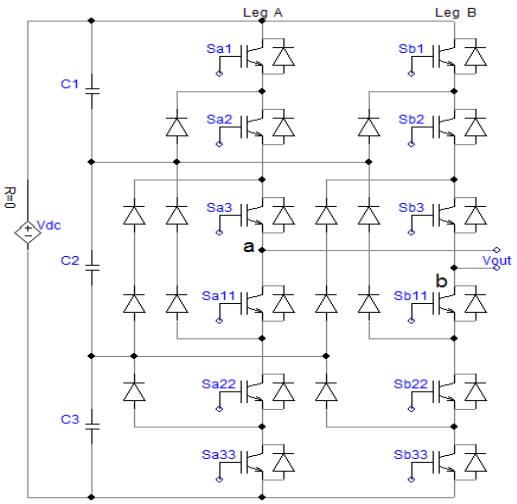

Figure 3. Single-phase four-level NPCMI

This topology has the following advantages; phases share a common DC bus, which minimizes the capacitance requirements of the inverter. This allow back-to-back implementation for high-voltage inter-connection or adjustable speed drive application. The capacitors can be pre-charged as a group. Efficiency is high for fundamental frequency switching.

The main drawback of this topology includes difficulty in real power flow for a single inverter because the intermediate DC levels will tend to overcharge or discharge without precise monitoring and control. The number of clamping diodes required is quadratically

related to the number of levels, which can be cumbersome for units with higher number of levels and not suitable for redundancy [23]-[25].

C. Flying Capacitor Multilevel Inverter (FCMI)

The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, it uses capacitors in their place, hence the name implies. The circuit topology of the flying capacitor multilevel inverter is shown in Fig. 4 [23]. This topology has a ladder structure of DC side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform [22].

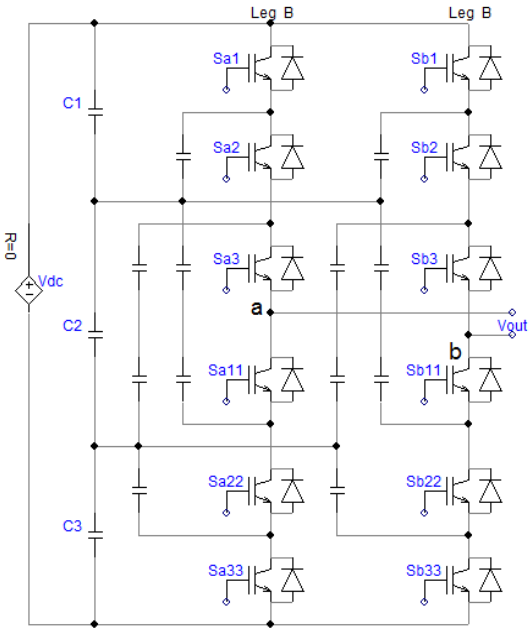

Figure 4. Single-phase four-level FCMI

Unlike the NPCMI, the flying capacitor inverter does not require all of the switches that are ON (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies [24]. These redundancies allow a choice of charging and discharging specific capacitors, and can be incorporated in the control system for balancing the voltages across the various levels.

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels. In another words, two or more valid switching combinations can synthesize an output voltage. Another merit of FCMI is the availability of phase redundancies for balancing the voltage levels of the capacitors. Real and reactive power flow can equally be controlled. The large numbers of capacitors enable the inverter to ride through short duration outages and deep voltage sags. It requires a single isolated dc supply voltage source [23], [24].

Like other topologies it has disadvantages of complicated control in tracking the voltage levels for all of the capacitors. Also, pre-charging all of the capacitors to the same voltage level and startup are complex. Switching utilization and efficiency are poor for real power transmission. The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is more difficult in inverters with higher number of levels [25].

D. Other Multilevel Inverter Structures

Besides the three basic multilevel inverter topologies previously discussed, other multilevel converter topologies have been proposed [26], however, most of these are "hybrid" circuits that are combinations of two of the basic multilevel topologies or slight variations to them. Additionally, the combination of multilevel power converters can be designed to match with a specific application based on the basic topologies.

- *Generalized Multilevel Topology*

The generalized converter topology called P2 topology proposed by Peng [27], as illustrated in Fig. 5.

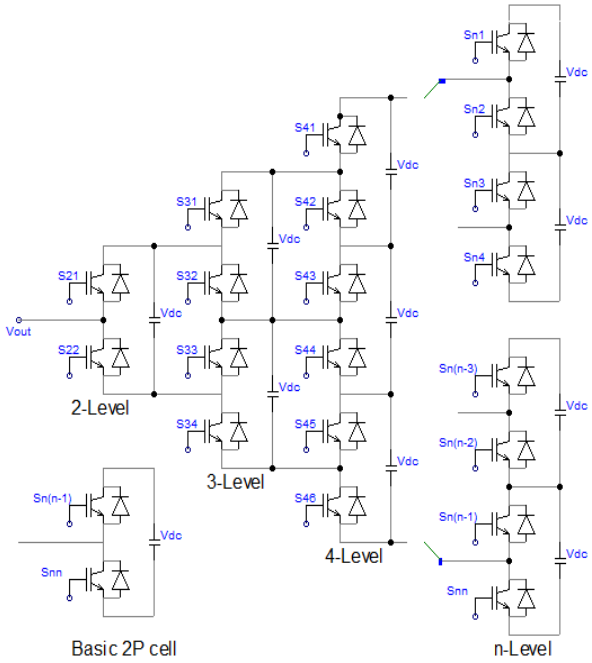

Figure 5. Generalized P2 multilevel converter topology

The basic 2P cell is conjoined in cascade to develop this inverter. The topology can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion and without any assistance from other circuits at any number of levels automatically. Thus, the topology provides a complete multilevel topology that embraces the existing multilevel converters in principle [26], [27].

- *Mixed-Level Hybrid Multilevel Inverter*

The configuration has mixed-level hybrid multilevel units because it embeds multilevel cells as the building block of the cascade inverter. To reduce the number of separate DC sources for high-voltage, high-power applications with multilevel inverters, diode-clamped or capacitor-clamped inverters could be used to replace the full-bridge cell in a cascaded inverter. Fig. 6 shows the 9-level cascade inverter integrating a 3-level diode-clamped inverter as the cell [26]. The original CHBMI requires four separate DC sources for one phase leg and twelve for a three-phase inverter [26], [28]. The advantage of the

topology lies in less separate DC sources requirements, while the disadvantage of this topology is the complexity in its control strategy due to its hybrid structure.

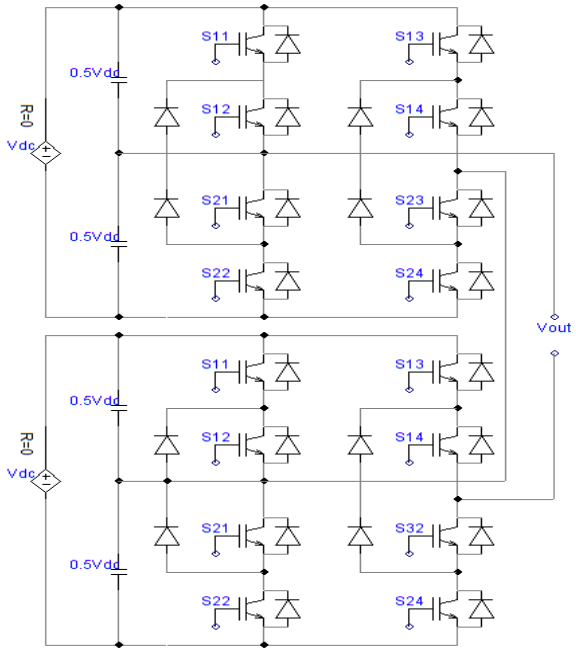

Figure 6. Mixed-level hybrid configuration

- *Back-To-Back Diode-Clamped Inverter*

Two multilevel inverters can be connected in a back-to-back procedure and then the arrangement can be connected to the electrical system in a series-parallel plan as shown in Fig. 7. Both the current needed from the utility and the voltage supplied to the load can be controlled at the same time simultaneously. This series-parallel active power filter has been referred to as a universal power conditioner when used on electrical distribution systems and as a universal power flow controller when applied at the transmission level [22], [29].

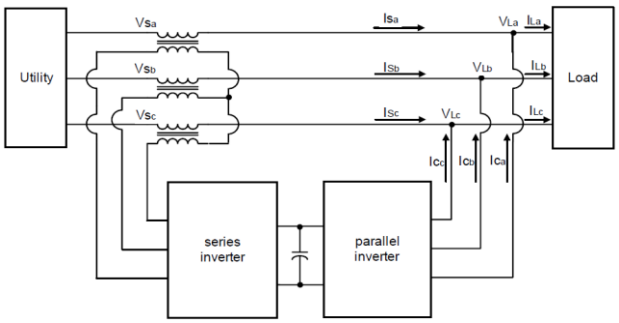

Figure 7. Back-to-back inverters

- *Soft-Switched Multilevel Inverter*

The soft-switching methods can be realized for diverse multilevel inverters to reduce the switching loss and to increase efficiency [26]. For the cascaded inverter, because each inverter cell is a bi-level circuit, the implementation of soft switching is not at all different from that of conventional bi-level inverters. For a flying capacitor or neutral point clamped inverters, soft-switching circuits have been proposed with different circuit arrangements [27]. One of the soft switching circuits is zero-voltage-switching type which includes auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations [22], [29].

III. Multilevel Inverter Modulation Techiques

Sequel to the increased number of level, higher level of complexity is experienced while controlling MLI. However, this complexity could be used to add additional capabilities to the modulation technique, namely; reducing the switching frequency, minimizing the common-mode voltage, or reducing the DC link voltage imbalance [10], [30]. Several modulation techniques have been proposed for cascaded multilevel inverters which are usually an extension of the two-level modulations. These techniques can be classified based on switching frequencies, as shown in Fig. 8.

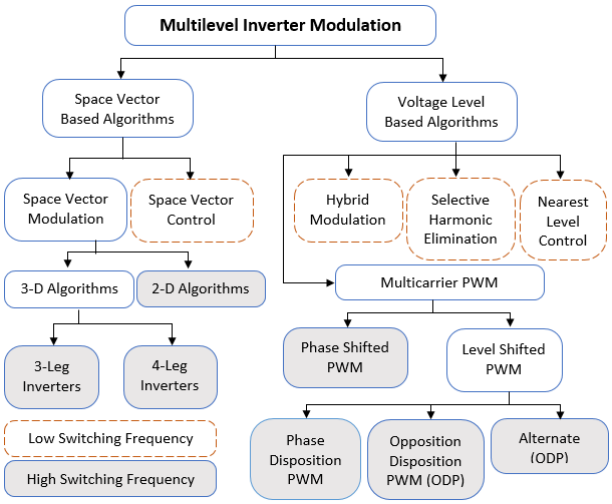

Figure 8. Classification of multilevel inverter modulation [31]

A. Sinusoidal Pulse Width Modualtion.

SPWM involves the superimposing a sinusoidal modulating signal (reference) on to a high frequency triangular carrier signal (the most common and easiest technique) per phase. (k-1) carrier signals are required k-level inverter. The instantaneous intersections between these two signals switch the switching device 'ON' if the modulating signal is greater than carrier signal assigned to that switch. The ratio of these signals' amplitude and frequency called amplitude modulation index, m_a and frequency modulation ratio, m_f defined in (1) and (2).

$$m_a = \frac{A_{sin}}{A_{tri}} \tag{1}$$

$$m_f = \frac{f_{tri}}{f_{sin}} = 3k \quad (k \in N+) \tag{2}$$

where A_{sin}, A_{tri}, f_{sin} and f_{tri} are amplitudes and frequencies of the modulating signal and carrier signal respectively. Table I summarizes the implication of this modulation indices to the output of the inverter.

TABLE I. IMPLICATION OF MODULATION INDEX TO SPWM

Modulation Index	Modulation	Consequences
$0 \le m_a \le 1$	Linear Modulation.	The output, V_o is a linear function of m_a and the inverter DC input, hence is the desired region of operation.
$m_a > 1$	Over Modulation.	The output no longer possess that linearity, and causes the carrier signal to undergo phase reversal.
$m_f = 3k$ $(k \in 2N+1)$	---	It is advisable to choose large f_{tri} (range of 2-15 kHz) and odd triple multiple of the f_{sin}. This minimize the harmonic content and prevent high frequency components to prevail.

Fig. 9 illustrates one of the three carrier-based techniques used in conventional inverter that can easily be applied to MLI. It is achieved by comparing a sinusoidal reference with a triangular carrier signal.

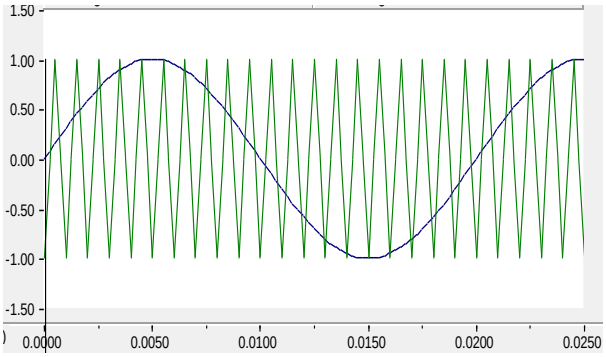

Figure 9. Sinusoidal PWM schematics

Other interesting carrier-based multilevel PWM are sub harmonic PWM (SHPWM) and switching frequency optimal PWM (SFO-PWM) [7]. By super-imposing the carrier signal on one another as shown in Fig. 10, level shift PWM and phase shift PMW are achieved. This method is further classified into three as shown in Fig. 3 based on the carrier signal orientation.

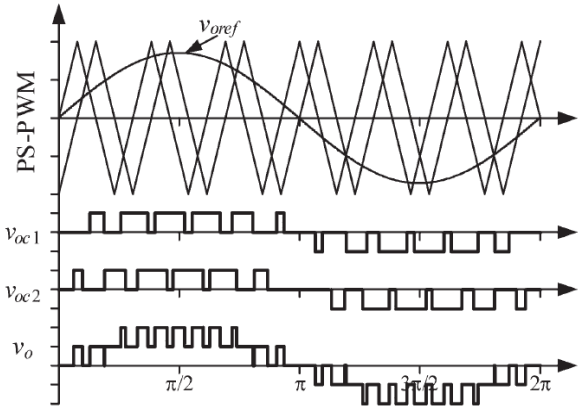

Figure 10. Multilevel phase-shifted carrier-based techniques [30]

B. Multilevel Space Vector Modulation (MSVM)

(MSVM) algorithm is basically a PWM strategy with difference switching times, which are computed based on three phase space vector representation of the reference and the inverter switching states instead of the per-phase in time representation of the reference and the output levels [1]. It involves expressing a reference voltage (V_{ref}) in a vector form and by matching it with discrete switching states, the reference voltage simulated at the inverter output [31]. With increasing *n*, redundant switching states and the complexity in the algorithm (selecting the switching state) and mathematical computation also increase significantly [32]. V_{ref} as depicted in Fig. 11 can be obtained by computing the corresponding duty cycles T_j, T_{j+1}, and T_{j+2} [31].

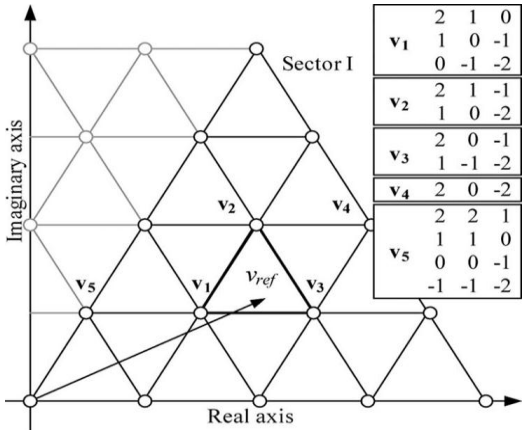

Figure 11. Multilevel SVM [31]

$$V_{ref} = \frac{T_j V_j + T_{j+1} V_{j+1} + T_{j+2} V_{j+2}}{\tau} \quad (3)$$

$\tau = T_j V_j + T_{j+1} V_{j+1} + T_{j+2} V_{j+2}$ is the PWM total period.

C. Selective Harmonic Elimination PWM (SHE-PWM)

SHE-PWM is a low switching frequency PWM method developed for traditional inverters in which a few switching angles per quarter fundamental cycle are predefined and pre-evaluated via Fourier series expansion described in (5), to ensure the elimination of undesired low-order harmonics [18].

$$Hn = \begin{cases} \frac{4}{n\pi} \sum_{k=1}^{m} V_k \left(\cos n\alpha_k\right)? & for\ odd\ n \\ 0, & for\ even\ ,n? \end{cases} \quad (4)$$

where H_n is the amplitude of n^{th} harmonic of the waveform, V_k is the k^{th} level of DC voltage and α_k is the switching angles. The condition: $\alpha_1 < \alpha_2 < \ldots < \alpha_m < \pi/2$ must be satisfied, so as to set the harmonics that will be eliminated to zero [32]. With this operation, a voltage depict in a staircase. In this regard, SHE-PWM provides a narrow range of modulation index, which is its main drawback.

IV. SIMULATION RESULTS AND DISCUSSION

A case study simulation of single phase single source multilevel inverter is considered in this paper. The proposed cascaded H-Bridge inverter model used, consists of three parallel connected H-bridge modules, fed through a single DC voltage source supply. Each of the H-bridge modules has four semiconductor switches and is configured in such a way, that it generate a quasi-

square voltage waveform (+E, 0, -E) at its output terminal. *E* is the main DC source from the supply unit. S_1, S_2, S_3 …S_{12}, are the semiconductor switches V_{P1}, V_{P2}, and V_{P3} are the output terminals of the respective bridges. The total output voltage of the inverter in the Fig. 12 is

$$V_{out} = V_{p1} + V_{p2} + V_{p3} \quad (5)$$

The modulation technique employed on any kind of the inverter topology plays a major role in determining the properties of its output waveform. The selective harmonic elimination method is the modulation technique used in generating the 11-level of the output voltage. Therefore, the switching angles need to be carefully chosen such that the selected odd harmonics are eliminated [33], [34].

This technique apart from producing a power quality output with a lower total harmonic distortion THD, it also reduces the amount of electro-Magnetic interference EMI and switching losses caused by high switching frequency modulation [2], [35]. Specifically in this paper the switching angle used is proposed in [36]. In an effort to verify the proposed multilevel inverter design procedure were set up in PSIM software platform package, both circuit was supply with 100V DC as an input voltage supply, and switching frequency of 5 kHz, details are presented in [37].

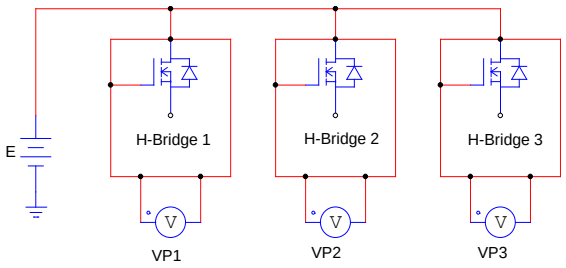

Figure 12. Proposed topology

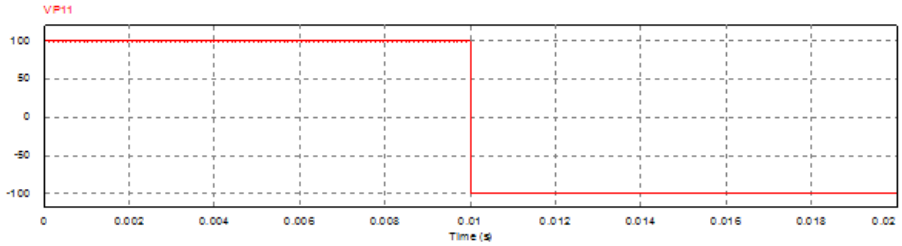

Figure 13. Simulated output terminal voltage for H-bridge 1 (V_{P1})

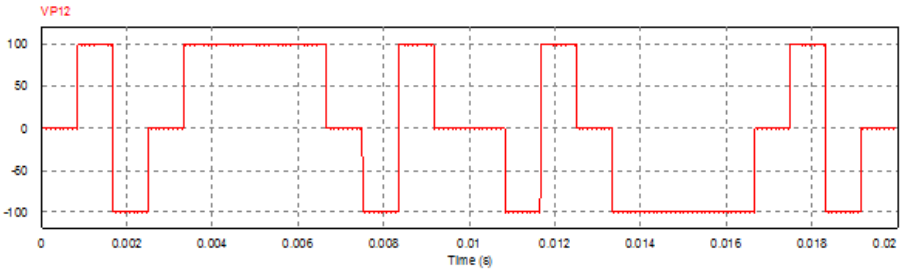

Figure 14. Simulated output terminal voltage for H-bridge 2 (V_{P2})

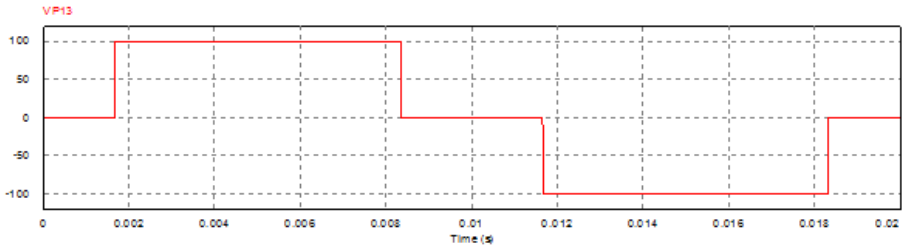

Figure 15. Simulated output terminal voltage for H-bridge 3 (V_{P3})

Fig. 13, Fig. 14, and Fig. 15 are the terminal voltage waveform (V_{P1}, V_{P2}, and V_{P3}) which depict the contribution given by each respective bridge. The total output voltage is obtained by combining these signals as given in (5). From the above terminal voltage, it can be clearly seen that, each respective H-bridge is capable of producing constant output signal without distortion.

The circuit configuration in Fig. 12 is simulated using a load of 100 Ω to avoid floating of the system output terminal during the simulation, and the following results are obtained.

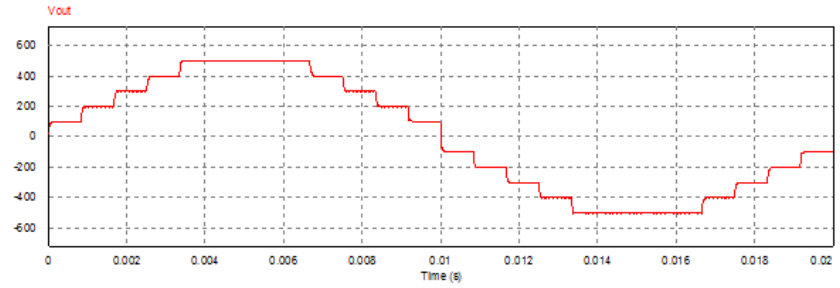

Figure 16. Voltage output waveform of the inverter

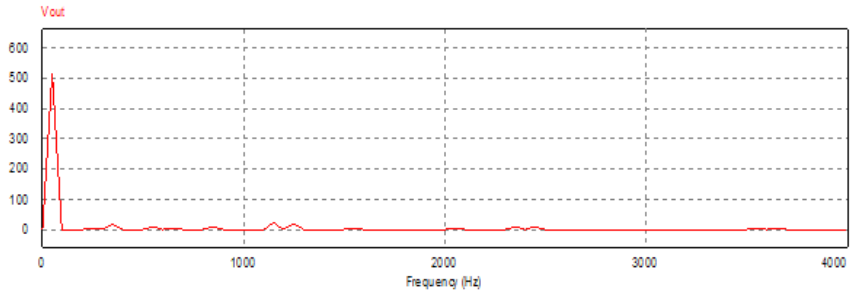

Figure 17. FFT analysis of the inverte

From the Fig. 16 and Fig. 17 it can be seen that an 11-level staircase output signal was obtained with total harmonic distortion (THD) of 5.5%. The voltage waveform and FFT analysis spectrum shows the magnitude of fundamental component and that of harmonic at the above frequencies. The fundamental component amplitude is much higher than that of harmonic order component. It can also be observed that the triple harmonics are concealed out automatically, only the non-triple harmonics are present at lower amplitude.

A combination of resistor-inductor, resistor-capacitor, inductor-capacitor, and combination of both was simulated in each case at nominal values as in Fig. 18.

The value was selected arbitrarily to represent approximate value for the purpose of design and simulation. The actual impedance may vary considerably depending application, in this study nominal impedance is implicitly referring to the frequency response of the circuit under consideration, in which the change in voltage or current waveform, and harmonic level of the inverter is observed. Form Fig. 18 it clearly shows that combination of resistor-capacitor has the lowest THD compare to the rest, meaning for filter design capacitor filter will be of significant choice for this inverter type. For RL, LC, and RLC loads are having almost similar harmonic contain level.

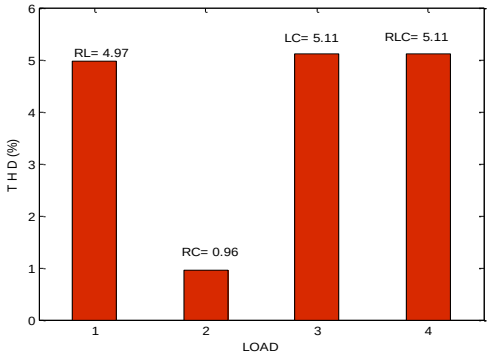

Figure 18. Different load combination against THD

Finally all the simulation result obtained are within theoretical expectation and provided us with detail characteristic of multilevel inverter performance characteristic under different load condition prior to implementation.

V. Conclusion

Multilevel inverters have matured from being a growing technology to a sound-established practical approached solution for low to medium voltage and high power application. The three major reported topology are cascaded H-bridge with separate DC source, neutral point clamp and flying capacitor. While in this paper a proposed cascaded H-bridge with a single DC source was proposed and simulated and various hybrid multilevel inverter was also presented. Various Multilevel control strategy and application are also discussed. Due to numerous applications of multilevel inverter and flexibility to design the hybrid topologies, and switching control especially in the digital era with numerous simulation software, this paper cannot cover all the area, but an insight to the useful literature.

Acknowledgment

The author Gaddafi Sani Shehu wish to thank The Scientific and Technological Research Council of Turkey (TUBITAK) for supporting his PhD program.

References

[1] Rodriguez, *et al*, "Multilevel converters: An enabling technology for high-power applications," in *Proc. the IEEE*, vol. 97, no. 11, November 2009, pp. 1786-1817.

[2] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, vol. 52, no. 2, pp. 1114–1128, February 2011.

[3] P. K. Dewangan and U .T. Nagdeve, "Review of an inverter for grid connected Photovoltaic (PV) Generation System,"

Internatıonal Journal of Scientific & Technology Research, vol. 3, no. 10, October 2014.
[4] I. D. Pharne and Y. N. Bhosale, "A review on multilevel inverter topology," in *Proc. International Conference on Power, Energy and Control*, 2013, pp. 700-703.
[5] S. S. Das, S. C. Gupta, and U. Rajkiran, "Harmonıc mitigation in wind energy conversion system by multilevel inverter," *International Journal of Electrical, Electronics and Data Communication*, vol. 2, no. 9, September, 2014.
[6] R. Seyezhai and B. L. Mathur, "Hybrid multilevel inverter using ISPWM technique for fuel cell applications," *International Journal of Computer Applications (0975 – 8887)*, vol. 9, no.1, pp. 41-46, November 2010.
[7] Leopoldo, *et al*, "The age of multilevel inverter arrives," *IEEE Industrial Electronics Magazine*, pp.28-39, June 2008.
[8] S. Cherukuru, C. Joel., S. J. Jonish, and K. Sathiyasekar, "New modified cascaded H-bridge multilevel inverter topology with reduced switches," *International Journal of Engineering Trends and Technology*, vol. 9, no. 4, pp. 178-181, March 2014.
[9] A. Vinodkumar and S. Hariprasad, "Modeling of new multilevel inverter topology with reduced number of power electronic components," in *Proc. International Conference on Innovations in Electrical & Electronics Engineering*, Hyderabad, 2014, pp. 23-30.
[10] S. Divya and G. Umamaheswari, "Voltage unbalance elimination in multilevel inverter using coupled inductor and feedback control," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, vol. 3, no. 4, pp. 9253-9258, April 2014.
[11] B. Rajashekar, T. P. Kumar, and R. Ramesh, "Cascaded H-bridge multilevel inverter with a new selective harmonic mitigation technique to meet grid codes under non-equal Dc link voltages with power quality enhancement*," International Journal of Innovative Research in Science, Engineering and Technology*, vol. 3, no. 9, pp. 15857-15863, September 2014.
[12] A. Tuteja, A. Mahor, and A. Sirsat, "A review on mitigation of harmonics in cascaded H-bridge multilevel inverter using optimization techniques," *International Journal of Emerging Technology and Advanced Engineering*, vol. 4, no. 2, pp. 861-865, February 2014.
[13] H. Sira-Ramírez and R. Silva-Ortigoza, *Control Design Techniques in Power Electronics Devices*, 1st ed. Mexico City, ch. 6, pp. 361-366.
[14] K. B. Bhaskar1, T. S. Sivakumaran, and M. Devi, "Implementation of 11 level cascaded multilevel inverter using level shifting pulse width modulation technique with different loads," *IPASJ International Journal of Electrical Engineering*, vol. 2, no. 10, pp. 20-31.
[15] P. Premananth and S. B Chitrapreyanka, "A new multilevel inverter topology for DC-AC conversion," *International Journal of Innovative Research in Science, Engineering and Technology*, vol. 3, no. 2, pp. 194-202.
[16] P. Sanjeevikumar, "Analysis and implementation of multiphase-multilevel inverter for open-winding loads," Ph.D. dissertation, Dept. Elect. Eng., Univ. Of Bologna, Bologna, Italy, March 2012.
[17] L. M. Tolbert and F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," *IEEE Power Engineering Society Summer Meeting*, vol. 2, pp. 1271-1274, July 2000.
[18] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel converters," in *Proc. 34th IAS Annual Meeting IEEE Industry Application Conference*, vol. 2, Oct. 1999, pp. 1186–1192.
[19] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: Survey of topologies, controls, and applications," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 724-738, Aug. 2002.
[20] S. Khomfoi and L. M. Tolbert, *Multilevel Power Converters*, Chapter 17, Power Electronics Handbook, 2nd Ed., Elsevier, 2007.
[21] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," *IEEE Power Electronics Specialists Conference*, PESC'92, vol. 1, pp. 397-403, 1992.
[22] J. S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transaction on Industry Application*, vol. 32, no. 3, pp. 509-517, May/June 1996.
[23] I. H. Shannon, *Multilevel Converters: The Future of Renewable Energy: Design, Simulation and Implementation of a Multilevel Converter*, pp. 05-43, LAP LAMBERT Academic Publishing USA, November 6, 2012.
[24] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, pp. 36-44, 1999.
[25] S. Daher, *Analysis, Design and Implementation of a High Efficiency Multilevel Converter for Renewable Energy System*, PhD Dissertation, and University press GmbH kessel, 2006.
[26] S. Khomfoi and L. M. Tolbert, *Multilevel Power Converters*, ch. 17, Power Electronics Handbook, 2nd Edition, Elsevier, 2007.
[27] F. Z. Peng, "A generalized multilevel converter topology with self-voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no.2, pp. 611–618, Mar./Apr. 2001.
[28] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel converters," in *Proc. 34th IAS Annual Meeting IEEE Industry Application Conference*, vol. 2, Oct. 1999, pp. 1186–1192.
[29] A. V. Zyl, J. H. R. Enslin, and R. Spee, "A new unified approach to power quality management," *IEEE Transactions on Power Electronics*, vol. 11, no. 5, pp. 691-697, Sept. 1996.
[30] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans on Industrial Electronics*, vol. 57, no. 7, pp. 2197-2206, July 2010.
[31] N. Mittal, B. Singh, S. P Singh, R. Dixit, and D. Kumar, "Multilevel inverters: Survey of topologies, controls, and applications," in *Proc. 2nd International Conference on Power, Control and Embedded System*, 2012, pp. 978-986.
[32] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: Survey of topologies, controls, and applications," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 724-738, Aug. 2002.
[33] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Transaction on Industry Applications*, vol. 33, no.1, pp. 202–208, Jan./Feb. 1997.
[34] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transaction on Industrial. Electronics*, vol. 49, no.4, pp. 858-886, 2002.
[35] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Transaction on Power Electronics*, vol. 21, no. 2, pp. 459-469, March 2006.
[36] F. L. Lou, "Investigation on best switching angles to obtain lowest THD for multilevel DC/AC inverter," in *Proc. IEEE 8th Conference on Industrial Electronics and Application*, Anhui University, Hefei, China, 2013, pp. 1814-1818.
[37] G. Shehu, T. Yalcinoz, and A. Kunya, "Modelling and simulation of cascaded H-bridge multilevel single source inverter using PSIM," in *Proc. World Academy of Science, Engineering and Technology, International Science Index 89, International Journal of Electrical, Robotics, Electronics and Communications Engineering*, vol. 8, no. 5, pp. 744 – 749, 2014.

Gaddafi S. Shehu received his Bachelor of Electrical Engineering in 2009 from Bayero University Kano-Nigeria. He obtained his M.Sc. in Electrical and Computer Engineering with research in the area of multilevel converter from Meliksah University, Kayseri-Turkey in 2014. Currently pursuing his PhD at Mevlana University Konya-Turkey. His area of research interest are Multilevel Converters, Renewable Energy, and Electric Vehicles.

Abdullahi B. Kunya was born in Kunya/Kano, Nigeria in 1988. He received, in the year 2011, his B.Eng. Electrical from prestigious Ahmadu Bello University, Zaria-Nigeria where he is currently working as Lecturer II. He obtained his M.Sc. in Electrical and Computer Engineering with research in Application of Power Electronic Devices on Smart Grids from Meliksah University, Kayseri-Turkey. He is, at present, a PhD student at Mevlana University, Konya-Turkey. His research interests include Power Electronic Converters, Smart Grids, Optimization theory and Neural Networks.

Tankut Yalcinoz received the B.Sc. degree in electrical and electronic engineering from Karadeniz Technical University, Turkey in 1990 and the M. Sc. degree from Cukurova University, Turkey in 1993. In 1998 he obtained a Ph. D. from Imperial College, London University in London. He is a professor at Mevlana University, Turkey. He is the author or coauthor of more than 100 published papers, including 48 articles in refereed journals. His main interests are in power system planning and operation, computational intelligence, renewable energy, flexible ac transmission systems, power electronics and fuel cells. He is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE).

Ibrahim Haruna Shanono received his B.Eng. and M.Sc. degree from Bayero University Kano and Nottingham University in 2008 and 2012 respectively. He is currently working with the Department of Electrical Engineering, Bayero University Kano, Nigeria. His research interest Power Electronics and Automatic Control System.