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A Low-voltage Low-loss Active Reflected Wave Canceller for a Medium Voltage SiC Motor Drive based on a Generalized Multilevel Inverter Topology

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***Abstract*- Multilevel topologies with SiC devices for medium voltage (MV) motor drive have advantages to reduce the harmonics and device voltage stress as well as to increase the efficiency. However, with the application of SiC devices, the reflected wave phenomenon still happens in multilevel motor drive due to its high dv/dt, resulting in overvoltage at motor terminals. This paper proposed a T-type circuit based active reflected wave canceller (ARWC) to suppress the overvoltage of a M-level motor drives with reduced voltage rating of V_{dc}/(M-1). A coupled inductor is applied to isolate the ARWC output and the main inverter. In addition, the coupled inductor is designed with a small resistor to allow low current flowing into ARWC. The proposed ARWC configuration can be applied for general multilevel topologies. A 3-level ANPC converter with 3.3 kV SiC device is built in the laboratory. A 1.2 kV SiC module is applied in the proposed ARWC. The experimental results at 1.6 kV V_{dc} and 16 A (RMS) load current with and without proposed ARWC are provided and compared to verify the validity of proposed method.**

I. Introduction

Two-level (2-L) VSI and several multilevel voltage source inverter (VSI) topologies are popular for industrial motor drive applications [1]. For example, 2-L VSI, three-level neutral point clamped (3-L NPC) converter, five-level active neutral point clamped (5-L ANPC), and cascaded H-bridge (CHB) converter have been employed in commercial products [2][3]. On the other hand, SiC MOSFETs has lower switching loss and higher temperature operation compared to the Si- counterparts, therefore when they are applied to motor drive, the motor drive will gain benefits in weight, volume, as well as lifetime and cost associated with loss. However, the fast switching speed of SiC devices will aggravate the reflected wave phenomenon which results in overvoltage at motor terminals. It is reported in [4] that the overvoltage ratio at the motor terminal increased from 20% to 100% when PWM voltage rise time decreased from 200 ns to 25 ns with 20 ft cable length. This surge voltage has been recognized as a main source of premature winding insulation failures in drive systems [5].

Several papers have presented solutions to address the dv/dt issues of 2-L SiC motor drives [4] -[8]. In [4], a passive dv/dt filter is developed for a 75 kW high frequency (40kHz switching frequency) SiC motor drive. The dv/dt filter consisting of R-L-C networks can reduce dv/dt from 8 V/ns to 1 V/ns. The measured damping resistor loss is around 600 W with optimized design. The authors in [6] has proposed another passive dv/dt filter. By using the stray inductance between the power device and the converter output, only a small R-C network on a standard low-cost printed circuit board is required for the dv/dt filter. The dv/dt can be reduced from 23 V/ns to 7.5 V/ns with the designed filter. The calculated resistor power loss of proposed filter for a 100 kW converter with 5 kHz switching frequency is less than 200 W. Compared to active methods, passive dv/dt filter is usually bulky and lossy.

To reduce the filter size and power loss, the cancellation concept is applied with active devices [7][8]. Reference [7] utilized T-type topology in 2-L motor drive applications to generate two-step voltage waveforms. The reflected voltage of the first step can be cancelled by the one of the second step. The size of the total system can be reduced because there are no passive components for this method. The load current, however, will flow through T-branch switches, the increased loss and cost is therefore not small for higher power applications. In addition, this T-type topology can only achieve the cancellation effect for 2-L motor drives, a 3-L motor drive will require a 5-L topology to achieve reflective wave cancellation.

Reference [8] provides a lower-loss lower-cost method to achieve the cancellation effect. This method adopts an external clamping circuit to generate a nanosecond voltage pulse to break the rising/falling edge into two steps for reflected voltage cancellation. Compared to method of [7], the external clamping circuit can be implemented with low current rating devices since the load current does not flow through it. In addition, the power loss of the external circuit is also low which is only 22 W for 6 kVA/phase application. This external clamping circuit is designed for 2-L motor drive and needs to be modified for multilevel motor drive applications.

Most of the state of the art methods to solve reflective wave phenomenon are for 2-L motor drives [4]-[8]. Recently SiC devices have been applied to multilevel motor drive due to their better thermal conductivity, higher current density, and smaller losses. Reference [1] has reported that the 5-L ANPC converter based on MV SiC MOSFETs would feature considerably higher efficiency compared to MV Si IGBTs. Reference [9] and [10] have demonstrated the advantages of hybrid "Si +SiC" in 3-L

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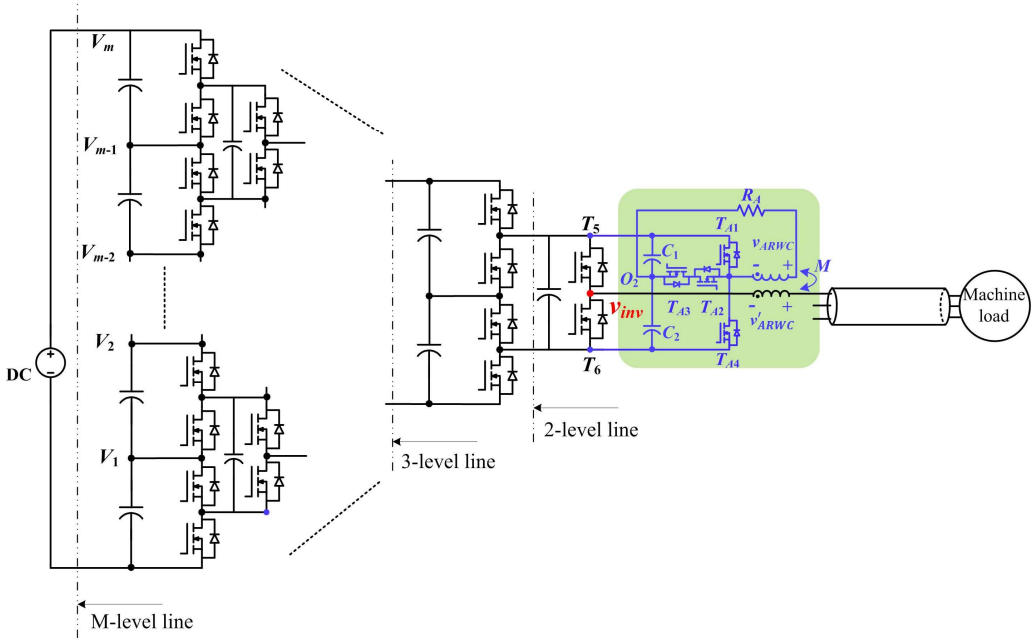

Fig. 1 Proposed ARWC for a MV motor drive with a generalized multilevel inverter topology

ANPC and 5-L ANPC motor drive, respectively. Because of SiC device adoption, the reflective wave phenomenon still exists for above multilevel motor drive.

The passive dv/dt filter can still be applied for SiC multilevel application. It is reported in [4] that the power loss of the damping resistor is proportional to the dc voltage squared and the switching frequency. Therefore, the power loss of passive dv/dt filter will be extremely high in MV SiC motor drive applications which has high voltage and high switching frequency. When the cancellation method in [7] is extended to multilevel applications, a higher-level topology is required. The multilevel topology can also generate quasi-two-level waveforms for the cancellation of reflected voltage [11]. All the switches in these two cancellation methods need to be designed with high current rating devices. In addition, the switching loss and conduction loss induced by the extra switches will be high in MV applications which will reduce the efficiency. The method presented in [8] can also be extended to multilevel motor drive. But the external clamping circuit needs more devices to clamp the voltage to the neutral-point of each level when the main inverter topology is neutral-point clamped inverter (NPC), cascaded H-bridge inverter or modular multilevel converter (MMC). For example, for a M-level motor drive, the external clamping circuit of [8] needs at least $2 \times (M-1)$ active devices.

This paper proposes a low-voltage low-loss active reflected wave canceller (ARWC) for multilevel SiC motor drive based on the cancellation concept. The ARWC utilizes low current rating devices and only requires four active devices per phase for M-level inverter. The ARWC is connected to the main inverter through a coupled inductor for isolation, allowing the ARWC applied for a general multilevel topology regardless of level numbers. In addition, the canceller does not need a separate dc power supply. The proposed ARWC for multilevel motor drive is introduced in Section II. The operation modes of ARWC for a 3-L ANPC SiC inverter is presented in Section III. The experimental verification of ARWC for one phase 8 kVA application is provided in Section IV while the conclusion is presented in Section V.

II. Multilevel Motor Drive and Proposed ARWC

The proposed ARWC applied for a MV motor drive with a generalized multilevel inverter topology is shown in Fig. 1. Due to symmetrical feature, only a single phase circuit is illustrated in detail. The general multilevel topology has been introduced in [12]. The proposed ARWC, highlighted in green, consists of a T-type circuit with devices T_{A1} - T_{A4}, one small resistor R_A, two split high frequency capacitors C_1, C_2, and one coupled inductor L_H for each phase.

The key voltage waveforms of ARWC for a 3-L and 5-L motor drive are presented in Fig. 2. For 3-L inverter output voltage shown in (b), at each rising edge of v_{inv}, the inverter output PWM voltage waveforms, T_{A1} turns on and ARWC generates a negative voltage pulse, breaking the rising edge of v_{inv} into two steps. After a nano-second dwell time, T_{A3} turns on and ARWC operates in freewheeling mode. Similarly, at each falling edge, T_{A4} turns on and ARWC generates a positive voltage pulse, breaking the falling edge of v_{inv} into two steps. After a nano-second dwell time, T_{A2} turns on and ARWC operates in freewheeling mode. Therefore, the rising/falling edge is broken into two steps which have a dwell time (t_D) between these two steps. Similarly, each voltage-level of 5-L inverter output voltage can be split into two steps. Therefore the reflected voltage at motor terminal of the first step can be cancelled by the one of the second step with accurately controlling t_D.

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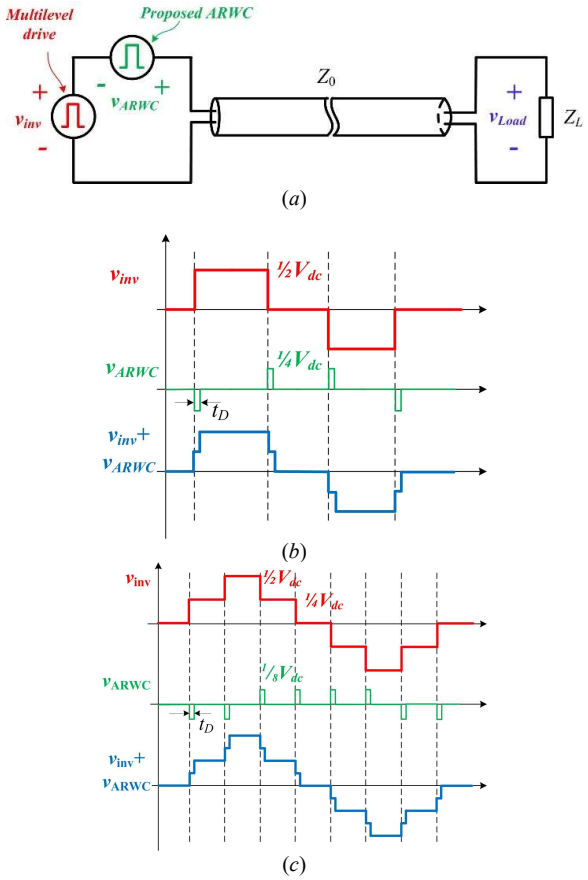

Fig. 2 Key waveforms of proposed ARWC for multi-level motor drive: (*a*) schematics of ARWC with multi-level motor drive; (*b*) voltage waveforms of ARWC for 3-L motor drive; (*c*) voltage waveforms of ARWC for 5-L motor drive.

For a M level motor drive, each step voltage is $\frac{V_{dc}}{M-1}$, therefore, the magnitude of v_{ARWC} should be $\frac{V_{dc}}{2(M-1)}$, which should be $\frac{V_{dc}}{4}$ for a 3-L motor drive and $\frac{V_{dc}}{8}$ for a 5-L motor drive. Therefore, the proposed ARWC can be developed with low voltage rating devices. In addition, the proposed ARWC can be designed with small current rating devices. Because the ARWC operates in freewheeling mode during most of time. A small resistor R_A is designed to reduce the ARWC current.

It is important to note that the proposed ARWC device numbers will not increase with the number of levels. The proposed ARWC, which has 4 active devices for each phase, can be applied not only for 3-L but also for M-level inverters.

III. Operation Mode Analysis

Fig. 3 shows the proposed ARWC for a 3-L ANPC motor drive where T_1-T_4 are operated at fundamental frequency and T_5-T_6 are switching at high frequency, which is suitable to be implemented with hybrid "Si IGBT+ SiC MOSFETs" for MV applications. The operation modes of proposed ARWC and design principle are presented in this section for this 3-L ANPC motor drive.

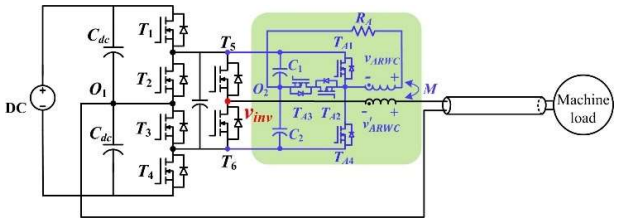

Fig. 3 Proposed ARWC for a 3-L ANPC motor drive (one phase)

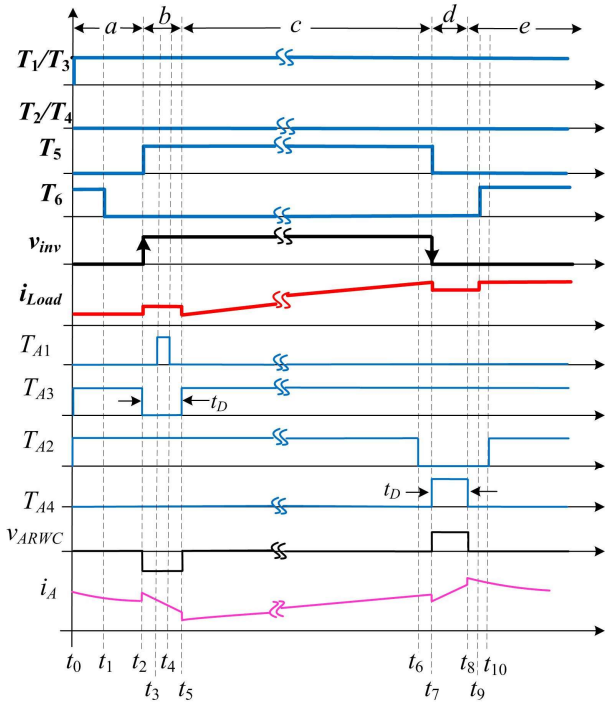

Fig. 4 Key waveforms and operation mode illustration during rising edge and falling edge of v_{inv}.

Considering the similar operation principle of ARWC for each phase, the analysis of ARWC is illustrated on one-phase. Fig. 4 shows key waveforms and operation modes during rising edge/falling edge of v_{inv} where *Mode* (*a*) – (*c*) are for v_{inv} rising edge, *Mode* (*c*) – (*e*) are for v_{inv} falling edge respectively. The commutation of *mode* (*a*) – (*c*) are presented in Fig. 5. Each operation mode is described as follows:

Mode (*a*) [t_0 – t_2]: both ARWC and motor drive are operated in freewheeling mode. During [t_0, t_1], T_5 is off, T_6 is on, T_{A2} & T_{A3} are on. During [t_1, t_2], T_6 turns off at t_1, i_{load} flows through the body diode of T_6. The corresponding equivalent circuit is shown in Fig. 6 (*a*) and following (1):

$$\begin{cases} L_A\frac{di_A}{dt} - M\frac{di_{Load}}{dt} + R_A i_A = 0 \\ -M\frac{di_A}{dt} + (L_A + L_{Load})\frac{di_{Load}}{dt} + R_{Load} i_{Load} = 0 \end{cases} \quad (1)$$

where R_A represents the total resistance in the ARWC circuit loop, M is the mutual inductance of the coupled inductor, L_A is the inductance of the coupled inductor. In *Mode* (*a*), i_{Load} can be approximately treated as DC value, i_A is thereby derived in (2):

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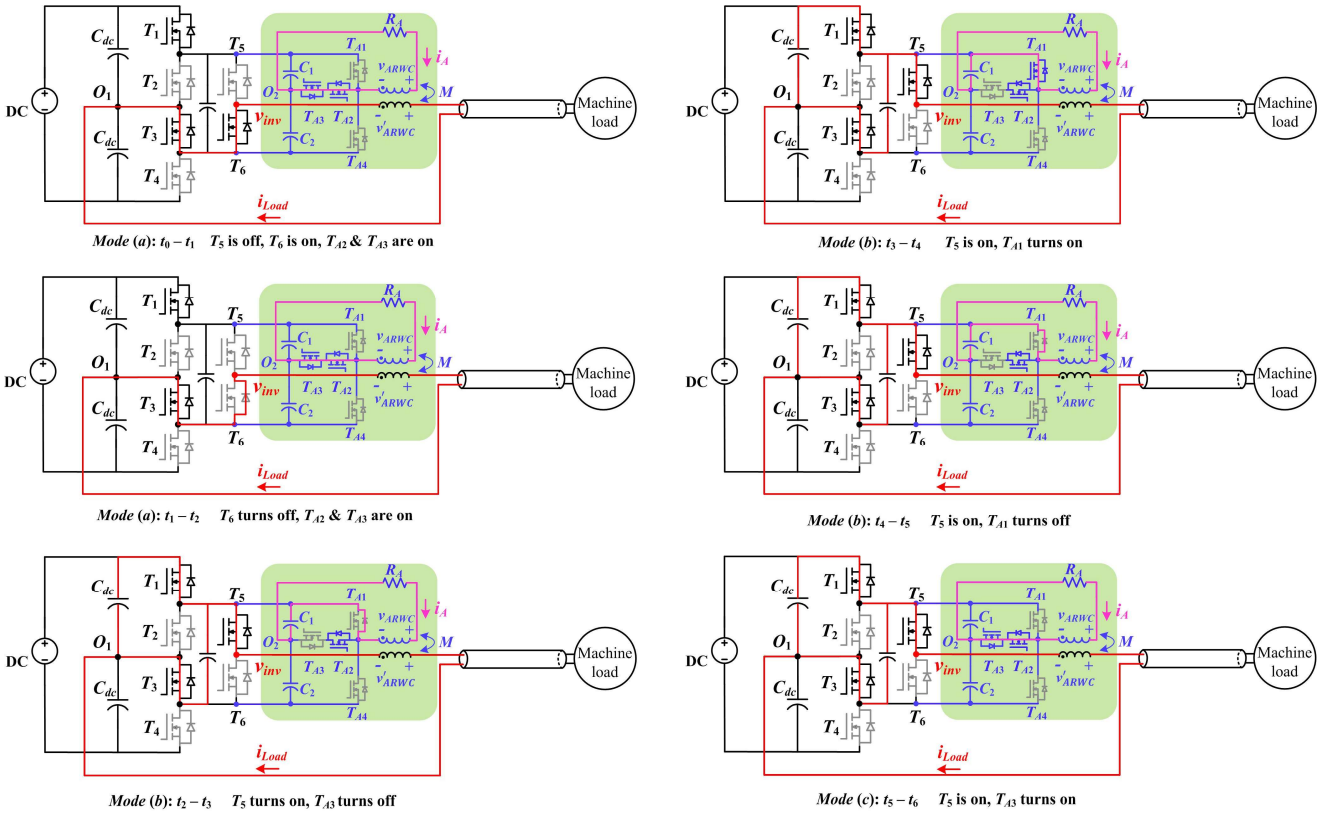

Fig. 5 Operation modes commutation to achieve reflective wave cancelation at rising edge of v_{inv} for 3-L ANPC motor drive.

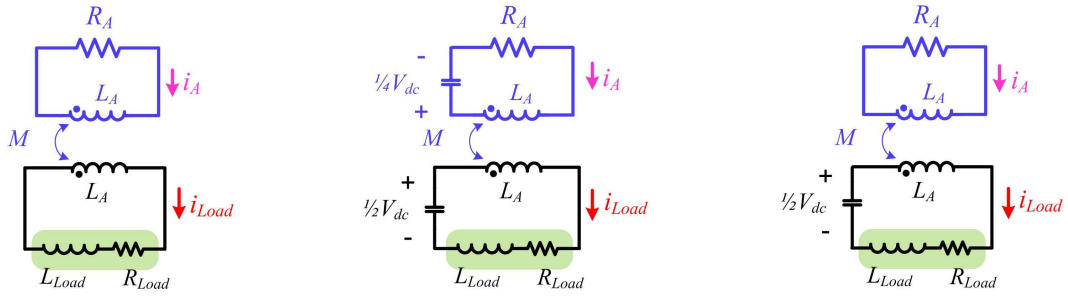

Fig. 6 Equivalent circuit for different operation modes: (a) equivalent circuit for Mode (a); (b) equivalent circuit for Mode (b); (c) equivalent circuit for Mode (c).

$$i_A(t) \approx I_A(t_0) e^{-\frac{R_A}{L_A} t} \tag{2}$$

The magnitude of i_A will decrease slowly and the decreasing slope depends on R_A and L_A.

Mode (b) [t_2 - t_5]: neither ARWC nor motor drive is operated in freewheeling mode. At t_2, T_5 turns on thereby the rising edge of v_{inv} appears. The ARWC needs to generate a negative voltage pulse. Therefore, T_{A3} is turned off at t_2. T_{A1} is turned on from [t_3, t_4] to allow i_A flowing through it. In *Mode* (b), v_{ARWC} is determined by the capacitor voltage V_{C1}, which is ¼V_{dc}. The equivalent circuit is shown in Fig. 6 (b) and following (3):

$$\begin{cases} L_A \dfrac{di_A}{dt} - M \dfrac{di_{Load}}{dt} + R_A i_A = -\dfrac{1}{4} V_{dc} \\ -M \dfrac{di_A}{dt} + (L_A + L_{Load}) \dfrac{di_{Load}}{dt} + R_{Load} i_{Load} = \dfrac{1}{2} V_{dc} \end{cases} \tag{3}$$

therefore i_A of *Mode* (b) can derived in (4):

$$i_A(t) \approx -\frac{1}{4} \frac{V_{dc}}{L_A} (t - t_2) + I_A(t_2) \tag{4}$$

It should be noted that i_{Load} and i_A change instantaneously at t_2 because the cable needs a charging current which can be calculated as $\frac{1}{4} \frac{V_{dc}}{Z_0}$, where Z_0 is the cable characteristic impedance.

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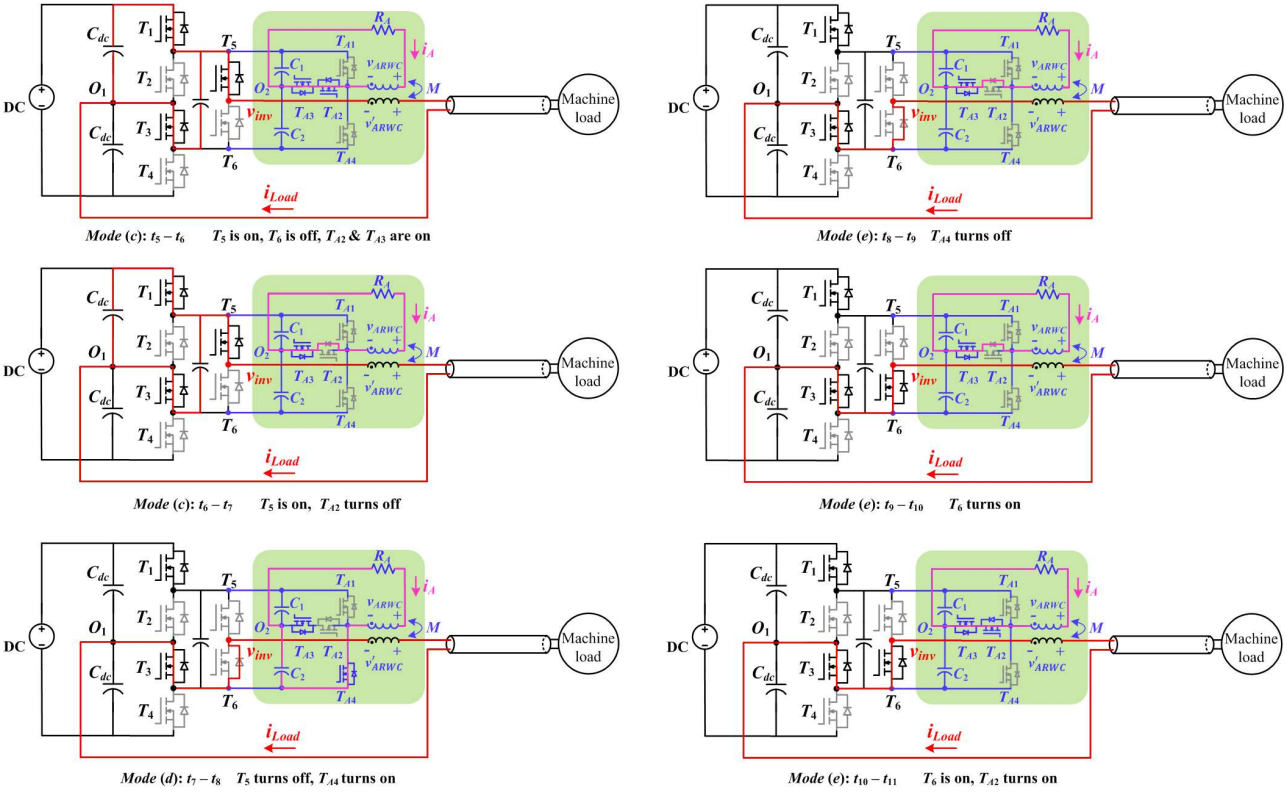

Fig. 7 Operation modes commutation to achieve reflective wave cancelation at falling edge of v_{inv} for 3-L ANPC motor drive.

Mode (*c*) [t_5, t_6]: Only ARWC is operated in freewheeling mode. T_{A3} turns on at t_5, ARWC is in freewheeling mode and the voltage across the coupled inductor is close to zero. The equivalent circuit is shown in Fig. 6 (*c*) and following (5):

$$\begin{cases} L_A\dfrac{di_A}{dt} - M\dfrac{di_{Load}}{dt} + R_A i_A = 0 \\ -M\dfrac{di_A}{dt} + (L_A + L_{Load})\dfrac{di_{Load}}{dt} + R_{Load} i_{Load} = \dfrac{1}{2}V_{dc} \end{cases} \tag{5}$$

i_A of *Mode* (*c*) can derived in (6), where $\tau_A = \frac{L_A}{R_A}$, $\tau_{Load} = \frac{L_{Load}}{R_{Load}}$. From the equation, it can be found that although the ARWC is in freewheeling mode, i_{Load} will be coupled to the ARWC. When R_{Load} is small, i_A will be large, which is a worst case for ARWC loss. In this case, i_A can be derived from (5) by letting $R_{Load} \approx 0$ as follows:

$$i_A(t) \approx I_F + [I_A(t_5) - I_F]e^{-\frac{t}{\tau_A}} \tag{7}$$

where $I_F = \frac{V_{dc}}{2R_A}\frac{L_A}{L_{Load}}$.

It is important to mention that the commutation analysis of Fig. 5 is based on the assumption that i_A does not decrease to zero in *Mode* (*a*). Then the pulse width of v_{ARWC} from t_2 - t_5 should equal to t_D (as shown in Fig. 2) to achieve the cancellation effect. It is possible that at the end of Mode (*a*), i_A decreases to zero, then commutation of [t_2, t_3] will not happen. In this situation, the pulse width of v_{ARWC} appearing from t_3 - t_5 should be equal to t_D.

The commutation stages for falling edge of v_{inv} are similar to those of rising edge, which are presented in Fig.7.

Mode (*c*) [t_6, t_7]: T_{A2} turns off at t_6, i_A flows through the body diode of T_{A2} and ARWC is still in freewheeling. v_{ARWC} is the voltage drop of the resistance in the loop which is close to zero. i_A follows (6).

Mode (*d*) [t_7, t_8]: T_5 turns off and T_{A4} turns on. When T_5 turns off, i_{Load} goes through the body diode of T_6 and the falling edge of v_{inv} appears. The ARWC needs to generate the positive voltage pulse. T_{A4} turns on, v_{ARWC} equals to the capacitor voltage V_{C2}.

$$\begin{cases} L_A\dfrac{di_A}{dt} - M\dfrac{di_{Load}}{dt} + R_A i_A = \dfrac{1}{4}V_{dc} \\ -M\dfrac{di_A}{dt} + (L_A + L_{Load})\dfrac{di_{Load}}{dt} + R_{Load} i_{Load} = 0 \end{cases} \tag{8}$$

Therefore,

$$i_A(t) \approx \left\{I_A(t_5) - \frac{\tau_A}{\tau_A - \tau_{Load}}\left[I_{Load}(t_5) - \frac{V_{dc}}{2R_{Load}}\right]\right\}e^{-\frac{t}{\tau_A}} + \frac{\tau_A}{\tau_A - \tau_{Load}}\left[I_{Load}(t_5) - \frac{V_{dc}}{2R_{Load}}\right]e^{-\frac{t}{\tau_{Load}}} \tag{6}$$

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$$i_A(t) \approx \frac{1}{4}\frac{V_{dc}}{L_A}(t - t_7) + I_A(t_7) \quad (9)$$

It should be noted that in this falling case, only in Mode (*d*) that the ARWC generates pulse voltage. Therefore, the voltage pulse v_{ARWC} from t_7 - t_8 should equal to t_D to achieve the cancellation effect. *Mode* (*d*) is similar to *Mode* (*b*).

Mode (*e*) [t_8 - t_{11}]. Both ARWC and motor drive are operated in freewheeling mode. During [t_8, t_9]: T_{A4} turns off. i_A flows through the body diode of T_{A2} and ARWC is in freewheeling. During [t_9, t_{10}]: T_6 turns on. i_{Load} goes through T_6 rather than the body diode. During [t_{10}, t_{11}]: T_{A2} turns on. i_A goes through T_{A2} rather than the body diode.

The commutation stages of Fig. 5 and Fig.7 are derived based on Fig. 4 where i_{Load} is positive. If i_{Load} becomes negative, the rising/falling edge will switch their commutation stages. For example, the rising edge will appear at t_1 when i_{Load} is negative. Therefore T_{A3} of ARWC should also turn off at t_1. For falling edge which will appear at t_9, if i_{Load} becomes negative, then T_{A4} should also turn on at the same time. The gate signals of ARWC are generated based on i_{Load} direction. The control signals of ARWC for 5-level ANPC is similar to that of 3-level ANPC where the voltage pulse generated by the ARWC should always be synchronized with the rising/falling edge of ANPC. The experimental verification of ARWC on a 3-L ANPC is demonstrated in next section.

The proposed ARWC can also be applied to MMC-based motor drives. Recently SiC based MMC motor drive has been reported in [13]. The MMC inverter has smaller voltage steps than the 2-L inverter, however, the voltage's rising/falling edge of each voltage step is still high due to fast SiC switching speed. Therefore, the reflected voltage happens in each rising/falling edge. The operation modes and control of ARWC for MMC-based motor drive is similar to that of the 3-L ANPC motor drive where the ARWC breaks each rising/falling edge into two steps to achieve the cancellation effect. The simulation verification of MMC based motor drive with proposed ARWC is shown in Fig. 8 where MMC consisting of four submodules in each upper arm and lower arm to generate 5-L voltage waveforms. Each submodule contains a half-bridge switching

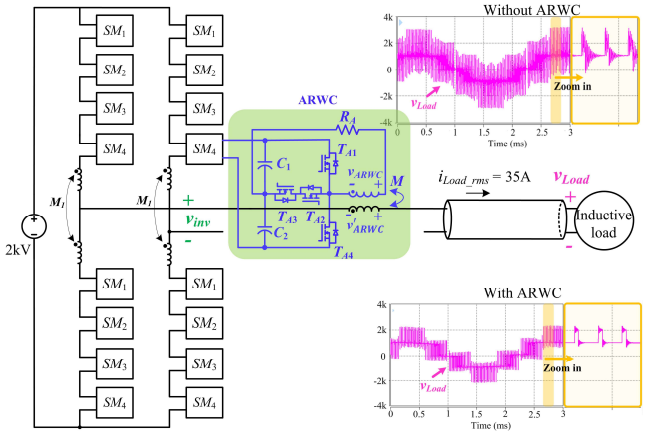

Fig. 8 Simulation results of a MMC based motor drive with proposed ARWC.

at 10 kHz. The DC voltage is 2 kV, the cable length is 100ft and output voltage frequency is 400 Hz. The load terminal voltage increases to 3 kV due to the reflected voltage. The load voltage can achieve 40% reduction with the proposed ARWC which is reduced from 3 kV (150%) to 2.2 kV (110%).

IV Experimental Verifications

A single-phase 3-L ANPC inverter is developed in the laboratory to verify the proposed ARWC since the operation principle of ARWC is the same for each phase. The key parameters of test setup with 3-L ANPC inverter, ac load and ARWC is listed in Table 1. The DC input voltage is 1600 V and the load current is 16 A (RMS). T_1 - T_4 are 3.3 kV SiC devices, GR40MT33N, from GeneSiC and T_5-T_6 is a 3.3 kV SiC module developed by GE Aviation. A 1.2 mH inductor is served as the load, which the impedance at high frequency range is much larger than the cable characteristic impedance, enabling full reflected wave phenomenon at load terminal. In order to evaluate the worst loss case of ARWC, only inductive load is adopted in the experiment. The cable length is 100 ft, which requires 150 ns transmission time for the voltage travelling from the inverter side to the load terminal. T_{A1} - T_{A4} in ARWC is implemented using a 1200V SiC T-type module from Wolfspeed. The characteristics of this T-type module and detailed gate driver design can refer to [14]. Since the commutation of T_1 - T_4 also generates rising/falling edge, resulting reflected wave phenomenon. The ARWC needs to generate voltage pulse during the commutation of T_1 - T_4 as well. Therefore, the switching frequency of T_{A1} - T_{A4} is 10.4 kHz in this experiment.

R_A and L_A are designed based on i_A. The analysis of Section III has illustrated that i_{load} will be coupled to i_A, R_A is therefore inserted in the ARWC circuit loop to help reduce i_A in the freewheeling mode. In addition, i_A also relates to L_A. R_A and L_A should be therefore designed together to achieve a low peak value of i_A.

Table 1 Key Parameters of Experimental testbed

Parameters	Specs
V_{dc}	1600 V
i_{Load}	16 A (RMS)
T_1-T_6	3.3 kV SiC MOSFET
f_0	400 Hz
f_{SW}	10 kHz
L_{Load}	1.2 mH
l_{cable}	100 ft
t_t	150 ns
L_A	15 µH
R_A	1 Ω
T_{A1}-T_{A4}	1200 V SiC T-type module
f_{SW_ARWC}	10.4 kHz
C_1/C_2	2.2 µF Film capacitor

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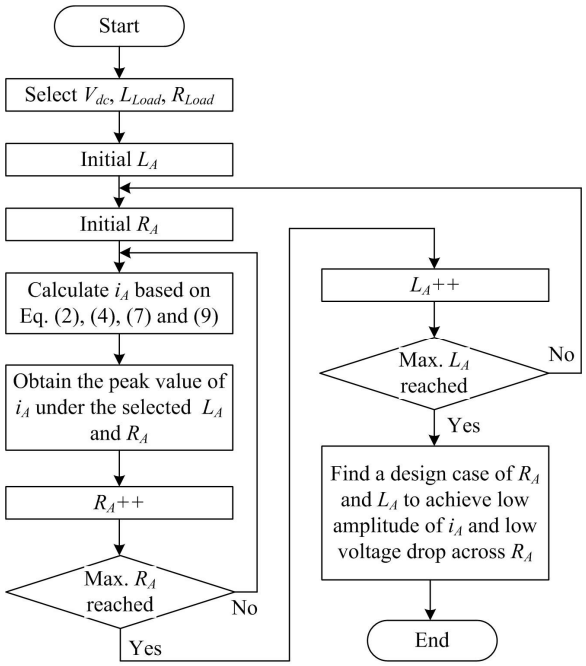

Fig. 9 Flowchart of R_A and L_A design

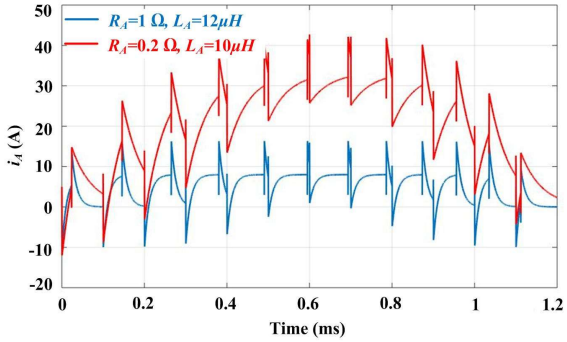

Fig. 10 The waveforms of i_A with different R_A and L_A.

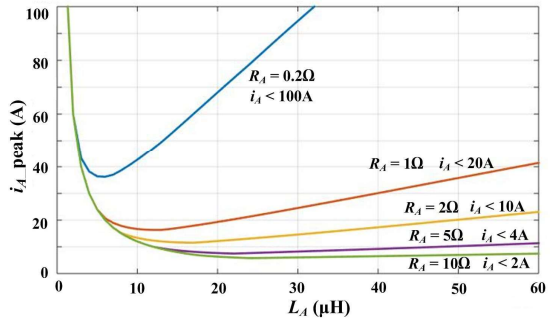

Fig. 11 Peak value of i_A with different R_A and L_A.

The flowchart to design R_A and L_A is presented in Fig. 9. With initial R_A and L_A, i_A can be derived based on (2), (4), (7) and (9). Since i_A does not decrease to zero at each switching cycle, the peak value of i_A should be derived in a fundamental period. A peak value can be obtained for the selected R_A and L_A design. As an example, Fig. 10 presents i_A waveforms with two different design cases of R_A and L_A. When R_A = 0.2 Ω and L_A = 10 μH, the peak value of i_A is 42 A. When R_A = 1 Ω and L_A = 12 μH, the peak value of i_A is 17 A. By sweeping R_A and L_A, the peak value of i_A can be derived for different R_A and L_A as shown in Fig. 11. A larger R_A can help reduce i_A during the freewheeling mode. For example, when R_A = 1Ω, L_A = 20 μH, the peak value of i_A is 20 A while the peak value of i_A is only 7 A when R_A = 10 Ω, L_A = 20 μH.

However, larger R_A also leads to a high voltage drop across the resistor (ΔV_{RA}), resulting in a lower v_{ARWC} than the designed value. For example, if R_A = 10 Ω, i_A = 10 A, the voltage drop across R_A is 100 V which will reduce v_{ARWC} to 300 V. This will cause the voltage level of the first step not matching that of the second step, degrading the cancellation performance as shown in Fig. 12. The blue curve shows the ideal waveforms while the red curve represents the waveforms considering ΔV_{RA}. Due to the reflected wave phenomenon, ΔV_{RA} will be doubled at the load terminal, causing overvoltage. Therefore, ΔV_{RA}, which should be as small as possible, is another consideration for R_A and L_A design. In this experiment, ΔV_{RA} is designed to be smaller than $5\% \times \frac{1}{4} V_{dc}$ which is 20 V.

After comparing different R_A and L_A cases, L_A is finally selected as 15 μH and R_A is 1 Ω since this combination can achieve small peak current and low ΔV_{RA} which are 17 A and 17 V respectively. With the designed L_A and R_A, the waveform of i_A is derived in Fig. 13.

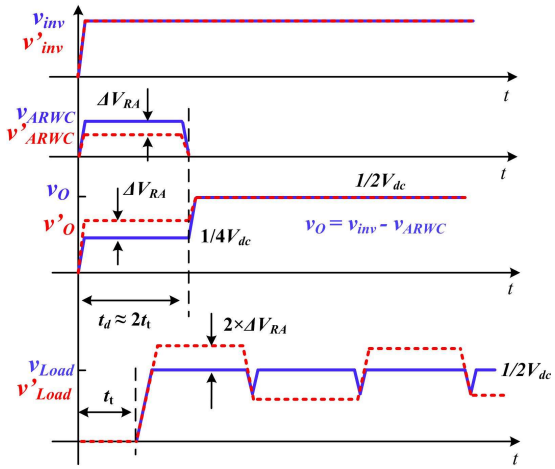

Fig. 12 The effect of voltage drop across R_A

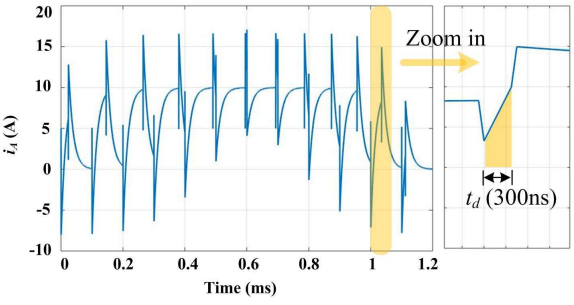

Fig. 13 Waveform of i_A with designed R_A and L_A.

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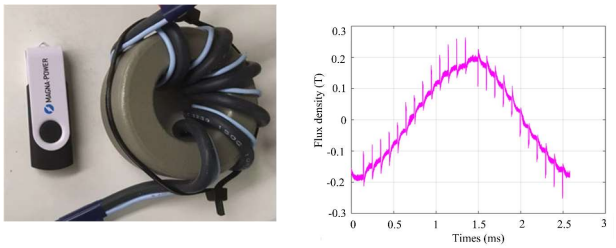
L_A is designed based on B_{max} which should be less than the saturation flux density B_{sat} of the core material and following (10).

$$B_{max} = \frac{L \cdot I_{peak}}{N \cdot A_e} < B_{sat} \tag{10}$$

The magnetic flux in L_A is induced by the sum of i_{Load} and i_A. Since i_A is small, i_{Load} has the main effect on the magnetic flux. The photo of the designed L_A is presented in Fig. 14 (a). The flux density is calculated based on i_{Load} and i_A as shown in Fig. 14(b). It should be noted that for the coupled inductor, the winding size of the inverter side is 10 AWG since it will carry i_{Load}, which is 16 A (RMS) in this experiment. The winding size of the ARWC side is 18 AWG since the current is only 2.7 A (RMS).

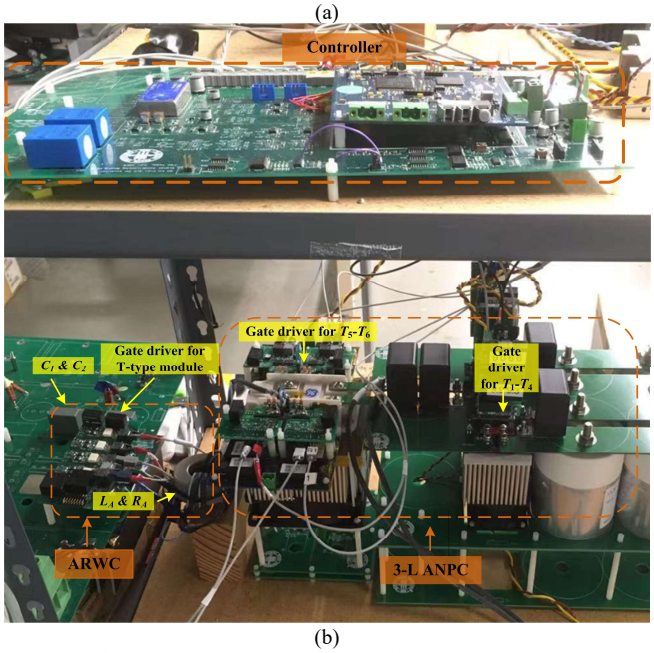


(a) (b)

Fig. 14. Designed L_A and its flux density: (a) the photo of designed L_A; (b) the flux density of L_A.

3.3kV SiC MOSFET (T_1) | 3.3kV SiC Module (T_5-T_6) | 1.2kV SiC T-type Module (T_{A1}-T_{A4})

(a)



(b)

Fig. 15 hardware prototype of 3-L ANPC with proposed ARWC: (a) photo of SiC devices; (b) experiment testbed.

The core loss is calculated with improved Generalized Steinmetz Equation (iGSE) based on i_{Load} and i_A as follows [15]:

$$P_{core} = k_i(\Delta B)^{\beta-\alpha}\left|\frac{dB}{dt}\right|^{\alpha} \tag{11}$$

where α and β are the Steinmetz Equation parameters. α is 1.38, β is 2.22 and k_i is 0.0103 for the core used in this design. Using open-source code for calculating the iGSE, provided in [16], the core loss is calculated as 2.04 W.

When ARWC generates voltage pulse such as in Mode (b) and Mode (d), i_A will charge/discharge C_1 and C_2. This voltage ripple will also result in degraded cancellation which is similar to the effect of ΔV_{RA}. Therefore, C_1 and C_2 are also designed to achieve a low voltage ripple which is smaller than 5% of $\frac{1}{4}V_{dc}$.

$$\Delta v = \frac{1}{C}\sum_{n=1}^{n=\frac{1}{2}fs/f0}\int_{(n-1)\cdot T_s}^{n\cdot T_s} i_A(t)dt < 5\% \times \frac{1}{4}V_{dc} \tag{12}$$

Based on (12), C_1 and C_2 are selected as 2.2 μF. It should be noted that the voltage of C_1 and C_2 are naturally balanced since the rising edge and falling edge in a fundamental period are symmetrical.

Fig. 15 presents the photo of hardware prototype built in the laboratory to verify the proposed ARWC. Fig.15 (a) shows the SiC devices used in the 3-L ANPC and the proposed ARWC. The experimental testbed is presented in Fig. 15(b). The single phase experiment results with and without the designed ARWC are presented in Fig. 16. Fig. 16(a) shows the ANPC output voltage (v_{inv}), load voltage (v_{Load}) and load current (i_{Load}) without ARWC. Each rising edge and falling edge of v_{inv} is half of V_{dc} which is 800 V. Due to the reflected wave phenomenon, the magnitude of v_{Load} at rising edge is 1625 V which has 103% overvoltage compared to the voltage level of each rising edge and falling edge. The magnitude of v_{Load} at falling edge is 1655 V which has 107% overvoltage. This overvoltage will increase the risk of winding insulation issue.

The experiment result with ARWC is presented in Fig. 16(b) which is able to achieve 77% reduction, suppressing the magnitude of v_{Load} at rising edge from 1625 V (103% overvoltage) to 1010 V (26% overvoltage) and suppressing the magnitude of v_{Load} at falling edge from 1655 V (103% overvoltage) to 1040 V (30% overvoltage).

The power loss of ARWC is 18 W at 8.7 kVA operation for single phase and 54 W for three phase. The power loss breakdown is analyzed by calculating the switching loss (7.8 W), conduction loss (0.38 W), inductor loss (2.6 W), and resistor loss (7.2 W) based on the experimental waveforms. It should be noted that the switches of the ARWC in the experiment utilizes 87 A current rating devices, which is much larger than the designed value. The conduction loss will increase when smaller current rating devices adopts. The total power loss is still an order of magnitude smaller than that of a passive filter. The power loss here is the worst case for pure inductive load, the power loss of ARWC for R-L load will be smaller.

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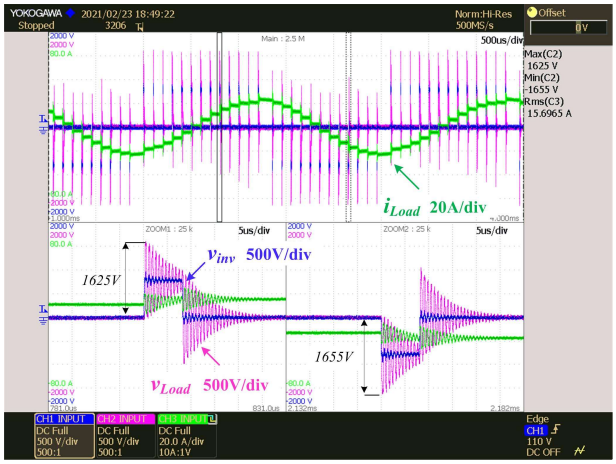
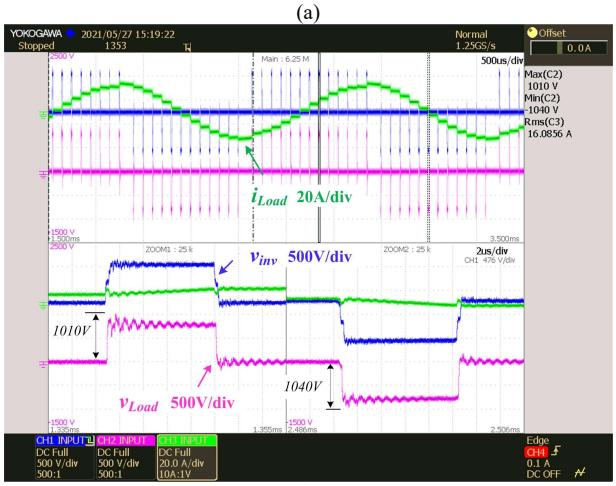


(a)



(b)

Fig. 16 Experimental results: (a) waveforms without ARWC; (b) waveforms with ARWC.

V. Conclusion

This paper has presented a low-voltage low-loss ARWC for MV SiC motor drive with a generalized multilevel inverter topology. With the coupled inductor, the output voltage of ARWC is isolated to the motor drive which allowing the ARWC can be applied to a generalized multilevel inverter, regardless of the level numbers. In addition, no extra DC power supply is needed for the ARWC.

The operation principle of ARWC has been analyzed on a SiC 3-L ANPC single phase inverter. A method for the parameters design to achieve low current rating and good cancellation performance has also been proposed. The experimental results have been provided to demonstrate the validation of the proposed method. The proposed ARWC can achieve 77% reduction in 3-L ANPC application under 1600 V DC voltage 100 ft cable length condition. The power loss is calculated as 18 W based on the experimental waveforms at 8.7 kVA with inducive load for single phase.

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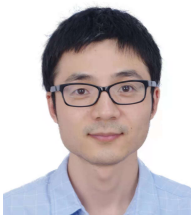

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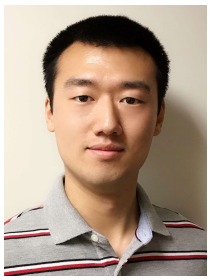

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