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Transformer-less Boost Converter with Reduced Voltage Stress for High Voltage Step-Up Applications

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***Abstract*—In this paper, a new Transformer-less Boost Converter (TBC) is proposed to achieve high step-up voltage with a reduced voltage across switches. The proposed topology has the advantage of providing a high voltage gain, the low voltage stress on the active switches, simplified control, and high efficiency. The structure is derived by modifying the classical Switched Inductor Boost Converter (SIBC) by replacing two of the diodes with a capacitor and a control switch, which results in a total output voltage equally shared by the two switches. Thus, the proposed converter needs a lesser number of diodes than the conventional SIBC, where the two active switches equally share the total output voltage and thereby reducing the voltage stress across the switches to half. Hence, low voltage rating switches can be used to design the proposed TBC structure. Also, a higher voltage gain is achieved using TBC without increasing the number of components of the existing SIBC. Furthermore, the proposed converter provides the common ground connection of source and load. The detailed analysis, effect of non-idealities, design, and comparison are presented. The experimental results of the proposed TBC are presented to validate its functionality and theoretical analysis.**

***Index Terms*— Boost Converter, DC-DC converter, Reduced voltage stress, Transformer-less, Voltage Step-up.**

I. Introduction

In today's world, the problems of climate change and global warming due to the largely increasing greenhouse gas emissions, have become a critical issue. Renewable energy generation sources like photovoltaic (PV), wind turbines, and fuel cells have emerged as favourable solutions. The output voltages of these renewable energy sources are low; therefore, high voltage gain converters are needed to attain suitable high voltage level for different applications such as high-intensity discharge lamps for automobiles, microgrid, hybrid vehicles, power supplies, and telecom power system [1]-[2].

Theoretically, a conventional boost converter may achieve an infinite voltage gain when the duty cycle value is equal to 1. However, the high duty cycle results in high conduction loss in the active switch and diode reverse recovery loss [3]-[4]. Also, the switch voltage stress is high i.e. equal to the output voltage. Isolated converters such as forward, flyback, half-bridge, full-bridge, and push-pull types, can provide a high voltage gain by increasing the transformers turns ratio [5]-[6]. However, there are some challenging problems such as leakage inductance and the parasitic capacitance developed by the secondary winding of the transformer, high voltage and current spikes, and high voltage stress of the switching devices, which increase switching losses due to high power dissipation and noise that will further degrade the system performance [7]-[8]. Coupled inductors in DC-DC converters can also be used to achieve a high voltage gain by properly adjusting the turns ratio of the coupled inductor [9]-[10], and its control is comparatively easier. However, the use of coupled inductors causes voltage spikes across the power switches. Moreover, the leakage inductance losses decrease the converter efficiency. Therefore, extra snubber circuits are required, resulting in a more complex circuitry [10]-[13]. Cascaded and quadratic boost converters can also be used to achieve high voltage gain, where two or more boost converters are cascaded [14]-[17]. However, the cascading of boost converters increases the number of stages and a large space is needed on the board to accommodate a large number of switches and gate driver circuits, and hence decreasing power density. Moreover, the voltage gain is highly non-linear with the duty cycle and the required voltage and current rating of the components and devices increases as the number of stages increases. The voltage gain can also be improved with the use of the switched inductor/capacitor technology. Different switched-inductor and switched capacitor topologies have been discussed in [17]-[19], where a built-in high voltage gain is attained by adjusting the series and parallel connections of the switched inductor. In the case of the classical Switched Inductor Boost Converter (SIBC), the voltage gain is limited and the voltage stress of the switch is high i.e. equal to output voltage [19]. In [20]-[25], power circuitries based on active switched inductors are proposed by using multiple switches. Nevertheless, these circuitries are only suitable for floating loads and required additional voltage lift networks and complex control. A high voltage gain can also be achieved with the use of some other converter topologies such as using multiple switched inductor/capacitor cells, voltage multiplier-cells based boost converter, and interleaved multilevel boost converter [26]-[28]. The voltage gain can be increased by using multiple stages but the number of circuit components increases, which results in complex power and control circuits. Moreover, the cost of the circuit is high and efficiency decreases as the number of stages increase to achieve higher voltage.

In this paper, a new Transformer-less Boost Converter is proposed to achieve high step-up voltage with a reduced voltage across switches. The proposed topology has the advantage of providing a high voltage gain, low voltage stress on the active switches, simplified control, and high efficiency. The structure is derived by modifying the classical SIBC by replacing two of the diodes with a capacitor and a control switch, which results in a total output voltage equally shared by the two switches. Thus, the proposed converter needs a lesser number of diodes than the conventional SIBC, where the two active switches equally share the total output voltage and thereby reducing the voltage stress across

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the switches to half. Hence, low voltage rating switches can be used to design the proposed TBC structure. Also, a higher voltage gain is achieved using TBC without increasing the number of components of the existing SIBC. Furthermore, the proposed converter provides the common ground connection of source and load. The paper is organized as follows: the proposed TBC circuitry, operation, characteristic waveforms, and voltage gain analysis are given in Section II. The non-idealistic model and effect of parasitic resistances are given in Section III. A Comparison of converters is presented in IV. The design of the proposed TBC is given in Section V. The experimental investigations of TBC are presented in Section VI, and the conclusion is given in section VII.

II. Proposed Transformer-less Boost Converter (TBC)

A higher voltage conversion ratio than the conventional boost converter can be obtained by using the classical SIBC [18], in which additional switched inductor circuitry is incorporated. However, the voltage stress across the switches is significantly increased with a voltage gain, which in turn leads to developing the total output voltage across the switch. In transformer-less active switched inductor converter [19], two switches are employed and the voltage stress across switches is reduced. However, the converter is suitable only for floating loads. To overcome these drawbacks Transformer-less Boost Converter (TBC) is proposed and the circuitry is shown in Fig. 1. In proposed TBC, voltage stress across the switches is reduced and higher voltage gain is achieved. The circuitry is derived by modifying the power circuitry of the classical SIBC without increasing the number of components. The circuitry of proposed TBC comprises of two control switches S_a and S_b, two diodes D_a and D_b, two inductors L_a and L_b with equal inductance rating (L), two capacitors C_a and C_b, and load R. The intermediate diodes of the classical SIBC are replaced by capacitor and control switch. The proposed TBC follows the principle of parallel charging of reactive components and series discharging of reactive components. Therefore, in ON state, two inductors and a capacitor are charged in parallel; and in OFF state, discharged in series to charge the load side capacitor and to provide energy to load.

In proposed TBC, the total output voltage is equally shared by the two active switches and hence reducing the voltage stress across the switches to half. Therefore, the power circuitry of the proposed TBC can be designed by using switches with a low voltage rating. It is important to note that the total number of components in TBC is the same as the classical SIBC converter and a higher voltage gain is achieved. For the proposed circuit,

$$L = L_a = L_b \tag{1}$$

To study Continuous Conduction Mode (CCM) and

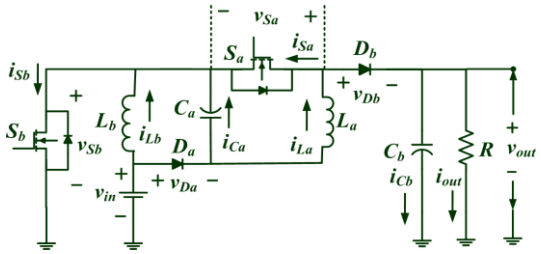

Fig. 1. The Power circuit of the proposed Transformer-less Boost Converter (TBC).

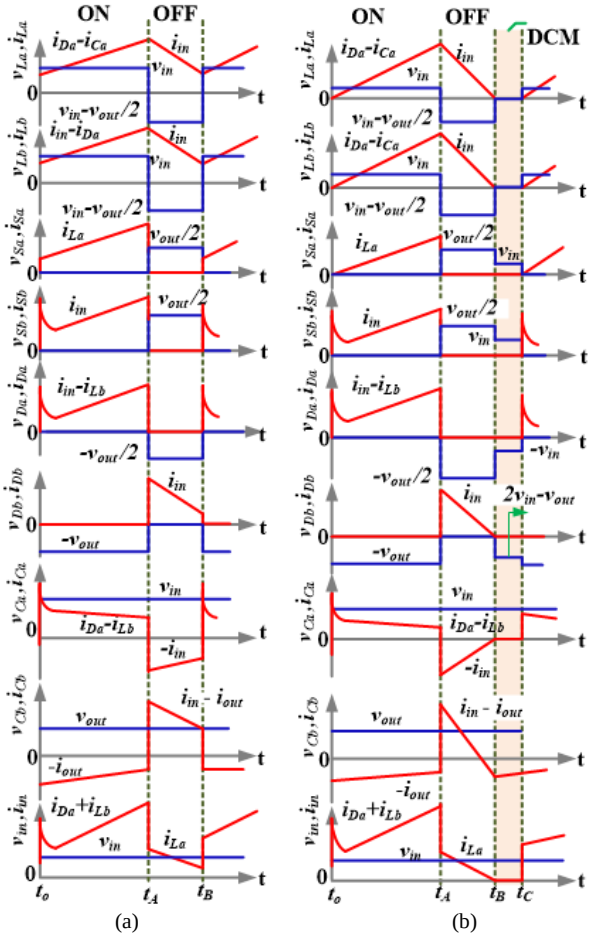

Fig. 2. Characteristics waveform of proposed TBC (a) CCM, (b) DCM.

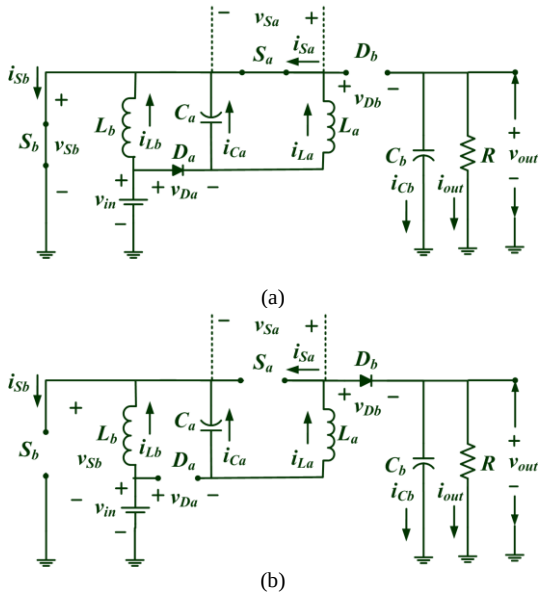

Fig. 3. Equivalent power circuitry, (a) Mode I (t_o-t_A), (b) Mode II (t_A-t_B).

Discontinuous Conduction Mode (DCM) characteristics, all the circuit components are considered to be ideal by neglecting the voltage drop across semiconductor devices or inductors due to internal resistance and having a capacitor that is too large to produce a constant voltage. Fig. 2(a)-(b) shows the typical TBC characteristics waveforms for CCM and DCM modes, respectively; where time t_o to t_A is the time period for mode I (i.e. ON time).

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A. Continuous Conduction Mode (CCM)

The CCM operation of the proposed TBC is split into two modes; first when both the switches S_a and S_b are in ON state and second when both the switches S_a and S_b are in OFF state.

1) Mode I (Time t_o-t_A)

Fig. 3(a) shows the equivalent circuit of TBC for mode I. In this mode, inductor L_b is charged by input supply (V_{in}) through switch S_b, inductor L_a is charged by input supply (V_{in}) through diode D_a and switches S_a and S_b, capacitor C_a is charged by input supply (V_{in}) through diodes D_a and switch S_b. It is worth to mention that the inductors L_a and L_b, and capacitor C_a are charged in parallel and the capacitor C_b is discharged through the load R. During this mode, diodes D_a and D_b are forward and reversed biased, respectively. The voltages across and currents through inductors and capacitors can be expressed as,

$$v_L^{\,I} = v_{La}^{\,I} = v_{Lb}^{\,I} \approx V_{in},\ V_{Cb}^{\,I} \approx V_{out} \tag{2}$$

$$i_{in}^{\,I} = i_{La}^{\,I} + i_{Lb}^{\,I} + i_{Ca}^{\,I},\ i_{Cb}^{\,I} = -i_{out} \approx -\frac{V_{out}}{R} \tag{3}$$

Where superscript represents the mode I and subscript represent the component.

2) Mode II (Time t_A-t_B)

Fig. 3(b) shows the equivalent circuit of TBC for mode II. In this mode, both the inductors L_a, L_b, and the capacitor C_a are discharged in series with the input voltage V_{in}; energy is supplied to the load R and capacitor C_b through the diode D_b. In this mode, diodes D_a and D_b are reversed and forward biased, respectively. The voltages across and currents through inductors and capacitors can be expressed as,

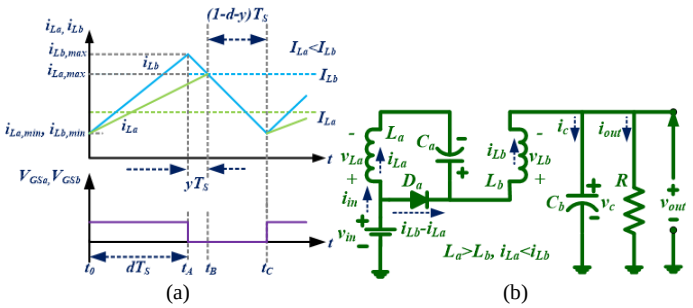
$$v_L^{\,II} = v_{La}^{\,II} = v_{Lb}^{\,II} \approx V_{in} - \frac{V_{out}}{2},\ V_{Cb}^{\,II} \approx V_{out} \tag{4}$$

$$i_L^{\,II} = i_{La}^{\,II} = i_{Lb}^{\,II} = i_{in}^{\,II}, i_{Cb}^{\,II} \approx i_L^{\,II} - \frac{V_{out}}{R} \tag{5}$$

Where superscript represents the mode II and subscript represents the component. Using inductor volt second balance principle, the voltage gain of TBC is expressed as,

$$V_G\big|_{CCM} = \frac{V_{out}}{V_{in}} = \frac{2}{1-d} \tag{6}$$

Where the voltage gain and duty cycle is represented by V_G, and d, respectively. Equation (6) validates that the voltage gain of TBC is higher than the classical SIBC and transformer-less active switched inductor converter.



(a) (b)

Fig. 4. When $L_a > L_b$ (a) inductor currents, and (b) Mode II.

B. CCM: When the value of L_a is larger than the value of L_b

The operation of the proposed converter depends on the values of the inductors L_a and L_b. Hence, the currents through inductors L_a and L_b depend on the values of L_a and L_b. The characteristics waveform of the inductor L_a and L_b currents are shown in Fig. 4(a) below. In this case, the converter operates in three modes as follows,

1) Mode I (time t_0 to t_A)

In this mode, switches S_a and S_b are turned ON and equivalent circuitry is the same as mode I of CCM. The input current i_{in} is the sum of inductor currents and the current through the capacitor C_a i.e. $i_{in}=i_{La}+i_{Lb}+i_{Ca}$. The slope of the inductor L_a and L_b currents can be obtained as follows,

$$\frac{d\ i_{La}}{dt} \approx \frac{v_{in}}{La}, \frac{d\ i_{Lb}}{dt} \approx \frac{v_{in}}{Lb} \tag{7}$$

In this mode, the current through inductor L_b is larger than the current through inductor L_a since L_b<L_a.

2) Mode II (time t_A to t_B)

This mode occurs for a small-time duration (yT_s as shown in Fig. 4(a)) when switches S_a and S_b are just turned OFF. The equivalent circuitry is shown in Fig. 4(b), where diode D_a is forward biased. During this mode, the current through inductor L_a increases with a positive slope and the current through inductor L_b decreases with a large negative slope. The value of current through inductor L_b is larger than the current through inductor L_a. Also, the input current i_{in} is equal to inductor L_b current i.e. $i_{in}=i_{Lb}$ and the resultant current through diode D_a is the subtraction of inductors L_b and L_a currents i.e. i_{Lb}-i_{La}. The slope of the inductors L_a and L_b currents are obtained as follows,

$$\frac{d\ i_{La}}{dt} \approx \frac{v_{Ca}}{La} \approx \frac{v_{in}}{La}, \frac{d\ i_{Lb}}{dt} \approx \frac{v_{in}-v_{out}}{Lb} \tag{8}$$

This mode ends as soon as the currents through inductor L_a and L_b are equal, and circuitry operates in mode III.

3) Mode III (time t_B to t_C)

In this mode, switches S_a and S_b are turned OFF and equivalent circuitry is the same as CCM mode II. In this case, input current and the current through inductor L_b and L_a are equal i.e. $i_{in}=i_{La}=i_{Lb}$. The voltage across inductor L_a and L_b can be obtained as follows,

$$\frac{d\ i_{La}}{dt} = \frac{2v_{in}-v_{out}}{L_a+L_b}, \frac{d\ i_{Lb}}{dt} = \frac{2v_{in}-v_{out}}{L_a+L_b} \tag{9}$$

Using small approximation and inductor volt second balance,

$$For\ La \Rightarrow v_{in}(d) + v_{in}(y) + \frac{2v_{in}-v_{out}}{La+Lb} La(1-d-y) = 0 \tag{10}$$

$$For\ L_b \Rightarrow v_{in}(d) + v_{in} - v_{out}\ \ y + \frac{2v_{in}-v_{out}}{L_a+L_b} Lb(1-d-y) = 0 \tag{11}$$

Solving (10)-(11), the voltage gain of TBC is obtained as,

$$v_{out}/v_{in}\big|_{L_a>Lb} = 2/\ 1\text{–}d \tag{12}$$

Similarly, one can easily understand the modes of the converter when inductance L_a is smaller than the value of inductance L_b and the voltage gain can be obtained as,

$$v_{out}/v_{in}\big|_{L_a<Lb} = 2/\ 1\text{–}d \tag{13}$$

Therefore, in the case of unequal inductances, the inductor average current is changed. However, voltage gain is still the same i.e. 2/(*1-d*).

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C. Discontinuous Conduction Mode

The DCM operation of the proposed TBC is split into three modes; first when switches S_a and S_b are in ON state, second when switches S_a and S_b are in OFF state with non-zero inductor currents, and third when switches S_a and S_b are in OFF state with zero inductor currents. Let's consider that, at time t_B the inductor current reaches to zero value as indicated in Fig. 2(b). In a particular DCM characteristics (Fig. 2(b)), d_1T is mode I time period (i.e. time t_o-t_A), d_2T (i.e. time t_A-t_B) is mode II time period, and d_3T (i.e. time t_B-t_C) is mode III time period.

1) Mode I (Time t_o-t_A)

The working of TBC and its equivalent circuit in this mode is the same as mode I of CCM. Consequently, during this mode, inductors L_a and L_b and the capacitor C_a are charged in parallel by the input voltage V_{in}. At the beginning of this mode (at the time t_o or t_o+T), the current through both the inductors L_a and L_b started from level zero and reached to the level of maximum current in the end. The maximum current through inductors L_a and L_b, and the capacitor C_a can be expressed as,

$$I_{L,\max}^{\ I} = I_{La,\max}^{\ I} = I_{Lb,\max}^{\ I} = \frac{1}{L}\ V_{in}d_1T \tag{14}$$

The maximum currents through the inductors L_a and L_b in mode I are $I_{La,max}^{\ I}$ and $I_{Lb,max}^{\ I}$, respectively, where superscript denotes the mode I. The current ripples through the inductors L_a and L_b can be expressed as,

$$\Delta I_L = \Delta I_{La} = \Delta I_{Lb} = \frac{1}{L}\ V_i d_1 T \tag{15}$$

Where, the current ripples through the inductors L_a and L_b are ΔI_{La} and ΔI_{Lb}, respectively.

2) Mode II (Time t_A-t_B)

During this mode, the working of TBC and its equivalent circuit is the same as mode II of CCM. Consequently, during this mode, inductors L_a and L_b, and the capacitor C_a are discharged in series with input voltage V_{in} to provide energy to capacitor C_b and load R. In the beginning of this mode (at time t_A or t_A+T), the current through both the inductors L_a and L_b started from the level of maximum current and reached to level zero in the end (at time t_B or t_B+T). Another expression for maximum current through inductors L_a and L_b can be obtained as,

$$I_{L,\max}^{\ II} = I_{La,\max}^{\ II} = I_{Lb,\max}^{\ II} = \frac{V_{out}d_2T}{2L} - \frac{V_{in}d_2T}{L} \tag{16}$$

The maximum currents through the inductors L_a and L_b in mode II are $I_{La,max}^{\ II}$ and $I_{Lb,max}^{\ II}$, respectively, where superscript denotes the mode II. The current ripples through the inductors L_a and L_b can be expressed as,

$$\Delta I_L = \Delta I_{La} = \Delta I_{Lb} = \frac{V_{out}d_2T}{2L} - \frac{V_{in}d_2T}{L} \tag{17}$$

3) Mode III (Time t_B-t_C)

Fig. 5 shows the equivalent circuit for this mode. During this mode, switches S_a and S_b are turned ON, and currents through inductors L_a and L_b and capacitor C_a are zero. Consequently, the energies in the inductors L_a and L_b are zero. Throughout this mode, both the diodes D_a and D_b are reversed biased and capacitor C_b is discharged through load R. The time period of mode II i.e. d_2T i.e. time t_A-t_B can be expressed as follows by using the equations (8) and (10),

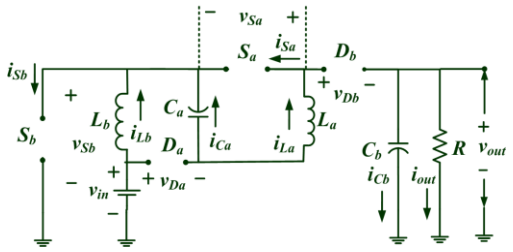

Fig. 5. DCM Equivalent power circuitry (t_B-t_C).

$$d_2T = 2d_1 \times \frac{V_{in}T}{V_{out}-2V_{in}} \Rightarrow d_2 = 2d_1 \times \frac{V_{in}}{V_{out}-2V_{in}} \tag{18}$$

It is well known that,

$$d_1 + d_2 + d_3 = 1 \tag{19}$$

The time period for mode III can be expressed as follows by using (11) and (12),

$$d_3T = T\left(1-\frac{V_{out}d_1}{V_{out}-2V_{in}}\right) = \frac{T\left[V_{out}\ 1-d_1\ -2V_{in}\right]}{V_{out}-2V_{in}} \tag{20}$$

With the use of geometry in Fig. 2(b) on the current waveform of the capacitor C_b, the average current through capacitor C_b can be expressed as,

$$I_{Cb} = \frac{I_{L,\max}\times d_2}{2} - I_{out} = \frac{I_{L,\max}\times d_2}{2} - \frac{V_{out}}{R} \tag{21}$$

Using equations (14), (20), and (21),

$$I_{Cb} = \frac{{V_{in}}^2{d_1}^2T}{L\ V_{out}-2V_{in}} - \frac{V_{out}}{R} \tag{22}$$

Since any capacitor average current is always zero under steady-state condition, equation (22) can now be expressed as,

$$\frac{{V_{in}}^2{d_1}^2T}{L\ V_{out}-2V_{in}} = \frac{V_{out}}{R} \tag{23}$$

Using (23),

$$\left(\frac{V_{out}}{V_{in}}\right)^2 - \frac{2V_{out}}{V_{in}} - \frac{{d_1}^2}{\delta_L} = 0 \tag{24}$$

The normalized time constant for inductors L_a and L_b is δ_L, which is equal to L/TR. Therefore, δ_L varies with the variation in the values of L, T, and R. The voltage gain of TBC in DCM ($V_G|_{DCM}$) can be obtained as,

$$V_G|_{DCM} = \frac{V_{out}}{V_{in}} = 1+\left(\frac{\delta_L+{d_1}^2}{\delta_L}\right)^{1/2} = 1+\left(1+\frac{{d_1}^2R}{Lf}\right)^{1/2} \tag{25}$$

Where f is the switching frequency. If the proposed TBC is working at the boundary of CCM and DCM, the voltage gain of CCM and DCM operations will be the same. Hence, by using equations (6) and (25),

$$1+\left(1+\frac{{d_1}^2R}{Lf_s}\right)^{1/2} = \frac{2}{1-d} \tag{26}$$

The mode I for CCM and DCM is the same i.e. d=d_1. Hence, the normalized boundary time constant ($\delta_{L\text{-}B}$) for inductors L_a and L_b

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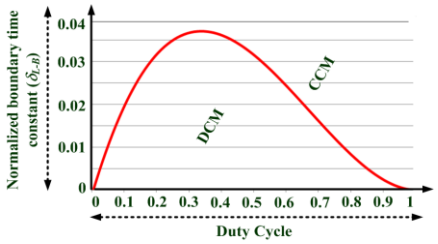

Fig. 6. Normalized boundary time constant versus duty cycle.

can be obtained as,

$$\delta_{L-B} = \frac{d\ 1+d^2-2d}{4} \tag{27}$$

The plot of $\delta_{L\text{-}B}$ versus d is shown in Fig. 6 with DCM and CCM boundary regions. The proposed TBC operates in DCM at a value of $\delta_{L\text{-}B}$ larger than δ_L.

III. Investigation of Non-idealities in TBC

The effects of non-idealities of different components and devices on the output voltage are studied by taking into account the non-idealities in the power circuit as depicted in Fig. 7. The resistances r_L are the Equivalent Series Resistance (ESR) of inductors L_a and L_b. The resistances r_S are the ON-state resistances of switches S_a and S_b. The resistances r_d and voltage V_{fd} are the forward resistance and threshold voltage of diodes D_a and D_b. The ESR of the capacitors C_a and C_b are shown by resistance r_c.

A. Effect of Inductors

The anomaly caused by non-idealities of switches S_a and S_b, diodes D_a and D_b, capacitor C_a and C_b are ignored (i.e. r_S, r_d, r_c, and V_{fd} are neglected) to study the effect of ESR of inductors L_a and L_b. With this consideration, the voltages across inductors L_a and L_b in mode I and II are expressed as follows,

$$v_{La}^{\ I} \approx V_{in} - I_{La}r_L, v_{Lb}^{\ I} \approx V_{in} - I_{Lb}r_L \tag{28}$$

$$v_{La}^{\ II} \approx V_{in} - I_{La}r_L - \frac{V_{out}}{2}, v_{Lb}^{\ II} \approx V_{in} - I_{Lb}r_L - \frac{V_{out}}{2} \tag{29}$$

By using (28) and (29),

$$v_{La}^{\ I} + v_{Lb}^{\ I} \approx 2V_{in} - I_{La}r_L - I_{Lb}r_L \tag{30}$$

$$v_{La}^{\ II} + v_{Lb}^{\ II} \approx 2V_{in} - I_{La}r_L - I_{Lb}r_L - V_{out} \tag{31}$$

Now applying small approximation and the principle of inductor volt-sec balance,

$$2V_{in} - I_{La}r_L - I_{Lb}r_L\ \ d = -\ 2V_{in} - I_{La}r_L - I_{Lb}r_L - V_{out}\ \ (1-d) \tag{32}$$

The voltage gain of TBC configuration with consideration of the effect of ESR of inductors L_a and L_b can be obtained as,

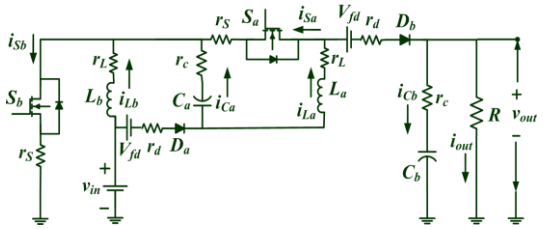

Fig. 7. The power circuit of TBC with non-idealities.

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_L} = \frac{2-\frac{r_L}{V_{in}}\ I_{La}+I_{Lb}}{1-d} \tag{33}$$

It is assumed that V_{dL} is the voltage drop across each inductor due to ESR (i.e. $I_{La}r_L$ and $I_{Lb}r_L$ are equal to V_{dL}). Then, (33) is written as follows,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_L} = \frac{2\left(1-\frac{V_{dL}}{V_{in}}\right)}{1-d} = \frac{2}{1-d} - \frac{2\ V_{dL}}{V_{in}\ 1-d} \tag{34}$$

From (33)-(34), it is clear that the voltage gain decreases significantly for greater values of V_{dL} and d, which signifies that the inductors ESR (r_L) and duty cycle (d) should not have a large value.

B. Effect of Switches

The anomaly caused by non-idealities of inductors L_a and L_b, diodes D_a and D_b, capacitor C_a and C_b are ignored (i.e. r_L, r_d, r_c, and V_{fd} are neglected) to study the effect of ON-state resistances of switches. With this consideration, the voltages across inductors L_a and L_b in mode I and II are expressed as follows,

$$v_{La}^{\ I} \approx V_{in} - \ I_{Sa} + I_{Sb}\ \ r_S, v_{Lb}^{\ I} \approx V_{in} - I_{Sb}r_S \tag{35}$$

$$v_{La}^{\ II} \approx V_{in} - \frac{V_{out}}{2}, v_{Lb}^{\ II} \approx V_{in} - \frac{V_{out}}{2} \tag{36}$$

By using (35) and (36),

$$v_{La}^{\ I} + v_{Lb}^{\ I} \approx 2V_{in} - \ I_{Sa} + 2I_{Sb}\ \ r_S \tag{37}$$

$$v_{La}^{\ II} + v_{Lb}^{\ II} \approx 2V_{in} - V_{out} \tag{38}$$

Now applying small approximation and the principle of inductor volt-sec balance,

$$2V_{in} - \ I_{Sa} + 2I_{Sb}\ \ r_S\ \ d = -\ \ 2V_{in} - V_{out}\ \ \ 1-d \tag{39}$$

The voltage gain of TBC configuration with consideration of the effect of ON-state resistance of switches S_a and S_b can be obtained as,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_S} = \frac{2-\frac{r_S}{V_{in}}\ \ I_{Sa}+2I_{Sb}\ \ d}{1-d} \tag{40}$$

It is assumed that V_{ds} is the voltage drops due to ON-state resistance of switches S_a and S_b (i.e. $I_{Sa}r_S$ and $I_{Sb}r_S$ are equal to V_{dS}). Therefore, (40) is now expressed as follows,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_S} = \frac{2-\frac{3V_{dS}}{V_{in}}d}{1-d} = \frac{2}{1-d} - \frac{3V_{dS}d}{V_{in}\ 1-d} \tag{41}$$

From (40)-(41), it is clear that the voltage gain decreases significantly for greater values of V_{dS}/V_{in} and d, which signifies that the ON-state resistance of switches should not have a large value.

C. Effects of diodes

The anomaly caused by parasitic of inductor L_a and L_b, capacitor C_a and C_b, and switches S_a and S_b are ignored (i.e. r_L, r_C, and r_S are neglected) to study the effect of diodes D_a and D_b. With this consideration, the voltages across inductors L_a and L_b in mode I and

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II are expressed as follows,

$$v_{La}^{I} \approx V_{in} - I_{Da} r_d - V_{fd}, v_{Lb}^{I} \approx V_{in} \tag{42}$$

$$v_{La}^{II} \approx v_{Lb}^{II} \approx V_{in} - \frac{I_{Db} r_d + V_{fd} + V_{out}}{2} \tag{43}$$

By using (42) and (43),

$$v_{La}^{I} + v_{Lb}^{I} \approx 2V_{in} - I_{Da} r_d - V_{fd} \tag{44}$$

$$v_{La}^{II} + v_{Lb}^{II} \approx 2V_{in} - I_{Db} r_d - V_{fd} - V_{out} \tag{45}$$

Now applying small approximation and the principle of inductor volt-sec balance,

$$2V_{in} - I_{Da} r_d - V_{fd} \quad d = - \quad 2V_{in} - I_{Db} r_d - V_{fd} - V_{out} \quad 1-d \tag{46}$$

The voltage gain of TBC configuration with consideration of the effect of diodes D_a and D_b can be obtained as,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_d,\, V_{fd}} = \frac{2 - \frac{V_{fd}}{V_{in}} - d\frac{r_d}{V_{in}} I_{Da} - (1-d)\frac{r_d}{V_{in}} I_{Db}}{1-d} \tag{47}$$

It is assumed V_d is the voltage drop due to forward resistance diodes (i.e. $I_{Da}r_d$ and $I_{Db}r_d$ are equal to V_d). Therefore, equation (47) is now expressed as follows,

$$\left.\frac{V_{out}}{V_{in}}\right|_{r_d,\, V_{fd}} = \frac{2 - \frac{1}{V_{in}} V_{fd} + V_d}{1-d} = \frac{2}{1-d} - \frac{V_{fd} + V_d}{V_{in}\ 1-d} \tag{48}$$

From (47)-(48), it is clear that the voltage gain decreases significantly for greater values of V_d and d, which signifies that the forward resistance and the threshold voltage of diodes should not have a large value.

D. Effects of Intermediate Capacitor C_a

In ON mode, capacitor C_a is charged by input voltage source V_{in}. Let's assume the voltage drop across resistance r_C is Vr_C. In the OFF state, the capacitor C_a voltage should be dropped down by ΔV_{Ca} since it is discharged by the current i_{La}. Therefore,

$$v_{Ca} = V_{in} - Vr_C - \Delta V_{Ca} \approx V_{in} - \frac{t}{C_a} i_{La} \tag{49}$$

At the end of OFF mode, the voltage across the capacitor C_a is obtained as follows,

$$v_{Ca} = V_{in} - \frac{1}{C_a} \int_{dT}^{T} i_{La}\, dt = V_{in} - \frac{1-d}{C_a} T i_{La} \tag{50}$$

During OFF mode, the expression for current i_{La} can be expressed as,

$$i_{La} = I_{out} + i_{Cb} = \frac{I_{out}}{1-d} \tag{51}$$

By using (50) and (51),

$$v_{Ca} = V_{in} - \frac{1-d}{C_a} T \frac{I_{out}}{1-d} = V_{in} - \frac{V_{out}}{fRC_a} \tag{52}$$

It is well known that the inductor currents are increasing and decreasing in ON and OFF mode, respectively. By comparing ON and OFF mode ripples,

$$\frac{dT}{L_a} V_{in} = \frac{1-d\ T}{L_a} \quad V_{out} - V_{in} - v_{Ca} \tag{53}$$

By considering (49), the equation (53) is re-written as,

$$\frac{dT}{L_a} V_{in} = \frac{1-d\ T}{L_a} \quad V_{out} - 2V_{in} + \Delta V_{Ca} \tag{54}$$

Using (52) - (54), the voltage gain is obtained as,

$$\left.V_{out}\right|_{C_1} = \frac{2V_{in}}{1-d\ \left(1 + \frac{t}{1-d\ \ RC_a}\right)} \tag{55}$$

Using (55), it is clear that the standard output voltage in mode II instant is

$$V_{out} = \frac{2V_{in}}{1-d} \tag{56}$$

Further, the output voltage is dropped and at the end of mode II,

$$\left.V_{out}\right|_{C_a} = \frac{2V_{in}}{1-d\ \left(1 + \frac{1}{fRC_a}\right)} = \frac{2V_{in}}{1-d\ \left(\frac{fRC_a + 1}{fRC_a}\right)} \tag{57}$$

Thus, the voltage gain and output voltage drop can be unsurprising if the value of fRC_a >>1 as,

$$\left.\Delta V_{out}\right|_{C_1} = \frac{2V_{in}}{1-d\ \ fRC_a} = \frac{V_{out}}{fRC_a} \tag{58}$$

Using (57), the voltage gain can be estimated as,

$$\left.\frac{V_{out}}{V_{in}}\right|_{C_a} = \frac{2}{1-d\ \left(1 + \frac{1}{fRC_a}\right)} \tag{59}$$

This gives the proper selection of the value of the load, switching frequency, and capacitance C_a.

E. Effects of Load Side Capacitor C_b

Let's assume Vr_C is the voltage drop across resistance r_C. In Mode I, the capacitor C_b is discharged through load R. Hence, the output voltage which is the voltage across capacitor C_b is decreased and the instantaneous output voltage can be formulated as,

$$v_{Cb} = V_{out} - Vr_C - \frac{t}{C_b} I_{out} \approx V_{out}\left(1 - \frac{t}{RC_b}\right) \tag{60}$$

At the end of the mode I, the final change in output voltage (Δv_{out}) can be expressed as,

$$\left.\Delta v_{out}\right|_{C_b} = \frac{dV_{out}}{fRC_b} \tag{61}$$

This signifies that the load resistance R, switching frequency f, and capacitance C_b should be properly selected.

F. Combined Effects of Capacitor C_a and C_b

The total output variation due to the combined effect caused by both capacitor C_a and C_b is as follows,

$$\left.\Delta v_{out}\right|_{C_a + C_b} = \left.\Delta v_{out}\right|_{C_a} + \left.\Delta v_{out}\right|_{C_b} = \frac{V_{out}}{fR}\left(\frac{1}{C_a} + \frac{d}{C_b}\right) \tag{62}$$

G. The Efficiency of the converter

The efficiency of the converter can be obtained as,

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$$\eta_{TBC} = \frac{2 - \frac{2\,V_{dL}}{V_{in}} - \frac{3V_{dS}d}{V_{in}} - \frac{V_{fd}+V_d}{V_{in}} - \frac{V_{r_c}}{V_{in}} - V_{r_c}}{2 + \frac{R\ 1-d}{V_{out}\times V_{in}} P_S} \quad (63)$$

Where P_S is total switching loss in the switches, and it can be calculated as,

$$PS = PS_{Sa} + PS_{Sb} = \frac{I_{Sa}V_{Sa}(T_{ra} + T_{fa}) + I_{Sb}V_{Sb}(T_{rb} + T_{fb})}{T} \quad (64)$$

Where P_{Sa} and P_{Sb} are switching losses of switches S_a and S_b, I_{sa} and I_{Sb} are average currents through switches S_a and S_b, V_{sa} and V_{Sb} are average voltages across switches S_a and S_b, T_{ra} and T_{rb} are rise time for switches S_a and S_b, T_{fa} and T_{fb} are fall time for switches S_a and S_b.

IV. Comparison of Converters

A comparison of the proposed TBC and other related converters is presented in Table I to highlight the advantages of the proposed converter. It can be noticed that the voltage stress across switches is reduced to half as well as a higher voltage conversion ratio is obtained with the TBC without increasing the number of components in the circuit. Furthermore, the converter's output terminal is grounded. The proposed converter has a lower input-current ripple and a higher voltage gain as compared to the conventional high-boost dc-dc converters. The proposed converter uses two diodes lesser than the Classical switched Inductor Boost converter in [19]. Furthermore, the switch voltage stress is reduced to half of the output voltage by employing one more switch in the circuit. Thus, low voltage rating active switches are suitable to design the proposed TBC configuration. The total required number of components is the same as the number of components in classical SIBC. Compared with the Transformer-less active switched inductor converter (Converter-I) [20], the proposed converter achieves a higher voltage gain and voltage stress across the switch is also reduced. In comparison with the Converter-II [20], the proposed converter's output terminal is grounded. The converters in [21]-[23], required additional voltage lift networks and complex control. The voltage gain can be increased by using multiple stages but the number of circuit components increase, which results in complex power and control circuit. Moreover, the cost of these circuits is high and efficiency decreases as the number of stages increase to achieve higher voltage as compared to the proposed converter. As compared to the Converter in [25], it can be noticed that a higher voltage conversion ratio is obtained with the proposed TBC without increasing the number of components in the circuit. Also, the proposed TBC uses a lesser number of components as compared to the converter in [29]. Furthermore, the proposed TBC converter provides the common ground connection of source and load, while there is no common ground connection between the source and the load for the converters in [20]-[23], and [29]. Therefore, for these converters to be used in PV systems, there will be a requirement of common-mode voltage and leakage current reduction techniques.

V. Design of Proposed TBC

To verify the working operation and performance of the proposed circuitry, a prototype of TBC configuration is developed in the laboratory. This prototype is developed by considering the parameters with a typical input voltage of 40 V, output power of 500 W, an output voltage of 400 V, and the switching frequency of 100 kHz.

A. Critical Inductances and Capacitances

The inductors and capacitors are designed with consideration of the worst-case scenario to obtain a good performance. Therefore, the required duty cycle is calculated by selecting the 90% worst efficiency (η^{worst}) as follows,

TABLE I. Comparison of proposed Converter with Related Available converters

Converter Performances		A	B	C	D	E	F	G	H	I	J
Number of components and devices	Total Components	4	8	6	8	8	10	10	8	10	8
	Switches	1	1	2	2	3	3	2	2	2	2
	Diodes	1	4	1	2	2	3	4	3	3	2
	Inductors	1	2	2	2	2	2	1	2	2	2
	Capacitors	1	1	1	2	1	2	3	1	3	2
Suitable load type		Grounded		Floating					Grounded	Floating	Grounded
Voltage Gain (V_G)		1/1-d	1+d/1-d		2/1-d	(1+d_1)/(1-d_1-d_2)	2-d_2/1-d_1-d_2	3-2d/1-2d	1+d/1-d	3+d/1-d	2/1-d
Normalized Switch Voltage stress (V_S/V_{out})		1	1	(1+V_G)/2V_G	½ , ½	(1+V_G)/2V_G, 1	½, (V_G-1)/V_G	(1-V_G)/2	½, ½	V_G/3+d	½, ½
Normalized Diode Voltage stress (V_D/V_{out})		1	(V_G-1)/2V_G, 1/ V_G, 1	(1+V_G)/V_G	½, 1	1	(1-V_G)/V_G, (1-V_G)/2V_G	(1-V_G)/2, (1-V_G)	(1-V_G)/2V_G, 1/ V_G, 1	2V_G/3+d	½, 1
Switch Current Stress		I_{in}	I_{in}	$\frac{2I_{in}}{1+d}$	I_{in}	I_{in}/2, I_{in}	$I_{in}d_1$/2, $I_{in}d_2$	$\frac{I_{in}}{(3-2d)}$	dI_{in}/2, dI_{in}	I_{in}/2, I_{in}/2	dI_{in}/2, dI_{in}
Designed Prototypes	Output Power	200W	50W	40W	-	100W	500W	200W	500W	200W	500W
	Voltage Gain	4	7	5-8	-	10	10.53	4-8	4	15	10
	Efficiency	98.33%	95.20%	92.70%	-	93.60%	93.43%	95.4%	97.17%	94.53%	92.43%

V_s is Voltage across the switch, V_D is Voltage across the diode, V_{out} is the output voltage, and I_{in} is the input current.
A: Conventional boost converter [24], B: Classical SIBC [19], C: Transformer-less active switched inductor converter [20], D: Converter –II [20], E: converter in [21], F: Converter in [22], G: Converter in [23], H: Converter in [25], I: Converter in [29], J: proposed converter.

$$d\big|_{\eta worst=90\%} = 1-\frac{2}{V_G|_{CCM}}\eta^{worst} = 1-\left(\frac{2}{10}\times 0.90\right) \approx 82\% \quad (65)$$

The inductors L_a and L_b critical inductance values can be obtained as,

$$L_{a,c} = L_{b,c} = V_{in}\frac{dT}{\Delta I_L} = V_{in}\frac{dT}{40\%\text{ of }I_L} \quad (66)$$

For the given parameters, the critical values are obtained as,

$$L_{a,c} = L_{b,c} = 40\times\frac{0.82}{4.5A\times 100kHz} \approx 72.5\ \mu H \quad (67)$$

The inductors L_a and L_b must possess a higher inductance and current rating than the obtained critical inductance values and input current, respectively. Hence, the prototype is designed by selecting the ferrite E type core inductors with a rating of 1mH/18A. It is observed that at the instant when switches are turned ON, maximum current is flowing through capacitor C_a. Therefore, the critical capacitance of the capacitor C_a is obtained as follows,

$$C_{a,c} = \frac{I_{in}(1-d)}{f\Delta V_{Ca}} = \frac{12.5\times 0.18}{100kHz\times 2V} = 11.25\mu F \quad (68)$$

The capacitor C_a must possess a voltage rating higher than the input voltage i.e. 40V. Hence, the prototype is designed by selecting a film type capacitor rated at 22µF/100V. The critical capacitance capacitor C_b can be obtained as follows,

$$C_{b,c} = d\frac{P_{out}}{V_{out}f\Delta V_{Cb}} = 0.82\frac{500}{400\times 100kHz\times 4} \approx 2.56\mu F \quad (69)$$

The capacitor C_b must possess a voltage rating higher than the output voltage i.e. 400V. Hence, the prototype is designed by selecting a film type capacitor rated at 3.3µF/450V.

B. *Critical Voltage and Current of Semiconductor Devices*

The critical voltage rating for switches S_a and S_b can be obtained as follows,

$$V_{Sa,c} = \frac{V_{out}}{2}\ \text{or}\ \frac{V_{in}}{1-d},\ V_{Sb,c} = \frac{V_{out}}{2}\ \text{or}\ \frac{V_{in}}{1-d} \quad (70)$$

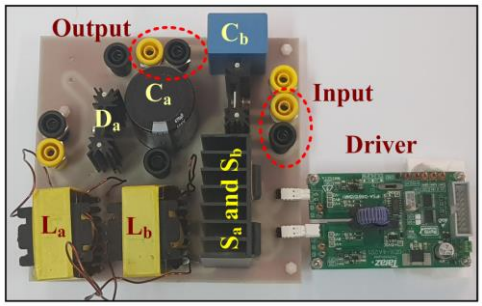

Fig.8. Designed prototype.

For the selected parameters, the switch voltage rating must be greater than 200V. The switches S_a and S_b must possess a current rating higher than the input current i.e. I_{sa} and $I_{Sb} > I_{in}$. Hence, to design the prototype, switches SQP90142E are selected. The critical voltage rating for diode D_a is obtained as follows,

$$V_{Da,c} = \frac{V_{out}}{2}\ \text{or}\ \frac{V_{in}}{1-d} \quad (71)$$

The critical voltage rating for diode D_b is obtained as follows,

$$V_{Db,c} = V_{out}\ \text{or}\ \frac{2V_{in}}{1-d} \quad (72)$$

For the selected parameters, the diodes D_a and D_b voltage rating must be greater than 200V and 400V, respectively. The diodes D_a and D_b must possess a current rating higher than the input current i.e. I_{Da} and $I_{Db} > I_{in}$. Hence, to design the prototype, diodes C3D10060A-ND and DPG10I400PM are selected.

VI. Experimental Results

The prototype of the TBC is implemented in the laboratory to validate the theoretical analysis and performance of the converter. The switches S_a and S_b are controlled with the switching frequency

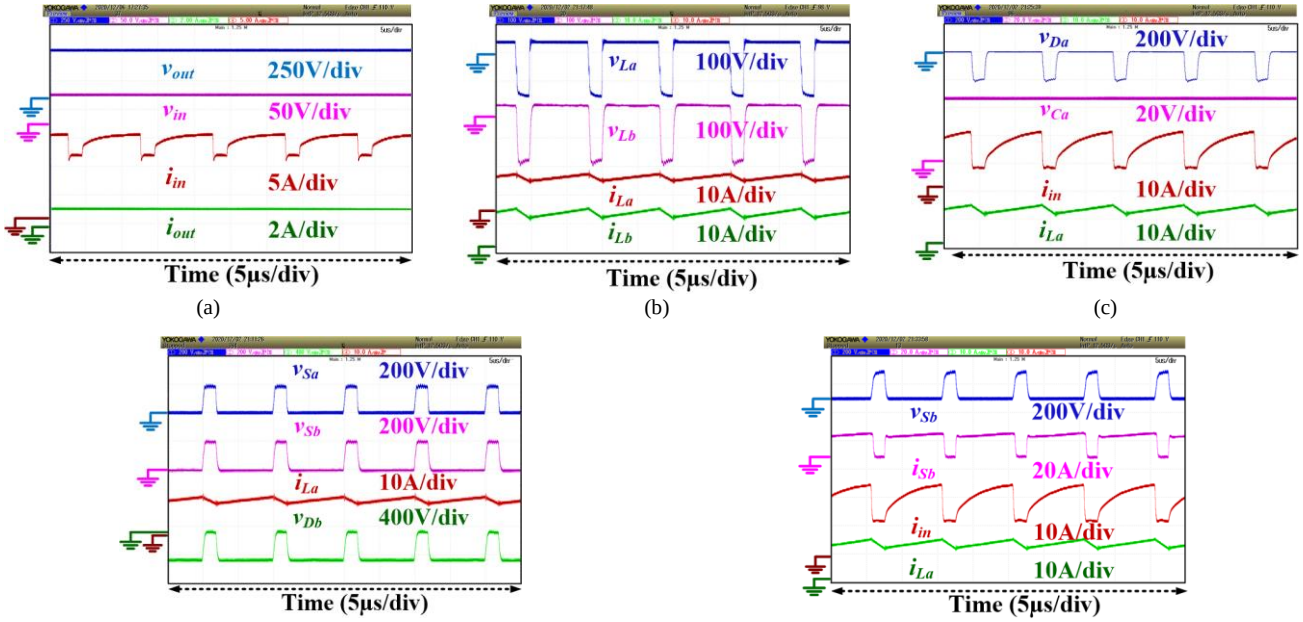

Fig. 9. Experimental results (a) output- and input- voltages, and output- and input- currents, (b) voltage and current across/through inductors L_a and L_b, (c) voltage across diode D_a, voltage across capacitor C_a, input current, and current through inductor L_a, (d) voltage across switches S_a and S_b, current through inductor L_a, and the voltage across diode D_b, (e) voltage and current across/through switch S_b, input current, and current through inductor L_a.

100kHz using Field Programmable Gate Array (FPGA) and supplied through drivers GDX4A2S1. The designed prototype is shown in Fig. 8. The transfer function of the proposed converter is calculated as follows,

$$G_{v_{in}(s)}\Big|_{\hat{d}(s)=0} = \frac{\hat{v}_{out}(s)}{\hat{v}_{in}(s)} = \frac{2/1-d}{S^2\frac{LC_b}{(1-d)^2}+\frac{sL}{R(1-d)^2}+1} \tag{73}$$

$$G_{d(s)}\Big|_{\hat{v}_{in}(s)=0} = \frac{\hat{v}_{out}(s)}{\hat{d}(s)} = \frac{\left(V_{out}/1-d\right)\left(1-sLI_L/V_{out}(1-d)\right)}{S^2\frac{LC_b}{(1-d)^2}+\frac{sL}{R(1-d)^2}+1} \tag{74}$$

The basic PI controller has been implemented to control the output voltage by using the system generator in the Xilinx. The sensed output voltage is converted to the digital signal with the help of the PMOD AD1. The desired voltage reference can be given in the per-unit form (1PU=400V). The suitable minimum and maximum duty ratios have been selected at 0.2 and 0.7 for the safe operation of the proposed converter. Sallen key filters are used to smoothen the signals flowing into and out of the FPGA. Fig. 9(a) shows the obtained experimental waveforms of output- and input-voltages, and output- and input- currents. The average values of the observed output voltage, input voltage, output current, and input current are 399.6V, 40.3V, 1.24A, and 13.3A, respectively. Due to the charging and discharging of both inductors L_a and L_b, and capacitor C_a, the input current is observed to be continuous, and the ON-state and OFF-state slope of the input current is found to be increasing and decreasing, respectively. Fig. 9(b) shows the obtained experimental waveforms of voltage and current across/through inductors L_a and L_b. The inductors L_a and L_b are observed to be charging in ON-state with the average voltage values of 40.1Vand 39.8V, respectively. The inductors L_a and L_b are discharging in OFF-state with the average voltage value of -159.7V and -159.7V, respectively. During the OFF state, the slight slope is observed in inductor voltages due to little practical difference in the values of both the inductances. The average values of the observed currents through inductors L_a and L_b are 11.1A and 10.9A, respectively. Fig. 9(c) shows the voltage across diode D_a, the voltage across the capacitor C_a, input current, and current through inductor L_a. It is observed that the peak voltage across diode D_a is -200.4V i.e. approximately half of the output voltage. It is observed that the voltage across capacitor C_a is 40.1V i.e. equal to the input voltage. Fig. 9(d) shows the experimentally observed voltages across switches S_a and S_b, the current through inductor L_a, and the voltage across diode D_b. It is observed that the voltages across the switches S_a and S_b are 200.7 and 200.4V, respectively i.e. approximately half of the output voltage. Moreover, it is also observed that the voltage stress for both the switches S_a and S_b is approximately the same. It is observed that the peak voltage across diode D_b is -400.3V. The voltage waveform of diode D_b validates that the diode D_b is reversed biased in ON state and forward biased in OFF state. Fig. 9(e) shows the voltage and current across/through switch S_b. It is observed that the average current through switch S_b is 11.4A.

A disturbance is initiated from the load and source sides to analyze the proposed converter's performance in a disturbed condition. The reference of the output voltage is set at 400V and the dynamic response of the system by varying the input voltage has been presented in Fig.10 (a) and the step-change in the load current

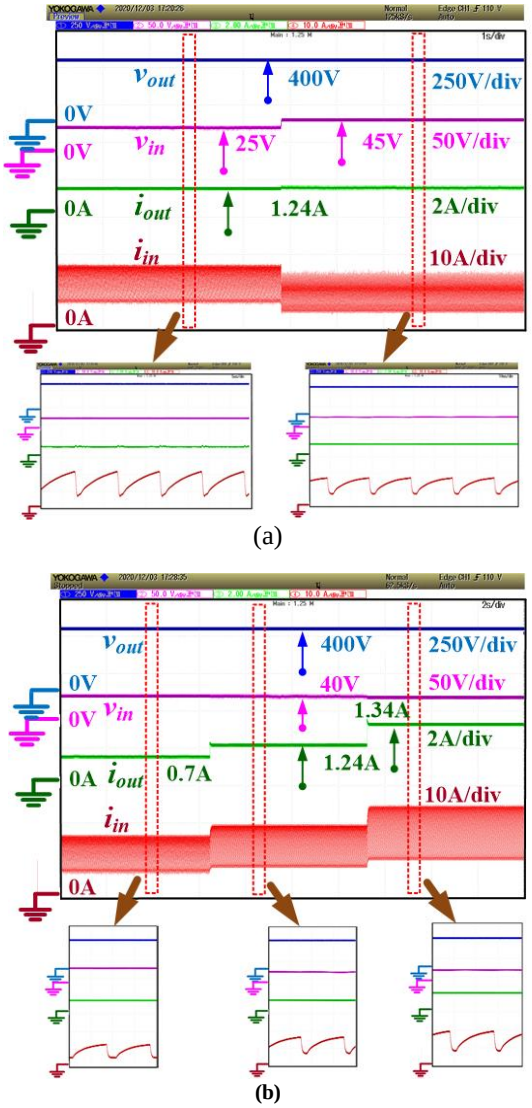

Fig. 10. Proposed converter TBC Experimental results (input/output voltages and currents) with disturbance, (a) Variation in the input voltage, (b) step change in the load current.

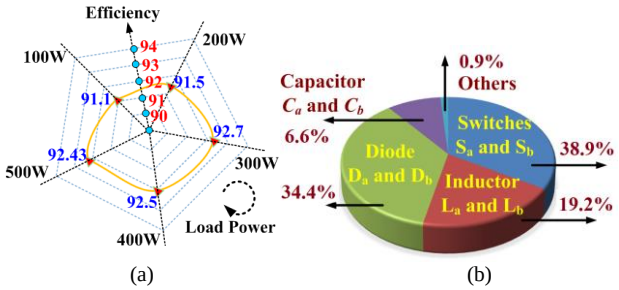

Fig. 11. Plots (a) Efficiency versus power at voltage gain=10, (b) Loss breakdown at 500W.

in Fig. 10(b). As seen from Fig. 10(a), constant output voltage of 400V is achieved even when the input voltage varies from the 25V to 45V. The respective variations in the input current to balance the power in the proposed topology and variation in the duty cycle of the converter are observed and the zoomed waveform is shown in Fig. 10(a). Similarly, in Fig. 10(b) the load is changed and the constant output voltage of 400V is achieved. Here, the load current is varying from 0.7A to 1.24A to 1.34A and the change in the input

current can assure the power balance between the input and the output. All the zoomed waveforms have been presented in Fig. 10(b) for clarity. To analyze the efficiency of the developed prototype, the performance of TBC is examined at different power levels (100W to 500W). Fig. 11(a) shows the graphical plot of efficiency versus power. The efficiency of the developed prototype is observed to be 92.43%, at a power of 500W and voltage gain 10. The loss breakdown is shown in Fig. 11(b). It is observed that the power loss due to switches, diodes, inductor, and capacitors are 38.9%, 34.4%, 19.2%, and 6.6% respectively. The power loss due to switches and diodes is higher compared to other elements.

VII. Conclusion

A new TBC configuration is proposed for step-up applications with reduced voltage stress across the switch. The total number of components required is the same as the number of components in classical SIBC. However, the voltage gain of the TBC is higher than the classical boost converter and SIBC. The proposed converter needed a lesser number of diodes than the conventional SIBC, and voltage stress across switches are half of the output voltage. Thus, low voltage rating active switches are suitable to design the proposed TBC configuration. The CCM and DCM modes' working principle, voltage gain, boundary conditions, the effect of non-idealities, comparison with the related converters, and design are presented. It is observed that a higher voltage gain can be achieved by incorporating lower voltage rating switches. The theoretical analysis and operation of the proposed TBC are verified by the experimental investigations and the efficiency is found to be 92.43% at a voltage gain of 10 and output power 500W. The limitation of the proposed converter topology is that the capacitor is directly connected to the input supply in Mode I with the help of diode D_a and switch S_b. Therefore, transient high peak current will flow through the capacitor C_a and the current will decrease with time since it is directly connected across the input voltage. However, the average current through any capacitor is zero.

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