High Efficiency DC-DC Boost Converter With Passive Snubber And Reduced Switching Losses

Andrzej Mondzik, *Member IEEE*, Robert Stala, *Member IEEE*, Stanisław Piróg, Adam Penczek, *Member IEEE*, Piotr Gucwa, Miłosz Szarek

***Abstract*— This paper presents a novel concept of switch-mode DC-DC boost converters with reduced switching losses. The converters use an auxiliary switching cell (ASC) to achieve zero voltage switching (ZVS) during the turn-off of a transistor. The novel concept facilitates an increase in the efficiency or switching frequency of an IGBT-based boost converter. The paper discusses the converters topology, the principle of operation, and issues related to the reduction of power losses, the range of optimal operation and selection of components. The concept of the converter was verified through simulation and a series of experiments that demonstrate the process of zero-voltage turn-off and the efficiency of the converter.**

***Index Terms*—DC-DC converter, boost converter, high efficiency, ZVS converter**

I. INTRODUCTION

THE switch-mode DC-DC boost converter is a fundamental power electronic circuit [1]. It can be used for a wide range of power of loads and is found in many applications, for example, the photovoltaic systems. The main advantages of the boost converter are its simple topology and control. High switching frequency is often used in order to minimize the volume of passive components in the converter; however, it is associated with an increase in switching losses, which is substantial in devices such as the high-power IGBT-based boost converter. Therefore, an improved design for the reduction of switching losses is required.

An IGBT is an appropriate switch in high power and high voltage systems. The IGBT technology is still being developed and various examples of IGBT switch concepts and IGBT-based converters can be found in [2]–[7]. A characterization of switching performance of an IGBT switch and a comparison to a SiC MOSFET are discussed in [2] and show that the limit of a switching frequency of an IGBT-based boost converter is significantly below the performance of a SiC-based setup. E_{off} losses are of particular importance for the performance and efficiency of an IGBT-based boost converter. A comparison of performance of a 10kW Interleaved Boost Converter (IBC) based on SiC and Si (IGBT) devices is presented in [3], and demonstrates a significant switching loss and an operation frequency limit of an IGBT-based design.

In [4], a detailed investigation of soft switching operation of an IGBT-based model demonstrates that several soft switching techniques can reduce losses of an IGBT-based boost converter and that their waveforms change in the commutation process. A soft turn-off is also a subject of research presented in [5] performed on an IGBT-based Dual Active Bridge (DAB) converter.

In [6] and [7], examples of switch concepts are presented. [6] demonstrates the performance of a boost converter operating at 55kW, 1.7kV to 7kV and 5kHz, based on a 4HSiC N-IGBT switch, and [7] describes the performance of a 15kV SiC N-IGBT switch.

In order to design an IGBT-based converter with a high switching frequency and with a small volume of passive components, the switching losses must be decreased. This can be achieved by the implementation of soft switching in a boost topology [8], [9] and by the application of auxiliary circuits [10]–[26] such as passive snubbers [18]–[20] and active circuits [10]–[17], [21]–[26]. In [9], a two-phase zero voltage switching (ZVS) boost converter was used in conjunction with resonant capacitors in parallel to the switches and with modified control. In [8], a boost converter with rated output power of 40kW and output voltage of 3kV in soft switching modes was achieved with an application of snubber capacitors in parallel to transistors and diodes, and in the boundary conduction mode (BCM) with interleaved control.

The use of active snubbers for soft switching of a boost converter are proposed in [10]–[17]. In [10]–[14], soft switching was accomplished in a converter with auxiliary resonant circuits controlled by switches, or by switches and diodes. In [15], IGBT turn-off losses were reduced by the use of a snubber with a variable capacitor controlled by a MOSFET switch. Another approach is proposed in [16] where a capacitor-switched circuit was used as a snubber of the IGBT to reduce turn-off losses. The snubber is composed of a capacitor, diodes, and active switches. A switched capacitor concept for a soft switching auxiliary circuit is presented in [17]. The ZVS turn-on and ZCS turn-off was achieved in the boost converter composed of an additional switch, a capacitor, and two diodes. The basic concept proposed in this paper is very favorable in

comparison to converters presented in [10]–[17] because the additional snubber does not utilize active switches. It simplifies power circuit, reduces number of required electronic components and minimize risk of failure. Furthermore the proposed solution is reliable and not expensive.

Passive snubbers for soft switching of a boost converter [18]–[20] are a very reliable solution as well. Such snubbers are composed of LC passive components and diodes. A larger number of components can increase the volume of the converter. Therefore, there is an important merit of the proposed converters visible, as that they use fewer number of passive components in auxiliary branches than converters with passive snubbers presented in the literature [18]–[20].

Analyzing the choke design issues and its volume it is seen that in some concepts, such as [13] the current stress of choke in a snubber reaches the value of the input current. In high power converters it affects volume of the snubber significantly, similarly as current stress of the auxiliary switches and diodes.

The converters analyzed in this paper have very limited current stress of auxiliary components. The input current flows through the auxiliary capacitor causing its discharging. This process requires very short time interval and causes nonsignificant current stress of the snubber capacitor and one of the auxiliary diodes. Charging the auxiliary capacitor occurs in the circuit composed of a resonant choke and a diode. The charging current and the current stress of the resonant choke is not significant as the snubber capacitor has small value (e.g. tens nanofarads).

The converters and methods for the reduction of switching losses presented in this paper are based on the idea of an auxiliary switching cell introduced in NPC 3-level voltage source inverters (VSI) in [21]–[23], whereby a voltage rise across the transistor (dv_{DS}/dt) is slowed down by a temporary circuit where the snubber capacitance is discharged during the turn-off process. The implementation of soft switching in an IGBT-based T-type three-level VSI results in a 0.47% improvement in efficiency.

A slower voltage rise across the transistor can be achieved in a switch-mode boost converter. This paper presents a novel concept of a boost converter with an auxiliary switching cell (ASC). The ASC introduced here assures zero voltage across the transistor at the beginning of the turn-off process and low voltage during the current commutation (Fig. 1 and Fig. 2). The voltage rise across the transistor is determined at the design stage by selecting an auxiliary capacitor which is discharged during the turn-off process by the current of the main inductor.

In a basic design, the ASC is a low-cost and low-complexity circuit. It comprises of two diodes, a low-volume auxiliary capacitor and a resonant inductor in a circuit responsible for charging the auxiliary capacitor (Fig. 1). For applications where the required voltage gain is greater than two, further modification of the proposed ASC concept is demonstrated (Fig. 2), whereby the auxiliary capacitor of the ASC is charged by the output voltage divider which appropriately ensures its optimal voltage.

The topologies and the concept of operation of the boost converter with ASC circuits have been introduced by the authors of this paper in patents [24]–[26]. Nevertheless, the results of research presented in this paper are novel and contribute significantly to the field of soft-switched high-power switch-mode boost converters and validate the proposed concept in the IGBT-based DC-DC converter. An improvement in efficiency as well as the ability to increase the switching frequency in comparison to the classic boost converter are demonstrated.

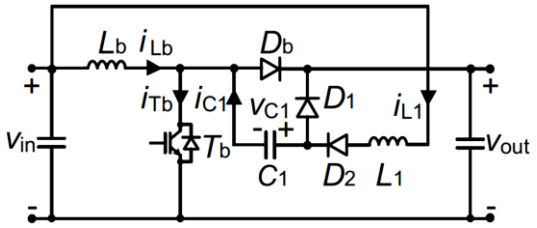


Fig. 1. The DC-DC boost converter with ASC (type A).

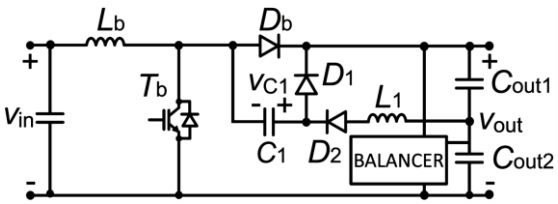


Fig. 2. The DC-DC boost converter with optimized ASC (type B).

The paper is organized as follows. Section I and Section II describe basic concepts of a boost converters with an ASC and their operation principle. Section III presents an analytical discussion of the ASC operation in the boost converter and its effectiveness. Section IV comprises simulation results that are the basis for the commutation and the relationship between the efficiency and the parameters of the ASC. Experimental results are presented in Section V and contain waveforms, infrared images and efficiency measurements that allow the comparison between the proposed soft commutated boost converter and the classic solution.

II. Concept of the Operation of the Boost DC-DC Converter with Auxiliary Switching Cell

In the boost converter with the proposed ASC, the voltage rise across the transistor is slower during its turn-off process. Therefore, during the turn-off, quasi-ZVS conditions are achieved. Fig. 3 presents the basic principle of operation of the boost converter with the auxiliary switching cell. The turn-off process can be divided into two stages, which are presented in Fig. 4 and Fig. 5. In STAGE 1, the inductive current starts flowing through the snubber capacitor C_1, the diode D_1 and the output capacitor. To achieve the optimal ZVS conditions, the capacitor C_1 should be charged to a voltage equal to the output voltage. In such a case, the voltage across the switch is zero at the beginning of the turn-off process. The inductive current then discharges the capacitor C_1 , which in turn causes a voltage rise across the transistor. When v_{C1} reaches zero, the diode D_1 stops conducting (STAGE 2).

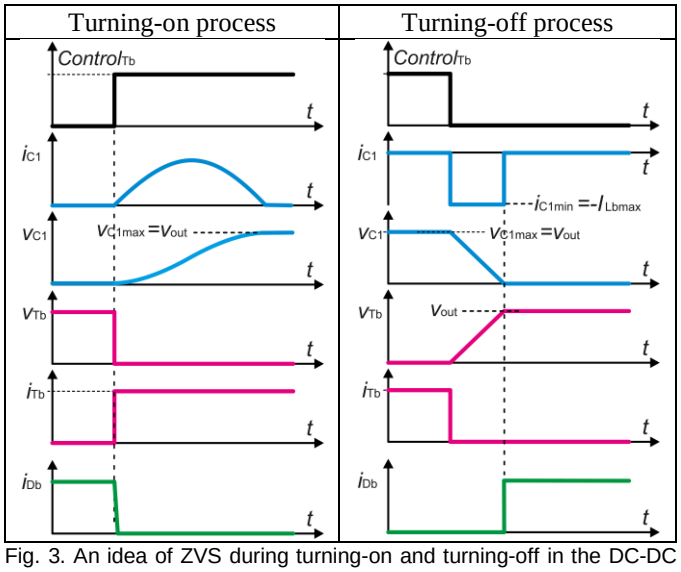


Fig. 3. An idea of ZVS during turning-on and turning-off in the DC-DC boost converter with the ASC.

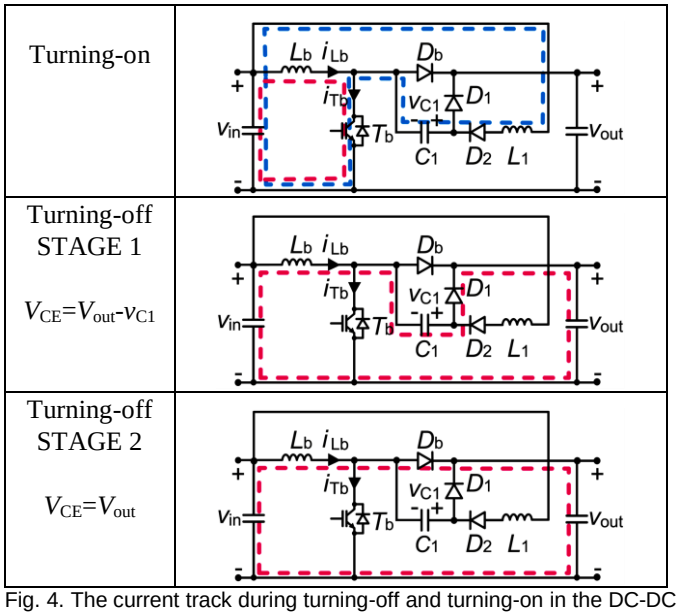


Fig. 4. The current track during turning-off and turning-on in the DC-DC boost converter with the A-type ASC.

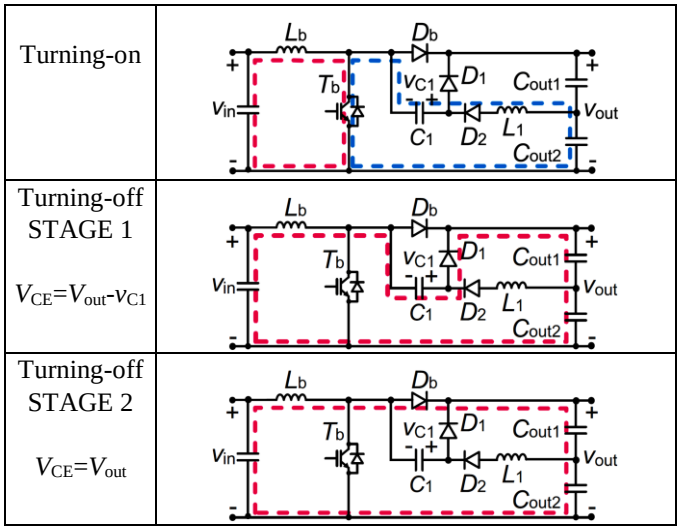


Fig. 5. The current track during turning-off and turning-on in the DC-DC boost converter with the optimized B-type ASC.

When the transistor starts to conduct, charging of the auxiliary capacitor C_1 begins. C_1 is charging in an oscillatory circuit composed of the inductor L_1, the diode D_2, the main switch T_b and the input source (Fig. 4 and Fig. 5). When the duty cycle D is 50% or less, the voltage across the capacitor C_1 reaches the value $v_{C1max} = v_{out}$. It is the optimal value that assures the ZVS during the turn-off.

When the boost converter operates with a double or higher voltage gain, the DC-DC boost converter with a B-type ASC (Fig. 2 and Fig. 5) can be applied to achieve the optimal turn-off conditions. In such configuration, the auxiliary capacitor C_1 is charged by the voltage, which equals $v_{out}/2$. To achieve that, an output voltage divider can be used (two series capacitors with a voltage balancer) (Fig. 2) or low power DC-DC converter for resonant circuit supply. In the experimental tests DC-DC buck was used which produces ½(V_{out}) from the output voltage. An average power required for the recharging of C_1=44nF capacitor to maximum voltage V_{C1max}=400V and frequency 32.2kHz is approximately P_r≈50W. It can produce additional below 5W power losses under the assumption that the buck operates with the efficiency above 90%. This part of losses are included in experimental results of efficiency presented in Section V. Voltage stress of the switch and the diode of the auxiliary buck converter should assume 400V rated voltage but its current stresses relates to the power but also the design concept. In such a topology, the optimal operation of the ASC is accomplished for a wide range of the duty cycle variation. The electronic balancer could be replaced by an output voltage divider with a resistive stabilization. It is less complex solution but generates more losses. The C_1 capacitor is then charged from the lower capacitor C_{out2} of the divider and discharged to the series branch of the output capacitors. It creates imbalance of their voltages and power losses required for the passive output voltage balancing exceed the value $P_r/2$.

III. Analytical Considerations

A. The capacitor C_1 charging

C_1 is charged in the oscillatory circuit composed of C_1, L_1, T_b, D_2. (Fig. 4 and Fig. 5: Turning-on):

$$i_{L1}(t) = \frac{(V_S - V_0)}{\rho_{ch}} sin\omega_{ch}\, t;\; u_{C1}(t) = V_S + (V_0 - V_S)\, cos\omega_{ch}\, t \quad (1)$$

where: V_S is the supply voltage of the capacitor C_1: $V_S = V_{in}$ for the A-type ASC, $V_S = 0.5V_{out}$ for the B-type ASC, V_0 is the initial voltage across the capacitor C_1, $\omega_{ch} = \sqrt{\frac{1}{L_1 \cdot C_1}}$, $\rho_{ch} = \sqrt{\frac{L_1}{C_1}}$.

The charging time of the capacitor C_1 is equal to a half of the recharging time of the oscillatory circuit. It should be shorter that the conducting time of the main transistor T_b:

$$t_{ch} = \frac{1}{2}T_{ch} = \pi\sqrt{L_1 C_1} < DT \quad (2)$$

where: T is the pulse repetition period of the transistor T_b, D is the duty cycle.

Assuming zero initial conditions, V_{C1} is charged to $2V_S$ but not more than V_{out}.

B. Conditions of the capacitor C_1 discharging

The capacitor C_1 is discharged in the circuit composed of C_1, L_b and D_1 with initial current I equal to I_{Lbmax}. Due to a high value of the input inductance (L_b), the oscillation period of this circuit is significantly longer than the time required for full discharging of the capacitor C_1 ($\omega_{dis} = (L_bC_1)^{-0.5}$). Therefore, it can be assumed that C_1 is linearly discharged by the input inductor current:

$$dv_{C1}/dt = I_{Lbmax}/C_1 \quad (3)$$

The discharging time t_{dis} of the capacitor C_1 should not be longer than the non-conducting time of the transistor T_b (for continuous current $T(1\text{-}D)$) and not shorter than its turn-off time t_{off}.

$$t_{off} \le t_{dis} = \pi\sqrt{L_bC_1} \le T(1-D) \quad (4)$$

In case operation with the rated power the condition $t_{dis} << T$ is fulfilled. It can be assumed that at the beginning of Stage I (Fig. 4 and Fig. 5) the input inductor current i_{Lb} increases very insignificantly and $I_{Tbmax} = I_{Lbmax}$. After the transistor went into the turn-off state the voltage on the inductor (u_{Lb}) remains positive. It occurs in the very short time interval, until the C_1 capacitor is discharged to the value $u_{C1} = u_{out}\text{-}u_{in}$. Before this time the current rise di_{Lb}/dt decreases until it reaches zero.

C. Selection of the ASC parameters

Within the turn-off time t_{off} of the transistor T_b at the maximum current I_{Lbmax}, the voltage across the capacitor C_1 decreases with the assumed speed: dv_{C1}/dt. It determines the C_1 capacitance selection:

$$C_1 = I_{Lbmax}\frac{dt}{dv_{C1}} \quad (5)$$

To determine the minimum of snubber capacitance, the rated conditions where the discharging process is the longest should be assumed. It occurs at the assumed minimum input current (I_{Lbmin}) and in the case when the C_1 capacitor is discharged within the period of time $t=T(1\text{-}D)$ starting from $V_{C1max}=V_{out}$. Therefore, the capacitance should not be higher than:

$$C_{1max} = \frac{I_{Lbmin}T(1-D)}{V_{out}} = \frac{I_{Lbmin}(1-D)}{f_{sw}V_{out}} \quad (6)$$

The current which charges the C_1 capacitor adds to the input current in the branch of the T_b switch. Assuming the limit of its collector current the minimum resonant inductance is the following:

$$L_{1min} = C_1\frac{V_s^2}{(I_{Cmax}-I_{Lbmin})^2} \quad (7)$$

The upper limit of the resonant inductance is determined by oscillation time of the current during the C_1 capacitor charging and the time period when the transistor is turned on:

$$L_{1max} = \frac{D_{min}^2}{C_1 f_{sw}^2 \pi^2} \quad (8)$$

The amplitude of the C_1 charging current is:

$$I_{L1max} = \frac{V_S}{\rho_{ch}} = V_S\sqrt{\frac{C_1}{L_1}} \quad (9)$$

The currents of diodes D_1 and D_2 are the discharging and charging currents of the capacitor C_1, respectively. Across the diode D_1 the maximum voltage equal to the output voltage V_{out} can occur, while across the diode D_2 the voltage difference $V_{C1max}\text{-}V_{in}$ for the A-type ASC, or a half of the output voltage $0.5V_{out}$ for the B-type ASC can be found.

D. Power losses in the ASC

When the auxiliary capacitor is charging, the current flowing through L_1, D_2, C_1 and T_b (Fig. 3 and Fig. 4) causes the following power losses:

$$\Delta P_{ASCch} = I_{L1av}(V_{FD2} + V_{CEonTb}) + I_{L1rms}^2(R_{L1} + R_{C1}) \quad (10)$$

where: V_{FD2} is the forward voltage of diode D_2, V_{CEonTb} is the collector-to-emitter saturation voltage of T_b, and R_{L1} and R_{C1} are equivalent series resistances of L_1 and C_1.

The currents I_{L1av} and I_{L1rms} depend on L_1 and C_2 according to the following relationships:

$$I_{L1av} = \frac{2}{\pi}\frac{V_S}{\rho_{ch}}\frac{t_{ch}}{T} = \frac{2}{\pi}I_{L1m}\frac{t_{ch}}{T}; \qquad I_{L1rms} = \frac{1}{\sqrt{2}}I_{L1m}\sqrt{\frac{t_{ch}}{T}} \quad (11)$$

where: I_{L1m} is the amplitude of the current I_{L1}.

Finally, the model of the ASC losses during the charging stage is as follows:

$$\Delta P_{ASCch} = I_{L1m}\frac{t_{ch}}{T}\left[\frac{2}{\pi}(V_{FD2} + V_{CEonTb}) + \frac{1}{2}I_{L1m}(R_{L1} + R_{C1})\right] = f_{sw}C_1V_S\left[\frac{2}{\pi}(V_{FD2} + V_{CEonTb}) + \frac{V_S}{2\rho_{ch}}(R_{L1} + R_{C1})\right] \quad (12)$$

In [5], the behavior of the IGBT during hard and soft switching is analyzed in detail. For the case presented in this paper, the essential differences between the hard and soft switching are presented in Table I and Fig. 6.

TABLE I
TURN-OFF PROCESS PARAMETERS FOR THE MODEL OF LOSSES

	Hard switching	Soft switching
Collector current (i_c) during Miller-plateau period (0-t_a in Fig. 6)	Constant	Fast decrease
Tail current (I_T)	Depends on a switch	Can be longer than in the case of hard switching
Collector-emitter voltage rise	Fast $dv_{CE}/dt = V_{out}/t_a$	Slow $dv_{CE}/dt = I_{Lbmax}/C_1$

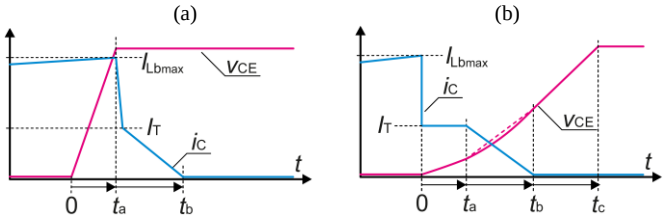


Fig. 6. The model of the turn-off process and parameters for the model of losses: (a) – the simplified case of hard switching, (b) – soft switching turn-off.

The ASC introduces power losses during the time period when the transistor T_b is turned-off. Taking into consideration the

model of hard and soft IGBT turn-off, presented in Fig. 6, the proportion of power losses can be estimated as:
Conduction losses during the 0-t_a time period are:

$$\left.\frac{\Delta P_{\mathrm{ASCav}}}{\Delta P_{T\mathrm{bav}}}\right|_{0-t_\mathrm{a}} = \frac{(I_{L\mathrm{bmax}}-I_\mathrm{T})V_{FD1}}{I_{L\mathrm{bmax}}\frac{V_{\mathrm{CEmax}}}{2}} = 2\frac{(I_{L\mathrm{bmax}}-I_\mathrm{T})}{I_{L\mathrm{bmax}}}\frac{V_{FD1}}{V_\mathrm{out}} \tag{13}$$

Resistive losses during the 0-t_a time period are:

$$\left.\frac{\Delta P_{\mathrm{ASCr}}}{\Delta P_{T\mathrm{br}}}\right|_{0-t_\mathrm{a}} = \frac{(I_{L\mathrm{bmax}}-I_\mathrm{T})^2}{I_{L\mathrm{bmax}}^2}\frac{R_{C1}+R_{D1}}{R_{T\mathrm{b}}} = \frac{R_{C1}+R_{D1}}{R_{T\mathrm{b}}}\left(1-2\frac{I_\mathrm{T}}{I_{L\mathrm{bmax}}}+\frac{I_\mathrm{T}^2}{I_{L\mathrm{bmax}}^2}\right) \tag{14}$$

From (13) it is seen that the ASC introduces significantly lower conduction losses than the transistor T_b in hard switching mode (proportional to V_{FD1}/V_{out} which can be for example 0.1%). The resistive losses of the ASC in relation to T_b during the turn-off time can be comparable. However, this part of losses in the IGBT-based converter can be neglected in the whole balance of power. Conduction losses during the t_a-t_b time period are:

$$\left.\frac{\Delta P_{\mathrm{ASCav}}}{\Delta P_{T\mathrm{bav}}}\right|_{t_\mathrm{a}-t_\mathrm{b}} = \frac{0.5(I_{L\mathrm{bmax}}-I_\mathrm{T})V_{FD1}}{0.5I_\mathrm{T}V_{\mathrm{CEmax}}} = \frac{(I_{L\mathrm{bmax}}-I_\mathrm{T})}{I_\mathrm{T}}\frac{V_{FD1}}{V_\mathrm{out}} \tag{15}$$

where: I_T is the initial value of the tail current, t_a-t_b is the tail current duration. These parameters can be achieved by the transistor characterization.
From (13) and (15) it follows that power losses of the ASC during the turn-off process are significantly lower than the losses produced in the main IGBT transistor of the converter.
Power losses in the ASC results from periodic recharging of the capacitor C_1 and depend on its parameters (capacitance and ESR) and increase proportionally with increasing switching frequency (12). As ASC operates with a relatively low power (approx. 50W), the losses resulting from its operation are very small.

E. Power losses in the main IGBT transistor during turn-off process

From the model of hard and soft turn-off of the IGBT switch (Fig. 6), the proportion of power dissipated in the switch can be derived:

During the time period 0-t_a:

$$\left.\frac{\Delta P_\mathrm{soft}}{\Delta P_\mathrm{hard}}\right|_{0-t_\mathrm{a}} = \frac{0.5v_{\mathrm{CE}(ta)}I_\mathrm{T}}{0.5V_\mathrm{out}I_{L\mathrm{bmax}}} = \frac{(I_{L\mathrm{bmax}}-I_\mathrm{T})I_\mathrm{T}t_\mathrm{a}}{C_1V_\mathrm{out}I_{L\mathrm{bmax}}} \tag{16}$$

During the time period t_a-t_b:

$$\left.\frac{\Delta P_\mathrm{soft}}{\Delta P_\mathrm{hard}}\right|_{t_\mathrm{a}-t_\mathrm{b}} = \frac{(I_{L\mathrm{bmax}}-I_\mathrm{T})t_\mathrm{a}+0.25I_\mathrm{T}(t_\mathrm{b}-t_\mathrm{a})}{C_1V_\mathrm{out}} \tag{17}$$

During the further time of the linear v_{CE} voltage rise (t_b-t_c) (Fig. 6), power losses are not produced in the switch. From (16) and (17) it follows that in the cases of operation with a higher V_{out}, C_1 improves the power losses reduction in the soft switched boost converter with the ASC. Similarly, the application of the transistor with shorter t_a and lower I_T makes the boost converter with the ASC more efficient.
Assuming C_1=44nF, P_{out}=4.5kW, the measured (in the laboratory setup) time periods and currents are the following: t_a=240ns, t_b=430ns, I_{Lbmax}=32.8A, I_T=12.8A, which gives the power losses proportion in the transistor described by (16) and (17) is $(\Delta P_{soft}/\Delta P_{hard})$=0.41. The total power losses proportion in the experimental tests of the converters is $(\Delta P_{soft}/\Delta P_{hard})_{total}$=0.61. It is less favorable value that the theoretical as it contains other power losses in the converter. E.g. for the assumed parameters power losses in the ASC described by (12) have the value ΔP_{ASCch}=0.44W. The model equations (12) and (16) - (17) can be used for calculation of the C_1 capacitance (for selected operating point of converter)

F. Voltage gain of the converter with the ASC

Voltage gain of the boost converter with the ASC can be evaluated on the basis of the volt second equation related to the input inductor in a steady state, as presented in Fig. 7 (assuming the ideal case with voltage drops on semiconductor switches and parasitic resistances neglected):

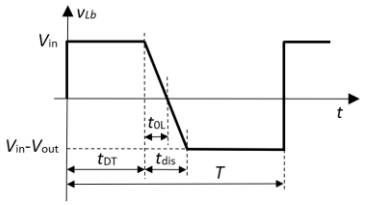


Fig. 7. The simplified voltage waveform on the input choke (L_b) in the boost converter with the ASC under the CCM operation.

$$V_\mathrm{out}\left(T-t_\mathrm{DT}-\frac{t_\mathrm{dis}}{2}-\frac{t_\mathrm{0L}}{2}\right)-V_\mathrm{in}\left(T-\frac{t_\mathrm{dis}}{2}\right)=0 \tag{18}$$

where: t_{DT} is the conducting time of the transistor T_b, t_{diss} is the interval of time when the C_1 capacitor is discharged and t_{0L} is the time required to the voltage on the inductor reaches zero.

The times associated with the C_1 capacitor discharging are:

$$t_\mathrm{0L}=\frac{C_1V_\mathrm{in}}{I_{L\mathrm{bmax}}},\ t_\mathrm{dis}=\frac{C_1V_\mathrm{out}}{I_{L\mathrm{bmax}}} \tag{19}$$

Using (19), the equation (18) is:

$$(1-D)V_\mathrm{out}-\frac{C_1f_\mathrm{sw}}{2I_{L\mathrm{bmax}}}V_\mathrm{out}^2-V_\mathrm{in}=0 \tag{20}$$

For very small value of the component $(\frac{C_1f_\mathrm{sw}}{2I_{L\mathrm{bmax}}})$ the equation (20) leads to classic voltage gain function: V_{out}/V_{in}=1/(1-D). The detailed solution of (20) shows that the voltage gain depends on the parameters I_{Lbmax}, C_1 and f_{sw} in the following way:

$$V_\mathrm{out}=\frac{I_{L\mathrm{bmax}}\left[(1-D)-\sqrt{(1-D)^2-2\frac{C_1f_\mathrm{sw}}{I_{L\mathrm{bmax}}}V_\mathrm{in}}\right]}{C_1f_\mathrm{sw}}= =\frac{1-D}{C_1f_\mathrm{sw}}I_{L\mathrm{bmax}}\left(1-\sqrt{1-\frac{2C_1f_\mathrm{sw}V_\mathrm{in}}{(1-D)^2I_{L\mathrm{bmax}}}}\right) \tag{21}$$

IV. Simulation Results

This section presents LTspice simulation results of the converters operation, mainly the comparison of the steady state operation and the switching in the boost DC-DC converter and the DC-DC boost converter with the auxiliary switching cell.

The models for the switches and diodes were obtained from the manufacturers of the components that have been used in the laboratory setup. Table II lists the basic characteristics of the passive components.

TABLE II
PARAMETERS OF THE SIMULATED CIRCUITS

Parameter	L_b	L_1	C_1	*R (windings and connections)*	C_1 *ESR*
Value	150µH	80µH	44nF	10mΩ	5mΩ

A. Operation of the converter

Fig. 7 shows waveforms of the transistor current, collector-to-emitter voltage, and power losses during the turn-off of the transistor in the boost converter with and without the ASC. Simulation test were performed for: f_{sw}=32.2kHz, P_{load}=4.5kW and C_1=44nF. From the waveforms in Fig. 8, it follows that for the circuit with the ASC less time is required for the current to decrease and that the voltage derivative is lower. These improvements result in approximately 12-fold decrease in the maximum instantaneous power as compared to the circuit without the ASC.

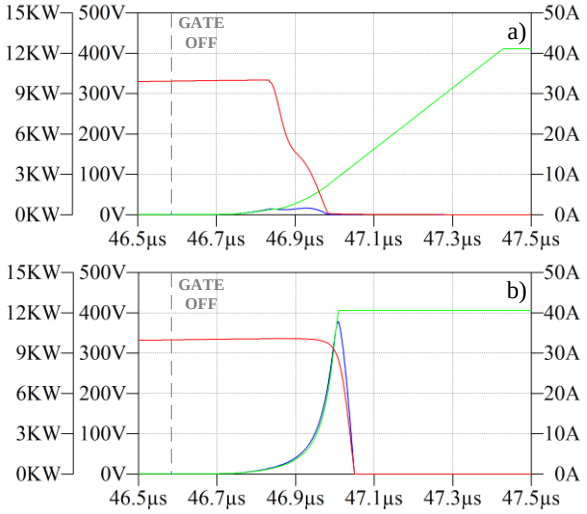


Fig. 8. Waveforms of voltage, current and power losses on the transistor during the turn off process in the: (a) – boost with A-type ASC, (b) – the classic boost converter; red – collector current i_C; green – collector emitter voltage v_{CE}; blue – transistor power losses ΔP_{off}.

B. Turn-off power losses versus C_1

To examine the effect of the capacitance value on the circuit efficiency and the losses during the transistor turn-off, a series of simulation tests was carried out for six load values. The simulation tests were performed for the switching frequency f_{sw}=32.2kHz. Characteristics shown in Fig. 9 and Fig. 10 indicate that increasing the capacitance C_1 results in a decrease in the turn-off losses of the IGBT transistor. For low power (1kW) and the capacitance of the capacitor of over 100nF, the circuit losses become higher, due to the undercharging of the capacitor, and thus failure of the ASC to operate to the full extent.

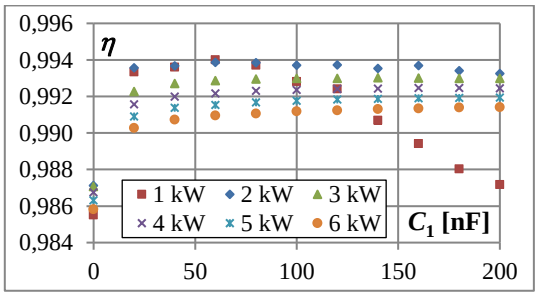


Fig. 9. Efficiency vs. C_1 capacitance for different output power levels.

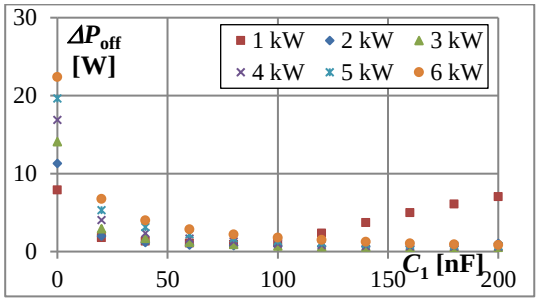


Fig. 10. Switching-off power losses vs. C_1 capacitance for different output power levels.

C. Comparison of power losses

To compare the power losses in each component, specifically the switching losses of the transistor, simulation tests of the converters with and without the ASC were performed with the circuit parameters described in *A*.

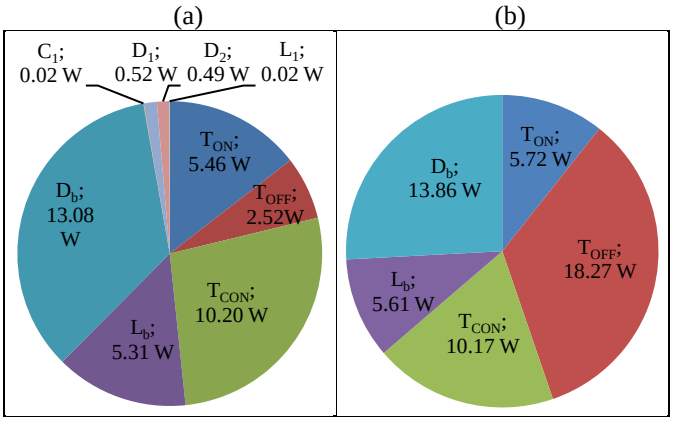


Fig. 11. Comparison of power losses in DC-DC boost converter: (a) – with A-type ASC, (b) – without the ASC. T_{CON} – conducting losses, T_{ON} – turn-on losses, T_{OFF} – turn-off losses.

Fig. 11 shows an over 7-fold decrease in the turn-off (T_{OFF}) losses of the transistor when the ASC was used, which led to a decrease in the overall losses of the circuit from 53.63W to 37.62W. Additional losses of the ASC amounted to 1.05W. Adding the ASC reduced power losses approximately by 30%.

V. EXPERIMENTAL RESULTS

A. The laboratory setup

During experimental testing, a basic boost converter was compared with the boost converter with the A-type and the B-type ASC assembled in two variants: with the capacitance of the capacitor C_1 of 44nF, and of 22nF. Inductance L_1 of the ASC was taken as 80µH. The output voltage of the circuit V_{out}=400V and the output power P_{out}=4.5kW were assumed, which, for parameters taken as listed in Table III and an input voltage V_{in}=200V, resulted in the maximum transistor current I_{max}=32.9A. Parameters of the power circuit in the boost converter were selected according to typical relationships.
According to (5) for ΔV=150V and t_{off} =t_b=200ns (Fig. 6) the capacitor of the ASC was selected as C_1=44nF. In other tests, ΔV=300V was assumed and in this case C_1=22nF was used.

For initial conditions equal to zero and no resistance of the circuit, this ensured the maximum charging time and charging current of the capacitor C_1: t_{ch}=5.9µs; I_{L1}=9.3A for 44nF and

t_{ch}=4.2μs; I_{L1}=6.6A for 22nF. The DC-DC converter operated under closed-loop control with output voltage regulation. Fig. 12 shows a photo of the setup. The Tektronix MSO 5204 oscilloscope and TPHD0200, TCP0150, CWTMini HF1B and CWTUM/06/B sensors were used for measurements.

TABLE III
BASIC PARAMETERS OF THE SYSTEM

Component	Parameters
T_b, D_b	IXGX120N60B3, SCS240KE2HR
D_1, D_2	RFN10BM6SFHTL
Passives	L_b=150uH, C_{out}=9.4uF, C_1=44nF (22nF), L_1=80uH, f_{sw}=32.2kHz

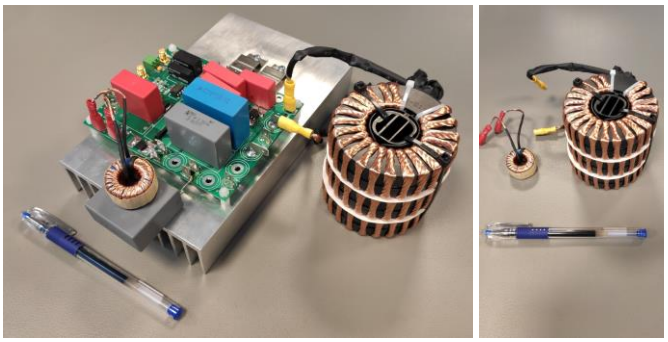


Fig. 12. The laboratory setup of the converter.

B. Results of operation and efficiency

Fig. 13 and Fig. 14 show voltage and current waveforms of the transistor T_b and the capacitor C_1 (C_1=44nF and C_1=22nF) of the DC-DC converter with the A-type and the B-type ASC operating in the continuous mode. The oscillogram was recorded for the input voltage V_{in}=200V, gain 2 (D=0.5) and the output power P_{out}=4.5kW. The switching frequency of the transistor T_b was f_{sw}=32.2kHz.

At the beginning of a period, charging of the capacitor C_1 can be observed. The charging current flows through the capacitor C_1 and the inductor L_1 and depends on the voltage and the characteristic impedance of the resonant circuit ($I_{L1\max} = V_S/\rho_{ch} = V_S\sqrt{C_1/L_1}$). The charging time was t_{ch}≈6μs, whilst the maximum charging current was I_{L1}≈6A for C_1=44nF, and t_{ch}≈4μs I_{L1}≈4A for C_1=22nF, respectively. During the turn-off of the transistor T_b, its current dropped to approximately 10A and 20A for the A-type and the B-type ASC respectively, and then decreased down to (the tail current of the IGBT) in approximately 500ns. The capacitor C_1=44nF discharged in t_{dis}≈750ns, at the maximum current of I_{C1}≈32A and equal to that of the transistor T_b at the very first moment of the turn-off. After t_{off}, the potential across the capacitor decreased by ΔV≈80V. For the capacitor C_1=22nF, after t_{off}, the discharge time was t_{dis}≈500ns and the voltage drop was ΔV≈120V. As the capacitor discharged, the collector-to-emitter voltage of the transistor T_b increased much slower and was greater than zero during the occurrence of the tail current that was small compared to the maximum value. As a result, the transistor turn-off losses in the circuit with the ASC were significantly reduced.

Fig. 15 compares the turn-off process of the transistor T_b for the basic boost converter and two boost converters with the A-type ASC: with the capacitor C_1=44nF and C_1=22nF. Presented waveforms was generated in the MATLAB software as a compilation of three recorded series of measurements under the same operating conditions (V_{in}=200V, V_{out}=400V, P_{out}=4.5kW) and oscilloscope settings.

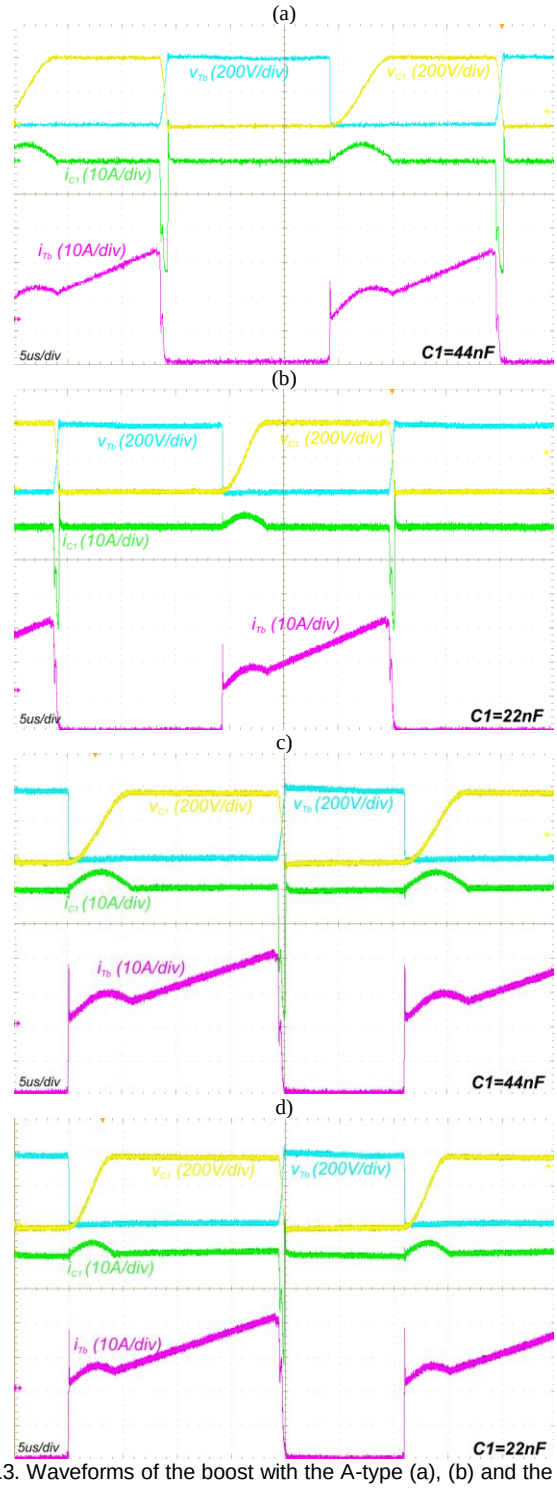


Fig. 13. Waveforms of the boost with the A-type (a), (b) and the B-type (c), (d) ASC for C_1=44nF and C_1=22nF. V_{in}=200V (A-type) and 150V (B-type) V_{out}=400V, P_{out}=4.5kW. CH1 – v_{C1}, CH2 – v_{Tb}, CH3 – i_{Tb}, CH4 – i_{C1}.

For the classic boost converter, the transistor current T_b started to decrease at its maximum voltage v_{CE}, producing turn-off losses. For the boost converter with the ASC under the same conditions, the current started to drop when the voltage v_{CE} was still zero and this voltage increased relatively slowly, resulting in lower power losses. During the turn-off, the transistor current decreased to a lower value and voltage v_{CE} across the transistor

terminals increased slower when the capacitance of the capacitor C_1 was higher.

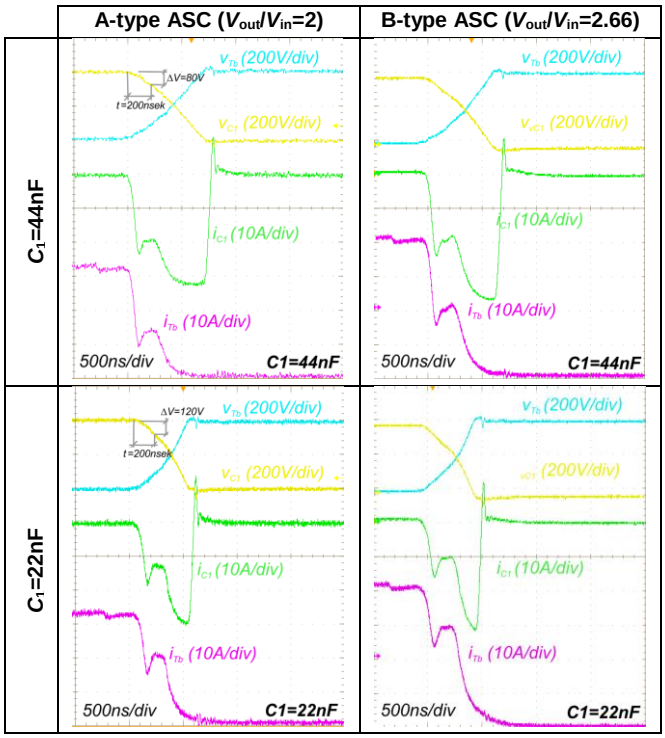


Fig. 14. Waveforms of the boost with the A-type (V_{in}=200V) and the B-type V_{in}=150V) ASC during the turn-off process for C_1=44nF and C_1=22nF, V_{out}=400V, P_{out}=4.5kW. CH1 – v_{C1}, CH2 – v_{Tb}, CH3 – i_{Tb}, CH4 – i_{C1}.

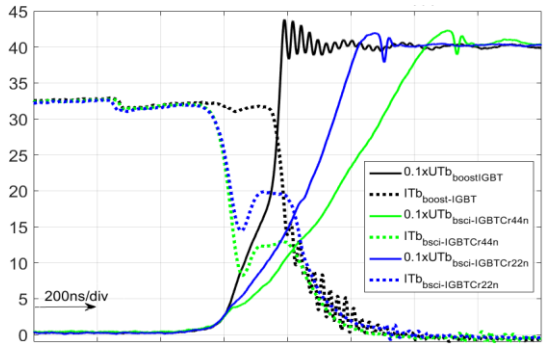


Fig. 15. Comparison of the T_b transistor voltage (v_{CE}) and current waveforms during the turn-off process: black – boost; blue – boost with A-type ASC, C_1=22nF; green – boost with A-type ASC, C_1=44nF. V_{in}=200V, V_{out}=400V, P_{out}=4.5kW.

Fig. 16 shows the voltage stresses of the components D_b, D_1, D_2 and C_1 for the boost converter with the ASC. The measurements were taken for the voltage gain of 200V/400V. The voltage of 200V occurred across the diode D_2, while 400V across the other components. Under the same conditions, the voltage stress of the transistor T_b can be seen in Fig. 13 to Fig. 15. The voltages across the components match those listed in Section III.

Fig. 17 to Fig. 19 show the results of efficiency measurements for various operating conditions of the boost converter with the A-type and the B-type ASC with the capacitor C_1=44nF and C_1=22nF compared with those for the boost converter without the ASC as well as infrared images of the circuits. The efficiency measurements were performed with the aid of the Yokogawa WT3000 precision power analyzer, and the images were captured with a FLIR SC660 camera.

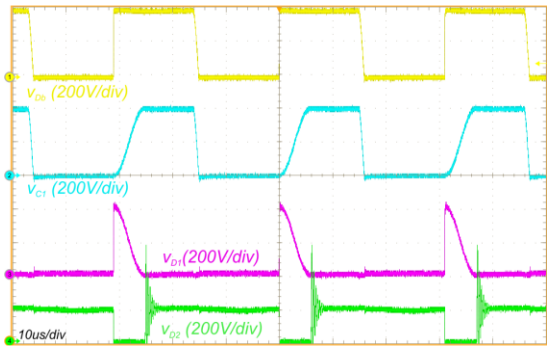


Fig. 16. Waveforms of voltage on components: D_b, D_1, D_2, C_1 in the boost with the ASC. V_{in}=200V, V_{out}=400V, P_{out}=4,5kW. CH1 – v_{Db}, CH2 – v_{C1}, CH3 – v_{D1}, CH4 – v_{D2}.

Fig. 17a presents the results of efficiency measurements of the boost converters with and without the ASC as a function of the load. The parameters of the circuits matched those listed in Table III for the voltage gain V_{in}/V_{out}=200V/400V. The efficiency of the DC-DC converter with the A-type ASC was greater than that of the boost converter without the ASC by 0.7% to 1.7% under the same load conditions. This proves the effectiveness of the ASC as a means for reducing the turn-off losses of the transistor T_b. The maximum efficiency was 97.35% for the boost converter without the ACS, 98.28% for the one with the ASC and C_1=22nF, and 98.32% for the one with the ASC and C_1=44nF.

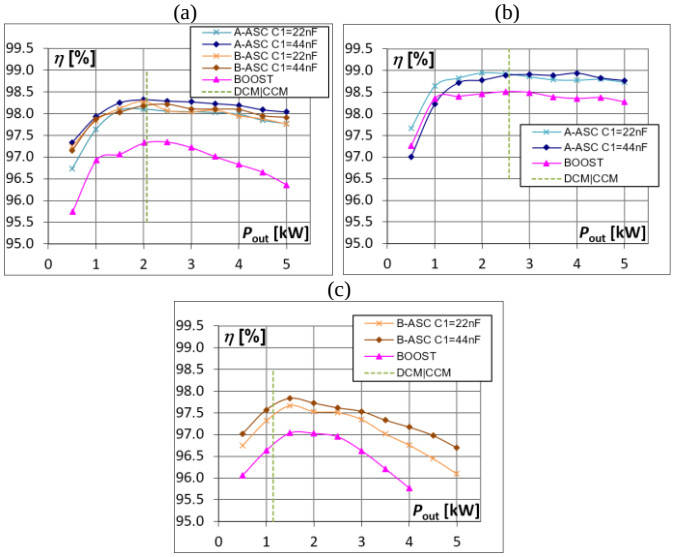


Fig. 17. Efficiency vs. output power of the boost with and without the ASC for f_{sw}=32.2kHz: V_{in}/V_{out}=200V/400V (a), V_{in}/V_{out}=300V/400V (b), V_{in}/V_{out}=150V/400V (c).

For the circuit with the voltage gain V_{in}/V_{out}=300V/400V (Fig. 17b), higher absolute efficiencies were achieved: 98.95% and 98.94% for the boost converter with the ASC and 98.51% for the one without the ASC, as well as smaller differences in efficiency: approximately 0.5% for the output power $P_{out} \geq$2.5kW. For P_{out} <1.5kW, the converter with the ASC and C_1=44nF was less efficient than the one without the ASC. For selected values of L_1 and C_1, the charging time of the capacitor C_1 was longer than the conducting time of the transistor T_b, thus making it impossible to minimize turn-off losses. Furthermore

the charging current is terminated which causes additional switching loss in T_b. This part of losses and overall losses of the ASC are insignificant in higher power but for low power can be important in the total power balance.

Fig. 17c presents the results of efficiency measurements of the boost converters without and with the B-type ASC for the voltage gain V_{in}/V_{out}=150V/400V. The efficiency of the DC-DC converter with the B-type ASC was greater than that of the boost converter without the ASC by 0.5% to 1.4% under the same load conditions. Due to a high temperature of the transistor T_b, measurements of the boost converter were performed up to P_{out}=4.0kW.

Fig. 18 shows temperature distributions of the basic boost converter and a converter with the ASC and C_1=44nF, drawn when the measurements were recorded for the diagram shown in Fig. 17a for the output power of 4.5kW. Temperatures in specific points are highlighted, including transistor T_b, diode D_b, diode D_1, and diode D_2. Temperatures of the transistor T_b in both converters differed by 30^{O}C.

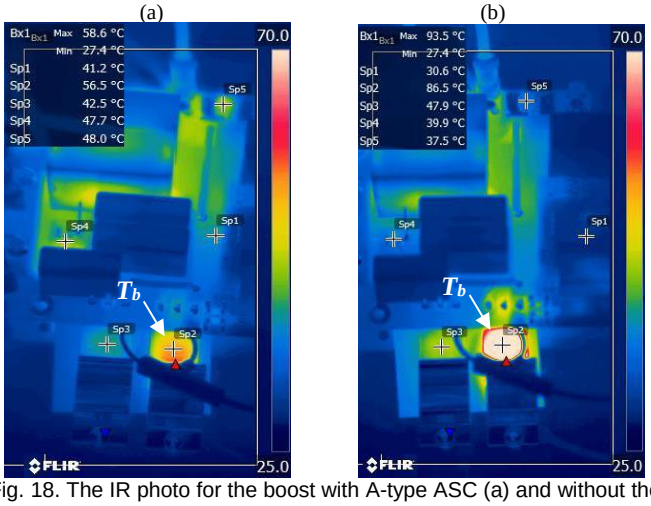


Fig. 18. The IR photo for the boost with A-type ASC (a) and without the ASC (b). P_{out}=4.5kW; f_{sw}=32.2kHz; V_{in}=200V; V_{out}=400V; C_1=44nF. Sp2 – transistor T_b, Sp3 – diode D_b, Sp4 – diode D_1, Sp5 – diode D_2

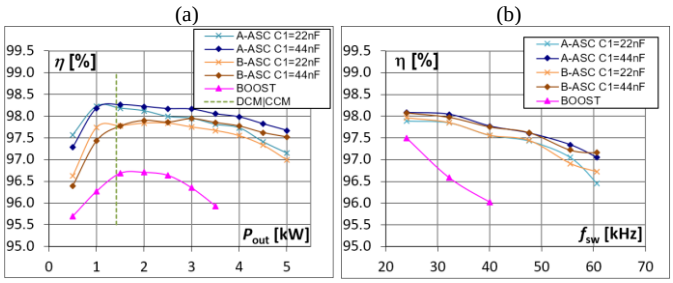


Fig. 19. Efficiency vs. output power for f_{sw}=48.7kHz (a) and vs. switching frequency for P_{out}=4.5kW (b). Various configurations of the converter and the ASC, V_{in}=200V for A-type ASC; V_{in}=150V for B-type ASC; V_{out}=400V.

The results of circuit efficiency measurements for the transistor switching frequency increased to f_{sw}=48.7kHz and voltage gain V_{in}/V_{out}=200V/400V are shown in Fig. 19a. The maximum efficiencies were lower than in the previous cases, whilst the differences were greater for higher values of the output power. Measurements were performed up to P_{out}=3.5kW due to a high temperature of the transistor T_b (about 100 ^{O}C).

Fig. 19b presents the results of the converters efficiency measurements as a function of the transistor switching frequency f_{sw}, for the output power P_{out}=4.5kW and the voltage gain V_{in}/V_{out}=200V/400V. As the frequency increased, switching losses of the boost converter transistor became higher, which led to a drop in the efficiency. Due to a high temperature of the transistor, measurements of the boost converter were performed up to the frequency f_{sw}=40 kHz. The difference between the efficiencies of the converters was significantly larger for higher frequencies, which indicates that the ASC is effective. The efficiency measurements prove that the boost converter equipped with the ASC, which minimizes turn-off losses of the transistor, can operate with a higher load at a higher switching frequency than the basic boost converter. This has additional benefits, such as minimizing the passive components of the circuit and the cost reduction.

VI. Conclusions

The concept of soft switching boost converters that are presented in the paper allows for significant improvement of the efficiency of IGBT-based DC-DC boost converters that leads to a reduction of losses associated with the transistor turn-off process by utilizing an auxiliary snubber composed of diodes and passive components. From the comparison of the results obtained for the classic IGBT-based boost converter and the converter with the ASC it follows that:

- Peak efficiency achieved by a DC-DC boost converter with the ASC is approximately 1% higher.
- An improvement of efficiency of the boost converter with the ASC is greater for higher values of the output power.
- The boost converter with the ASC is better suited for operation with a higher switching frequency. In the tests presented in this paper, it achieved nearly 98% of peak efficiency at the switching frequency of 48.7kHz.
- The boost converter with the ASC can operate with a higher switching frequency and enables cost reduction by minimizing volume of passive components: L_b, C_{in}, and C_{out}.

The proposed concepts allows for important efficiency improvement. Furthermore, it has favorable topology in comparison to existing solutions, which is summarized in Table IV.

TABLE IV
COMPARISON AMONG THE PROPOSED CONVERTERS WITH OTHER CONCEPTS

Converter	Efficiency [%]	Parameters of experiments			Number of auxiliary components			
		V_{out}/V_{in}	P_{out} [kW]	f_{sw} [kHz]	Switch	Diode	C	L
Refs. [10], [11]	96.23	2.67	0.6	30	1	2	2	2
Ref. [12]	93.9	-	0.3	20	1	4	2	2
Ref. [13]	>98	1.07	1.2	80	1	1	2	1
Ref. [14]	98	1.29	1	100	1	4	2	2
Ref. [16]	≈96.5	1.6	≈2	30	2	2	1	0
Ref. [18]	96	2	0.2	100	0	4	1	3
Ref. [19]	≈97	1.5	0.3	180	0	2	2	1
Ref. [20]	97	2	≈0.1	100	0	3	1	3
Proposed A-type	98.95	1.33	2	32.2	0	2	1	1
Proposed B-type	98.28	2	2	32.2	1	3	1	1

References

[1] F. L. Tofoli, D. d. C. Pereira, W. Josias de Paula and D. d. S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up dc–dc topologies based on the

boost converter," *IET Power Electronics*, vol. 8, DOI: 10.1049/iet-pel.2014.0605., no. 10, pp. 2044-2057, October 2015.
[2] S. Hazra *et al*., "High Switching Performance of 1700-V, 50-A SiC Power MOSFET Over Si IGBT/BiMOSFET for Advanced Power Conversion Applications," *IEEE Transactions on Power Electronics*, vol. 31, . DOI: 10.1109/TPEL.2015.2432012, no. 7, pp. 4742-4754, July 2016.
[3] G. R. Chandra Mouli, J. H. Schijffelen, P. Bauer and M. Zeman, "Design and Comparison of a 10-kW Interleaved Boost Converter for PV Application Using Si and SiC Devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, DOI: 10.1109/JESTPE.2016.2601165, no. 2, pp. 610-623,June 2017.
[4] D. W. Berning and A. R. Hefner, "IGBT model validation for soft-switching applications," *IEEE Transactions on Industry Applications*, vol. 37, DOI: 10.1109/28.913733, no. 2, pp. 650-660, March-April 2001.
[5] E. Ogawa, Y. Onozawa and R. W. De Doncker, "Investigation of Switching Behavior of an IGBT under Soft Turn-off in Application for Dual-Active Bridge Converters," *2018 Int. Power Electron. Conf. (IPEC-Niigata 2018-CCE Asia)*, Niigata, 2018, pp. 2768-2773. DOI: 10.23919/IPEC.2018.8507434
[6] S. Ryu et al., "Ultra high voltage IGBTs in 4H-SiC," *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, Columbus, OH, 2013, DOI: 10.1109/WiPDA.2013.6695557, pp. 36-39.
[7] A. Kadavelugu, S. Bhattacharya, S. Ryu, E. Van Brunt, D. Grider and S. Leslie, "Experimental switching frequency limits of 15 kV SiC N-IGBT module," in *2014 Int. Power Electron. Conf. (IPEC-Hiroshima 2014 - ECCE ASIA)*, DOI: 10.1109/IPEC.2014.6870034, pp. 3726-3733, Hiroshima, 2014.
[8] D. Gerber and J. Biela, "Interleaving of a Soft-Switching Boost Converter Operated in Boundary Conduction Mode," *IEEE Trans. on Plasma Science*, vol. 43, DOI: 10.1109/TPS.2015.2422476 no. 10, pp. 3374-3380, Oct. 2015.
[9] A. Van den Bossche, V. Valtchev, J. Ghijselen and J. Melkebeek, "Soft-switching boost converter for medium power applications," *in 1998 International Conference on Power Electronic Drives and Energy Systems for Industrial Growth, 1998. Proceedings.*, Vol. 2. DOI: 10.1109/PEDES.1998.1330739, pp. 1007-1012, Perth, WA, Australia, 1998.
[10] S. Park, S. Park, J. Yu, Y. Jung and C. Won, "Analysis and Design of a Soft-Switching Boost Converter With an HI-Bridge Auxiliary Resonant Circuit," *IEEE Transactions on Power Electronics*, vol. 25, DOI: 10.1109/TPEL.2010.2046425, no. 8, pp. 2142-2149, Aug. 2010.
[11] S. Park, G. Cha, Y. Jung and C. Won, "Design and Application for PV Generation System Using a Soft-Switching Boost Converter With SARC", *IEEE Transactions on Industrial Electronics*, vol. 57, DOI: 10.1109/TIE.2009.2036025, no. 2, pp. 515-522, Feb. 2010.
[12] Wei Qian, Xi Zhang and Zhe Li, "Design and operation analysis of a novel coupled-inductor based soft switching boost converter with an auxiliary switch," in *2016 IEEE 8th Int. Power Electron. and Motion Control Conf. (IPEMC-ECCE Asia)*, DOI: 10.1109/IPEMC.2016.7512697, pp. 2534-2537, Hefei, 2016.
[13] Yungtaek Jang and M. M. Jovanovic, "A new, soft-switched, high-power-factor boost converter with IGBTs," *IEEE Trans. on Power Electronics*, vol. 17, DOI: 10.1109/TPEL.2002.801002, no. 4, pp. 469-476, July 2002.
[14] S. Cetin, "Power-Factor-Corrected and Fully Soft-Switched PWM Boost Converter," *IEEE Transactions on Industry Applications*, vol. 54, DOI: 10.1109/TIA.2018.2821101 no. 4, pp. 3508-3517, July-Aug. 2018.
[15] B. Wang, T. Q. Zheng and J. Zhang, "Voltage controlled variable capacitor based snubber for the further reduction of IGBT's turn-off loss," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, 2014, DOI: 10.1109/ECCE.2014.6953499, pp. 935-940.
[16] J. Bauman and M. Kazerani, "A Novel Capacitor-Switched Regenerative Snubber for DC/DC Boost Converters," *IEEE Trans. on Industrial Electron.*, vol. 58, DOI: 10.1109/TIE.2010.2046576, no. 2, pp. 514-523, Feb. 2011.
[17] T. Mishima, Y. Takeuchi and M. Nakaoka, "Analysis, Design, and Performance Evaluations of an Edge-Resonant Switched Capacitor Cell-Assisted Soft-Switching PWM Boost DC–DC Converter and Its Interleaved Topology," *IEEE Transactions on Power Electronics*, vol. 28, DOI: 10.1109/TPEL.2012.2227504, no. 7, pp. 3363-3378, July 2013.
[18] M. Mohammadi, E. Adib and M. R. Yazdani, "Family of Soft-Switching Single-Switch PWM Converters With Lossless Passive Snubber," *IEEE Transactions on Industrial Electronics*, vol. 62, DOI: 10.1109/TIE.2014.2371436 no. 6, pp. 3473-3481, June 2015.
[19] H. Choe, Y. Chung, C. Sung, J. Yun and B. Kang, "Passive Snubber for Reducing Switching-Power Losses of an IGBT in a DC–DC Boost Converter," in *IEEE Transactions on Power Electronics*, vol. 29, DOI: 10.1109/TPEL.2014.2304551, no. 12, pp. 6332-6341, Dec. 2014.
[20] J. A. Lambert, J. B. Vieira, L. Carlos de Freitas, L. dos Reis Barbosa and V. J. Farias, "A boost PWM soft-single-switched converter with low voltage and current stresses," *IEEE Transactions on Power Electronics*, vol. 13, DOI: 10.1109/63.654956 no. 1, pp. 26-35, Jan. 1998.
[21] M. W. Gekeler, "Soft switching three level inverter with passive snubber circuit (S3L inverter)," in *Proceedings of the 2011 14th European Conf. on Power Electronics and Applications*, Birmingham, 2011, pp. 1-10.
[22] M. W. Gekeler, "Soft switching three level inverter (S3L inverter)," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, DOI: 10.1109/EPE.2013.6631756, , pp. 1-10, Lille, 2013.
[23] P. Wen, X. Yang, T. Q. Zheng, T. Fujihira and S. Igarashi, "The Soft-Switching Technique for RB-IGBT based T-Type Three-Level Inverter," in *2018 IEEE Int. Power Electronics and Application Conf. and Exposition (PEAC)*, DOI: 10.1109/PEAC.2018.8590643, pp. 1-6, Shenzhen, 2018.
[24] R. Stala, A. Penczek, A. Mondzik, S. Szot, M. Szarek, M. S. Ryłko, "Hochsetzsteller, entsprechender Wechselrichter und Verfahren zur Verminderung von Ausschaltverlusten", DE 102014119015B4, Published: 2016-12-01.
[25] R. Stala, A. Penczek, A. Mondzik, S. Szot, M. Szarek, M. S. Ryłko, "Voltage Increasing Converter, Appropriate Inverter And Method For Reducing The Trip-out Losses", PL 225731B1 Published: May 31, 2017.
[26] M. Willenberg, R. Knoke, A. Falk, R. Stala, M. Ryłko, J. Masłoń, A. Mondzik, S. Szot, A. Penczek, M. Szarek, "Step-up converter, corresponding inverter and method of operation", US 10491103 B2, Published: 2019-11-26.

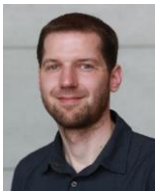
Andrzej Mondzik received the M.S. and Ph.D. degrees in electrical engineering from AGH University of Science and Technology, Krakow, Poland, in 1997 and 2005, respectively. He is currently an Assistant Professor at AGH UST. His research interests include power electronic converters (mainly dc–dc and resonant converters), active filtering and reactive power compensation.

Robert Stala received the M.S., Ph.D., and Habilitation degrees in electrical engineering from the AGH University of Science and Technology, Krakow, Poland, in 1998, 2003, and 2011, respectively. He is currently an Associate Professor at AGH UST. His research interests include power electronic converters, DC-DC, DC-AC, multilevel, and resonant converters, FPGA control and cosimulation, photovoltaic systems, electronic ballasts, and LED lighting.

Stanislaw Pirog (M'94) received the M.Sc., Ph.D., and Dr. Habilitation degrees in electrical engineering from AGH University of Science and Technology, Krakow, Poland, in 1972, 1977, and 1990, respectively. He is currently a Professor at AGH UST. His current research interests include power electronics, electrical power quality, and permanent-magnet motor drives. Prof. Pirog is a member of the Committee on Electrical Engineering, Polish Academy of Sciences.

Adam Penczek received the M.Sc. Eng., Ph.D. and Ph.D. DSc. degrees in electrical engineering from the AGH University of Science and Technology, Krakow, Poland, in 1998, 2003 and 2019, respectively. He is currently an Associate Professor at AGH UST. In 2008, he joined the Research Staff of DTW sp. z o.o., (currently SMA-Magnetics). His main research interests include power electronics (mainly dc-dc and dc-ac converters), and FPGA-based control systems.

Piotr Gucwa recieved the B.S degree in electrical engineering from the AGH University of Science and Technology, Cracow in 2020. His interest include DC-DC power electronics converters and computer simulation.



Miłosz Szarek received the M.S. and Ph.D. degrees in electrical engineering at AGH University of Science and Technology, Kraków, Poland, in 2008 and 2017 respectively. He is currently Head of Power Electronics Development in SMA Magnetics Sp. z o. o. (Group of SMA Solar Technology AG). His research interests relate to all aspects of power electronics, especially grid-tied solar inverters, DC-DC converters, control systems and component level reliability.