Proceedings of the Fifth International Conference on Electronics, Communication and Aerospace Technology (ICECA 2021)
IEEE Xplore Part Number: CFP21J88-ART; ISBN: 978-1-6654-3524-6

Challenges in Low Power VLSI Design: A Review

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2021 5th International Conference on Electronics, Communication and Aerospace Technology (ICECA) | 978-1-6654-3524-6/21/$31.00 ©2021 IEEE | DOI: 10.1109/ICECA52323.2021.9676055

Abstract—**The need for decreasing the standby power in battery aided devices is the main design objective for very large-scale integration (VLSI) engineers. Many leakage controlling techniques have been designed so far each with its pros and cons. The focus of this paper is on the comparative study of the current best domino logic methods using FinFETs. The unity noise gain for SCDNDTDL is 3.77X higher than the SG FinFET logic. This paper will help the researchers to get a technical hunch of choosing a technique over another.**

Keywords—FinFETs, Threshold voltage, Subthreshold Conduction, FinFETs, Leakage Control Transistor (LCT), power delay product.

I. INTRODUCTION

Following the Moore's law, technology has scaled down very rapidly in the past few decades to account for higher packaging density ICs. Portable devices can't merely rely on batteries as there has not been any revolutionary improvement in modern battery life until now. Constant field scaling is usually employed where the critical dimensions of transistors along with the power supply voltage are scaled down. With the relentless scaling down of technology node the cost associated with cooling of these chips is sky high. So, the techniques to reduce the static leakage power at almost all levels of abstraction especially at circuit level are the need of the hour.

Power dissipation in MOSFETs has dynamic and static components. The static power dissipation overweighs the dynamic power dissipation at lower technological nodes. The major component of static power leakage is subthreshold conduction. Subthreshold current is the current which flows when the MOSFET has not completely turned ON. It flows even when the input voltage is below the threshold voltage. Due to the square dependence of switching power dissipation with VDD the scaling down of VDD proved very effective in curbing the power dissipation [1]. To counter the speed degradation due to scaling of VDD, the threshold voltage (Vth) is also scaled down by the same factor as the VDD. The reduction of propagation delay due to the scaling of Vth is pronounced at lower power supply voltages [2]. The increase in sub-threshold current along with the reduction in noise margins puts a limitation against the reduction in Vth. Leakage due to the subthreshold conduction becomes a significant part of total power consumption when Vth voltage becomes less than 0.2V [3].

The techniques used to achieve low power and high-speed are implemented at various levels of abstraction from device to circuit to algorithm level. Device features like Vth, device sizes and interconnect properties are modeled to lower the power consumption. The proper choice of circuit design style, clocking strategies and reduction of voltage swing are the measures applied at circuit level to reduce power dissipation [4]. The measures adopted at architecture level include the utilization of pipelining and parallelism, proper design of bus structures and power management of various system blocks.

With the aim of decreasing the power dissipation along with improving the delay of VLSI circuits, scientists have scaled down the channel length of MOSFET transistors to 7 nm [5]. The main challenges which the researchers face while scaling down the transistors are the sources of leakage in MOSFETS like subthreshold leakage, Drain Induced Barrier Induced Drain Lowering, Reverse Bias PN Junction leakage and so on [6]. With a view to improve the subthreshold slope, reduce the leakage currents and improve the power efficiency, FinFETs are now replacing MOSFETs as the later provide a much better cover over the entire channel by covering it on all sides.

The dynamic logic in VLSI had a severe issue in cascading several stages. So, the domino logic replaced the dynamic logic. Domino logic is a modification of dynamic logic. The dynamic logic differs from the static logic as in former the logic is implemented using clock. In domino logic the problem of cascading of logic blocks is removed. The additional advantage of static inverter in domino logic is increase in noise immunity of the circuits due the use of static inverter at the output.

The paper is divided in the following parts: Part II discussed the previous related work in the field of low power VLSI design. The comparison analysis of different low power techniques is provided in part III. Paper is concluded in section IV.

II. LITERATURE REVIEW

Different researchers had proposed different methodologies for reducing the power dissipation and managing the balance between the tradeoff parameters for domino logic circuits. The important methods are discussed here.

A. Footer-less Domino logic(FLDL)

Domino logic is replacing the dynamic logic due to its lesser power and area requirements. In this logic style one PMOS transistor is used as a Pull-up Network (PUN). When clock is set low in FLDL dynamic node is pulled to a high voltage through pre-charge transistor MP1 because of which

the inverter drives the output to low logic. Mp2 turns ON during pre-charge phase, the dynamic node remains at logic high. When clock is at logic high MP1 is OFF and state of MP2 is decided by the output of domino logic. So, output changes as an input combination are applied to the pull-down network leading to charge at output capacitances to be shared between the transistor and Junction Capacitance. So, a Keeper transistor needs to be introduced whose gate is fed by the output of domino logic [7]. The schematic diagram of footer-less domino logic (FLDL) OR gate is shown in Fig 1.

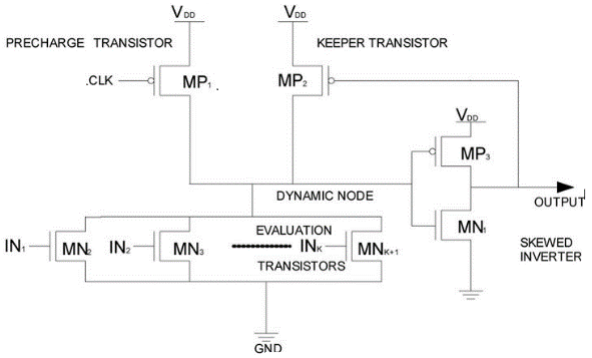

Fig. 1. Footer-less Domino logic OR gate

This keeper transistor is put in parallel with the pre-charge transistor. Keeper improves Robustness of this circuit by preventing the leakage and charge sharing at the dynamic node. In evaluation phase the leakage current through PDN is a disadvantage in FLDL.

B. Series Connected Dynamic Node Driven Transistor Domino Loic (SCDNDTDL)

One of the logics with improved performance characteristics in contrast to conventional domino logic is SCDNDTDL. The circuits simulated using SCDNDTDL have two operating modes-SG (Short gate) and LP (Low power) [8]. The two gates of FinFET are kept at same potential in SG mode so the FinFET attains better hold over the channel as the gate shields the channel on three sides. In SG FinFETs gates at same voltage lead to to reduction of delay and in LP mode the back gate is fed by different voltages in *n* channel and *p* channel FinFETs. SCNDTDL technique which utilizes FinFETs in SG mode realizing an OR gate is shown in FIG 2. The evaluation transistors MNE1 to MNEn are shown separately and realize an OR gate. The keeper transistor also acts as a feedback transistor here and is fed by the output voltage.

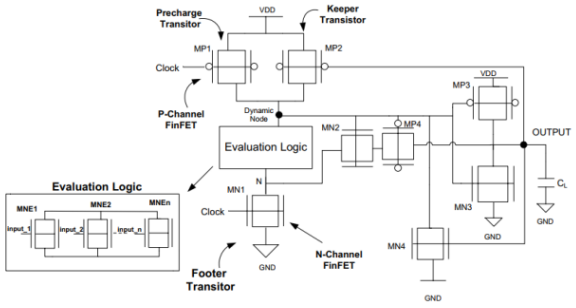

Fig. 2. SCNTDTL in Short Gate mode

In the *pre-charge* phase of circuit, the output high voltage turns the keeper MP2 ON which keeps the dynamic node at high voltage to prevent the discharge of that node. Also, MN1 is low reducing the power dissipation in evaluation phase due to stacking. MN4 keeps the voltage at the dynamic node as desired, by the acting as feedback. MP4 comes in the middle of path between the dynamic node and ground providing a high OFF state resistance.

In *evaluation* phase MN1 turns ON and MP1 turns OFF as the clock is high and if any of the inputs is high, it turns ON the corresponding n-FinFET through which the dynamic node is discharged to ground and output is pulled to high which is the OR gate logic. Further to prevent leakage through transistor MN2, MP2 is connected to MP4 so that MP4 is ON and MN2 is OFF when the dynamic node is at logic low. So, MP4 again furnishes a high OFF state resistance path of node N and output.

The clock is high in evaluation mode but low in pre-charge phase. Inputs does not affect the output as the footer transistor is not ON during the pre-charge phase. When any of the input's switches to logic high during evaluation mode output of the circuit is high because MN1 is ON during this phase.

C. FinFET domino logic with independent gate keepers(FDLIGK)

Short channel effects lead to rise in subthreshold leakage due to single gate MOSFETs. So, two electrically coupled gates giving a very good control on thin silicon body are used as Double-Gate FinFET to reduce the leakage effects. The contention current in this logic is reduced as the threshold voltage of keeper transistor keeps changing during the circuit operation. In this logic when clock is low, PDN is in cutoff during the pre-charge phase. One gate of keeper transistor is disabled when the keeper control signal is pulled up to VDD. The discharging of output node activates the other gate of keeper. The high threshold voltage keeper is active in a single gate mode. When the clock goes high evaluation mode begins. The contention current in the evaluation mode is significantly reduced as the keeper threshold is improved by the single-gate bias. Lower contention current in the keeper transistor reduces the short circuit power dissipation and increases the speed. Keeper is in cutoff as the output node charges to VDD.[9] If for some input combination the PDN is not switched ON, the dynamic node remains at high potential in the evaluation mode. After some time, the keeper control signal discharges to ground. The dynamic node is retaining the active high logic as the both the gates of keeper are fully turned ON. The non-inverted delay elements consist of cascaded transmission gates as shown in Fig 3.

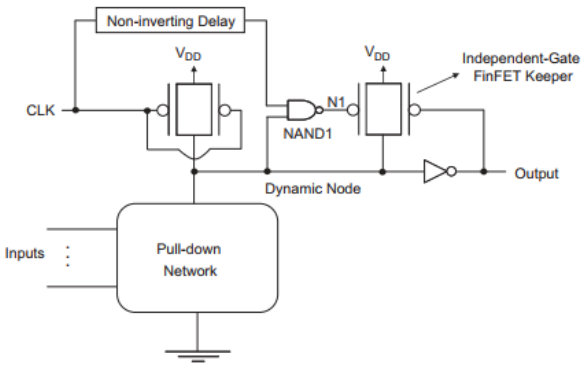

Fig. 3. Variable threshold voltage keeper independent-gate FinFET domino logic circuit technique

The delay of delay element and NAND gate determines that the delay equals to delay during evaluation mode of domino gate as it determines the number of stages of the delay circuit. So, after the beginning of an evaluation or a pre-charge mode this technique vigorously alters the threshold voltage of the keeper transistor after a specific delay by independently biasing the multiple gates of keeper transistor.

D. Multi-threshold technique (MTCMOS) technique

In this technique a Sleep transistor is formed by inserting a low threshold transistor in series with a high threshold transistor. Transistors connected to power lines are high V_{th} and transistors in the evaluation network are low V_{th} as shown in Fig 4.

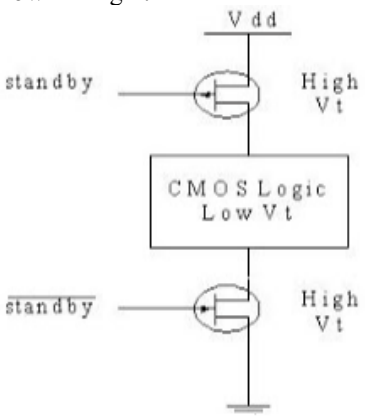

Fig. 4. MTCMOS Logic

For efficient power management active and sleep modes exist in these MTCOMS circuits. In the Sleep mode the sleep transistors are ON and come into the path between the evaluation network and power supply which reduces the subthreshold conduction. In the active mode Sleep transistors are OFF cutting off the main circuitry from VDD reducing the standby current [10]. Low Vth devices are used in evaluation network as fast switching is important and high Vth devices are used between real power rails and virtual power rails to reduce the static power dissipation.

E. ONOFIC Logic

In this technique the leakage current is minimized by the insertion of an extra logic block called ONOFIC between PUN and PDN. In this block the NMOS and a PMOS transistors are so connected that the gate of NMOS is shorted to the drain of PMOS and the gate of PMOS remains at the output node [11]. The source of NMOS and PMOS is at ground and VDD respectively as shown in Fig 5.

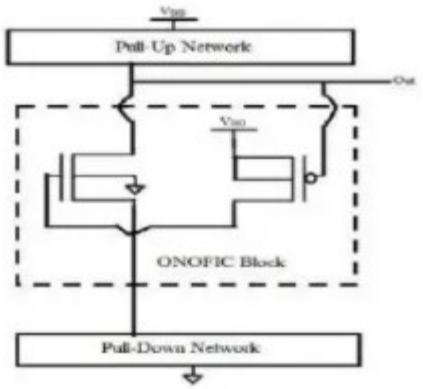

Fig. 5. ONOFIC Logic

This block remains in OFF state when both transistors are OFF and turns ON when both transistors are in linear region. So, the concept of stacking is exploited in this block to provide precise control of leakage current by varying the resistances when in OFF and ON state respectively.

F. Leakage Control Transistor (LECTOR) with footed diode Inverter in Domino Circuits

In this logic stacking from the path between VDD to ground is efficiently used for the reduction of leakage power. The concept of stacking is that if in a circuit there is only one transistor OFF leaks more power than the circuit in which there are multiple transistors in OFF state in the path between VDD to ground [12], [13].

The Lector Stacking is shown in FIG 6. In this circuit MP2 and MN2 are the leakage control transistors (LCTs) which lie in the path of pre-charge and evaluation networks. The sources of these transistors control their gates[13]. The common connection of drains of MN2 and MP4 form the input to the Inverter. One of the LCTs will operate in its near cut-off range for any pair of inputs in the PDN which opposes the current flow between VDD and ground leading to leakage power reduction.

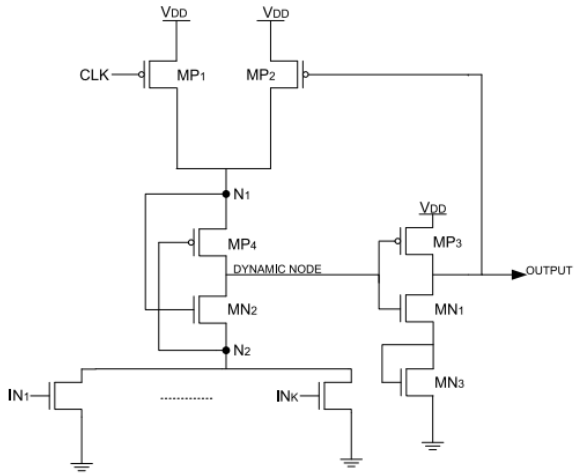

Fig.6. LECTOR with Footed Diode Inverter Domino logic OR gate

While pre-charging the dynamic node is pre-charged to VDD through MP4 and MP1 when the clock is low. This pre-charge is independent of previous input clock state. MP4 offers a low leakage path as node N2 will be at zero potential if the inputs are low before the clock is low. The logic level at N2 is not sufficiently high to fully turn OFF

MP4. Due to less than OFF resistance of MP4 the dynamic node is charged to a high voltage. So, the output during pre-charge phase is independent of the inputs applied.

In the evaluation phase the clock turns high and the dynamic node will be at a potential determined by the input combinations. The dynamic node is not discharged when all the inputs are low so MP2 turns ON as it is connected to the output of inverter. As MP2 is on voltage at N1 is high which turns ON MN2 but voltage at N2 is not high enough to completely cut-off MP4 thus any subthreshold leakage current in the path between the power supply and ground faces the high resistance of MP4. Dynamic node is discharged when all inputs are high, so the output of inverter is high which turns OFF MP2 which in turn turns MN2 OFF, again offering a high resistance path. So, the introduction of LCTs has increased the resistance between the high (VDD) and low(ground) power supply. hence decreased the static power dissipation but at the same time increased the delay which can be taken care of by proper sizing of LCTs. In the footed diode configuration below transistor MN1, another transistor can be added in series which will further reduce the OFF-state leakage currents by stacking.

G. Leakage Control NMOS Transistor(LCNT) Logic

In this technique two NMOS leakage control transistors LCT1 and LCT2 are kept between PUN and PDN. Gates of both the transistors are connected to output node NP as shown in Fig 7. With inputs In1 In2 are 00 output is pulled to VDD which turns ON LCT1 and LCT2 and there is a 2 Vt drop which causes a reduced voltage from output node to ground path. Also, the OFF transistors in PDN offer more resistance hence low leakage current [14]. When the inputs AB are 10 or 01, it turns OFF one PMOS in PUN and one NMOS in PDN. When inputs are AB=11, both the NMOS transistors are turned ON in PDN and both the PMOS transistors are turned OFF in PUN. So, both the LCTs enter into cut-off region forming a stack presenting an elevated resistance to any static current from PUN to PDN.

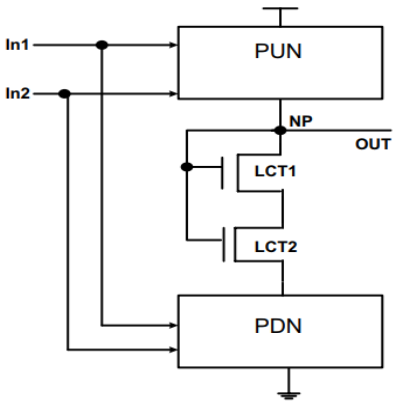

Fig. 7. LCNT Logic

III. SIMULATION STUDY AND ANALYSIS

Table1: comparison of some important parameters studied in these techniques with respect to FLDL technique

Technique	ONOFIC	SCDNDTDL	LCNT	LECTOR	MTCMOS	FDLIGK	FLDL
Technology Node (Nm)	32	32	32	45	32	32	45s
Simulated Circuit	NAND 2	OR2	NAND2	OR2	NAND2	0R16	OR2
Power Dissipation(nW)	13.351	221.2	6.98	__	0.94	__	3200
Propagation Delay (ps)	350.06	16.75	1910	__	278.5	__	23.9
No. Of Transistors	6	16	6	9	6	__	6
Power Delay Product (aJ)	4.674	3.70	0.14	__	0.261	__	76.48
Power Supply (V)	1	0.9	0.8	1	1.1	__	1

In footer-less domino logic there is a reduction of one transistor in PDN which improves the delay as well as static power dissipation. PMOS keeper transistor restores the voltage at dynamic node which improves the cascading capabilities of the logic. In the evaluation logic when the input combination is all zeros the leakage current face a low resistance path through PDN which is a disadvantage.

In SCDNDTDL leakage currents are reduced by the use of MN1 and the series pair of MN2-MP4 which improves the noise immunity of the logic. The transistor MN4 which is driven by output reduces the leakage current in the middle of dynamic node and ground in both pre-charge and evaluation phases. The circuits simulated using SCDNDTDL show a power reduction of 73.16% as compared to conditional stacked keeper domino logic (CSK-DL) in SG mode and a delay reduction of 36.36% as compared to voltage comparison-based domino logic (VCD) in SG mode. A 16-input OR gate simulated using SCDNDTDL logic shows a 68.47% reduction in power consumption as compared to conventional CMOS. The Unity Noise Gain of the circuit simulated using SCDNDTDL logic is 3.77 times higher than the previous techniques in FinFET SG mode. FDLIGK changes the V_{th} of keeper dynamically with a certain delay after the beginning of each phase as the logic independently biases the multiple gates of keeper transistor. This decreases the keeper contention current and makes the logic more prone to noise as with respect to standard tied gate FinFET logic circuit.

In ONOFIC there is an improvement of delay and power dissipation of inverter by 51.64% and 25.9% respectively when compared to the Complementary Metal Oxide Semiconductor (CMOS) inverter. In LCNT there is a 48.4% leakage reduction as compared to CMOS. In LECTOR the insertion of an extra transistor MN3 in the diode footed configuration below MN1 produces stacking in the inverter which reduces the subthreshold current. LCNT logic passes good 1 but in ONOFIC logic 0 is better as compared to LCNT logic. In 16-input footer-less domino OR gate there is 70% enhancement of Low Noise Margin with keeper sizing accompanied with decrease in speed and increase in power

dissipation due to its high contention current. In FDLIGK the control of contention current is achieved by varying the threshold voltage of keeper with the circuit operation. The dynamic variation of threshold voltage leads to the decrease in noise immunity in FDLIGK logic in comparison to standard tied gate FinFET domino logic. In FDLIGK there is 49% and 46% improvement in delay and power dissipation with respect to tied gate FinFET domino logic at 32 nm without immolating the noise immunity of the logic.

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IV. CONCLUSION

In this paper the standby component of leakage current in MOSFETS and some of their leakage reduction techniques has been discussed which can be used as domino logic. To obtain an optimal trade-off between static power dissipation and delay of the circuit is a design challenge. The 2 input OR gate implemented using domino logic SCDNDTDL technique showed a power minimization of 73.16% and delay reduction of 36.36% in comparison to CSK-DL logic. Transistor count in SCDNDTDL puts a burden on area requirements but at the same time reduces the propagation delay in comparison to all other techniques discussed. which simulated OR2 gate at 32 nm. The active power dissipation in two input OR gate simulated using LECTOR with footed diode inverter domino logic decreases by 13.66% with respect to standard footer-less domino circuits.

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