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Control of transformerless T-type DVR using multiple delayed signal cancellation PLL under unbalanced and distorted grid condition

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ABSTRACT

In the near future, the power system network may experience severe voltage distortions due to association of renewable energy sources (RES), and the large penetration of power electronic based loads into the microgrid. To protect sensitive loads from these distorted and unbalanced grid conditions, the commonly used dynamic voltage restorer (DVR) requires effective control algorithms. The effective control algorithm comprises a controller, and accurate estimation of grid phase angle/frequency, and magnitude, thereby the reference DVR voltage is accurately estimated. The synchronous reference frame based phased locked loop (SRF-PLL) is commonly used for phase angle estimation. However, during unbalanced, distorted, and dc-offset conditions, the performance of SRF-PLL is unsatisfactory. To improve its performance, it is cascaded with prefilters such as dual second order generalized integrator (DSOGI), cascaded delayed signal cancellation (CDSC), and multiple delayed signal cancellation (MDSC). Among these prefilters, MDSC has superior performance under all grid conditions with less delay time and memory requirement. In addition to an effective control algorithm, the DVR system requires high power density converters. The power density of the system is increased using transformerless T-type converter. In this paper, the effectiveness of MDSC-PLL for the transformerless T-type converter based DVR is evaluated in MATLAB/Simulink for various grid conditions such as voltage sag/swell, unbalance voltage sag/swell, harmonics, and dc-offset.

1. Introduction

Now a days, the proliferation of renewable energy sources and the power electronic converter based loads deteriorates the power quality (PQ) indices in the distribution network. The distribution network with deteriorated power quality leads to more power losses, and malfunction of sensitive loads [1]. Therefore, power quality has become a serious concern for power industries, domestic, and commercial applications. To improve power quality indices in the network, custom power devices such as dynamic voltage restorers (DVRs), distribution static compensator (DSTATCOM), and unified power quality conditioner (UPQC) are used [2]. The voltage related power quality issues are experienced with the presence of non-linear loads, short/open circuit faults, and power mismatch between load demand and power generation. To protect sensitive loads from these PQ issues, DVR is connected in series between load, and source. DVR injects voltage in series with the grid such that the load voltage is regulated to desired value for various grid conditions [3,4].

For the improved performance of DVR system, it requires effective control algorithm comprising of controller, and reference voltage generation method. In literature, numerous control strategies have been addressed for single-phase, and three-phase DVRs [5]. The feedforward and feedbck controllers are introduced in [6,7] for the reference voltage generation, and compensation. DVR reference voltage generation requires an accurate extraction of the grid phase angle. The commonly used synchronous rotating reference frame PLL (SRF-PLL) does extract an accurate phase angle for only fundamental balanced grid voltage conditions. However, in distorted, and under unbalanced grid conditions, the fundamental frequency negative sequence (FFNS), and harmonic components of grid voltages leads to oscillations in the equivalent dq frame grid voltages calculated by SRF-PLL [8]. To overcome this, many efforts have been made by researchers. The extracted fundamental positive, and negative sequence components are transformed to dq frame with an angular frequency of $+\omega$ and $-\omega$ respectively. The resultant dq components are fed to two SRF-PLLs and it is named

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as double decoupled synchronous reference frame PLL (DDSRF-PLL). However, it gives satisfactory results only for fundamental unbalanced grid condition but not for distorted grid. Its implementation for distorted grid is complex, since it involves more computations to extract sequence components of each frequency signals, and many transformations which slows down its dynamic performance [9]. To address the distorted grid cases with reduced complexity, several advanced PLLs are introduced such as moving average filter based PLL (MAF-PLL) [10,11], notch filter PLL (NF-PLL) [12], second order generalized integrator PLL (SOGI-PLL) [13], and delayed signal cancellation PLL (DSCPLL) [10,14]. Each advanced PLLs have their own merits, and demerits which are detailed in [15,16]. The SOGI introduced in [17] also generates the quadratic signal which indeed helps in single -phase systems to extract the phase angle and magnitude. An extension of SOGI-PLL known as dual second order generalized integrator PLL (DSOGI-PLL) [18] is also commonly used for grid synchronization. However, it gives poor performance, when grid voltage contains dc offset value. Another SOGI-PLL is known as second order SOGI-PLL (SOSOGI-PLL) [17] has been implemented for the extraction of the fundamental component in unbalanced grid voltage conditions. The drawbacks of SOSOGI-PLL has more computational burden, and lower dynamic response in highly distorted grid conditions [19]. In recent years, filter with transfer delay is widely used in PLLs thereby the filtering capability of the PLL under non-ideal grid voltage conditions is enhanced. One such PLL is cascaded delayed signal cancellation PLL (CDSC-PLL) proposed in [20]. The CDSC-PLL has simplicity, robustness, and promptness. However, it has more delay time, and memory requirement compared to recently proposed multiple delayed signal cancellation (MDSC) PLL [21]. The performance effect of DVR system with MDSC-PLL is not yet studied in the literature. This paper presents the performance of MDSC-PLL for the transformerless T-type converter based DVR is evaluated in MATLAB/Simulink for various grid conditions such as voltage sag/swell, unbalance voltage sag/swell, harmonics, and dc-offset.

This paper contains the following sections. The system configuration, and design are explained in Section 2. The basic working principle of MDSC operator with mathematical equations, and comparison of its frequency response, under various grid conditions, with the frequency response of SRF-PLL, DSOGI-PLL, and CDSC-PLL are presented in Section 3. The proposed MDSC operator based DVR controller is discussed in Section 4. Simulation results and analysis are explained in Section 5, followed by comparison of the proposed method with state of the art in Section 6, and finally, Section 7 presents the conclusion.

2. System configuration and design

The three-phase linear and nonlinear loads are connected to three-phase distribution system with a transformerless DVR based on T-type multilevel inverter (MLI) as shown in Fig. 1. The transformerless DVR is assumed to be supplied by an ideal dc power source, and it consists of filter inductor and filter capacitor. Five level T-type MLI consists of midpoint voltage source with equal magnitude i.e., $V_{dc1} = V_{dc2} = V_{dc}$ for each phase [22]. The number of switches needed for these MLI topologies with 'n' level voltages are $N_{sw} = 2(n-1)$. Gating pulses are procured by reduced carrier PWM technique (RCPWM) to drive IGBT switches of T-type MLI [23].

2.1. Filter inductor (L_f)

Filter inductor (L_f) is to be calculated using Eq. (1) which depends on a peak to peak ripple current of filter inductor [24].

$$L_f = \frac{V_{max}dc}{24 f_{sw} \triangle il_{p-p}} \tag{1}$$

where L_f is filter inductor, V_{max} is maximum dc voltage, f_{sw} is switching frequency, and $\triangle il_{p-p}$ is the peak to peak ripple current of filter inductor.

$$\triangle il_{p-p} < 25\% \frac{P_{rated}}{V_{inj_{max}}} \tag{2}$$

where P_{rated} is the rated power of the voltage source converter, and $V_{inj_{max}}$ is the maximum injection voltage of T-type multilevel inverter.

2.2. Ripple filter (R_f, C_f)

Ripple filter consisting of Resistor R_f, and capacitor C_f connected in series. These values are calculated using Eq. (3). Ripple filter is generally tuned at half of the switching frequency [25]

$$C_f = \frac{1}{2\pi f_r R_f} \tag{3}$$

where R_f is filter resistance, C_f is filter capacitance, and $f_r = \frac{f_{sw}}{2}$. Ripple filter time constant should be very small compared to the fundamental time period (T) $R_f \times C_f \ll \frac{T}{10}$ [26].

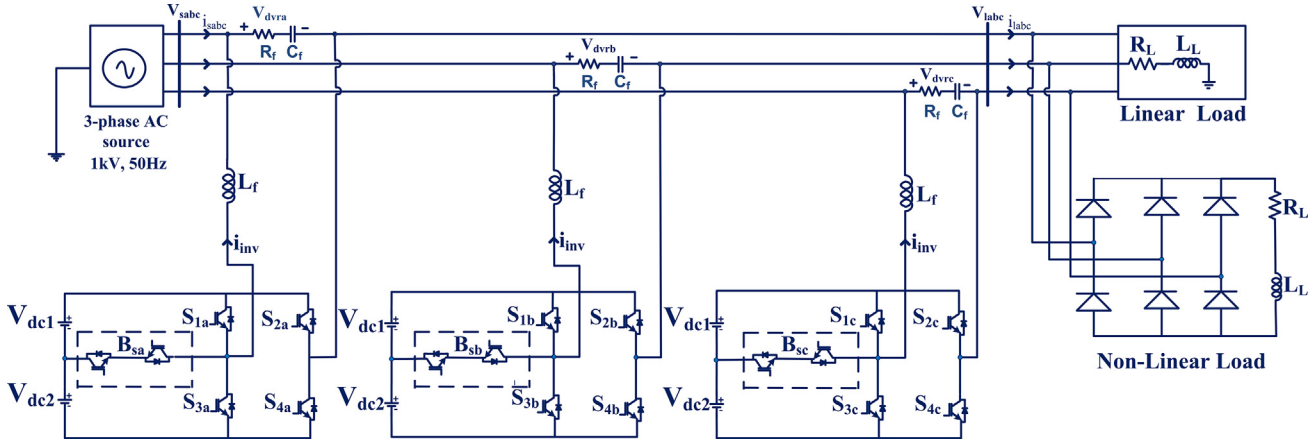

Fig. 1. Configuration of Transformerless T-type Dynamic Voltage Restorer.

3. Multiple Delayed Signal Cancellation (MDSC)

The power system grid voltage is present with unbalance, harmonics, and dc component. The conventional PLLs results inaccurate phase angle output. To extract fundamental frequency positive sequence components, many prefilters are addressed in literature. The operator DSC_4 eliminates second harmonic signals in dq frame, thereby the unbalance effect is nullified on SRF-PLL performance. To filter out group of harmonics, multiple DSC operators are cascaded or paralleled to form the CDSC operator or MDSC operator respectively. However, CDSC requires large delay time and more memory requirement. Therefore, MDSC is the best solution to eliminate the group of harmonics at a time. Let us consider the input sinusoidal signal u(t) = Asin(ωt) is delayed by $\frac{T}{n}, \frac{2T}{n}, \frac{3T}{n}$, - - - - $\frac{(n-1)T}{n}$ signals. The integer multiple of original, and delayed signal results in the cancellation of the original signal. The sinusoidal input signal u(t) and delayed (n-1) signals are summed together, and the resultant signal equal to zero. The following mathematical equation is as follows

$$\sum_{m=0}^{n-1} s\left(t-\frac{Tm}{n}\right)=\sum_{m=0}^{n-1} Asin\left(\omega t-\frac{2\pi m}{n}\right)=0 \tag{4}$$

where 'n' is delay operator, T is the fundamental time period, and m = 0, 1, 2 - - - - (n-1). The mathematical equation of the MDSC operator in the dq-frame can be expressed as follows

$$dqMDSC_n[\vec{S}_{dq}(t)]=\frac{1}{n}\sum_{m=0}^{n-1}\vec{S}_{dq}\left(t-\frac{Tm}{n}\right)=0 \tag{5}$$

where dqMDSC$_n$[.] express the MDSC operator signals in $\vec{S}_{dq}(t)$ dq-frame. The stationary reference frame ($\alpha\beta$-frame) signals(6) can be obtained from the dq-frame signals in(5) using inverse parks transformation [27] as follows

$$MDSC_n[\vec{S}_{\alpha\beta}(t)]=[R_m][MDSC_n[\vec{S}_{dq}(t)]] \tag{6}$$

Where $[R_m]=\begin{bmatrix}\cos\theta_m & -\sin\theta_m\\ \sin\theta_m & \cos\theta_m\end{bmatrix}$, $[\theta_m]=\frac{2\pi h^* m}{n}$, m = 0, 1, 2, - - - - (n-1) h^* = 1 for fundamental component extraction.

$$MDSC_n[\vec{S}_{\alpha\beta}(t)]=\frac{1}{n}\begin{bmatrix}\sum_{m=0}^{n-1}\vec{S}_d\left(t-\frac{Tm}{n}\right)\cos\theta_m-\vec{S}_q\left(t-\frac{Tm}{n}\right)\sin\theta_m\\ \sum_{m=0}^{n-1}\vec{S}_d\left(t-\frac{Tm}{n}\right)\sin\theta_m+\vec{S}_q\left(t-\frac{Tm}{n}\right)\cos\theta_m\end{bmatrix} \tag{7}$$

In this paper, the MDSC operator implemented in $\alpha\beta$-frame is shown in Fig. 2. The mathematical expression of MDSC operator in $\alpha\beta$-frame is as follows

$$MDSC_n[\vec{S}_{\alpha\beta}(t)]=\frac{1}{n}\begin{bmatrix}\sum_{m=0}^{n-1}\vec{S}_\alpha\left(t-\frac{Tm}{n}\right)\cos\frac{2\pi m}{n}-\vec{S}_\beta\left(t-\frac{Tm}{n}\right)\sin\frac{2\pi m}{n}\\ \sum_{m=0}^{n-1}\vec{S}_\beta\left(t-\frac{Tm}{n}\right)\cos\frac{2\pi m}{n}+\vec{S}_\alpha\left(t-\frac{Tm}{n}\right)\sin\frac{2\pi m}{n}\end{bmatrix} \tag{8}$$

In general, the MDSC operator can eliminate DC components and all harmonic signals except 1±np. For example, when n = 15 and p = 1, MDSC $_{15}$ extract DC component, and eliminate the all harmonics signals except +16, and −14 which are even without phase shift, whereas in CDSC$_{2,4,8,16,32}$ are −31, and +33. The MDSC operator can not eliminate the lowest undesired harmonics(i.e, 1±n). These harmonic orders can be configured to any desired harmonic order by appropriate selection of 'n' value. In specifically, when 'n' is odd integer, the lowest undesired harmonics are even. This makes MDSC operator performance as superior than CDSC operator. Since CDSC operator does not eliminate lower order odd harmonics which are often present in the grid voltages. In unbalanced voltage sag with harmonics case the extraction of frequency by using various PLLs such as MDSC-PLL, CDSC-PLL, DSOGI-PLL, and SRF-PLL are shown in Fig. 3. During unbalanced voltage sag from time 1.7 s to 1.9 s, the ripple in frequency is observed only for SRF-PLL which leads to error in phase angle tracking. The small ripples are noticed in DSOGI-PLL output. Therefore, both DSOGI and SRF PLLs are inefficient during harmonic conditions. Therefore MDSC-PLL gives accurate performance than CDSC-PLL during unbalanced voltage sag with the harmonic condition. The grid voltage detected by SRF-PLL oscillates at a double frequency of supply voltage, and similarly DSOGI-PLL, CDSC-PLL shows small distortions while extracting the fundamental positive sequence component voltage. Whereas in MDSC-PLL shows a smooth curve, and eliminates distortions while tracking the positive sequence grid voltage. Hence MDSC-PLL is the best solution to extract the fundamental positive sequence component(FPSC) voltage. Fig. 4(a), (b) shows V_d, and V_q components under unbalanced voltage sag with harmonic conditions from time 1.7 s to 1.9 s. Fig. 5(a), (b) shows V_d, and V_q components under unbalanced voltage swell with harmonic conditions from time 2.1 s to 2.3 s. The small ripples are observed in dq voltage components extracted by DSOGI-PLL and CDSC-PLL. These ripples are considerable when compared to MDSC-PLL. Therefore, MDSC-PLL is the best choice to extract the FPSC voltage.

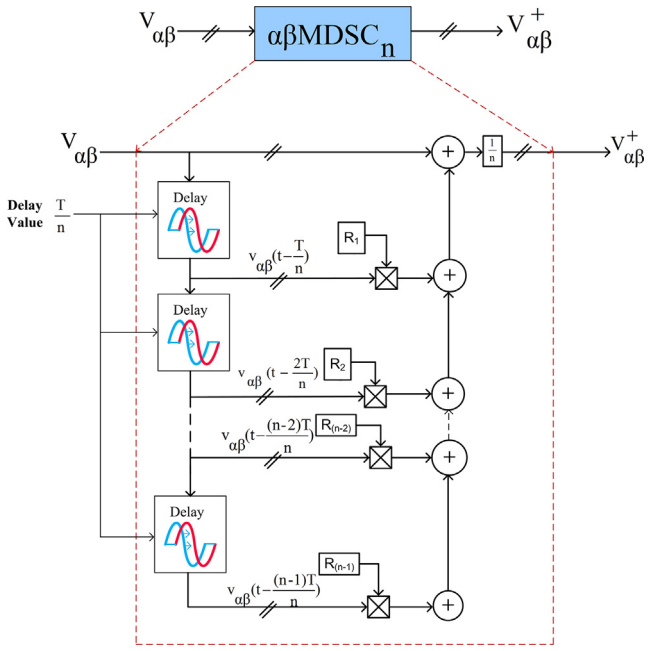

Fig. 2. MDSC operator structure in $\alpha\beta$-frame.

4. DVR controller

The complete control diagram for transformerless DVR is shown in Fig. 6. The accuracy of reference signal generation for DVR depends on the extraction of FPSCs of the supply voltage. Therefore, extraction of FPSCs plays a major role in DVR control operation. To extract FPSCs from the supply voltage (V_{sabc}), a MDSC-PLL is used as shown in Fig. 6. The supply voltages (V_{sa}, V_{sb}, V_{sc}) are transferred to $\alpha\beta$-frame as V_α, V_β using Clark's transformation. The V_α, and V_β voltage components are fed to MDSC operator, which generates the fundamental frequency positive sequence components V_α^+, and V_β^+.

The amplitude of the FPSC (V_s^+) is calculated using (9), before the components V_α^+, and V_β^+ are transformed to V_{sa}^+, V_{sb}^+, and V_{sc}^+ using inverse Clarke's transformation.

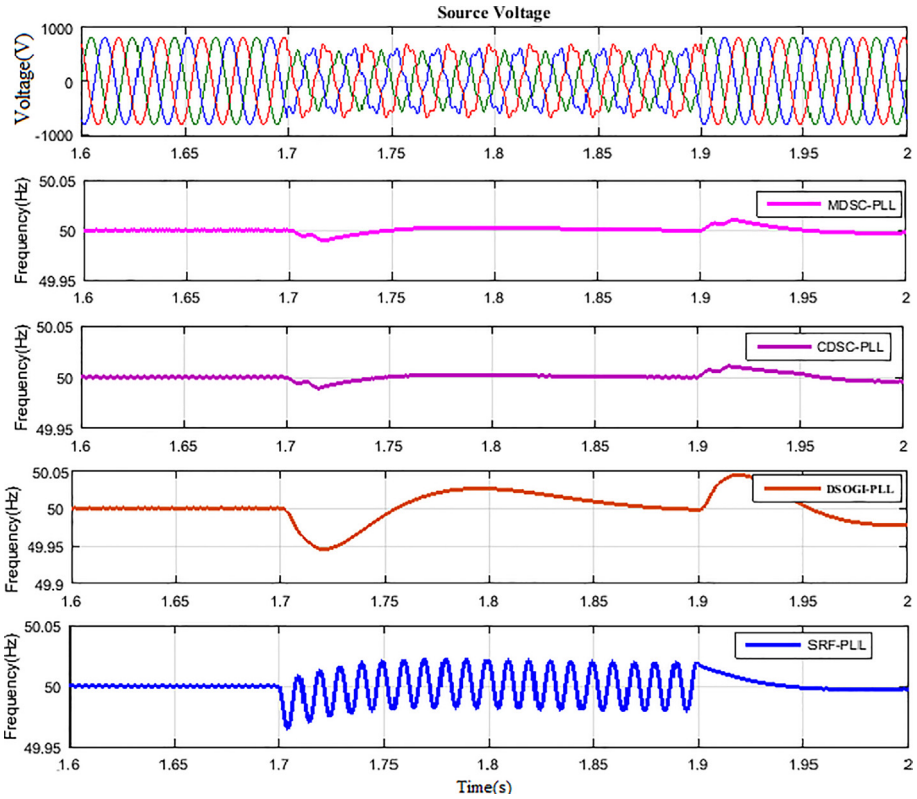

Fig. 3. Comparison of frequency curves under unbalanced voltage sag with harmonics.

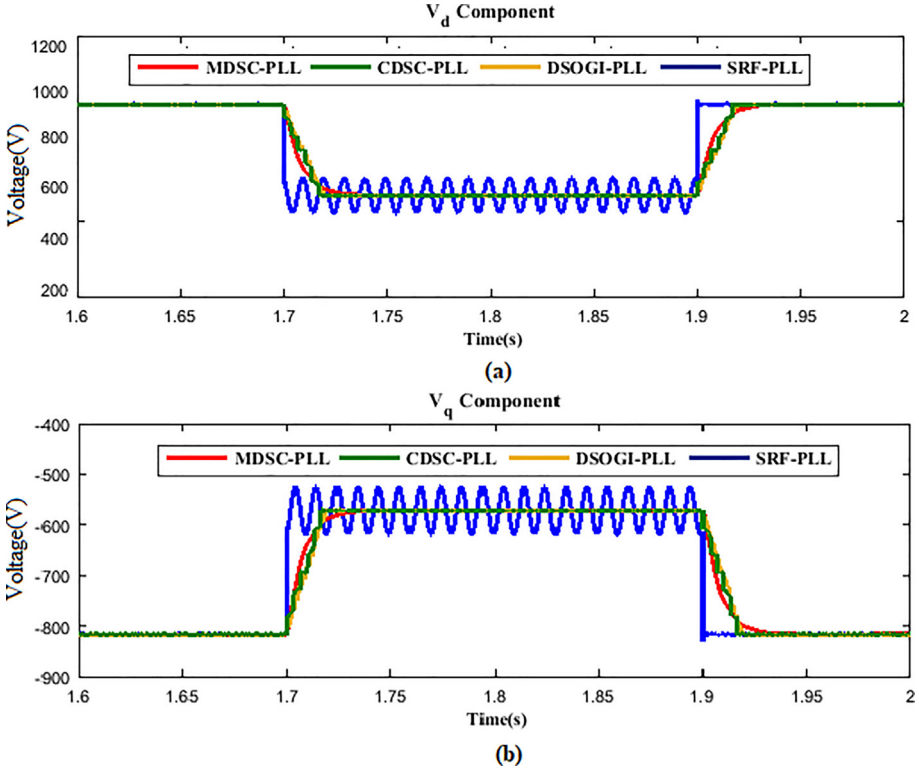

Fig. 4. Computed V_d, and V_q components by MDSC-PLL, CDSC-PLL, DSOGI-PLL, and SRF-PLL under unbalanced voltage sag with harmonics.

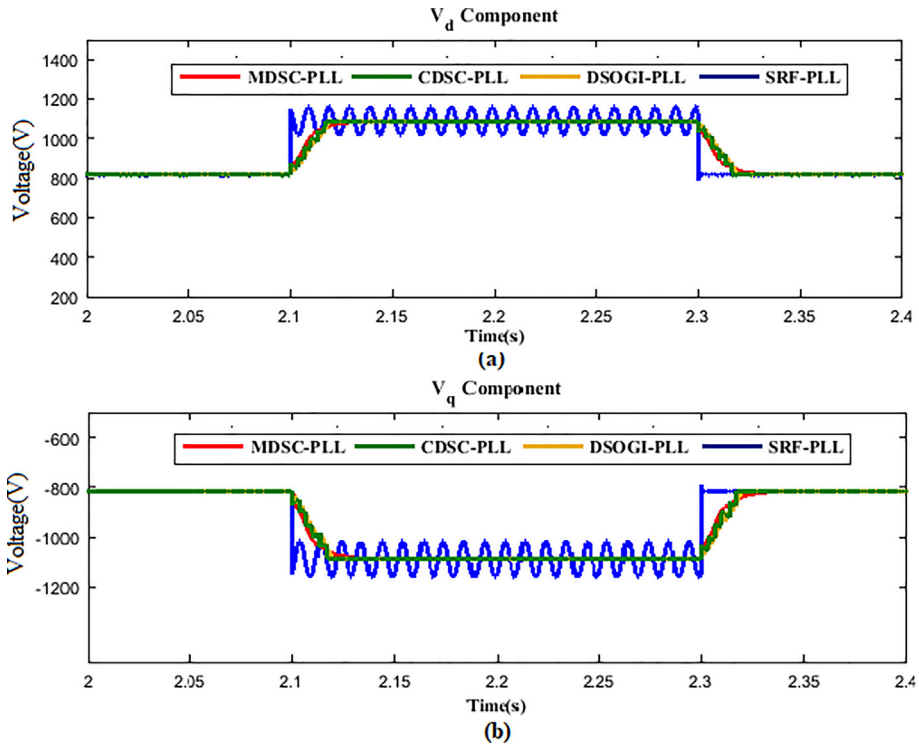

Fig. 5. Computed V_d, and V_q components by MDSC-PLL, CDSC-PLL, DSOGI-PLL, and SRF-PLL under unbalanced voltage swell with harmonics.

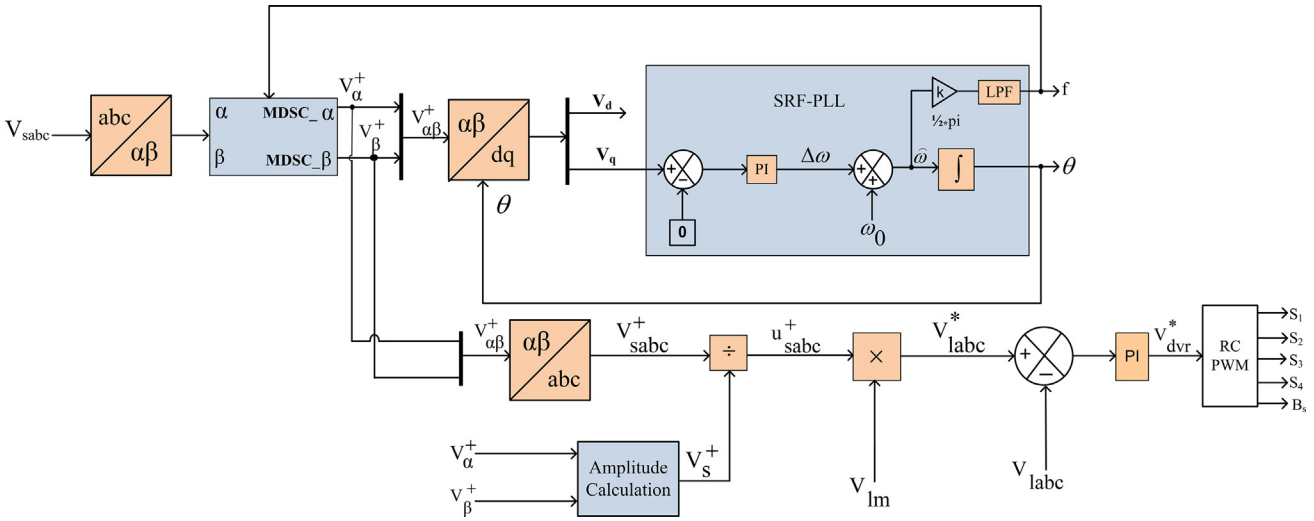

Fig. 6. DVR control circuit with MDSC based PLL.

$$V_s^+ = \sqrt{(V_\alpha^+)^2 + (V_\beta^+)^2} \tag{9}$$

The unit template of fundamental grid voltage u_{sabc}^+ is obtained from the ratio of fundamental supply voltage V_{sabc}^+ to the amplitude of the fundamental positive sequence component voltage(V_s^+) as follows

$$u_{sabc}^+ = \frac{V_{sabc}^+}{V_s^+} \tag{10}$$

The load reference voltage(V_{labc}^*) is obtained by multiplying a unit sine template (u_{sabc}^+) with the used defined peak load voltage (V_{lm}) as follows.

$$V_{labc}^* = u_{sabc}^+ \times V_{lm} \tag{11}$$

The difference of reference load voltages (V_{labc}^*) with actual load voltage (V_{labc}) is passed through a PI controller. The PI control output is reference DVR voltage (V_{dvr}^*). These reference DVR voltages are fed to reduced carrier PWM technique (RCPWM) for generating gating pulses of T-type MLI.

5. Simulation results and analysis

The T-type MLI based transformerless DVR using MDSC-PLL based control algorithm is modeled in MATLAB/Simulink. The system parameters are shown in Table 1. The performance of the DVR system with the proposed control algorithm is investigated for various grid conditions such as balanced voltage sag/swell, unbalanced voltages sag/swell, harmonics, and DC-offset conditions.

5.1. Case I: Balanced voltage sag

The balanced voltage sag is the sudden fall in load voltage, which is generally due to sudden rise in load demand, sudden fall in power generation or during starting of a three-phase large induction motor. To analyses this balanced sag condition, source voltage is programmed to 0.5 pu during time t = 0.6 s to 0.8 s as shown in Fig. 7(a). The control algorithm identifies the sag instant and controls the inverter switches such that inverter output reaches the generated DVR reference voltage as shown in Fig. 7 (b). Fig. 7(c) shows that the control algorithm accurately regulates the load voltage during balanced voltage sag.

5.2. Case II: Unbalanced voltage sag

Unbalanced voltage sag occurs due to uneven loading of phases, all types of short circuit (SC) faults excluding three phase SC fault. To replicate this grid condition, source voltage is programmed to 0.4 p.u, 0.3 p.u, and 0.2 p.u for phases A, B, and C respectively during time period t = 1.2 s to 1.4 s as shown in Fig. 8(a). Figs. 8(b)–(c) show that the DVR performance is satisfactory during unbalanced voltage sag also.

Table 1
System parameters.

Sl.No	Parameters	Values
1	Grid voltage (V_{rms} L-L)	1 kV
2	Grid frequency	50 Hz
3	Resistance(R_s)	0.005 ohm
4	Inductance(L_s)	0.1 mH
5	Filter Capacitance(C_f)	320 μF
6	Filter Resistance (R_f)	0.5 ohm
7	Filter Inductance(L_f)	2 mH
8	DC-link Voltage(V_{dc})	600 V
9	Switching Frequency(f_s)	2 kHz
10	PI controller gains	K_p = 1, K_i = 0.1
11	Sensitive load	100 kVA, 0.9 p.f

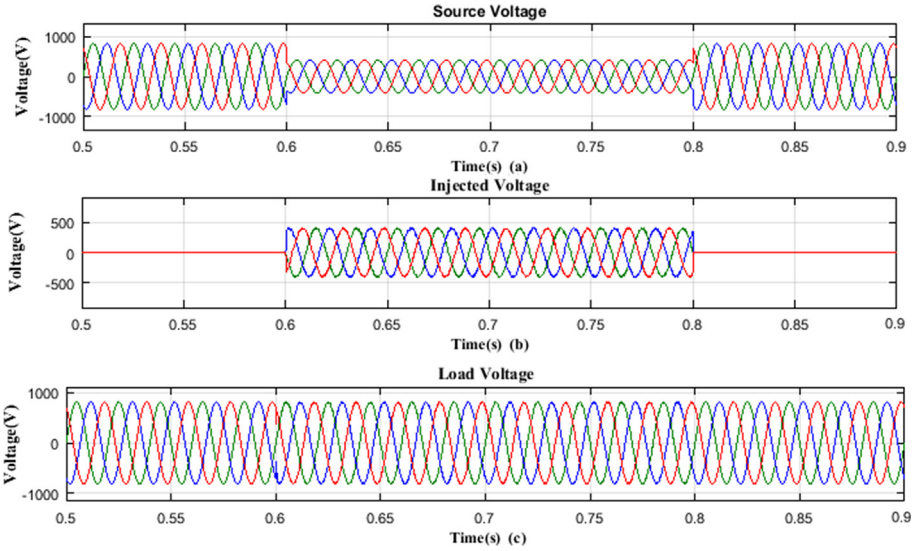

Fig. 7. Simulation results for balanced sag condition a) three-phase balanced voltage sag b) DVR compensation voltage c) load voltage after compensation.

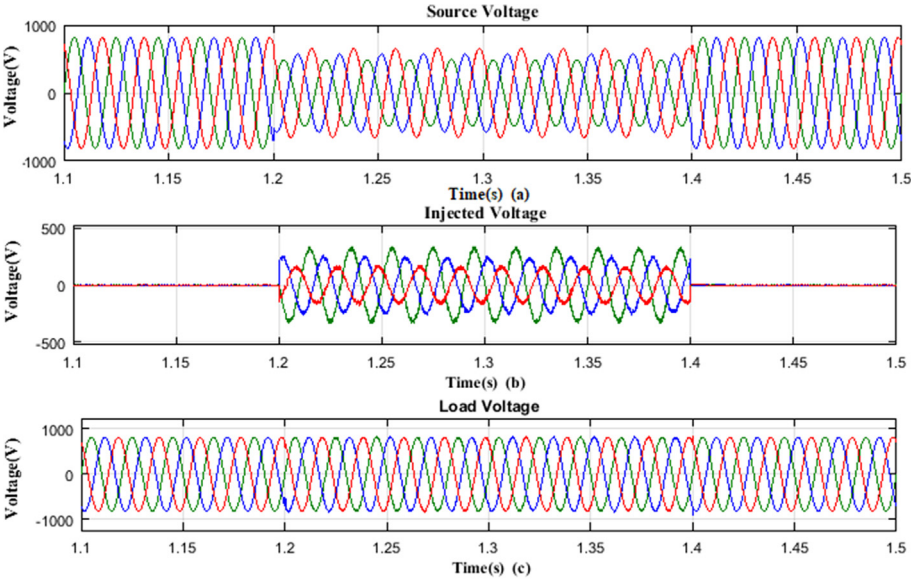

Fig. 8. Simulation results for unbalanced sag condition a) three-phase unbalanced voltage sag b) DVR compensation voltage c) load voltage after compensation.

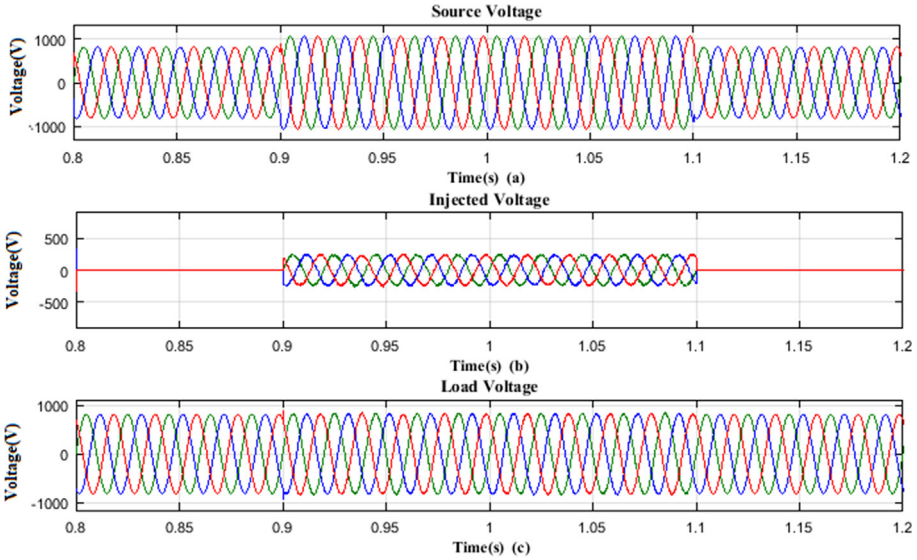

Fig. 9. Simulation results for balanced swell condition a) three-phase balanced voltage swell b) DVR compensation voltage c) load voltage after compensation.

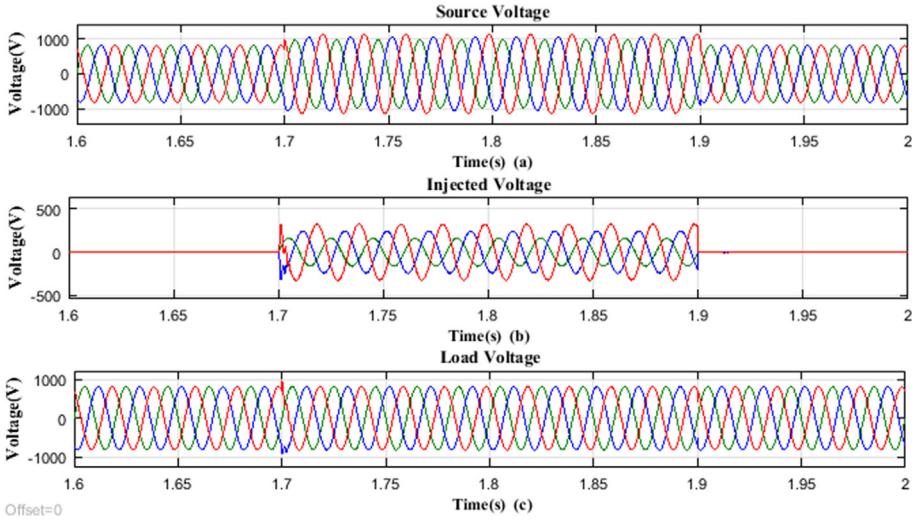

Fig. 10. Simulation results for unbalanced swell condition a) three-phase unbalanced voltage swell b) DVR compensation voltage c) load voltage after compensation.

5.3. Case III: Balanced voltage swell

It is contrast to the balanced voltage swell. The occurrence of balanced voltage swell is due to de-energization of a large loads, and energization of large capacitor banks. This condition is programmed in MATLAB during time period t = 0.9 s to 1.1 s. The considered voltage swell in three-phase system is 1.2 p.u as shown in Fig. 9(a). The proposed control algorithm rapidly detects the balanced voltage swell instant, and injects the necessary voltage with 180◦ phase opposition to source voltage as shown in Fig. 9(b). Thereby, the load voltage is maintained to the desired voltage level shown in Fig. 9(c).

5.4. Case IV: unbalanced voltage swell

Unbalanced voltage swell condition is assumed from time t = 1.7 s to 1.9 s. In addition, the phases A, B and C voltages are programmed respectively to 1.2 p.u, 1.3 p.u, and1.4 p.u as shown in Fig. 10(a). From Figs. 10(b)–(c), it is concluded that the DVR performance in regulating load voltage for unbalanced voltage swell condition is also satisfactory.

5.5. Case V: Harmonics

The currents drawn by non-linear loads will distort the PCC voltage. In addition, power electronic converter interfaced sources also introduce a less severe harmonics to the PCC voltage. To study the performance of proposed control algorithm, the source is programmed with harmonics from time instant t = 2.1 s to 2.3 s as shown in Fig. 11(a). From Figs. 11(b)–(c), it is noted that the DVR immediately compensates the harmonic voltages, and the load voltage is maintained to the desired value.

5.6. Case VI: Unbalanced voltage sag with harmonics

In this case, it is assumed that the unbalanced voltage sag with harmonics is occurred during time t = 1.7 s to 1.9 s as shown in Fig. 12(a). The DVR compensation voltages and the load voltages

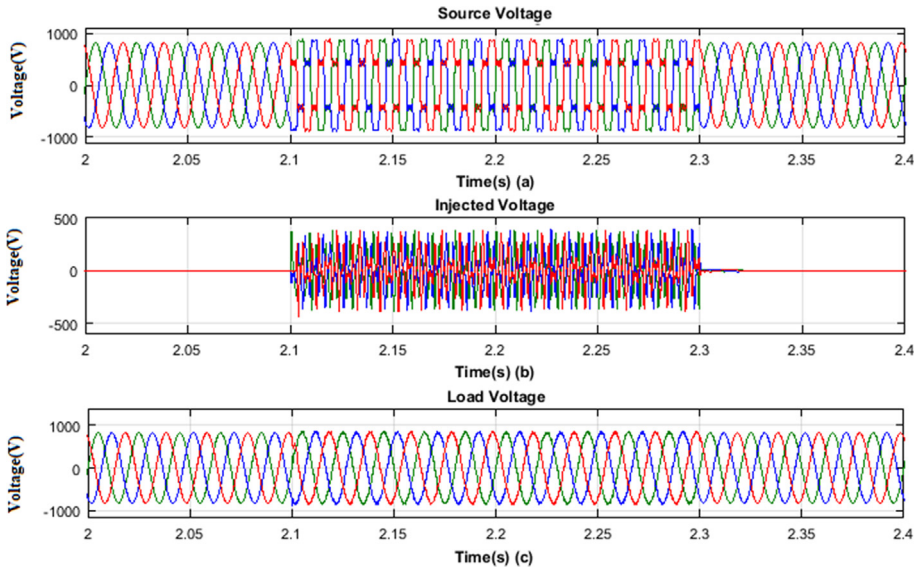

Fig. 11. Simulation results for harmonics condition a) three-phase source voltage with harmonics b) DVR compensation voltage c) load voltage after compensation.

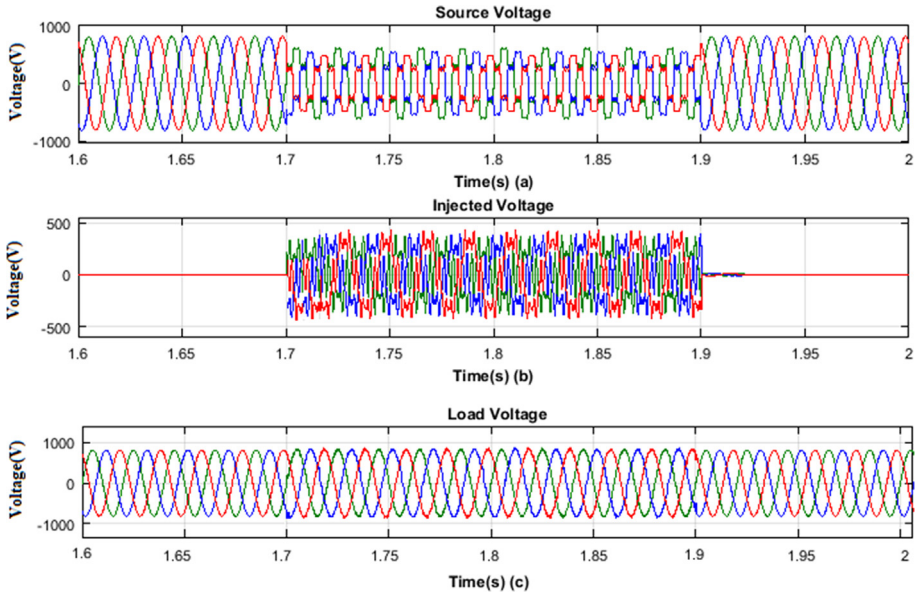

Fig. 12. Simulation results for unbalanced voltage sag with harmonics condition a) unbalanced voltage sag with harmonics b) DVR compensation voltage c) load voltage after compensation.

are shown respectively in Figs. 12(b), and (c). It is observed that the proposed control algorithm's performance is satisfactory.

5.7. Case VII: Unbalanced voltage swell with harmonics

In this case, it is assumed that the unbalanced voltage swell with harmonics is occurred during time t = 2.1 s to 2.3 s as shown in Fig. 13(a). DVR compensation voltages and the load voltages are shown in Figs. 13(b), and (c) respectively. It is observed that the proposed control algorithm's performance is satisfactory.

5.8. Case VIII: DC offset

In this case, it is assumed that the dc offset of 100 V is added to the grid voltage during time t = 0.6 s to 0.8 s as shown in Fig. 14(a). The DVR compensation voltages and the load voltages are shown in Figs. 14(b), and (c) respectively. It is observed that the proposed control algorithm's performance is satisfactory.

5.9. Analysis of total harmonic distortion (THD)

The analysis of total harmonic distortion (THD) is a salient feature measure to count the level of harmonic distortion in the voltage waveforms [28]. Hence the measured THD values of the source and load voltages are verified for the effectiveness of the proposed DVR. The THD value of source voltage of phase 'a' during harmonics condition is 27.42%, and after harmonics compensation the THD value of load voltage of phase 'a' is 3.16% are shown in Figs. 15, and 16 respectively. Similarly, the THD value of source voltage of phase 'a' during unbalanced voltage sag with harmonics condition

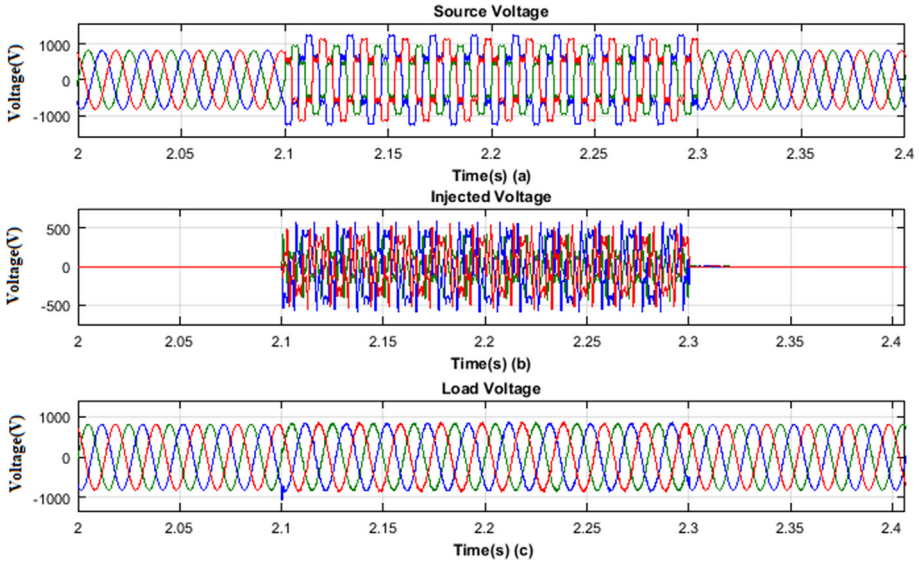

Fig. 13. Simulation results for unbalanced voltage swell with harmonics condition a) unbalanced voltage swell with harmonics b) DVR compensation voltage c) load voltage after compensation.

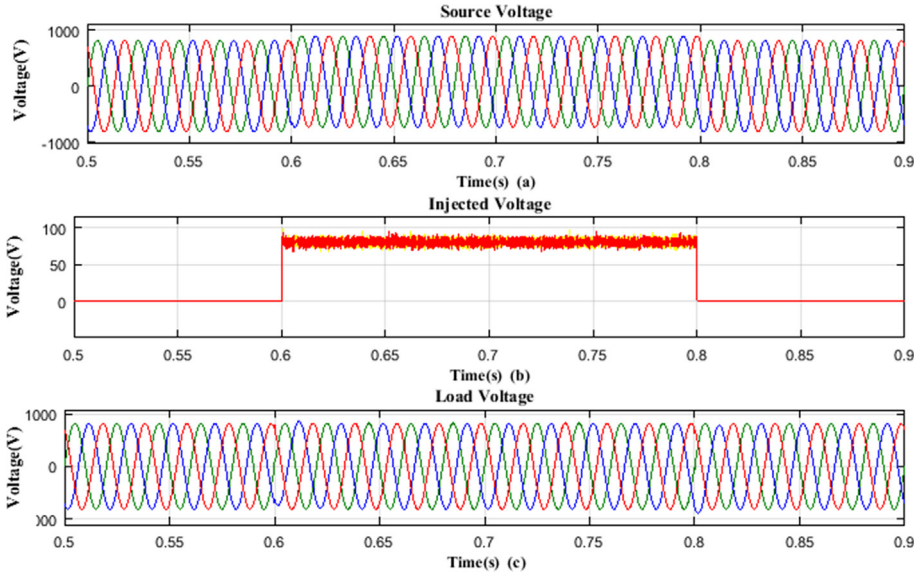

Fig. 14. Simulation results for DC offset condition a) DC offset voltage b) DVR compensation voltage c) load voltage after compensation.

is 27.58%, and after compensation, the load voltage of phase 'a' is 3.21% are shown in Figs. 17, and 18 respectively. It is observed that the THD values of load voltages are reduced (<5%) under the limits of the IEEE-519 standard [29].

6. Comparisons of the proposed method with the State of the art

The occurrence of voltage related problems is more often in this modern distribution system due to a large proliferation of power electronic converter interfaced sources, and loads. In order to overcome these voltage related PQ problems, the most generalized solution is to use DVR. The effective operation of DVR is based on accurate fault detection, reference voltage generation, and control method. A comparison of proposed PLL method with other PLL methods is presented in Table 2. In [8], the DVR reference voltage generation is done using SRF-PLL. It is observed from Fig. 3 that the SRF-PLL gives an inaccurate phase angle during unbalanced, distorted grid voltages or in the presence of dc offset in grid voltage. Therefore, DVR performance is poor during those grid conditions. In [18], the DVR reference voltages are generated using DSOGI-PLL. Therefore, its performance is unsatisfactory during highly distorted, and DC off-set grid conditions. In [21], the authors have used CDSC-PLL to extract the grid voltage phase angle from which DVR reference voltages are generated. Although, its performance is satisfactory for all grid conditions, CDSC-PLL requires more delay time, and memory requirement. Therefore the proposed control algorithm based on MDSC-PLL achieves satisfactory DVR performance for all grid conditions with less delay and memory requirement.

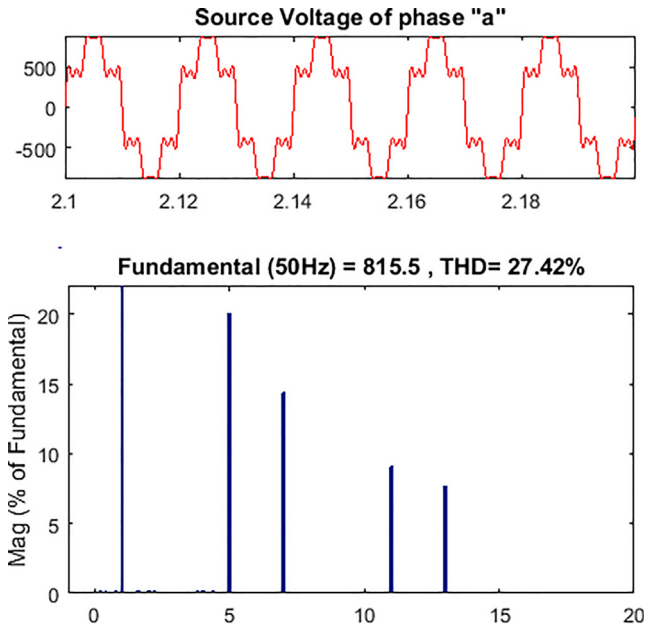

Fig. 15. THD of the source voltage without DVR during the harmonic condition.

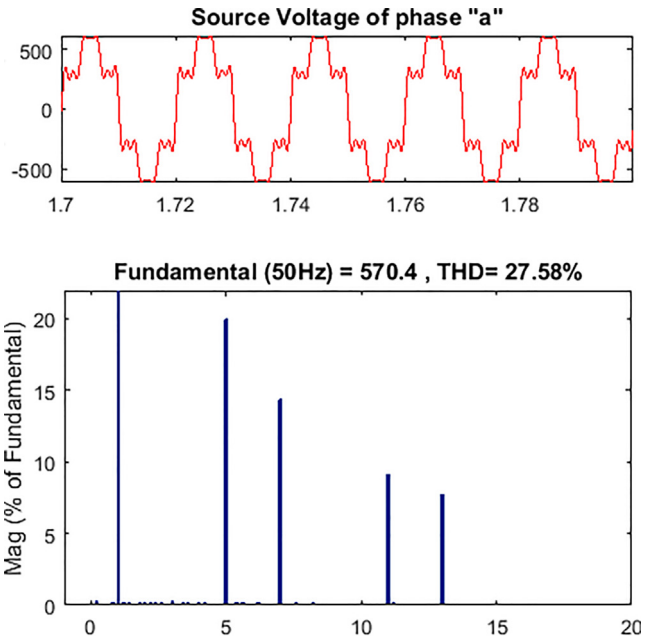

Fig. 17. THD of the source voltage without DVR during unbalanced voltage sag with harmonic condition.

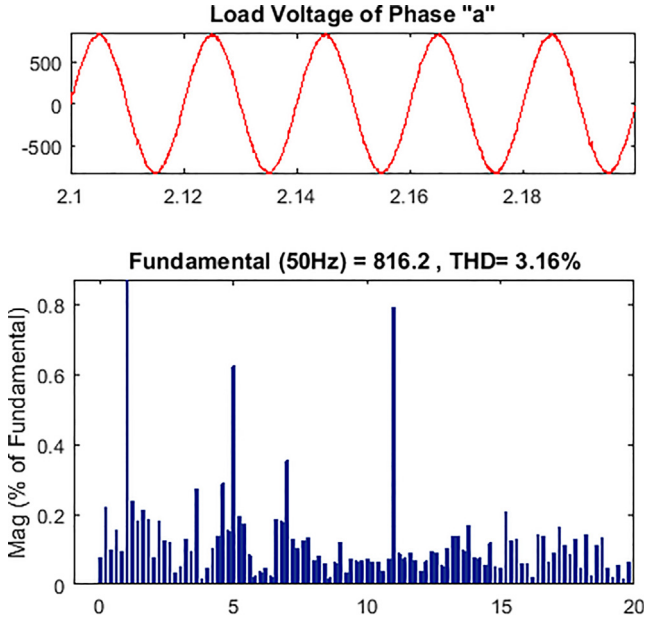

Fig. 16. THD of the load voltage with DVR during the harmonic condition.

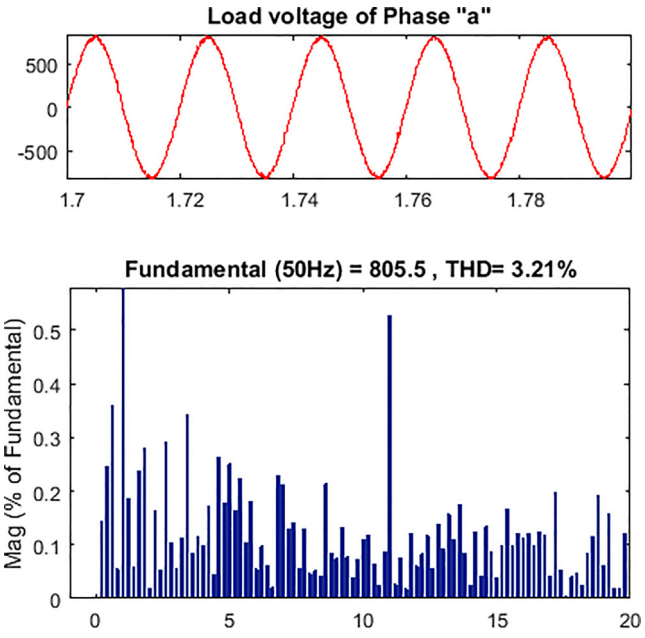

Fig. 18. THD of the load voltage with DVR during unbalanced voltage sag with harmonic condition.

7. Conclusion

In this paper, MDSC-PLL based control algorithm is proposed for transformrless T-type DVR for the accurate extraction of fundamental positive sequence component (FPSC), thereby to generate an accurate DVR reference voltage under various grid conditions. The detailed comparison of MDSC-PLL with other PLLs such as SRF-PLL, DSOGI-PLL, CDSC-PLL, is provided for various grid conditions. Although CDSC-PLL gives satisfactory performance, MDSC-PLL is used in this paper due to less requirement of delay time and memory. The performance of MDSCPLL based control algorithm verified by MATLAB/Simulink for various power quality problems such as voltage sag/swell, unbalance voltage sag/swell, harmonics, and dc-offset. Moreover proposed control algorithm not only gives good steady-state and dynamic response under unbalanced and distorted grid voltage condition but also reduce the load voltage THD to 3.21% (from 27.58%) in unbalanced voltage

Table 2
Comparison of the proposed MDSC-PLL with other PLL methods

Sl.NO	Power Quality problems	PLL-methods SRF-PLL [8]	DSOGI-PLL [18]	CDSC-PLL [21]	Proposed MDSC-PLL
1	Balanced voltage sag	✓	✓	✓	✓
2	Balanced voltage swell	✓	×	×	✓
3	Unbalanced voltage sag	×	✓	✓	✓
4	Unbalanced voltage swell	×	×	×	✓
5	Harmonics	✓	✓	✓	✓
6	Unbalanced voltage sag with harmonics	×	×	✓	✓
7	Unbalanced voltage swell with harmonics	×	×	×	✓
8	DC offset	×	×	×	✓

sag with harmonics and 3.16% (from 27.42%) in harmonics case which are under limits of the IEEE-519 standard.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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