Small-Signal Modeling and Parameters Design for Virtual Synchronous Generators

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***Abstract*—The concept of the virtual synchronous generator (VSG) is emerging as an attractive solution for controlling the grid-connected inverter when the renewable energy has a high penetration level into the grid. This paper focuses on the small-signal modeling and parameters design of the power loop of the VSG, and points out that the bandwidth of the power loop should be far less than twice the line frequency for the purpose of avoiding the VSG output voltage to be severely distorted. Consequently, the line-frequency-averaged small- signal model of the VSG is derived for system analysis and parameters design. Based on the model, the decoupling conditions between the active and reactive power loops of the VSG are given. Finally, a step-by-step parameters design method is proposed to facilitate the design of the control parameters of the VSG. A 10 kVA prototype is built and tested in the lab, and the experimental results are given to verify the effectiveness of the theoretical analysis and the proposed parameters design method.**

***Index Terms*—Virtual synchronous generator (VSG), grid-connected inverter, line-frequency-averaged small-signal model, coupling effect, parameters design.**

I. Introduction

Nowadays, distributed power generation system (DPGS) based on renewable energy has been drawing more and more attentions for the environmental friendly features. As the interface between the DPGS and the power grid, the grid-connected inverter plays an important role in injecting high-quality power into the grid, as well as guaranteeing the safety operation and providing grid support [1].

In the past, the DPGS is not required to take part in the power regulation of the grid due to the low penetration level. For example, according to the original grid codes, such as IEEE std. 1547-2003 and IEC 61727 [2], [3], the DPGS is required to produce as much energy as possible with satisfactory quality of the injected grid current in normal operation, and should cease to energize under grid faults within the certain clearing time. The policy is reasonable since the low penetration level of the DPGS has negligible influence on the grid. Any random power fluctuation of the DPGSs will be compensated by large conventional synchronous generators (SGs), and some of these generators will also take care of the overall power balance, system stability, and fault ride through.

However, when the penetration of the DPGS reaches to a certain level, such "irresponsible" behavior of the DPGS may threaten the stability of the grid [4]. Therefore, the DPGS is required to actively take part in the power regulation of the grid, just like the conventional SGs. Based on this idea, the concept of virtual synchronous generators (VSGs) was proposed to control the grid- connected inverter to emulate the essential behavior of the SGs, including the droop mechanism and the inertial characteristic. As a result, the VSG has the ability of providing grid support by automatically changing its active and reactive powers according to the frequency and amplitude of grid voltage, respectively. Meanwhile, the inertial characteristic emulated by the VSG also contributes to the total inertia of the grid, which is helpful to enhance the transient frequency stability. Besides the grid-connected mode, the VSG can also be operated in standalone mode and ensures load sharing naturally in the same way as the conventional SG does. Various implementations of the VSG have been proposed [4]–[9]. It was pointed out that the VSG can be considered to be controlled with a droop control method together with virtual inertia introduced by a first-order low pass filter in the power loop [10]. This conclusion built the bridge between the VSG and droop control and provided the useful insight for the system analysis.

Since the VSG algorithm is implemented in the software, the parameters of the VSG (includes the droop coefficients and virtual inertia) are not constrained by the physical design of any real SG and can be set arbitrarily. Therefore, these parameters can be tuned freely to achieve the desired performance.

The instantaneous output power of the VSG pulsates at twice the line frequency ($2f_{line}$) if the local loads or the grid voltages are unbalanced [11], resulting in the double-line-frequency ripple (DLFR) in the frequency and amplitude of the output voltage of the VSG, which is harmful to critical loads. Therefore, the bandwidth of the power loop of the VSG should be far less than $2f_{line}$ to attenuate these DLFR. Meanwhile, other conventional control requirements, such as the system stability and robustness, as well as the best possible dynamic performance, should be also taken into consideration in the parameters design.

In recent years, the parameters design of the VSG has been discussed [12], [13]. Due to the equivalence of the VSG and droop control, the parameters design methods of droop control also provide the design guidance for the VSG [14]–[16]. The root-locus design method was used in [12], but it did not consider the attenuation requirement of the DLFR, thus the designed parameters may not be good enough and further adjustment are needed to obtain optimized results. In [14]–[16], the closed-loop characteristic equation of the power loop with droop control was derived for system analysis and parameters design. However, due to the coupling effect between the active power loop (APL)

Manuscript received February 20, 2015; revised May 29, 2015, August 16, 2015, December 22, 2015 and February 4, 2016; accepted February 9, 2016. This work was supported by the National Natural Science Foundations of China under Award 50837003, Jiangsu Province 333 Program for Excellent Talents under Award BRA2012141 and the Project Funded by the Priority Academic Program Development of Jiangsu Higher Education Institutions.

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and the reactive power loop (RPL), the parameters design of the two loops is very difficult, and the control parameters were partially tuned by trial-and-error.

In this paper, the inherent coupling effect between the APL and RPL is analyzed, and it is pointed out that the inherent coupling effect can be ignored if the phase margin of the APL and RPL loop gain is greater than 30° and the short circuit ratio of the system is no less than 10. Therefore, the parameters of each loop can be designed independently, which greatly simplifies the design procedure. After that, this paper proposes a simple step-by-step parameters design method with consideration of all the aforementioned control requirements. With this method, the control parameters of the power loops of the VSG can be easily determined without trial-and-error. Moreover, this design method can also be extended to other implementations of VSGs and droop control, such as "Virtual Synchronous Machine (VISMA)" concept proposed in [5], [6] and "Synchronverter" concept proposed in [7]–[9].

The rest of this paper is organized as follows. Section II introduces the basic operation principle of the VSG. Section III demonstrates the necessity of lowering the bandwidth of the power loops of VSG to attenuate the DLFR and derives the line-frequency-averaged small-signal model of the VSG. Based on the model, the decoupling conditions of the APL and RPL are discussed in Section IV, and a step-by-step design method of the power loops of the VSG is presented in detail in Section V. The experimental results are presented in Section VI to verify the theoretical analysis and parameters design method. Section VII concludes this paper.

II. Basic Operation Principle of the VSG

Fig. 1 shows the topology and control diagram of the VSG. A typical three-phase voltage-source inverter is connected to the grid at the point of common coupling (PCC) through an *LC* filter, which is composed of the inverter-side inductor L_1, and filter capacitor C_f. Z_g denotes the grid impedance at the PCC. The control diagram shown in Fig. 1 is similar to that proposed in [8].

The output active and reactive powers of the VSG can be calculated according to the instantaneous power theory [17]. The calculation can be conducted in the *abc* frame, $\alpha\beta$ frame, or *dq* frame. In this paper, the $\alpha\beta$ frame is adopted due to its simple implementation, and the output active and reactive powers of the VSG can be expressed as

$$P = v_{o\alpha} i_{g\alpha} + v_{o\beta} i_{g\beta} \tag{1}$$

$$Q = v_{o\beta} i_{g\alpha} - v_{o\alpha} i_{g\beta} \tag{2}$$

where, $v_{o\alpha}$ and $v_{o\beta}$ are the capacitor voltages in the $\alpha\beta$ frame, $i_{g\alpha}$ and $i_{g\beta}$ are the injected grid currents in the $\alpha\beta$ frame.

The output active power P is fed into the active power controller to work out the phase angle of the voltage reference, θ_{ref}, while the output reactive power Q is fed into the reactive power controller to work out the amplitude of the voltage reference, $\sqrt{2}V_{ref}$.

The active power reference P_{ref} consists of the setting value P_{set} and the droop value P_{droop}. P_{droop} is calculated by multiplying the difference between the actual angular frequency of the capacitor voltages ω and the nominal angular frequency ω_n with a droop coefficient D_p. Note that ω is obtained by the phase-locked loop (PLL). So $P_{ref} = P_{set} + D_p(\omega_n - \omega)$. Since $\omega \approx \omega_g$, the VSG can automatically change its output active power according to the grid frequency, where ω_g is the angular frequency of the grid. This introduces the *P*-ω droop mechanism. Meanwhile, the integral term K_{ip}/s is adopted here to introduce the virtual inertia.

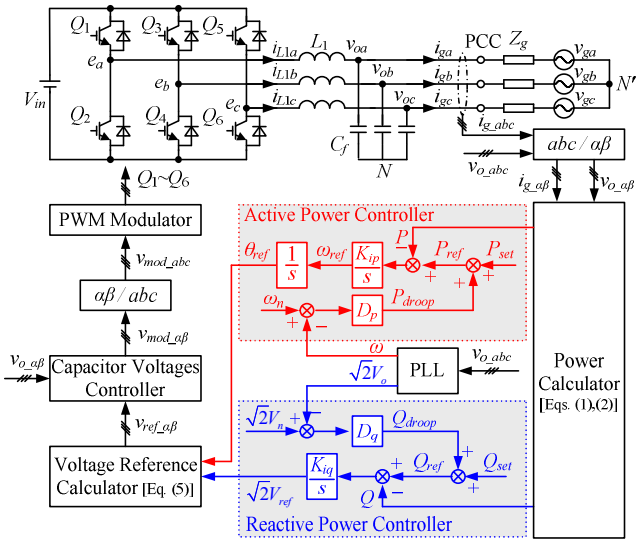

Fig. 1. Topology and control diagram of the VSG.

The operating principle of the reactive power controller is similar to that of the active power controller. The *Q*-*V* droop mechanism is introduced by making $Q_{ref} = Q_{set} + \sqrt{2}\, D_q(V_n - V_o)$. Since $V_o \approx V_g$, the VSG can automatically change its output reactive power according to the grid voltage, where V_g is the root-mean-square (RMS) value of the grid voltages. The virtual inertia is embodied by the integral term K_{iq}/s.

So, the power control scheme shown in Fig. 1 is indeed reproducing the essential behavior of a real SG, including the droop mechanism and the inertial characteristic, which is beneficial to improving the grid stability.

According to Fig. 1, we have

$$\omega_{ref} = K_{ip} \int \left[P_{set} + D_p(\omega_n - \omega) - P \right] dt \tag{3}$$

$$\sqrt{2}V_{ref} = K_{iq} \int \left[Q_{set} + \sqrt{2} D_q (V_n - V_o) - Q \right] dt \tag{4}$$

θ_{ref} is the integral of ω_{ref}. Thus, the voltage references in the $\alpha\beta$ frame, v_{ref_α} and v_{ref_β}, can be calculated as

$$\begin{cases} v_{ref\_\alpha} = \sqrt{2}V_{ref} \cos\theta_{ref} \\ v_{ref\_\beta} = \sqrt{2}V_{ref} \sin\theta_{ref} \end{cases} \tag{5}$$

The capacitor voltages controller in the $\alpha\beta$ frame is introduced here to make the capacitor voltages accurately track the voltage references. The outputs of the capacitor voltages controller are transformed into the *abc* frame from the $\alpha\beta$ frame, and then they are fed into the PWM modulator to generate the drive signals of power switches Q_1 to Q_6.

With properly design of the capacitor voltages control loop, the capacitor voltages can accurately track the voltage references. Thus, we have

$$\omega \approx \omega_{ref} \tag{6a}$$

$$\theta \approx \theta_{ref} \tag{6b}$$

$$V_o \approx V_{ref} \tag{6c}$$

Note that when the voltages and currents are sampled, the values are usually proportionally scaled, which may introduce extra sampling coefficients to the control loops. For simplicity, the DSP is programmed to automatically transform the sampled values to actual ones once receiving them, so that the sampling coefficients can be equivalently considered as 1, and they are omitted in the control diagrams in this paper. This paper focuses on the modeling and

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parameters design of the power loop of the VSG, and the parameters design of the inner capacitor voltages loop, which has been discussed in [18], is not presented here.

III. Line-Frequency-Averaged Small-Signal Model of the VSG

A. Calculation of the Average Values of the Active and Reactive Powers over Half of the Line Period

If the local loads or the grid voltages are unbalanced, the instantaneous output power of the VSG will pulsate at $2f_{line}$. As shown in Fig. 2, if the DLFR in the active and reactive power is not well attenuated by the power control loops, it may be reflected in the frequency and amplitude of the voltage reference. As a consequence, the capacitor voltages of the VSG will be distorted. To avoid this problem, the APL and RPL must be designed to have sufficiently low loop gain at $2f_{line}$ to attenuate the DLFR in the active and reactive power. With this consideration, it is unnecessary to model the system's high-frequency behavior when designing the low-bandwidth power loops of the VSG. So, the instantaneous powers can be replaced by their low-frequency averaged values during the modeling procedure [19], expressed as

$$P \approx \langle P \rangle_{T_{line}/2} = \frac{2}{T_{line}} \int_{T_{line}/2} P dt \tag{7}$$

$$Q \approx \langle Q \rangle_{T_{line}/2} = \frac{2}{T_{line}} \int_{T_{line}/2} Q dt \tag{8}$$

where $\langle P \rangle_{T_{line}/2}$ and $\langle Q \rangle_{T_{line}/2}$ denote the average values of P and Q over half the line period ($T_{line}/2$), respectively. Averaging over $T_{line}/2$ removes the DLFR, leaving the underlying low-frequency variations which are of concern.

The phasor representations of the sinusoidal voltage and current can be used to calculate the active and reactive powers [19]. When the three-phase grid voltages are balanced, $\dot{V}_g = V_g \angle 0°$ and $\dot{V}_o = V_o \angle \delta$ can be used to represent the phasors of the grid voltages and the capacitor voltages, respectively, where δ is the power angle, which is expressed as [20]

$$\delta = \int (\omega - \omega_g) dt \tag{9}$$

The grid impedance can be represented by $Z_g = r + jX_s$, where r denotes the resistive component, while X_s denotes the inductive component. On that basis, the phasor of the injected grid currents can be written as

$$\dot{I}_g = \frac{\dot{V}_o - \dot{V}_g}{r + jX_s} \tag{10}$$

Thus, the output complex power of the VSG can be expressed as

$$\begin{aligned} S &= 3\dot{V}_o \cdot \bar{\dot{I}}_g = 3\dot{V}_o \cdot \frac{\bar{\dot{V}}_o - \bar{\dot{V}}_g}{r - jX_s} \\ &= 3 \cdot \frac{V_o^2 - V_o V_g (\cos\delta + j\sin\delta)}{r - jX_s} \end{aligned} \tag{11}$$

where $\bar{\dot{V}}_o$, $\bar{\dot{V}}_g$ and $\bar{\dot{I}}_g$ are the conjugate phasors of $\dot{V}_o$, $\dot{V}_g$ and $\dot{I}_g$, respectively.

In this paper, it is assumed that the impedance Z_g is mainly inductive. If not, a virtual inductor can be introduced to be in series with it through the control strategy, and thus making the impedance to be inductive [21]. Therefore, $X_s >>$ r can always be guaranteed, and (11) can be rewritten as

$$S = 3V_o V_g \sin\delta / X_s + j3(V_o - V_g \cos\delta) V_o / X_s = P + jQ \tag{12}$$

where

$$P = 3V_o V_g \sin\delta / X_s \tag{13}$$

$$Q = 3(V_o - V_g \cos\delta) V_o / X_s \tag{14}$$

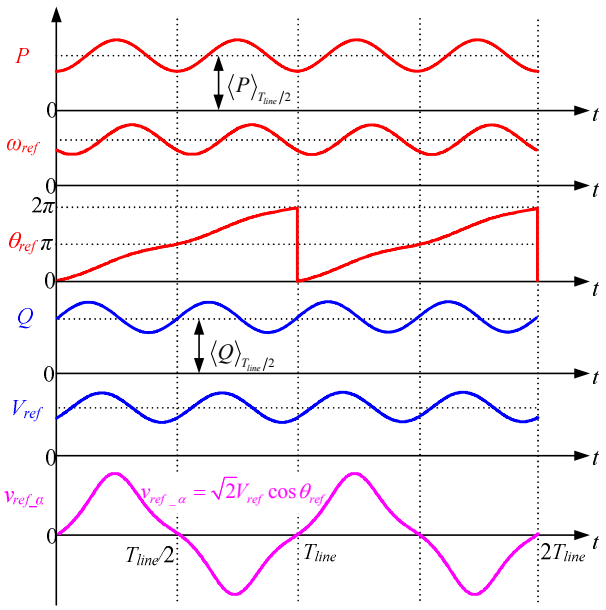

Fig. 2. DLFR in the instantaneous output power distort the PWM reference of the VSG.

Given that (13) and (14) are the mathematical descriptions of the average values of the instantaneous active and reactive powers over $T_{line}/2$, the model to be derived based on these equations is only valid for the frequency range which is lower than the line frequency [19]. Nevertheless, it is enough for system analysis and parameters design, and hereinafter this model is called line-frequency-averaged small-signal model.

B. Derivation of Line-Frequency-Averaged Small-Signal Model of the VSG

The mathematical descriptions of the VSG, i.e., (3), (4), (6), (9), (13) and (14), are used to derive the small-signal ac model of the VSG at the quiescent operating point. It is assumed that any state variable x in these equations is equal to the corresponding quiescent value X_n, plus superimposed small ac variation $\hat{x}$. Hence, we have

$$\omega = \omega_n + \hat{\omega} \tag{15a}$$

$$\omega_{ref} = \omega_n + \hat{\omega}_{ref} \tag{15b}$$

$$\omega_g = \omega_{gn} + \hat{\omega}_g \tag{15c}$$

$$\delta = \delta_n + \hat{\delta} \tag{15d}$$

$$V_o = V_{on} + \hat{V}_o \tag{15e}$$

$$V_{ref} = V_{on} + \hat{V}_{ref} \tag{15f}$$

$$V_g = V_{gn} + \hat{V}_g \tag{15g}$$

$$P = P_n + \hat{P} \tag{15h}$$

$$Q = Q_n + \hat{Q} \tag{15i}$$

$$P_{set} = P_{set\_n} + \hat{P}_{set} \tag{15j}$$

$$Q_{set} = Q_{set\_n} + \hat{Q}_{set} \tag{15k}$$

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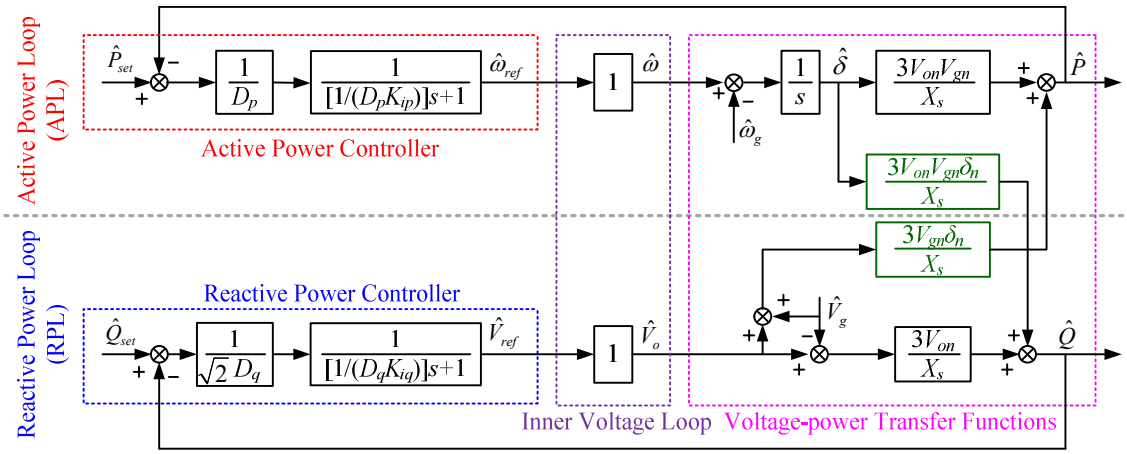

Fig. 3. Line-frequency-averaged small-signal model of the VSG.

Substituting (6a), (15b), (15h), (15j) into (3), and substituting (6c), (15f), (15i), (15k) into (4), then neglecting the dc terms, and applying Laplace transformation to the equations, we have

$$\begin{cases} \hat{\omega}_{ref}(s) = \dfrac{1}{D_p}\dfrac{\hat{P}_{set}(s)-\hat{P}(s)}{\dfrac{1}{D_pK_{ip}}s+1} \\ \hat{V}_{ref}(s) = \dfrac{1}{\sqrt{2}D_q}\dfrac{\hat{Q}_{set}(s)-\hat{Q}(s)}{\dfrac{1}{D_qK_{iq}}s+1} \end{cases} \tag{16}$$

From (16), the small-signal model of the active power controller and reactive power controller in Fig. 1 can be derived as shown in Fig. 3. As seen, each controller is equivalent to a proportional term and a first-order low pass filter in the forward path of the power loop. The proportional terms correspond to the droop coefficients in Fig. 1, reflecting the droop mechanism, while the first-order low pass filters correspond to the integral terms in Fig. 1, reflecting the virtual inertia.

Substituting (15a), (15b) into (6a), and substituting (15e), (15f) into (6c), then neglecting the dc terms, and applying Laplace transformation to the equations, we have

$$\begin{cases} \hat{\omega}(s) = \hat{\omega}_{ref}(s) \\ \hat{V}_o(s) = \hat{V}_{ref}(s) \end{cases} \tag{17}$$

According to (17), the inner capacitor voltages loop in Fig. 1, including the voltage reference calculator, capacitor voltages controller, PWM modulator, and the *LC* filter, can be considered as a follower in the forward path of the power loop, as depicted in Fig. 3.

Moreover, by substituting (15a), (15c), (15d) into (9), substituting (15d), (15e), (15g), (15h) into (13), and substituting (15d), (15e), (15g), (15i) into (14), then applying the approximations $\sin\delta_n \approx \delta_n$, $\sin\hat{\delta} \approx \hat{\delta}$, $\cos\delta_n \approx 1$, and $\cos\hat{\delta} \approx 1$, neglecting the dc terms, second and higher order ac terms, and applying Laplace transformation to the equations, we have

$$\begin{cases} \hat{\delta}(s) = \dfrac{\hat{\omega}(s)-\hat{\omega}_g(s)}{s} \\ \hat{P}(s) = \dfrac{3V_{on}V_{gn}}{X_s}\hat{\delta}(s) + \dfrac{3V_{gn}\delta_n}{X_s}\left(\hat{V}_o(s)+\hat{V}_g(s)\right) \\ \hat{Q}(s) = \dfrac{3V_{on}}{X_s}\left(\hat{V}_o(s)-\hat{V}_g(s)\right) + \dfrac{3V_{on}V_{gn}\delta_n}{X_s}\hat{\delta}(s) \end{cases} \tag{18}$$

From (18), the transfer functions from the capacitor voltages to the output powers, which are related to the grid impedances, grid voltages and power calculator in Fig. 1, can be derived, as shown in Fig. 3. This completes the line-frequency-averaged small-signal model of the VSG.

It is clear that the APL and RPL, which are shown respectively in the upper and lower parts of Fig. 3, are coupled due to the inherent nature of the output active and reactive power of the VSG, as both $\hat{P}(s)$ and $\hat{Q}(s)$ are related with $\hat{\delta}(s)$ (which is resulted from the APL) and $\hat{V}_o(s)$ (which is resulted from the RPL), which brings difficulty to system analysis and parameters design.

IV. Decoupling of the APL and RPL

According to Fig. 3, if the coupling items are ignored, the loop gains of the APL and RPL, $T_p(s)$ and $T_q(s)$, can be obtained as

$$T_p(s) = \frac{3V_{on}V_{gn}}{X_s}\frac{1}{D_p}\frac{1}{\dfrac{1}{D_pK_{ip}}s+1}\frac{1}{s} \tag{19}$$

$$T_q(s) = \frac{3V_{on}}{X_s}\frac{1}{\sqrt{2}D_q}\frac{1}{\dfrac{1}{D_qK_{iq}}s+1} \tag{20}$$

A. Decoupling of the APL

As shown in Fig. 3, when deriving the loop gain of the APL, $\hat{Q}_{set}$, $\hat{\omega}_g$ and $\hat{V}_g$ can be regarded as the perturbations of the APL, and they are set to zero. Thus, the loop gain of the APL when considering the coupling effect, T_{pc}, is derived as

$$T_{pc}(s) \approx T_p(s)\left(1-\frac{T_q(s)}{1+T_q(s)}\delta_n^2\right) \tag{21}$$

In (21), the term $T_q/(1+T_q)$ stands for the closed-loop transfer function of the RPL (regardless of the coupling effect), and its magnitude is smaller than 1/sinPM over the whole frequency range [22], where PM is the phase margin of $T_q(s)$. In order to ensure system stability and robustness, PM > 30° is usually expected. So, we have

$$\left|\frac{T_q(s)}{1+T_q(s)}\right| \le \frac{1}{\sin \mathrm{PM}} \le \frac{1}{\sin 30^\circ} = 2 \tag{22}$$

According to (13), we have

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$$P_n = \frac{3V_{on}V_{gn}}{X_s}\sin\delta_n \approx \frac{3V_{on}V_{gn}}{X_s}\delta_n \tag{23}$$

Eq. (23) can be rewritten as

$$\delta_n = \frac{P_n X_s}{3V_{on}V_{gn}} = \frac{(P_n/3)/V_{on}}{V_{gn}/X_s} = \frac{I_n}{I_{SC}} \tag{24}$$

where $I_n = (P_n/3)/V_{on}$ is the nominal current, and $I_{SC} = V_{gn}/X_s$ is the short circuit current of the grid at PCC. Normally I_{SC}/I_n, which is defined as the short circuit ratio, is required to be no less than 10 [23], yielding

$$\delta_n \le 0.1 \text{ rad} \tag{25}$$

According to (22) and (25), it can be obtained that

$$\left|\frac{T_q(s)}{1+T_q(s)}\delta_n^2\right| \le 0.02 << 1 \tag{26}$$

Eq. (26) indicates that the magnitude of the coupling term is far less than one and can be neglected. Therefore, (21) can be simplified as

$$T_{pc}(s) \approx T_p(s) \tag{27}$$

B. Decoupling of the RPL

The loop gain of the RPL when considering the coupling effect, T_{qc}, can be derived by letting $\hat{P}_{set}$, $\hat{\omega}_g$ and $\hat{V}_g$ to be zero in Fig. 3, and it is expressed as

$$T_{qc}(s) \approx T_q(s)\left(1-\frac{T_p(s)}{1+T_p(s)}\delta_n^2\right) \tag{28}$$

Similarly, the term $T_p/(1+T_p)$ stands for the closed-loop transfer function of the APL (regardless of the coupling effect), and its magnitude is smaller than 1/sinPM over the whole frequency range, where PM is the phase margin of $T_p(s)$. If PM > 30°, $|T_p/(1+T_p)| < 2$ will be guaranteed. Considering this and (25), it can be obtained that

$$\left|\frac{T_p(s)}{1+T_p(s)}\delta_n^2\right| \le 0.02 << 1 \tag{29}$$

Therefore, the coupling term of the RPL can also be neglected, and (28) can be approximated to

$$T_{qc}(s) \approx T_q(s) \tag{30}$$

In conclusion, the coupling effect between the APL and RPL can be neglected if the following conditions are satisfied:

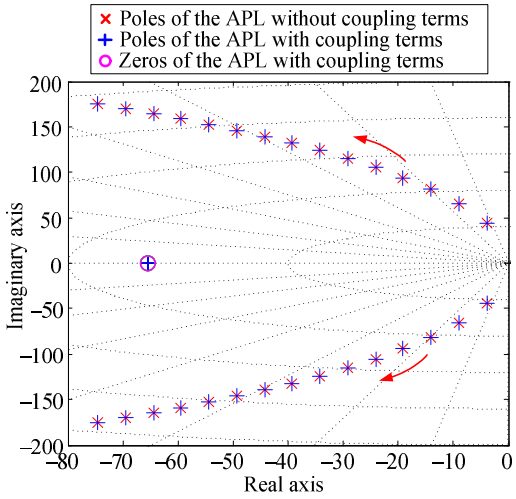
1) The phase margin of $T_p(s)$ and $T_q(s)$ is greater than 30°.
2) The short circuit ratio I_{SC}/I_n is no less than 10.

As a consequence, the control parameters of the APL and RPL can be designed independently, which greatly simplifies the design procedure. Usually, the first condition can be satisfied by tuning the parameters of the APL and RPL, which will be discussed in the next section. The second condition is always satisfied for the VSG.

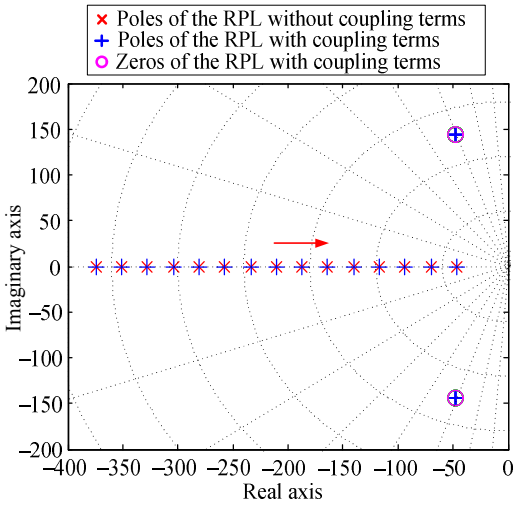
Fig. 4 shows the root locus plots of the APL and RPL with and without the coupling terms. As seen clearly, the loop gains of APL (RPL) with and without the coupling terms have similar poles, which are almost coincided with each other. The additional poles and zeros introduced by the coupling terms are very close and are cancelled by each other. Therefore, their impact on the control performance of the system can be neglected.

V. Parameters Design of the Power Loops of the VSG

Since the coupling terms between the APL and RPL can be ignored, the line-frequency-averaged small-signal model

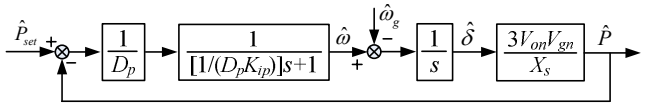


(a)

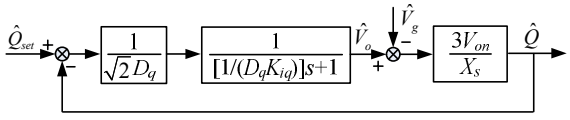


(b)

Fig. 4. Root locus plot of the APL and RPL with and without coupling terms. (a) The APL with K_{ip} varies from 0.005 to 0.1. (b) The RPL with K_{iq} varies from 0.045 to 0.03.



(a)



(b)

Fig. 5. Line-frequency-averaged small-signal model of the VSG regardless of the coupling terms. (a) APL. (b) RPL.

of the VSG shown in Fig. 3 can be simplified into that shown in Fig. 5. This section will propose an optimized parameters design method of the APL and RPL considering the requirements of system stability margin, DLFR attenuation, as well as the dynamic performance improvement. A design example will also be presented in this section to verify the effectiveness of the design method.

A. Parameters Design of the APL

There are two parameters to be determined in the APL, which are the integral coefficient K_{ip} and droop coefficient D_p. Basically, D_p is usually decided by the grid code. Thus only K_{ip} needs to be designed for ensuring the system stability and for meeting the requirement of attenuating the

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DLFR in the APL.

The corner frequency of the first-order low pass filter in the APL can be expressed as

$$f_{pL} = \frac{D_p K_{ip}}{2\pi} \tag{31}$$

Eq. (31) indicates that a smaller K_{ip} results in lower f_{pL}, which means a better attenuation ability of the DLFR. However, when f_{pL} decreases, the phase lag introduced by the first-order low pass filter increases, resulting in the reduction of the phase margin (PM) of the APL, and the whole system stability is degraded. So there is a tradeoff in choosing K_{ip}.

The magnitude of the APL loop gain at the crossover frequency f_{pc} is unity. Thus, according to (19), we have

$$\left|T_p\left(j2\pi f_{pc}\right)\right| = \frac{3V_{on}V_{gn}}{X_s D_p} \frac{1}{\left|\frac{j2\pi f_{pc}}{D_p K_{ip}} + 1\right|} \frac{1}{\left|j2\pi f_{pc}\right|} = 1 \tag{32}$$

According to (32), K_{ip} can be calculated as

$$K_{ip} = \frac{2\pi f_{pc}}{D_p \sqrt{\left(\frac{3V_{on}V_{gn}}{2\pi f_{pc} X_s D_p}\right)^2 - 1}} \tag{33}$$

According to (19), the magnitude of the APL loop gain at $2f_{line}$ can be expressed as

$$\left|T_p\left(j2\pi \cdot 2f_{line}\right)\right| = \frac{3V_{on}V_{gn}}{X_s D_p} \frac{1}{\left|\frac{j4\pi f_{line}}{D_p K_{ip}} + 1\right|} \frac{1}{\left|j4\pi f_{line}\right|} \tag{34}$$

Since f_{pL} is far below $2f_{line}$ to ensure the DLFR attenuation, the following approximation can be satisfied

$$\frac{1}{\left|\frac{j4\pi f_{line}}{D_p K_{ip}} + 1\right|} \approx \frac{1}{\left|\frac{j4\pi f_{line}}{D_p K_{ip}}\right|} \tag{35}$$

Thus, (34) can be simplified as

$$\left|T_p\left(j2\pi \cdot 2f_{line}\right)\right| \approx \frac{3V_{on}V_{gn}K_{ip}}{16\pi^2 f_{line}^2 X_s} \tag{36}$$

In order to attenuate the DLFR in the APL, the APL must have sufficiently small loop gain at $2f_{line}$. Define a_p as the magnitude requirement of the loop gain of the APL at $2f_{line}$, then $|T_p(j2\pi \cdot 2f_{line})| \le a_p$. So, we have

$$K_{ip} \le \frac{16\pi^2 f_{line}^{\ 2} X_s a_p}{3V_{on}V_{gn}} \triangleq K_{ip\max} \tag{37}$$

In order to meet the required phase margin $\mathrm{PM_{req}}$, the following condition should be satisfied.

$$\mathrm{PM} = 180° + \angle T_p\left(j2\pi f_{pc}\right) \ge \mathrm{PM_{req}} \tag{38}$$

Substituting (19) into (38), yields

$$90° - \arctan\frac{2\pi f_{pc}}{D_p K_{ip}} \ge \mathrm{PM_{req}} \tag{39}$$

According to (39), K_{ip} can be calculated as

$$K_{ip} \ge \frac{2\pi f_{pc}}{D_p} \tan\mathrm{PM_{req}} \triangleq K_{ip\min} \tag{40}$$

The design procedure of the parameters of the APL is proposed as follows.

Step 1: Determine the specifications of the loop gain of the APL. In general, PM is required in the range of (30°, 70°) for achieving good dynamic response and robustness. $a_p \le 0.1$ is required to ensure good attenuation of the DLFR in the APL.

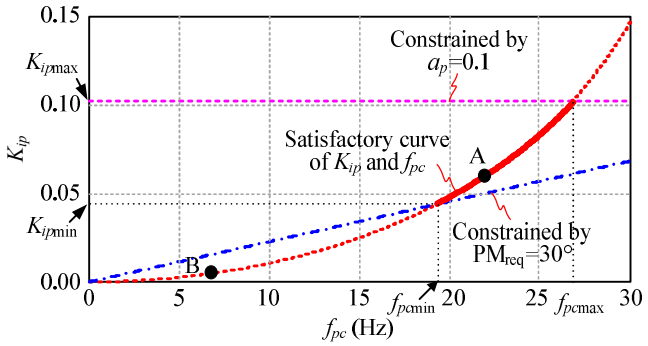

Fig. 6. Satisfactory curve of K_{ip} and f_{pc} constrained by $\mathrm{PM_{req}}$ and a_p.

Step 2: Based on the given specifications, according to (33), (37), and (40), the curves of K_{ip} as the function of f_{pc} are depicted as shown in Fig. 6, where $f_{pc\max}$ is the maximum cross-over frequency of APL determined by (33) and (37), while $f_{pc\min}$ is minimum cross-over frequency of APL determined by (33) and (40). The thick solid line is the satisfactory curve of the K_{ip} and f_{pc}.

Step 3: Choose an appropriate f_{pc} within the satisfactory curve. A larger f_{pc} in the corresponding satisfactory range is recommended since it is beneficial to improving the dynamic performance of the system. After f_{pc} is determined, K_{ip} can be directly calculated according to (33).

Step 4: Check the loop gain of the APL to ensure that all the specifications are well satisfied.

B. Parameters Design of the RPL

There are two parameters to be determined in the RPL, which are the integral coefficient K_{iq} and droop coefficient D_q. D_q is usually decided by the grid code. So, K_{iq} should be carefully designed to ensure system stability and meet the requirement of attenuating the DLFR in the RPL.

The corner frequency of the first-order low pass filter in the RPL is expressed as

$$f_{qL} = \frac{D_q K_{iq}}{2\pi} \tag{41}$$

Similar to the analysis of the APL, f_{qL} is decreased with the decreasing of K_{iq}, which means a better DLFR attenuation ability, a reduced phase margin and a slower dynamic response. So there is a tradeoff in choosing K_{iq}.

As seen in Fig. 5(b), there is only a first-order low pass filter in the RPL, the maximum phase lag introduced by this filter is −90°, which means the minimum phase margin of the RPL is 90°, and the phase margin requirement is always satisfied. Only the requirement of the DLFR attenuation as well as dynamic performance needs to be considered.

According to (20), the magnitude of the RPL loop gain at $2f_{line}$ can be expressed as

$$\left|T_q\left(j2\pi \cdot 2f_{line}\right)\right| = \frac{3V_{on}}{\sqrt{2}X_s D_q} \frac{1}{\left|\frac{j4\pi f_{line}}{D_q K_{iq}} + 1\right|} \tag{42}$$

Since f_{qL} is far below $2f_{line}$ to ensure the DLFR attenuation, the following approximation can be satisfied.

$$\frac{1}{\left|\frac{j4\pi f_{line}}{D_q K_{iq}} + 1\right|} \approx \frac{1}{\left|\frac{j4\pi f_{line}}{D_q K_{iq}}\right|} \tag{43}$$

Thus, (42) can be simplified as

$$\left|T_q\left(j2\pi \cdot 2f_{line}\right)\right| \approx \frac{3V_{on}K_{iq}}{4\sqrt{2}\pi f_{line} X_s} \tag{44}$$

Define a_q as the magnitude requirement of the loop gain

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of the RPL at $2f_{line}$, then $|T_q(j2\pi 2f_{line})| \le a_q$. So, we have

$$K_{iq} \le \frac{4\sqrt{2}\pi f_{line} X_s a_q}{3V_{on}} \triangleq K_{iq\max} \tag{45}$$

Eq. (45) gives the upper limit of K_{iq}, which is constrained by the requirement of attenuating the DLFR in the RPL. There is no lower limit of K_{iq} since the phase margin requirement of the RPL is always satisfied. However, f_{qL} is decreased when K_{iq} decreases, which affects the dynamic performance of the system, so K_{iq} should not be too small. In practice, it is reasonable to choose K_{iq} to be slightly smaller than $K_{iq\max}$ to ensure good attenuation ability, robustness and dynamic performance.

The design procedure of the parameters of the RPL is similar to that of the APL and is not repeated here.

C. Design Example

In order to verify the proposed design method, an example is given. The prototype parameters are given in Table I.

1) Determination of D_p and D_q

D_p and D_q are often determined based on the grid code. According to EN 50438 [24], it is required that the change of 100% active power corresponds to the change of 2% grid frequency, while the change of 100% reactive power corresponds to the change of 10% grid nominal voltage. So, the droop coefficients can be obtained as

$$D_p = \frac{\Delta P_{\max}}{\Delta \omega_{\max}} = \frac{10000}{(2\pi \cdot 50)\cdot 2\%} = 1592 \ (\mathrm{W\cdot s/rad}) \tag{46}$$

$$D_q = \frac{\Delta Q_{\max}}{\Delta V_{\max}} = \frac{10000}{220\sqrt{2}\cdot 10\%} = 321 \ (\mathrm{A}) \tag{47}$$

2) Determination of K_{ip}

For the loop gain of the APL, it is required that $\mathrm{PM_{req}}$ = 30° and a_p = 0.1. Based on the specifications and the parameters listed in Table I, according to (33), (37) and (40), the satisfactory curve of K_{ip} and f_{pc} are obtained as shown with the solid line in Fig. 6. As seen, the minimum value of K_{ip} is constrained by the phase margin requirement while the maximum value of K_{ip} is constrained by the requirement of attenuating the DLFR in the APL. According to Fig. 6, f_{pc} = 22 Hz, which corresponds to point A, is selected. Then K_{ip} is calculated as 0.06 from (33).

3) Determination of K_{iq}

As mentioned before, the phase margin requirement for the RPL is always satisfied, and only the requirement of attenuating the DLFR needs to be considered. By setting a_q= 0.1 and calculating the maximum value of K_{iq} according to (45), we have $K_{iq\max}$ = 0.051. Here we choose K_{iq} = 0.045.

When D_p, D_q, K_{ip} and K_{iq} are obtained, the bode diagrams of the loop gains of the APL and RPL are depicted in Fig. 7. As seen, the crossover frequency of the APL is 22 Hz, the PM is 34.6°, and the magnitude of the loop gain at $2f_{line}$ is −24.75 dB (which corresponds to 0.058). While the crossover frequency of the RPL is 8.6 Hz, the PM is 105°, and the magnitude of the loop gain at $2f_{line}$ is −21.05 dB (which corresponds to 0.089). It is obvious that all the specifications are satisfied as required.

VI. Experimental Results

The prototype of a 10 kVA three-phase grid-connected inverter with *LC* filter is fabricated and tested in the lab. The key parameters of the prototype are listed in Table I. The

TABLE I. Parameters of the Prototype

Parameters	Value	Parameters	Value
Input voltage V_{in}	800 V	Switching frequency f_s	10 kHz
Grid voltage V_g (RMS)	220 V	Inverter-side inductor L_1	3.2 mH
Rated Power	10 kVA	Filter capacitor C	10 μF
Line frequency f_{line}	50 Hz	Grid-side inductor L_g	1.2 mH

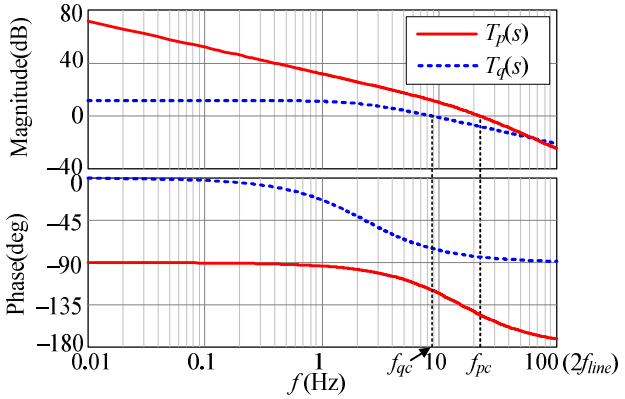

Fig. 7. Bode diagram of the loop gain.

inverter is implemented using six insulated gate bipolar transistor modules (CM100DY-24NF), which are driven by M57962L. The grid voltages and the capacitor voltages are sensed by voltage halls (LV25-P). The injected grid currents i_g are sensed by current halls (LA55-P). All the signals are sampled by a 14-bit A/D converter (MAXIM-1324ECM). The VSG algorithm is implemented in a DSP (TMS320F2812), and the active and reactive powers are calculated in the DSP and are output through a D/A converter (DAC7664). A programmable ac source (Chroma 61512) is used to simulate the grid voltages, for the purpose of arbitrarily setting the frequency and amplitude of the grid voltages to test the dynamic performance of the VSG.

Fig. 8 shows the steady-state waveforms of the VSG with K_{ip} = 0.06, K_{iq} = 0.045, $\omega_g = \omega_n$, $V_g = V_n$. As seen, the system is stable and works well in the steady state.

Fig. 9 shows the dynamic waveforms of the VSG when (a) P_{set} steps between 5 kW and 10 kW, and (b) Q_{set} steps between 5 kvar and 10 kvar. As seen, the output active and reactive powers track their setting values accurately and the overshoot is relatively small. The rising time of the active power is shorter than that of the reactive power, indicating faster dynamic response of the active power. This is because the crossover frequency of the APL (which is 22 Hz) is higher than that of the RPL (which is 8.6 Hz). However, the active power oscillates for a longer time than the reactive power as the PM of the APL (which is 34.6°) is smaller than that of the RPL (which is 105°).

Fig. 10 shows the dynamic waveforms of the VSG when (a) grid frequency drops 1% and then returns back to its nominal value, and (b) the amplitude of grid voltage drops 5% and then returns back to its nominal value. It can be seen that the VSG changes its output active (reactive) power at the moment when the grid frequency (voltage) changes, which demonstrates that the VSG has the ability of providing grid support.

Figs. 8 to 10 illustrate that the VSG has satisfactory steady and dynamic performance with K_{ip} = 0.06 and K_{iq} = 0.045, which verifies the effectiveness of the parameters design method proposed in Section V.

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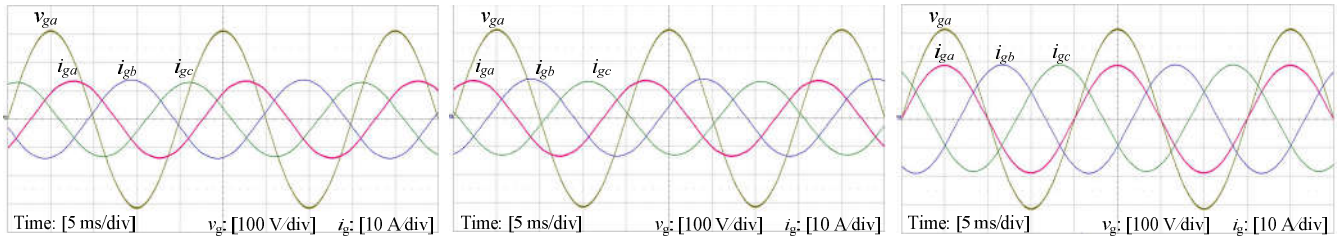

Fig. 8. Steady-state experimental results with K_{ip} = 0.06, K_{iq} = 0.045. (a) P_{set} = 5 kW, Q_{set} = 5 kvar (inductive). (b) P_{set} = 5 kW, Q_{set} = −5 kvar (capacitive). (c) P_{set} = 10 kW, Q_{set} = 0 var.

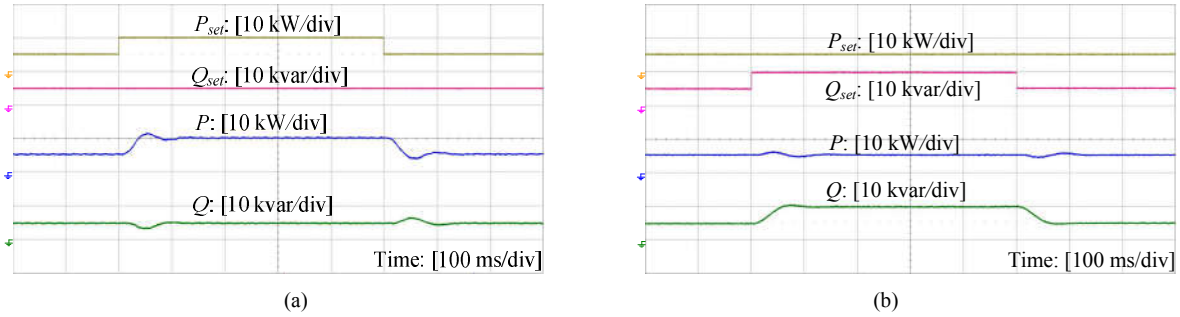

Fig. 9. Dynamic responses with K_{ip} = 0.06, K_{iq} = 0.045 when (a) P_{set} steps between 5 kW and 10 kW. (b) Q_{set} steps between 5 kvar and 10 kvar.

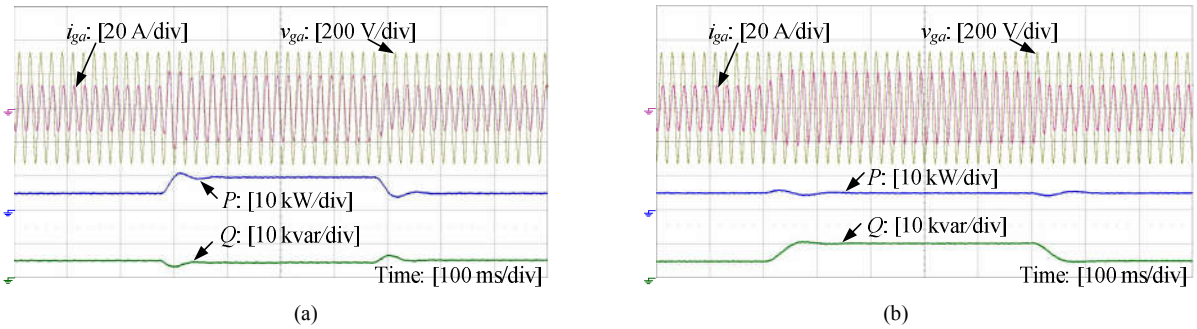

Fig. 10. Dynamic responses with K_{ip} = 0.06, K_{iq} = 0.045 when (a) Grid frequency drops 1% and then returns back to its nominal value. (b) The amplitude of grid voltage drops 5% and then returns back to its nominal value.

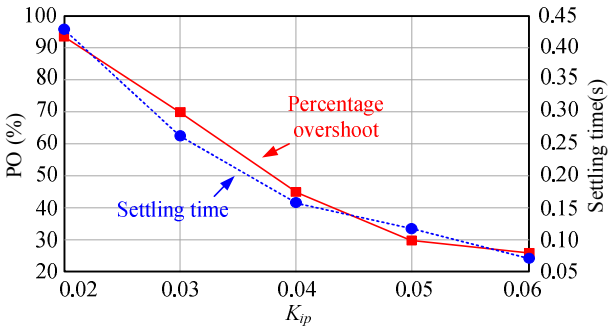

Fig. 11. Settling time and percentage overshoot of the active power when grid frequency drops 1% with K_{ip} varies.

Fig. 11 shows the diagram of the measured settling time and the percentage overshoot (PO) of the active power when grid frequency drops 1% with different K_{ip}. When K_{ip} decreases from 0.06 to 0.02, the settling time increases from 0.08s to 0.42s, while the PO increases from 24% to 96%. As discussed in Section V, the crossover frequency and phase margin of the APL are decreased when K_{ip} decreases, resulting in the degradation of system dynamic performance.

Fig. 12 shows the steady state and dynamic waveforms of the VSG when K_{ip} is decreased to 0.005, corresponding to point B outsides the satisfactory curve in Fig. 6. In this case, the crossover frequency of the APL is 6.93 Hz and the phase margin is only 10.4°. Obviously, the phase margin is not large enough to guarantee the system stability. Therefore, the system is more susceptible to the disturbance. As a result, low frequency oscillation appears in the injected grid current

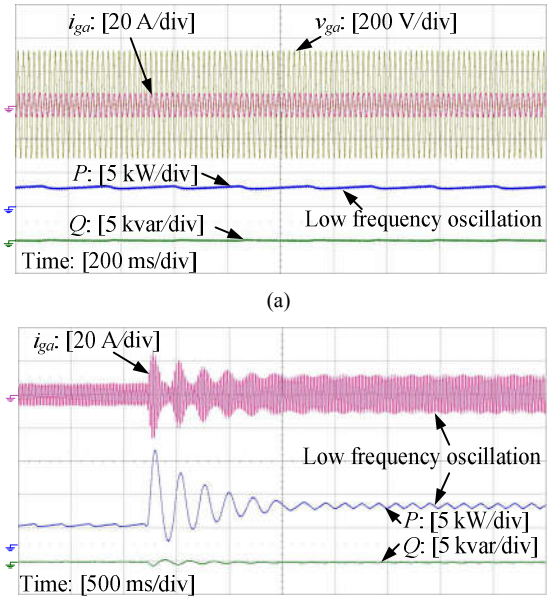

Fig. 12. Experimental results with K_{ip} = 0.005, K_{iq} = 0.045. (a) Steady-state with P_{set} = 3 kW, Q_{set} = 0 var. (b) Dynamic waveform when grid frequency drops 0.6%.

and the active power. The experimental results are in well agreement with the line-frequency-averaged small-signal model, and confirm its effectiveness to predict the low frequency oscillation behavior due to the inappropriately designed control parameters.

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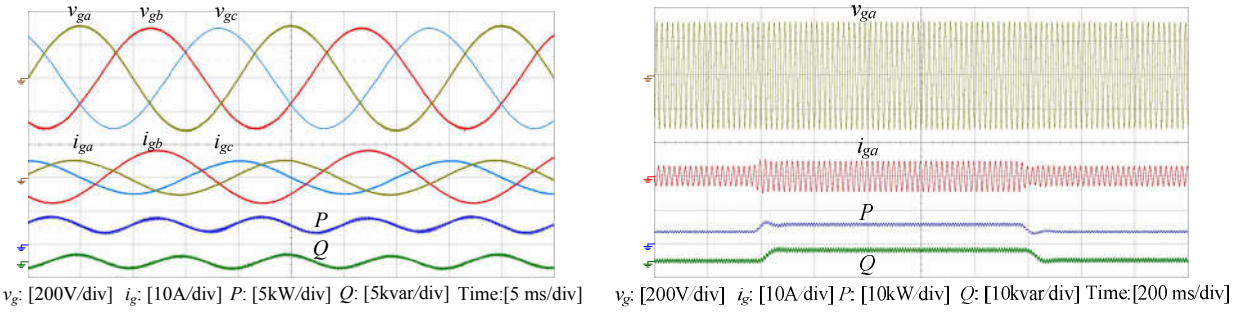
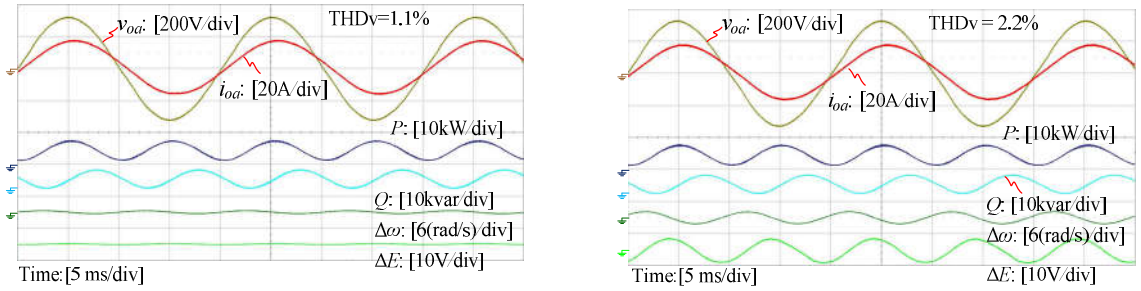


(a) (b)

Fig. 13. Steady-state and dynamic waveforms of the VSG under unbalanced grid voltage condition. (a) Steady-state with P_{set} = 3 kW, Q_{set} = 0 var. (b) Dynamic waveform with power demands step between P_{set} = 3 kW, Q_{set} = 0 var and P_{set} = 6 kW, Q_{set} = 3 kvar.



(a) (b)

Fig. 14. Experimental results when VSG works in the standalone mode with 100% unbalanced resistive-inductive loads (18+j3 Ω load in phase A , no load in phase B and phase C). (a) f_{pc} = 22 Hz, f_{qc} = 8.6 Hz (b) f_{pc} = 35 Hz, f_{qc} = 20 Hz.

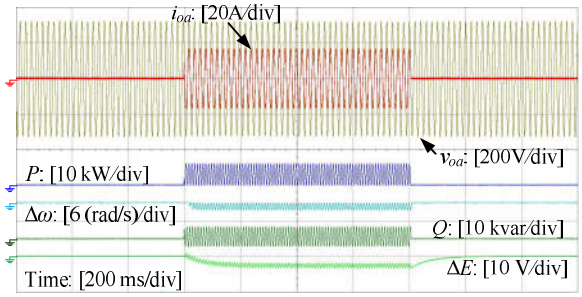


Fig. 15. Dynamic waveform of the VSG operating in the standalone mode with load in phase A steps between no load and 18+j3 Ω.

Fig. 13 shows the steady state and dynamic waveforms of the VSG under unbalanced grid voltage condition, the positive-sequence and the negative-sequence of the grid voltages are set to 0.97 pu and 0.03 pu, respectively. As seen, the VSG works stably and the dynamic performance is satisfactory. The output active and reactive powers of the VSG pulsate at $2f_{line}$ due to the unbalanced grid voltages. As pointed out in [9], the VSG is essentially a voltage-controlled inverter, and its output voltages are controlled to be balanced. Therefore, the unbalanced grid voltages will result in unbalanced injected grid current, which can be seen in Fig. 13(a). How to improve the quality of the injected grid currents under unbalanced grid voltages will be discussed in the near future.

Fig. 14 shows the experimental waveforms when the VSG works in the standalone mode with 100% unbalanced resistive-inductive (*R-L*) loads (18 + j3 Ω load in phase A, no load in phase B and phase C). Due to the unbalanced *R-L* loads, the instantaneous output active and reactive powers of the VSG pulsate at $2f_{line}$. As discussed in Section III, if not properly attenuated, the DLFR in the instantaneous active power will be reflected in the output frequency of the VSG through the APL, while the DLFR in the instantaneous reactive power will reflect in the amplitude of the output voltage of the VSG through the RPL, which results in degradation of the quality of the output voltage.

Fig. 14(a) shows the experimental waveforms with the designed parameters (f_{pc} = 22 Hz, f_{qc} = 8.6 Hz, and the corresponding loop gains of the APL and RPL at $2f_{line}$ are 0.058 and 0.089, respectively). As seen, the output frequency ripple is 0.15 Hz, the ripple of the voltage amplitude is 1.5 V, and the THD of the output voltage is 1.1%. For comparison, Fig. 14(b) shows the experimental waveforms with f_{pc} and f_{qc} are deliberately increased to 35 Hz and 20 Hz, respectively (the corresponding loop gains of APL and RPL at $2f_{line}$ are 0.233 and 0.185, respectively). It can be seen that the output frequency ripple is increased to 0.38 Hz, while the ripple of the output voltage amplitude is increased to 7.5 V, and the THD of the output voltage is increased to 2.2%. The experimental results in Fig. 14 are in well agreement with the theoretical analysis in Section III.

Fig. 15 shows the dynamic waveform of the VSG operating in standalone mode with the designed parameters (f_{pc} = 22 Hz, f_{qc} = 8.6 Hz). The load in phase A steps between no load and 18 + j3 Ω, while phase B and phase C keep no load. From Fig. 15, it is clear that the VSG responses quickly to the load step changes, and the dynamic performance is satisfactory. Meanwhile, the frequency and amplitude of the output voltage of the VSG are decreased with the increasing output active and reactive power, reflecting the P–ω and Q–V drooping characteristic of the VSG. Ref. [25] has pointed out that not only the droop effect, but also the load effect, will cause the output voltage drop when the load is increasing. There are related research discussing how to reduce the voltage drop caused by droop effect and load effect [25], [26], and it is not discussed here.

VII. Conclusions

The virtual synchronous generator (VSG) is the concept of controlling the grid-connected inverter to behave as a

synchronous generator to take part in the power regulation of the grid when the renewable energy has a high penetration level into the grid. This paper discusses the small-signal modeling and parameters design of the power loops of the VSG. Firstly, this paper points out that the bandwidth of the power control loops of the VSG should be far less than twice the line frequency to attenuate the impact of the double-line-frequency ripple (DLFR) in the instantaneous output power of the VSG, and thus the line-frequency-averaged small-signal model of the VSG is derived. Secondly, based on the model, the coupling effect between the APL and RPL of the VSG is discussed, and the decoupling conditions between the APL and RPL are analyzed. Finally, a simple step-by-step parameters design method, which takes the requirements of system stability margin, DLFR attenuation, and the dynamic performance improvement into consideration, is proposed in this paper. With this method, the control parameters of the power loop of the VSG can be easily determined without trial-and-error. A 10 kVA prototype is fabricated and tested in the lab, and the experimental results are given to verify the effectiveness of the theoretical analysis and the proposed parameters design method.

VIII. Acknowledgement

The authors would like to express their great appreciation to Lei Jia, a Master student from Nanjing University of Aeronautics and Astronautics for his great support in experimental verification and paper revision.

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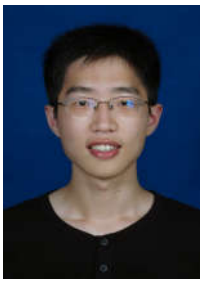

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