This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2850009, IEEE Transactions on Industrial Electronics

Dual P-Q Theory based Energy Optimized Dynamic Voltage Restorer for Power Quality Improvement in Distribution System

Manik Pradhan, *Student Member, IEEE,* and Mahesh K. Mishra, *Senior Member, IEEE*

***Abstract*—This paper deals with the protection of critical loads from voltage related power quality issues using Dynamic Voltage Restorer (DVR). A generalized control algorithm based on Instantaneous Space Phasor (ISP) and dual P-Q theory has been proposed to generate the instantaneous reference voltages to compensate the load voltages with direct power flow control. The proposed algorithm adapts energy optimized series voltage compensation, which results in a reduction of energy storage requirement. The proposed DVR control scheme can support the load from voltage related power quality issues irrespective of the load current profile. Each leg of the three-phase three-leg split capacitor inverter is used to inject series compensation voltage in respective phases of the system. Model-based computer simulation studies and real-time experimental results validate the effectiveness of the proposed control algorithm.**

***Index Terms*—Active power filter, brownout, dual P-Q theory, dynamic voltage restorer (DVR), instantaneous space phasor (ISP), load voltage compensation, power quality, sag, swell.**

I. Introduction

Modern domestic and industrial equipment are quite sensitive to voltage disturbances. Even a one-hundredth of a second voltage sag can halt modern equipment, which results in a complete restart of an industrial process. As a result, maintenance of power quality in the distribution system becomes an inescapably important requirement [1]. Power quality is a broad term, comprises various types of voltage and current related disturbances such as voltage sag/swell, flicker, voltage unbalance, harmonic current and poor power-factor, etc. Among these power quality problems, voltage related disturbance causes serious disruption on sensitive load and voltage sag is the most frequently occurring voltage related power quality problem thereof [2], [3].

As per the IEEE 519 [4] standard, different types of custom power devices are used to improve the power quality in the consumer premises [5–7]. Dynamic Voltage Restorer (DVR), one of the aforesaid devices, is used to protect the critical load (digital communication networks, advanced medical instruments, financial transactions system, elevator etc.) from voltage related power quality issues [8]. The DVR is connected in series with the grid terminal before the critical loads and injects the required amount of compensating voltage to maintain the load voltage within the specified value. A DVR generally consists of DC energy storage device, voltage source inverter (VSI), passive filter components and injection transformer. A single line diagram of a DVR circuit is shown in Fig. 1.

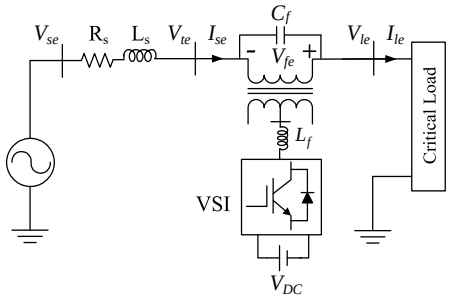

Fig. 1. Single line diagram of general Dynamic Voltage Restorer (DVR) circuit.

With the development of DVR, numerous voltage compensation strategies have been presented in the literature [9–14]. Based on the operation, these strategies are broadly classified as pre-sag, in-phase and energy optimized compensation [9], [13], [15]. As the name suggests, pre-sag compensation restores load voltage magnitude as well as phase angle same as pre-sag load voltage. In order to restore the load voltage magnitude, series injected DVR voltage is aligned with grid terminal voltage during in-phase compensation. In case of energy optimized compensation, DVR restores load voltage magnitude while optimizing the active power requirement. The characteristics of these strategies depend upon the injected voltage magnitude, phase jump and utilization of active power. Each has some advantages over others, which are briefly mentioned in Table I. If load is capable enough to withstand some phase jumps, then energy optimized voltage compensation strategy is mostly preferred as it reduces active power requirement as compared to others.

TABLE I
Comparison between compensation schemes

Control strategy	Voltage mag.	Phase jump	Active power
In-phase	low	high	high
Pre-sag	high	low	high
Energy optimized	high	high	low

Manuscript received November 20, 2017; revised February 24, 2018 and May 5, 2018; accepted Jun 1, 2018. This work is supported by the Department of Science and Technology, India (Project grant: IUSSTF/JCERDC-Smart Grids and Energy Storage/2017).

M. Pradhan and Mahesh K. Mishra are with the Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai 600036, India(e-mail: manik.pradhan15@gmail.com and mahesh@ee.iitm.ac.in).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2850009, IEEE Transactions on Industrial Electronics

Several control techniques focusing on energy optimized control algorithm or optimum rating DVR topology have been presented in the literature [9], [16], [17]. Depending upon the DVR topology and structure, energy storage requirement varies significantly [18]. A theoretical investigation of the energy optimized control strategy for medium voltage DVR is presented in [19]. However, voltage compensation in cases of nonlinear loads, distorted grid voltages and switched load conditions which are very common in power distribution system, are not fully addressed. Self-supported DVR for unbalance and non-linear loads are presented in [20], [21], but this involves additional investment on passive shunt filters. Considering the reliability aspect during under voltage or high depth voltage sag, DVR with battery energy support is presented in [22]. In order to improve the transient response, DVR based on hybrid energy storage system comprised of battery, supercapacitor or superconducting magnetic energy storage are proposed in [23], [24]. However, a robust DVR control scheme is required for smooth energy transfer. Several new DVR topologies using switching cell multilevel converter [25], cascaded open end winding transformer [26] are presented in the literature. An enhanced voltage sag compensation scheme is proposed in [16], which mitigates phase jump in the load voltage while improving the sag compensation time. An interesting pre-sag load voltage compensation scheme based on elliptical trajectory estimation and two degrees of freedom resonant DVR control schemes are presented in [27] and [28].

On the other hand, dual of the widely accepted PQ theory for shunt current compensation, has not been investigated closely for series voltage compensation purpose. In this paper, DVR control algorithm based on the Instantaneous Space Phasor (ISP) and Dual P-Q theory has been presented to address some of these aforesaid issues. The proposed algorithm is generalized enough to compensate instantaneous as well as long term voltage disturbances to protect the critical loads while optimizing the active power requirement. The proposed control algorithm has been tested through the computer simulation software MATLAB/Simulink and real-time experiments have been performed using MicroLabBox-dSPACE to show the validity and feasibility of the algorithm.

II. Concept of Instantaneous Space Phasor

Concept of instantaneous space phasor based on Clarke's transformation, can be used to monitor electric power flow, to observe the utilization of the transmission line, and to quantify the level of harmonic pollution injected by nonlinear loads etc. According to the Clarke's transformation, the power invariant transformation in between abc and $\alpha\beta 0$ is shown in (1) and (2).

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} \quad (2)$$

The ISP approach has an advantage that all the instantaneous three-phase quantities v_a, v_b, v_c or i_a, i_b, i_c are combined into one single entity, $\hat{V}$ and $\hat{I}$, respectively. The ISPs, $\hat{V}$ and $\hat{I}$ are defined as

$$\hat{V} = v_\alpha + jv_\beta \quad (3)$$

$$\hat{I} = i_\alpha + ji_\beta. \quad (4)$$

Where, v_α, v_β and i_α, i_β are the $\alpha\beta$ components of three phase voltages and currents, respectively.

If the electrical system is balanced and sinusoidal, the ISP $\hat{V}$ and $\hat{I}$ rotate with constant angular velocity $\omega = 2\pi f$ with magnitude of $\mid \hat{V} \mid = \sqrt{3}V$ and $\mid \hat{I} \mid = \sqrt{3}I$, where V, I are the RMS phase voltage, RMS line current and f is the system fundamental frequency, respectively. When the system is unbalanced or non-sinusoidal, the magnitude and the angular velocity of the ISPs will vary with time. The system effective line current (I_e) is defined from current-dependent power loss as given in (5) and the relationship with ISP $\hat{I}$ is given in (6) [29], [30].

$$I_e^2 = \frac{1}{3\tau}\int_{t-\tau}^{t} [i_a^2 + i_b^2 + i_c^2 + i_n^2]dt \quad (5)$$

$$I_e^2 = \frac{\left\langle \mid \hat{I} \mid^2 \right\rangle}{3} + \frac{4}{3}(i_0^2). \quad (6)$$

Similarly, the system effective line voltage (V_e) is defined from voltage-dependent power loss as given in (7) and the relationship with ISP $\hat{V}$ is shown in (8).

$$V_e^2 = \frac{1}{6\tau}\int_{t-\tau}^{t} [v_a^2 + v_b^2 + v_c^2 + \frac{v_{ab}^2 + v_{bc}^2 + v_{ca}^2}{3}]dt \quad (7)$$

$$V_e^2 = \frac{\left\langle \mid \hat{V} \mid^2 \right\rangle}{3} + \frac{(v_0^2)}{6} \quad (8)$$

where, $\left\langle \mid \hat{I} \mid^2 \right\rangle = \int_{t-\tau}^{t} [\mid \hat{I} \mid^2]dt$, $\left\langle \mid \hat{V} \mid^2 \right\rangle = \int_{t-\tau}^{t} [\mid \hat{V} \mid^2]dt$ and τ is the fundamental time period of the system.

III. Dual P-Q theory

In the application of active power filtering, P-Q theory is a widely accepted theory. This theory is suitable for shunt current compensation [31], [32]. The dual of this theory is suitable to perform series voltage compensation effectively. In Dual P-Q theory, it is assumed that the three-phase currents along with active, reactive and zero sequence power are known and the corresponding voltage components are calculated. The instantaneous active power ($p_{\alpha\beta}$), reactive power ($q_{\alpha\beta}$) and zero sequence power (p_0) based on α-β quantity is given in (9), (10), (11) and the matrix representation of same is given in (12).

$$p_0 = v_0\, i_0 \quad (9)$$

$$p_{\alpha\beta} = v_\alpha\, i_\alpha + v_\beta\, i_\beta \quad (10)$$

$$q_{\alpha\beta} = v_\alpha i_\beta - v_\beta i_\alpha \quad (11)$$

$$\begin{bmatrix} p_0 \\ p_{\alpha\beta} \\ q_{\alpha\beta} \end{bmatrix} = \begin{bmatrix} i_0 & 0 & 0 \\ 0 & i_\alpha & i_\beta \\ 0 & i_\beta & -i_\alpha \end{bmatrix} \begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} \quad (12)$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2850009, IEEE Transactions on Industrial Electronics

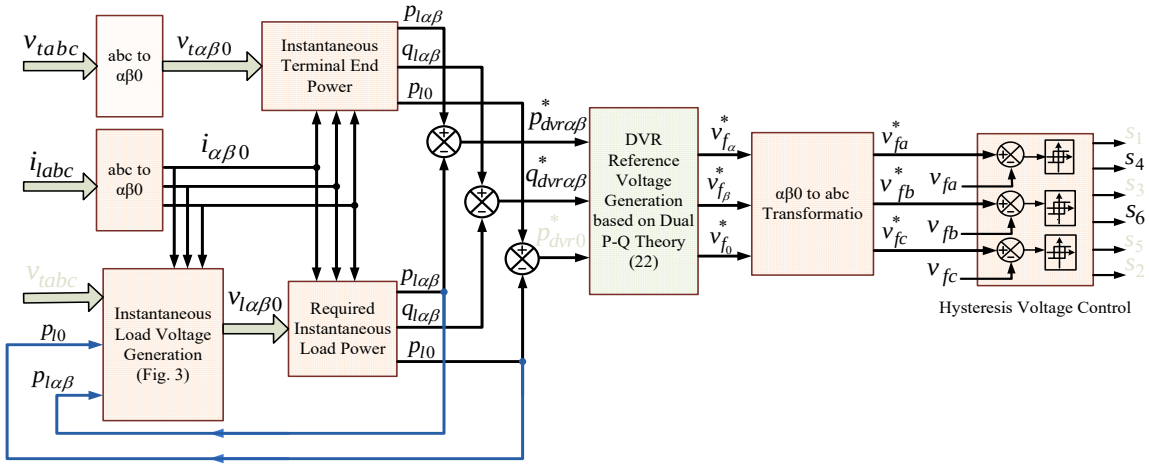

Fig. 2. Complete block diagram representation of the proposed control scheme.

The matrix representation of dual P-Q theory based voltage component extraction from instantaneous active, reactive power is derived from (12) and given in (13).

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \frac{1}{i_0} & 0 & 0 \\ 0 & \frac{i_\alpha}{{i_\alpha}^2+{i_\beta}^2} & \frac{i_\beta}{{i_\alpha}^2+{i_\beta}^2} \\ 0 & \frac{i_\beta}{{i_\alpha}^2+{i_\beta}^2} & -\frac{i_\alpha}{{i_\alpha}^2+{i_\beta}^2} \end{bmatrix} \begin{bmatrix} p_0 \\ p_{\alpha\beta} \\ q_{\alpha\beta} \end{bmatrix} \tag{13}$$

IV. Proposed DVR Control Strategies

In Fig. 1, V_{te}, I_{le}, V_{le} and V_{fe} are the effective line to neutral grid terminal voltage, line current, load voltage and DVR injection voltage, respectively. Whereas, V_{le}^* is the desired RMS line to neutral load voltage. The DC bus voltage is maintained constant by using energy storage devices. In order to ensure the optimum use of energy storage devices, the proposed algorithm should compensate the load voltage with optimum utilization of active power. The overview of the control algorithm is shown in Fig. 2.

A. Energy Optimized Compensation Technique

The system is assumed to be consisting of balanced and linear load, with an ideal DVR circuit, which maintains the rated voltages at the load end. If the system is balanced and sinusoidal, zero sequence component will be zero and the relationship between ISPs $\hat{V}$ and $\hat{I}$ with effective voltage $V_e$and I_e are given in (6) and (8), can be rewritten as following.

$$V_e = \frac{\left\langle \mid \hat{V} \mid \right\rangle}{\sqrt{3}}, I_e = \frac{\left\langle \mid \hat{I} \mid \right\rangle}{\sqrt{3}}. \tag{14}$$

From the information of the effective terminal voltage (V_{te}) and line current (I_{le}), the apparent power of the grid terminal is obtained as follows:

$$S_{teff} = 3V_{te}I_{le}. \tag{15}$$

Where, S_{teff} is the maximum active power (P_{tmax}) that can be delivered by the grid. The grid terminal active power P_t and desired load active power P_l can be defined as

$$P_t = 3V_{te}I_{le}\cos\theta \tag{16}$$

$$P_l = 3V_{le}^*I_{le}\cos\phi_{eff}. \tag{17}$$

Where, θ is the angle between effective terminal voltage V_{te} and effective line current I_{le} and ϕ_{eff} is effective load power factor angle.

In order to supply minimum active power through the DVR, the grid should supply the total load active power P_l during normal steady-state condition. However, during voltage disturbance, grid should supply maximum possible fraction of load active power, which is mathematically expressed as follows:

$$\begin{aligned} \min \quad & P_{dvr}(V_{te},\theta) = P_l - P_t \\ & P_{dvr}(V_{te},\theta) = 3V_{le}^*I_{le}\cos\phi_{eff}\{1 - \frac{V_{te}\cos\theta}{V_{min}}\} \\ \text{s.t.} \quad & g_1(V_{te},\theta) = \frac{V_{te}\cos\theta}{V_{min}} - 1 \le 0 \\ & g_2(\theta) = \cos\theta - 1 \le 0. \end{aligned} \tag{18}$$

In above,$V_{min} = V_{le}^*\cos(\phi_{eff})$, is the limiting value of terminal voltage for zero active power compensation.

If the load does not change with time, ϕ_{eff} will be fixed but θ can be controlled by injecting proper voltage V_{fe} by the DVR. By regulating the angle θ, grid active power flow can be controlled. Depending upon the magnitude of the effective terminal voltage $\mid V_{te} \mid$ and load power-factor angle ϕ_{eff} , θ is calculated as

$$\theta = \begin{cases} \cos^{-1}[V_{le}^*\cos(\phi_{eff})/V_{te}], & \text{if } V_{te} \ge V_{min} \\ 0 \quad , & \text{else.} \end{cases} \tag{19}$$

In order to define the position of the load voltage with respect to terminal voltage, a position angle δ is introduced (i.e., $V_{te}\angle 0$ and $V_{le} = V_{le}^*\angle\delta$). In Fig. 2, reference voltage generation based on this algorithm in $\alpha\beta$ reference frame is further detailed in Fig. 3 and the flow-chart for calculation of the angle δ is shown in Fig. 4. In order to give more insight about the proposed control algorithm phasor diagrams are shown in Fig. 5. Active and reactive power associated with energy optimized compensation are shown in Fig. 6 for different sags and load power factor.

1) Condition 1: Voltage sag: In the phasor diagram shown in Fig. 5, four grid terminal voltages (i.e., V_{te1} to V_{te4}),

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2850009, IEEE Transactions on Industrial Electronics

corresponding series injected DVR voltages (i.e., V_{fe1} to V_{fe4}) and load voltages (i.e., V_{le1} to V_{le4}) are shown to demonstrate the energy optimized DVR control algorithm during voltage sag or under voltage condition.

(i) During normal steady-state condition (i.e., $V_{te1} = V_{le}^*$), by satisfying (18) and (19), angle θ is calculated same as ϕ_{eff} and corresponding position angle δ is calculated as zero (i.e., V_{te1} and V_{le1} remain in-phase) and injected DVR voltage V_{fe1} is nearly zero.

(ii) During sag, if the magnitude of the effective terminal voltage does not fall below V_{min} (i.e., At V_{te2}), angle θ (i.e., $\phi_{eff} < \theta < 0$) and the corresponding position angle δ (i.e., $0 < \theta < \phi_{eff}$) is calculated using the algorithm shown in Fig. 4. The corresponding DVR injection voltage V_{fe2} becomes quadrature with the corresponding line current I_{le2}, which implies zero active power requirement for load voltage compensation.

(iii) If grid terminal voltage reduces further to V_{te3} (i.e., V_{te3}=V_{min}), angle θ is calculated as zero, indicates that grid supplying maximum active power P_{max} and corresponding angle δ is calculated as ϕ_{eff}. If $V_{te} \geq V_{te3}$, DVR does not require any amount of active power for load voltage compensation.

(iv) If sag becomes more severe and grid terminal voltage reduces further to V_{te4} (i.e., V_{te4}<V_{min}), then the angle θ and position angle δ are maintained same as the previous values (i.e., $\theta = 0$ and $\delta = \phi_{eff}$). The DVR injection voltage V_{fe4} which is shown in Fig. 5, is not in quadrature with the corresponding line current I_{le4}. This condition indicates that active power is required to compensate the load voltage fully, if grid terminal voltage falls below V_{min}.

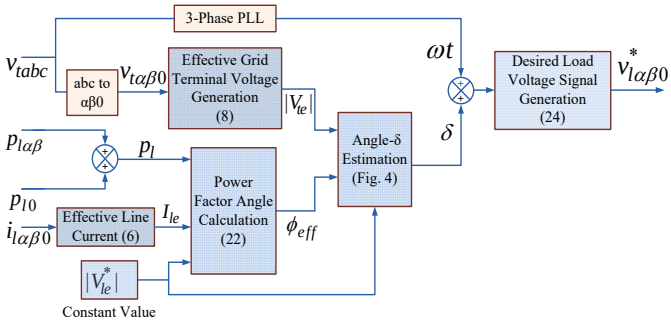

Fig. 3. Reference load voltage signal generation to obtain instantaneous load reference power.

2) Condition 2: Voltage swell: In the phasor diagram shown in Fig. 5, grid terminal voltage V_{te5}, the corresponding series injected DVR voltage V_{fe5} and load voltage V_{le5} are shown to demonstrate compensation strategy during voltage swell. Theoretically, with this proposed algorithm, DVR can compensate any amount of swell without supplying any amount of active power as $V_{te5} > V_{min}$. However, the rating of the DVR component decides the maximum value of the swell voltage to be compensated.

3) Condition 3: Unbalanced sag/swell and distorted grid voltages: During unbalanced and distorted grid voltage conditions, the magnitude and angular velocity of ISP, $\hat{V}_t$ varies abruptly. According to the energy optimized compensation,

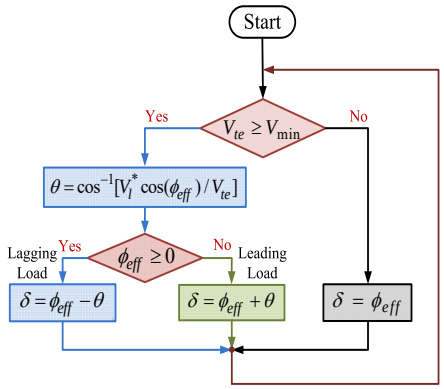

Fig. 4. Flowchart for load voltage position angle δ.

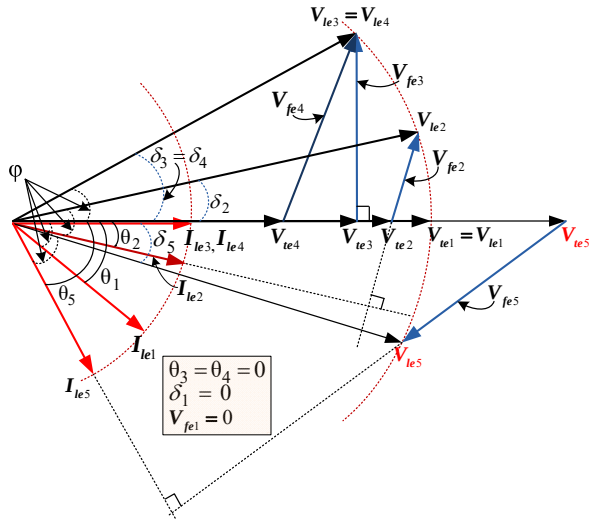

Fig. 5. Phasor diagram for voltage sag/swell compensation.

angle δ should change instantaneously with grid voltage. This introduces a phase jump in the load voltage, especially during grid voltage distortion. In order to avoid a sudden disturbance in the system, the change in angle δ is calculated over one cycle period which introduces transient non-zero real power supply at the onset and removal of the sag/swell.

B. Power Factor Angle Calculation

The total instantaneous active power can be calculated from (9), (10) and given below:

$$\begin{aligned} P_l &= \frac{1}{\tau}\int_t^{t+\tau} p\ dt \\ &= \langle v_\alpha i_\alpha + v_\beta i_\beta + v_0 i_0 \rangle \\ &= \langle p_{\alpha\beta} + p_0 \rangle . \end{aligned} \tag{20}$$

The effective apparent power at load end can be calculated from (6) and (8) as given in (21).

$$S_{leff} = 3V_{le}^* I_{le}. \tag{21}$$

Dividing (20) by (21), the effective power-factor angle is obtained as given in (22).

$$\phi_{eff} = \cos^{-1}(PF) = \cos^{-1}(\frac{P}{S_{leff}}). \tag{22}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2850009, IEEE Transactions on Industrial Electronics

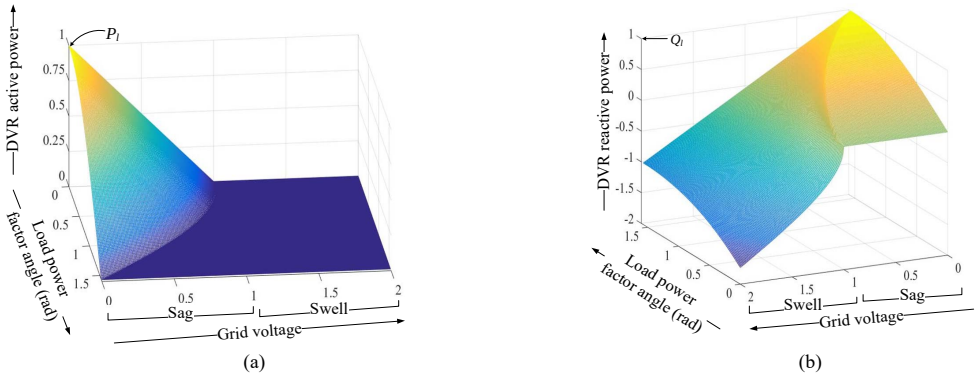

Fig. 6. (a) The Active power and (b) reactive power associated with energy optimized compensation method for different sag and power factor.

C. DVR Reference Voltage Generation

Instantaneous terminal voltage v_{tabc} and load current i_{labc} are measured by the sensors and transformed into $\alpha\beta$ reference frame. From the information of terminal voltage $v_{t\alpha\beta 0}$ and line current $i_{l\alpha\beta 0}$, instantaneous grid terminal active power ($p_{t_{\alpha\beta}}$), reactive power ($q_{t_{\alpha\beta}}$) and zero sequence power (p_{t_0}) are calculated in $\alpha\beta$ reference frame, which are given by the following equations:

$$\begin{aligned} p_{t0} &= v_{t0}\, i_{l0} \\ p_{t\alpha\beta} &= v_{t\alpha}\, i_{l\alpha} + v_{t\beta}\, i_{l\beta} \\ q_{t\alpha\beta} &= v_{t\alpha} i_{l\beta} - v_{t\beta} i_{l\alpha}. \end{aligned} \tag{23}$$

A Phase-Locked Loop (PLL) is used to obtain the phase angle ωt of the grid terminal voltage. With the information of ωt and load voltage position angle δ, desire load voltages $v_{l\alpha\beta 0}$ are obtained and given in (24)

$$\begin{aligned} v_{l0} &= 0 \\ v_{l\alpha} &= \sqrt{\frac{3}{2}} V_{le}^{*} \sin(\omega t + \delta) \\ v_{l\beta} &= -\sqrt{\frac{3}{2}} V_{le}^{*} \cos(\omega t + \delta). \end{aligned} \tag{24}$$

From the reference load voltage $v_{l\alpha\beta 0}$ and line current $i_{l\alpha\beta 0}$, required instantaneous load active power ($p_{l_{\alpha\beta}}$), reactive power ($q_{l_{\alpha\beta}}$) and zero sequence power (p_{l_0}) are calculated and given in the following equations.

$$\begin{aligned} p_{l0} &= v_{l0}\, i_{l0} \\ p_{l\alpha\beta} &= v_{l\alpha}\, i_{l\alpha} + v_{l\beta}\, i_{l\beta} \\ q_{l\alpha\beta} &= v_{l\alpha} i_{l\beta} - v_{l\beta} i_{l\alpha}. \end{aligned} \tag{25}$$

The required DVR power (26) can be obtained by subtracting (23) from (25).

$$\begin{aligned} p_{dvr0}^{*} &= p_{l_0} - p_{t_0} \\ p_{dvr\alpha\beta}^{*} &= p_{l\alpha\beta} - p_{t\alpha\beta} \\ q_{dvr\alpha\beta}^{*} &= q_{l\alpha\beta} - q_{t\alpha\beta}. \end{aligned} \tag{26}$$

Dual P-Q theory based transformation (13) is used to generate reference voltage in $\alpha\beta$ reference frame (27) and further Inverse Clark's Transform is performed to generate reference DVR voltage (v_{fabc}^{*}) in abc frame.

$$\begin{bmatrix} v_{f_0}^{*} \\ v_{f_\alpha}^{*} \\ v_{f_\beta}^{*} \end{bmatrix} = \begin{bmatrix} \frac{1}{i_{l0}} & 0 & 0 \\ 0 & \frac{i_{l\alpha}}{{i_{l\alpha}}^2+{i_{l\beta}}^2} & \frac{i_{l\beta}}{{i_{l\alpha}}^2+{i_{l\beta}}^2} \\ 0 & \frac{i_{l\beta}}{{i_{l\alpha}}^2+{i_{l\beta}}^2} & -\frac{i_{l\alpha}}{{i_{l\alpha}}^2+{i_{l\beta}}^2} \end{bmatrix} \begin{bmatrix} p_{dvr0}^{*} \\ p_{dvr\alpha\beta}^{*} \\ q_{dvr\alpha\beta}^{*} \end{bmatrix} \tag{27}$$

V. Energy Storage Requirement

In case of energy optimized compensation, the active power supplied by the DVR is obtained as,

$$P_{dvr} = P_l(1 - \lambda \frac{\cos\theta}{\cos\phi_{eff}}). \tag{28}$$

Where, λ is denoted as: $\lambda = V_{te}/V_{le}^{*}$. The initial energy stored in the DC capacitor W is given as follows.

$$W = \frac{1}{2} C_{dc} V_{dc}^2. \tag{29}$$

Where, V_{dc} is the initial DC link voltage. During high depth sag, the DC link voltage changes its initial voltage V_{dc} to final voltage $V_{dc} - \Delta V_{dc}$ for the time interval Δt due to active power flow. The final energy stored in the DC capacitor is given as follows.

$$P_{dvr}\Delta t = \frac{1}{2} C_{dc}\{V_{dc}^2 - (V_{dc} - \Delta V_{dc})^2\}. \tag{30}$$

Comparing (28) and (30), the required capacitance of the DC link capacitor is obtained as,

$$C_{dc} = \frac{2P_l(1 - \lambda\frac{\cos\theta}{\cos\phi_{eff}})\Delta t}{V_{dc}^2\{2\frac{\Delta V_{dc}}{V_{dc}} - (\frac{\Delta V_{dc}}{V_{dc}})^2\}}. \tag{31}$$

The initial energy stored in the DC capacitor, W_1 is obtained as follows.

$$W_1 = \frac{P_l(1 - \lambda\frac{\cos\theta}{\cos\phi_{eff}})\Delta t}{\{2\frac{\Delta V_{dc}}{V_{dc}} - (\frac{\Delta V_{dc}}{V_{dc}})^2\}}. \tag{32}$$

In case of in-phase compensation, similar way initial DC stored energy, W_2 can be obtained and given in (33)

$$W_2 = \frac{\lambda P_l \Delta t}{\{2\frac{\Delta V_{dc}}{V_{dc}} - (\frac{\Delta V_{dc}}{V_{dc}})^2\}}. \tag{33}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2850009, IEEE Transactions on Industrial Electronics

VI. Dynamic Voltage Restorer Power Circuit

In the previous section, the proposed DVR control algorithm based on ISP and dual P-Q theory has been discussed. In this section, the power circuit of the hardware experimental setup is discussed. A three-phase, three-leg, split capacitor inverter is used in the DVR circuit and connected to each phase of distribution terminal feeder through three single phase injection transformers and a passive LC filter [33]. Each leg explicitly injects voltage in series with the each phase terminal voltage. In this experimental setup 1:1 injection transformer is used to isolate the inverter from the distribution feeder.

The reference voltage of DVR is generated using the proposed algorithm as given in (27). To inject the compensating voltage in series with the distribution terminal feeder, an appropriate switching pulse for the inverter is generated using hysteresis control. The main advantage of the hysteresis controller is its simplicity and ease of implementation. The main disadvantage of hysteresis band control is variable switching frequency. An improved filter design based on variable switching frequency has been implemented from [34]. In order to improve the controller performance in terms of smooth tracking, a resistance is added in series with the filter capacitor. The use of band resistance (R_{sw}) results in an increase in power loss (I^2R_{sw}). However, this increase is marginal because the resistance increases the filter impedance, leads to a reduction in filter current.

VII. Simulation Studies

To show the validity and feasibility of the proposed control algorithm, comprehensive simulation studies have been carried out using MATLAB/Simulink. The details of simulation parameters are given in Table II. In order to test the dynamic performance of the proposed control algorithm, the simulation study is carried out for different types of grid voltage disturbance conditions. In each case, a low depth voltage sag (i.e., $V_{te} \geq V_{min}$) occurs at 0.05 s and continue till 0.1 s, after that a high depth voltage sag (i.e., $V_{te}<V_{min}$) occurs at 0.15 s to 0.2 s. This is followed by a voltage swell (i.e., V_{te} = 1.2 pu) appears at 0.25 s to 0.3 s. In the simulation results, v_{tabc}, v_{fabc}, v_{labc}, i_{labc}, i_{TH}, i_{IM} p_{dvr}, q_{dvr} are grid terminal voltages, DVR injection voltages, load voltages, total line current, thyristor bridge (TB) nonlinear current, induction motor (IM) current, DVR active and reactive power, respectively.

The DVR performance during balanced voltage disturbances (i.e., balanced sag, swell, etc.) and corresponding active and reactive power requirement for full load voltage compensation are shown in Fig. 7. It is observed that during low depth sag (i.e., 0.5 s to 0.1 s) and swell (i.e., 0.25 s to 0.3 s), DVR does not require any amount of active power. In order to maintain the load voltage, DVR needs to supply or consume required

TABLE II
System Parameters for Simulation Study

Parameter	Values
Supply	400 V RMS, 50 Hz, 3Φ
Filter parameters	$C_f = 30$ μF, $L_f = 5$ mH, $R_{sw} = 2$ Ω
Linear load	$Z_a = 53.2 + j25.13$ Ω, $Z_b = 57.7 + j29.31$ Ω, $Z_c = 56.7 + j30.34$ Ω.
Nonlinear load	3Φ full bridge diode rectifier feeding $R_{nl} = 100$ Ω, $L_{nl} = 90.12$ mH
Injection transformer	230 V, 1.4 kVA , Turns ratio 1:1

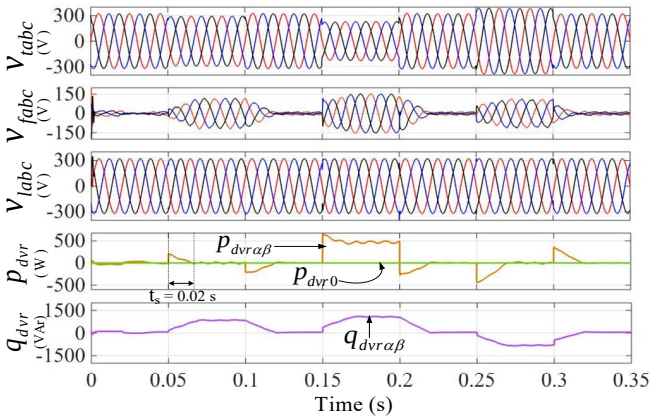

Fig. 7. Simulation results during balanced voltage disturbance compensation.

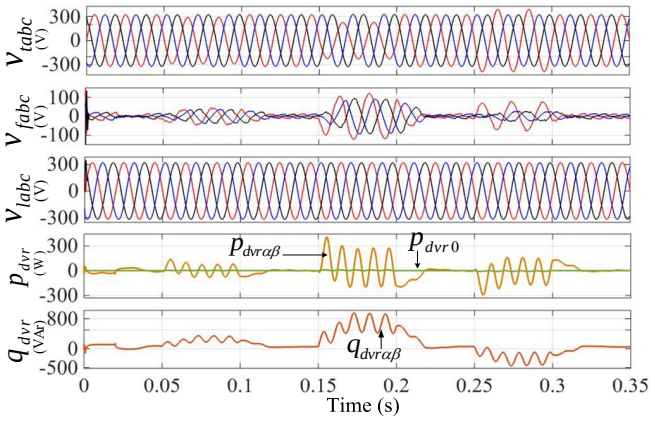

Fig. 8. Simulation results during unbalanced voltage disturbance compensation.

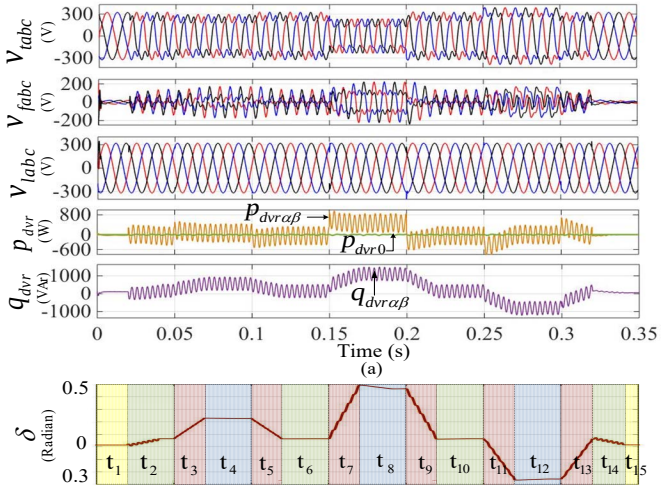

Fig. 9. Simulation results during compensation of voltage distortion: (a) grid terminal voltage, DVR injection voltage, load voltage, active, reactive power and (b) load angle δ.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2850009, IEEE Transactions on Industrial Electronics

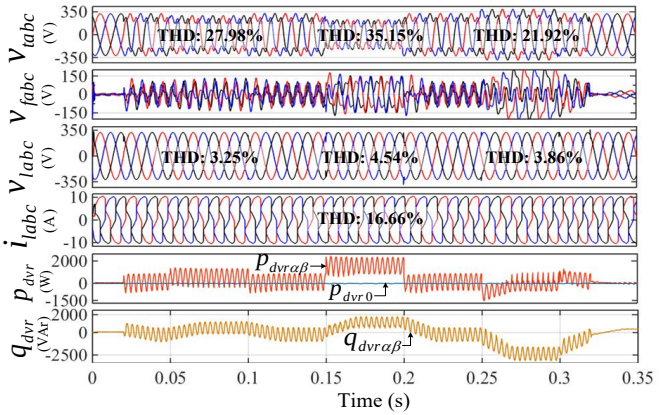

Fig. 10. Simulation results during compensation of voltage distortion with the presence of nonlinear load.

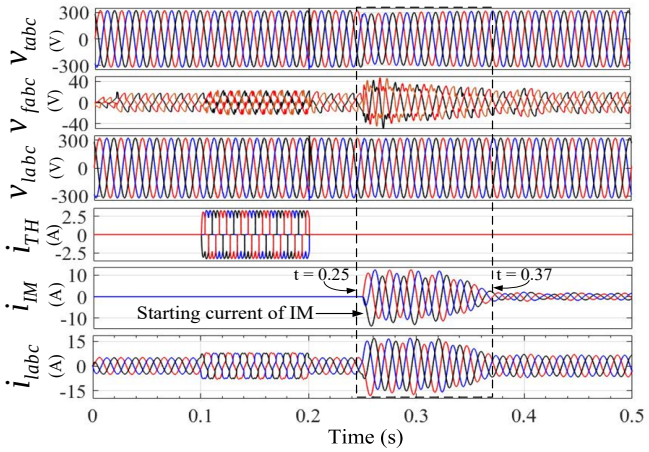

Fig. 11. Simulation results of compensated load voltage during switched load conditions.

reactive power depending upon the comparison of grid reactive power and load reactive power. But DVR has to supply active power and total load reactive power during high depth sag (i.e., 0.15 s to 0.2 s) for full load voltage compensation.

The DVR performance during single phase sag/swell (which are more common than three phase sag) and corresponding active and reactive power requirement for DVR are shown in Fig. 8. From the results, it is observed that DVR compensates the load voltage effectively and during low depth sag and swell, the mean active power required for load voltage compensation is nearly zero.

The DVR performance under distorted grid terminal voltage is shown in Fig. 9(a), where a voltage distortion occurs at 0.02 s to 0.32 s. It is observed that the DVR circuit is capable enough to compensate voltage distortion and sag/swell together. During grid voltage distortion, change in angle δ is shown in Fig. 9(b), where angle δ changes smoothly at t_3, t_5, t_7, t_9, t_{11} and t_{13} to optimize the active power requirement for the DVR.

In order to show the wide range of operation of the proposed DVR, a simulation study is conducted with the presence of 3-ϕ nonlinear load(diode bridge) and distorted grid voltages which is shown in Fig. 10. It is observed that the DVR maintains the load voltage Total Harmonic Distortion (THD) within specified value (i.e., THD<5%) for different grid voltage distortions. The results are compared to the reference [21] and are given in Table III.

TABLE III
COMPARISON OF COMPENSATION DURING GRID VOLTAGE DISTORTION

Measurement	Load voltage THD (%)	Load current THD (%)	Grid terminal voltage THD (%)
Reference [21]	5.2	40.5	13
Proposed scheme	4.54	16.66	35.15

In order to show the effectiveness of the proposed control scheme, the scheme is tested for load change consisting of TB nonlinear load and IM load. The results are shown in Fig. 11. It is observed from Fig. 11 that at 0.1 s nonlinear load is turned on and it is present till 0.2 s. After that, IM load is turned on at 0.25 s till 0.5 s. Due to the transient starting current of the IM, a voltage dip occurs at 0.25 s and settles at 0.37s as shown in Fig. 11 with dashed line. It is noticed from Fig. 11 that the DVR effectively compensates the voltage dip at load bus due to the starting of IM.

The dynamic performance of the proposed control scheme has been compared with references [17] and [22]. The proposed scheme shows the settling time t_s of the DVR active power as 0.02 s which is better than DVR control schemes [17] ($t_s = 0.06$) and [22] ($t_s = 0.04$).

VIII. Experimental Results

A photograph of a reduced scale experimental prototype of DVR is shown in Fig. 12. The grid voltage is considered as 50 V (RMS) and other circuit parameters are same as that of simulation studies as given in Table II. The hardware setup consists of an Elgar programmable power source, inductive load, inverter, LC filter, single phase injection transformer and MicroLabBox-dSPACE. The digital controller is implemented in the dSPACE, which processes the control algorithm based on measured input and generates the pulses for the inverter. The performance of the control algorithm for DVR has been tested in the following conditions

- Steady-state voltage compensation

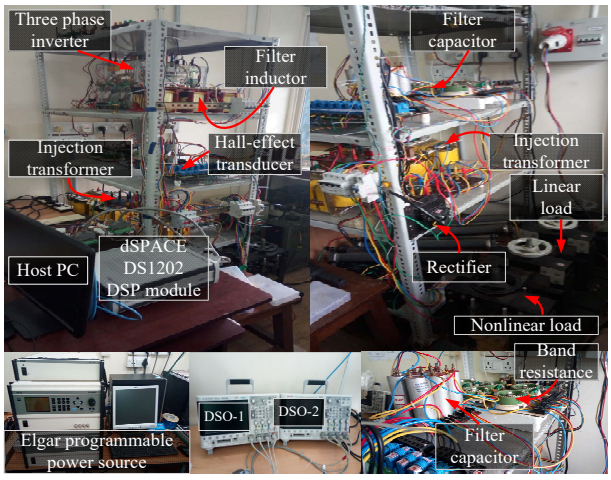

Fig. 12. Laboratory experimental setup.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2850009, IEEE Transactions on Industrial Electronics

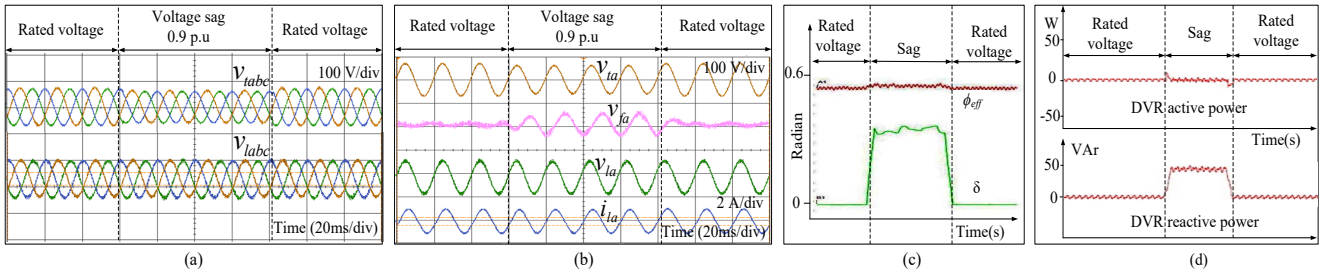

Fig. 13. Experimental results during low depth balanced sag (i.e., $V_{te} \geq V_{min}$) compensation: (a) three phase terminal voltages and load voltages, (b) phase-a terminal voltage, injection voltage, load voltage and line current, (c) power factor angle ϕ_{eff} and angle δ and (d) DVR supplied active power ($p_{dvr\alpha\beta}$), reactive power ($q_{dvr\alpha\beta}$).

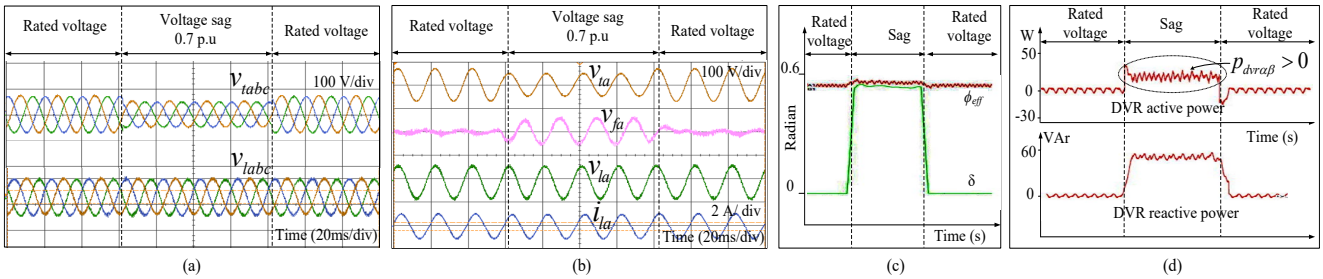

Fig. 14. Experimental results during high depth balanced sag (i.e., $V_{te} < V_{min}$) compensation: (a) three phase terminal voltages and load voltages, (b) phase-a terminal voltage, injection voltage, load voltage and line current, (c) power factor angle ϕ_{eff} and angle δ and (d) DVR supplied active power ($p_{dvr\alpha\beta}$), reactive power ($q_{dvr\alpha\beta}$).

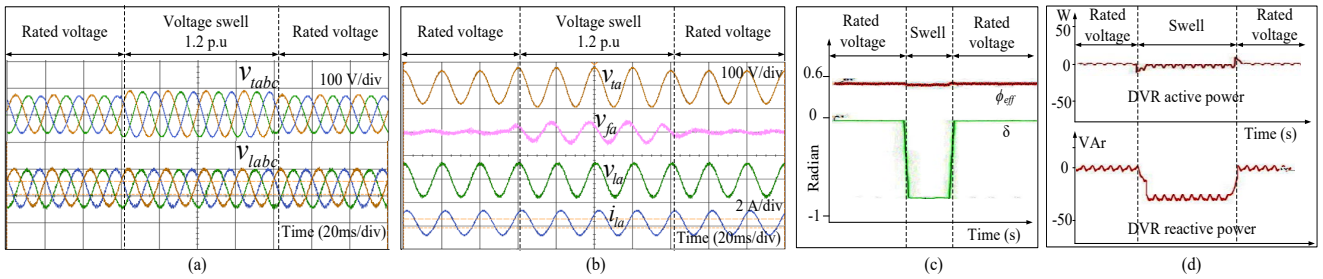

Fig. 15. Experimental results during balanced swell compensation: (a) three phase terminal voltages and load voltages, (b) phase-a terminal voltage, injection voltage, load voltage and line current, (c) power factor angle ϕ_{eff} and angle δ and (d) DVR injected active power ($p_{dvr\alpha\beta}$), DVR supplied reactive power ($q_{dvr\alpha\beta}$).

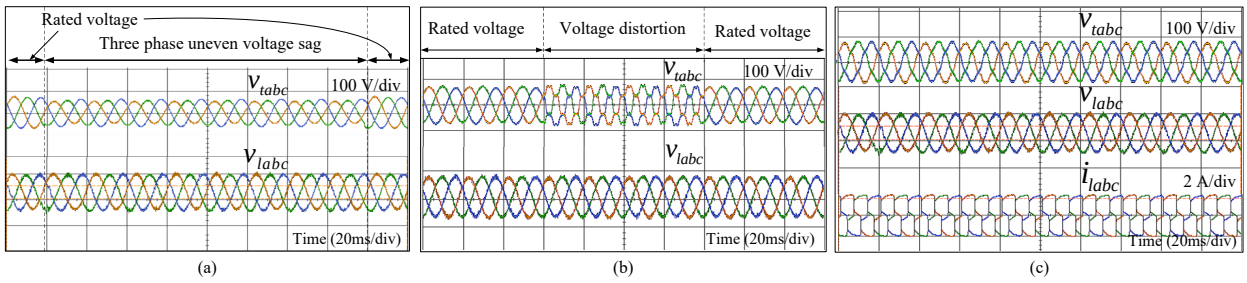

Fig. 16. Experimental result during (a) single phase voltage sag compensation, (b) compensation of grid voltage distortion and (c) compensation of grid voltage distortion with the presence of nonlinear load.

- Dynamic sag compensation
- Dynamic swell compensation
- Unbalanced and distorted grid voltage compensation.

The DVR performance during low depth dynamic voltage sag compensation is shown in Fig. 13. A sudden voltage sag of 0.9 pu (i.e., V_{te} = 0.9 pu $> V_{min}$) appears at the grid terminal end for four cycles and the corresponding compensated load voltage is shown in Fig. 13(a). During voltage compensation, phase-a parameters (i.e., terminal voltages, injection voltages, load voltages and line currents) are shown in Fig. 13(b). Load power factor angle ϕ_{eff} and change in position angle δ are shown in Fig. 13(c). The active and reactive powers required

for the DVR operation are shown in Fig. 13(d), which clearly shows that DVR needs to supply part of the load reactive power but does not require active power for load voltage compensation.

The DVR performance during high depth voltage sag compensation is shown in Fig. 14. A sudden voltage sag of 0.7 pu (i.e., V_{te} = 0.7 pu $<V_{min}$) occurs at grid terminal end for four cycles and the corresponding compensated load voltage is shown in Fig. 14(a). During voltage compensation phase-a parameters (i.e., terminal voltages, injection voltages, load voltages and line currents), power factor angle ϕ_{eff} and change in angle δ are shown in Fig. 14(b) and (c). The active power and reactive powers of DVR are shown in Fig. 14(d). These results indicate that the DVR needs to supply required amount of active power and total load reactive power for full load voltage compensation, when effective terminal voltage V_{te} falls below V_{min}.

The DVR performance during dynamic voltage swell compensation is shown in Fig. 15. A sudden voltage swell of 1.2 pu occurs at the grid terminal end for four cycles and the corresponding compensated load voltage is shown in Fig. 15(a). During load voltage compensation phase-a parameters (i.e., terminal voltages, injection voltages, load voltages and line currents) are shown in Fig. 15(b) and the load power factor angle ϕ_{eff} and change in angle δ for minimum active power injection are shown in Fig. 15(c). The active and reactive powers required for the DVR are shown in Fig. 15(d). From the results, it is observed that the DVR mitigates voltage swell making use of reactive power only.

Compensation of unbalanced voltage sag (i.e., single phase sag) and distorted grid voltages are shown in Fig. 16(a) and (b). Compensation of grid voltage distortion with the presence of nonlinear load is shown in Fig. 16(c). In each case, DVR maintains the load voltages as rated value. Therefore, the performance of the proposed DVR algorithm for series voltage compensation is satisfactory in terms of full load voltage compensation, while optimizing the active power requirement.

IX. Conclusion

A simple DVR control algorithm based on ISP and dual P-Q theory has been developed to generate the instantaneous reference voltage of the DVR to compensate load voltage. Depending upon the grid terminal voltage and load currents, the DVR compensates the load voltages with the optimized active power flow through DVR. This results in a reduction of DC energy storage requirement. This strategy is generalized enough to compensate not only short-term voltage disturbances but also support the load during long-term voltage disturbances, if there is a sufficient active power support from the dc link. The detailed simulation and experimental studies demonstrate that the proposed DVR control algorithm can compensate the load voltage effectively with the presence of nonlinear load and distorted grid voltages.

References

[1] R. S. Vedam and M. S. Sarma, "Power quality: Var compensation in power systems," *CRC Press 2009*, Boca Raton, FL,USA.

[2] J. A. Martinez and J. Martin-Arnedo, "Voltage sag studies in distribution networks-partI: system modeling," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1670–1678, July 2006.

[3] M. G. Simes and F. A. Farret, *POWER QUALITY ANALYSIS*. Wiley-IEEE Press, 2017.

[4] "IEEE recommended practices and requirements for harmonic control in electrical power systems," *IEEE Std 519-1992*, pp. 1–112, April 1993.

[5] M. Farhoodnea, A. Mohamed, and H. Shareef, "A comparative study on the performance of custom power devices for power quality improvement," in *2014 IEEE Innovative Smart Grid Technologies - Asia (ISGT ASIA)*, May 2014, pp. 153–157.

[6] C. Kumar and Mahesh K. Mishra, "Operation and control of an improved performance interactive dstatcom," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6024–6034, Oct 2015.

[7] S. B. Karanki, N. Geddada, Mahesh K. Mishra, and B. K. Kumar, "A modified three-phase four-wire upqc topology with reduced dc-link voltage rating," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3555–3566, Sept 2013.

[8] A. Ghosh and G. Ledwich, "Compensation of distribution system voltage using dvr," *IEEE Trans. Power Del.*, vol. 17, no. 4, pp. 1030–1036, Oct 2002.

[9] D. M. Vilathgamuwa, A. A. D. R. Perera, and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," *IEEE Trans. Power Del.*, vol. 18, no. 3, pp. 928–936, July 2003.

[10] C. Kumar and Mahesh K. Mishra, "Predictive voltage control of transformerless dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2693–2697, May 2015.

[11] M. I. Marei, E. F. El-Saadany, and M. M. A. Salama, "A new approach to control dvr based on symmetrical components estimation," *IEEE Trans. Power Del.*, vol. 22, no. 4, pp. 2017–2024, Oct 2007.

[12] P. Li, L. Xie, J. Han, S. Pang, and P. Li, "New decentralized control scheme for a dynamic voltage restorer based on the elliptical trajectory compensation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6484–6495, Aug 2017.

[13] S. S. Choi, J. D. Li, and D. M. Vilathgamuwa, "A generalized voltage compensation strategy for mitigating the impacts of voltage sags/swells," *IEEE Trans. Power Del.*, vol. 20, no. 3, pp. 2289–2297, July 2005.

[14] F. B. Ajaei, S. Afsharnia, A. Kahrobaeian, and S. Farhangi, "A fast and effective control scheme for the dynamic voltage restorer," *EEE Trans. Power Del.*, vol. 26, no. 4, pp. 2398–2406, Oct 2011.

[15] M. Danbumrungtrakul, T. Saengsuwan, and P. Srithorn, "Evaluation of dvr capability enhancement-zero active power tracking technique," *IEEE Access*, vol. 5, pp. 10 285–10 295, 2017.

[16] A. M. Rauf and V. Khadkikar, "An enhanced voltage sag compensation scheme for dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2683–2692, May 2015.

[17] H. K. Al-Hadidi, A. M. Gole, and D. A. Jacobson, "Minimum power operation of cascade inverter-based dynamic voltage restorer," *IEEE Trans. on Power Del.*, vol. 23, no. 2, pp. 889–898, April 2008.

[18] T. Jimichi, H. Fujita, and H. Akagi, "Design and experimentation of a dynamic voltage restorer capable of significantly reducing an energy-storage element," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 817–825, May 2008.

[19] C. Meyer, R. W. D. Doncker, Y. W. Li, and F. Blaabjerg, "Optimized control strategy for a medium-voltage DVR theoretical investigations and experimental results," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2746–2754, Nov 2008.

[20] P. Kanjiya, B. Singh, A. Chandra, and K. Al-Haddad, "SRF theory revisited to control self-supported dynamic voltage restorer (DVR) for unbalanced and nonlinear loads," *IEEE Trans. Ind. Appli.*, vol. 49, no. 5, pp. 2330–2340, Sept 2013.

[21] A. Javadi, A. Hamadi, L. Woodward, and K. Al-Haddad, "Experimental investigation on a hybrid series active power compensator to improve power quality of typical households," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4849–4859, Aug 2016.

[22] P. Jayaprakash, B. Singh, D. P. Kothari, A. Chandra, and K. Al-Haddad, "Control of reduced-rating dynamic voltage restorer with a battery energy storage system," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1295–1303, March 2014.

[23] D. Somayajula and M. L. Crow, "An integrated dynamic voltage restorer-ultracapacitor design for improving power quality of the distribution grid," *IEEE Trans. Sustain. Energy*, vol. 6, no. 2, pp. 616–624, April 2015.

[24] A. M. Gee, F. Robinson, and W. Yuan, "A superconducting magnetic energy storage-emulator/battery supported dynamic voltage restorer," *IEEE Trans. Energy Convers.*, vol. 32, no. 1, pp. 55–64, March 2017.

[25] S. Kim, H. G. Kim, and H. Cha, "Dynamic voltage restorer using switching cell structured multilevel AC AC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8406–8418, Nov 2017.
[26] G. A. de Almeida Carlos, C. B. Jacobina, J. P. R. A. Mello, and E. C. d. Santos, "Cascaded open-end winding transformer based DVR," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1490–1501, March 2018.
[27] P. Li, L. Xie, J. Han, S. Pang, and P. Li, "A new voltage compensation philosophy for dynamic voltage restorer to mitigate voltage sags using three-phase voltage ellipse parameters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1154–1166, Feb 2018.
[28] A. P. Torres, P. Roncero-SÃ¡nchez, and V. F. Batlle, "A two degrees of freedom resonant control scheme for voltage-sag compensation in dynamic voltage restorers," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4852–4867, June 2018.
[29] D. L. Milanez and A. E. Emanuel, "The instantaneous-space-phasor: a powerful diagnosis tool," *IEEE Trans. Instrum. Meas.*, vol. 52, no. 1, pp. 143–148, Feb 2003.
[30] A. E. Emanuel and D. L. Milanez, "Clarke's alpha, beta, and zero components: A possible approach for the conceptual design of instrumentation compatible with ieee std. 1459," *IEEE Trans. Instrum. Meas.*, vol. 55, no. 6, pp. 2088–2095, Dec 2006.
[31] S. Aunet, Y. Berg, and T. Saether, "Discussion of instantaneous reactive power PQ theory and power properties of three-phase systems"," *IEEE Trans. Neural Netw.*, vol. 14, no. 6, pp. 1582–1582, Nov 2003.
[32] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, pp. 625–630, May 1984.
[33] G. A. d. A. Carlos, C. B. Jacobina, and E. C. dos Santos, "Investigation on dynamic voltage restorers with two dc links and series converters for three-phase four-wire systems," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1608–1620, March 2016.
[34] S. Sasitharan and Mahesh K. Mishra, "Constant switching frequency band controller for dynamic voltage restorer," *IET Power Electron.*, vol. 3, no. 5, pp. 657–667, September 2010.

Manik Pradhan (S'16) was born in Contai, West Bengal, India. He received the B.Tech. degree in electrical engineering from Narula Institute of Technology, Kolkata, India, affiliated with West Bengal University of Technology, Kolkata, India, in 2014. He is currently working toward the M.S. by Research degree in electrical engineering at the Indian Institute of Technology Madras, Chennai, India.

His research interests include power electronic applications in power systems, power quality, electric vehicle and renewable energy system.

Mahesh K. Mishra (S'00-M'02-SM'10) received the B.Tech. degree from College of Technology Patnagar, India, in 1991, the M.E degree from the Indian Institute of Technology, Roorkee, India, in 1993, and the Ph.D. degree from the Indian Institute of Technology, Kanpur, India, in 2002, all in electrical engineering.

He has about 28 years of teaching and research experience. For about ten years, he was with the Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur, India. He is currently a professor with the Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai, India. His research interests include the areas of power distribution system, power quality, power electronics, microgrids and renewable energy systems.

Dr. Mishra is a Life Member of the Indian Society of Technical Education. He received the IETE prof. Bimal Bose Award in 2015 and elected as Fellow of the Indian National Academy of Engineering (INAE) in 2017 for his contribution towards research. He serves as an Editor for the IEEE Transactions on Sustainable Energy.