Design of a Low-Power Linear SAR-Based All-Digital Delay-Locked Loop

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***Abstract*— A 500 MHz to 1.5 GHz 8-bit SAR-based all-digital delay-locked loop (ADDLL) designed and simulated in a 130 nm CMOS technology is presented in this paper. The proposed ADDLL employs a novel digitally controlled delay line (DCDL), which presents a good linearity for the SAR code-delay curve and low power consumption. Compared to other SAR-based ADDLLs, there is no complex binary to thermometer decoder in the proposed DCDL that leads to low power dissipation and small area. Based on the simulation results, the proposed DCDL is fully monotonic and exhibits a good performance in terms of linearity at all PVT corners. The presented ADDLL locks in 32 cycles of input clock and dissipates 1.15 mW at 1.5 GHz clock frequency and 1.2 V supply voltage.**

Keywords*— *All-digital delay-locked loop (ADDLL), Successive approximation register (SAR), Digitally controlled delay line (DCDL)

I. INTRODUCTION

With the advances in CMOS technology and the reduction of transistors sizes, the number of transistors on a chip and the frequency of the circuits have increased. This increase in frequency and transistor count on a chip results in significant clock skew problem, especially in high performance and synchronous systems [1],[2]. Phase-locked loops (PLLs) and delay-locked loops (DLLs) are widely employed in clock and data recovery systems (CDR) [3], DRAM interfaces [4],[5] and high performance microprocessors [6] to reduce the clock skew problem and improve the I/O timing margins.

PLLs are high-order systems with sophisticated design concepts. Their loop bandwidth may change due to process, voltage, temperature and load (PVTL) variations. Furthermore, the voltage controlled oscillator (VCO) accumulates jitter over oscillation cycles because of its feedback structure. DLLs are preferred due to easier design, lower jitter, lower power consumption and smaller area compared to PLLs [7]-[9].

A DLL consists of a variable delay line, a phase detector and a controller circuit. The phase detector compares the reference clock with the delayed signal by the variable delay line. The controller block changes the delay of the variable delay line according to the output of the phase detector to insert desired delay time between reference clock and output clock [1].

Conventional analog DLLs [10],[11] have the advantage of good performance in clock skew and jitter [12] but these structures suffer from large area and power dissipation, long locking time and PVT-sensitive characteristics [7],[13]-[15]. On the other hand, digital DLLs benefit from low chip area and power consumption, process immunity, fast locking time and easy migration to the advanced technologies but suffer from poor jitter performance [4],[15].

Based on the controller circuit, digital DLLs can be grouped into four categories [15],[16]. The first one is the register-controlled DLL [17]. This type of DLL suffers from long locking time and high power consumption because the locking time and number of delay cells increase exponentially with the value of control code [1],[15]. The second type is the counter-controlled DLL [18] which adopts an up/down counter and binary weighted delay line. This structure needs fewer number of delay elements compared to the register-controlled approach. However, the locking time of the counter-controlled DLL is similar to the register-controlled DLL [1],[15]. The third category is the successive-approximation register (SAR)-controller DLL [1]. This approach can reduce locking time and hardware complexity by adopting binary search algorithm but due to its open-loop characteristics, cannot track PVTL variations [15]. The last one is the time to digital (TDC)-based DLL [16]. Its locking time is the shortest among other types of DLLs but needs large area and power consumption [15].

In this paper, an SAR-based all digital delay-locked loop (ADDLL) is proposed which presents a good linearity for the SAR code-delay curve of the digitally controlled delay line (DCDL) and has low power consumption. In the proposed digitally controlled delay line there is no complex binary to thermometer decoder that leads to low power dissipation and small chip area. In order to track PVTL variations, once the ADDLL locks, the SAR controller circuit is converted into a counter.

This paper is organized as follows. Section II describes the structure and circuits of the proposed SAR-based ADDLL. The simulation results of the proposed ADDLL are illustrated in section III. Finally, some conclusions are given in section IV.

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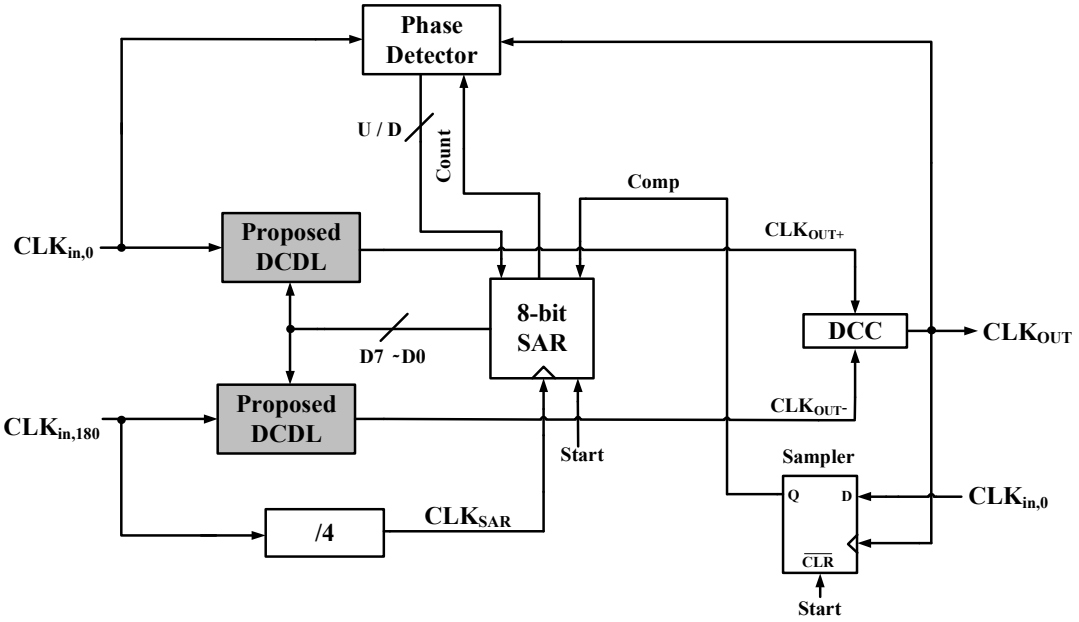

Fig. 1. Block diagram of the proposed SAR-based ADDLL.

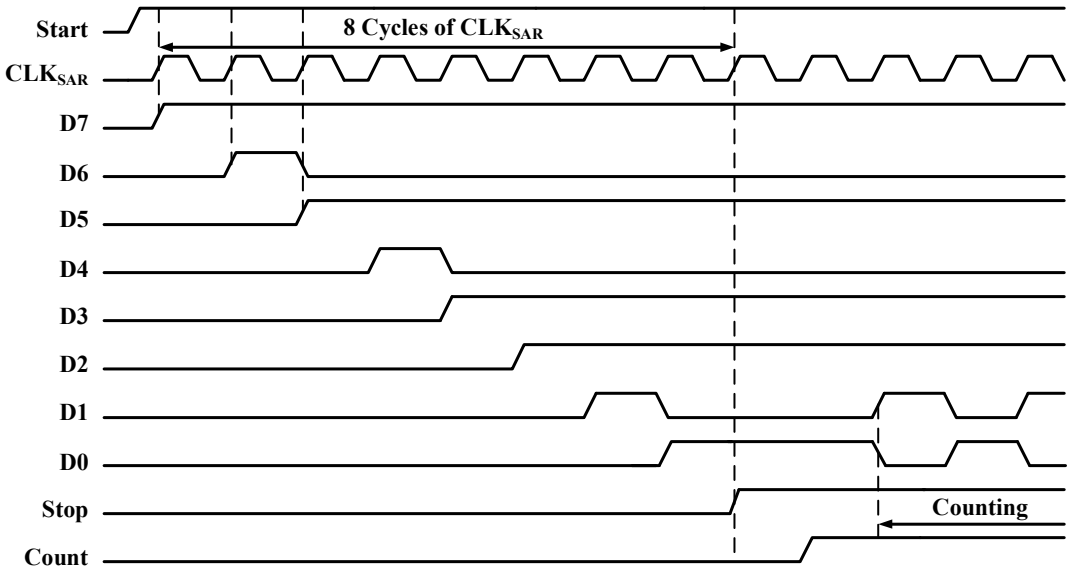

Fig. 2. Timing diagram of the proposed SAR-based ADDLL.

II. Architecture and Circuit Description of the Proposed ADDLL

The proposed SAR-based all-digital DLL is shown in Fig. 1. This structure is similar to the structure presented in [7] with the difference that the number of SAR bits and architecture of digitally controlled delay line (DCDL) has changed. The proposed DLL consists of two DCDLs, an 8-bit SAR controller circuit, a digital phase detector, a frequency divider, a duty cycle corrector (DCC) [22] and a D-type flip-flop (DFF) as a sampler. The timing diagram of the proposed DLL is shown in Fig. 2. When the Start signal goes to logic one, the binary search begins. At first, the most significant bit (MSB) is logic one and the other bits stay zero. With the first rising edge of the CLK_{SAR}, the control SAR code changes the delay of DCDLs and the delayed signals CLK_{OUT+} and CLK_{OUT-} are merged by the DCC circuit and generate CLK_{OUT}. CLK_{IN0} and CLK_{OUT} are compared by the sampler and according to the output of the sampler the MSB stays logic one or goes to zero. The binary search continues until all of the control bits are specified. When the binary search is complete, the stop signal arises and the SAR controller converted into an 8-bit counter for closed-loop operation. At the end, the signal stop goes to logic one in order to activate the digital phase detector to track PVTL variations. The key components of the proposed ADDLL is described in the following subsections.

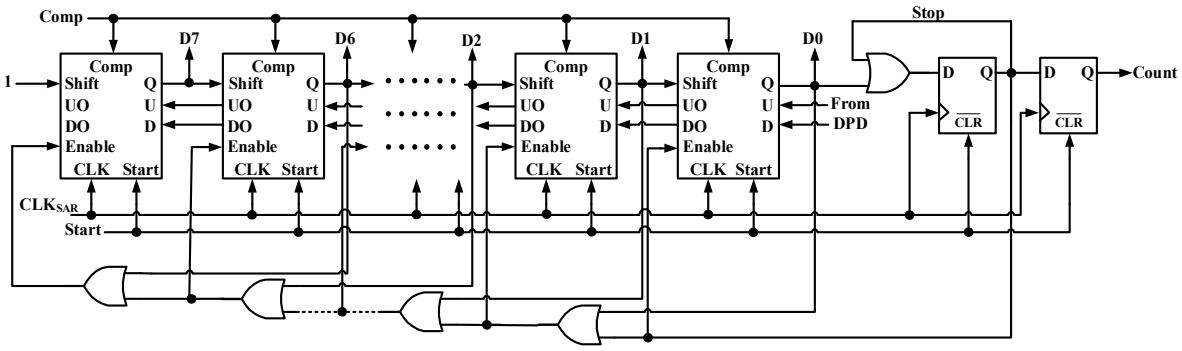

Fig. 3. SAR controller circuit.

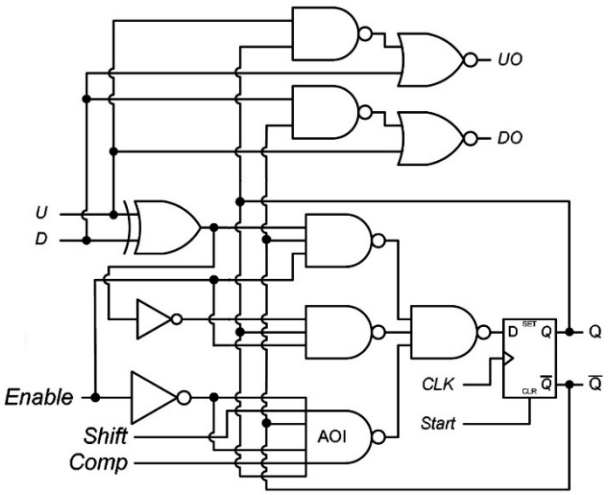

Fig. 4. Schematic of the SAR unit [7].

A. SAR controller

The 8-bit SAR controller schematic is shown in Fig. 3. It consists of eight SAR units, two DFFs, and eight OR gates. In the binary searching mode, the control bit D7 goes to logic one and the signal comp determines that the D7 stays at logic one or goes to zero. After that, D6 goes to logic one and latch the value of D7. This procedure continues until all of the control bits are specified. At the end, the signal stop arises to ensure that all of the SAR bits have been stabilized. Afterwards, the signal count goes to logic one and the SAR controller circuit converted into a counter and the closed-loop operation is achieved. The SAR unit is illustrated in Fig. 4 [7]. It consists of a number of logic gates that determine each one of the control bits according to the input control signals. While the signal Enable is logic one, the signals Shift and Comp are ignored and the signals U and D decide the output of the SAR units.

B. Digitally controlled delay line

The digitally controlled delay line (DCDL) is the most power and chip area consumer in an ADDLL and its code-delay curve linearity is one of the important features that needs to be considered. The proposed DCDL is illustrated in Fig. 5. It consists of a coarse delay line (CDL) and a fine delay line (FDL). Unlike the presented DCDLs in [14],[21], this structure does not adopt any complex binary to thermometer decoders, which causes remarkable reduction in power consumption and chip area.

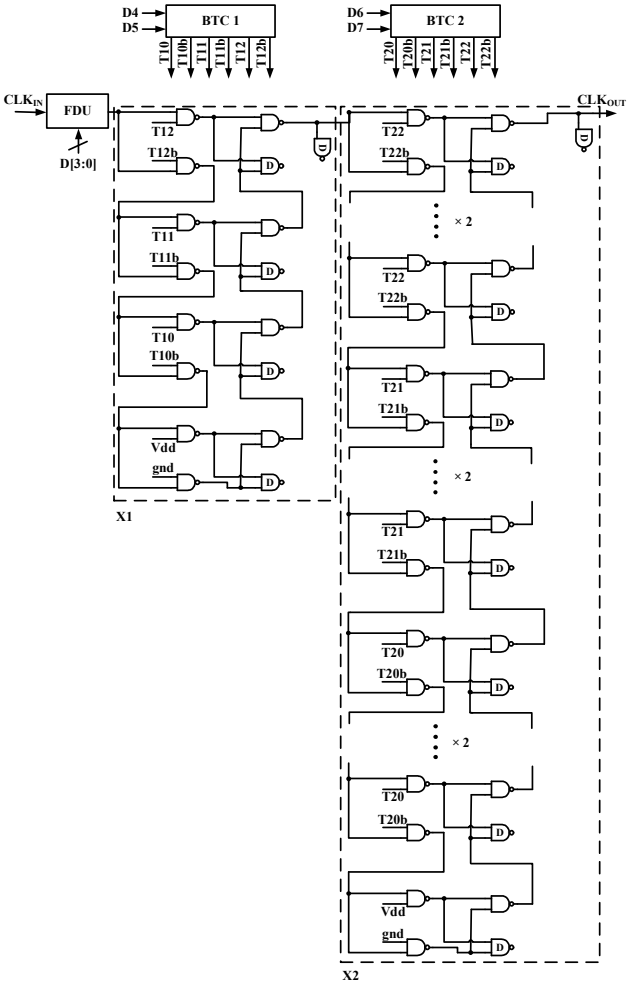

Fig. 5. Schematic of the proposed DCDL.

The CDL consists of two binary weighted groups [16] X1 and X2. In the group X1, there is 17 NAND gates. If both of the control bits D4 and D5 are logic one, the output of the 2-bit BTC changes to "111" and the delay of this group equals to two NAND gate delays. The maximum delay of this group occurs when both of the control bits D4 and D5 are zero. In this situation, the delay amount to the next group equals to 8 NAND gates. The procedure of changing delay in the group X2 is similar to the group X1. The maximum delay of the whole structure occurs when all of the control codes D4-D7 goes to logic zero and equals to 34 NAND gate delays.

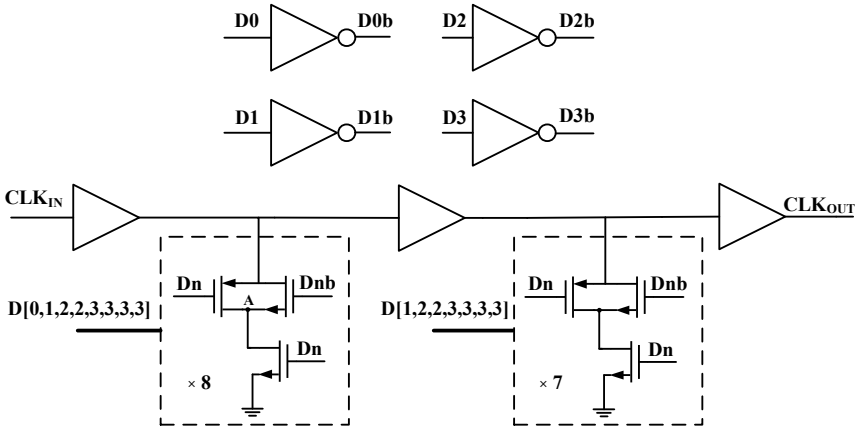

Fig. 6. Schematic of the proposed FDL.

TABLE I. COMPARISON BETWEEN THE PROPOSED FDL AND OTHER STRUCTURES.

	Power Consumption (µW)	# of transistors
Proposed FDL	70.5	65
Current starved	150.7	128
Tri-state buffer	189.7	134

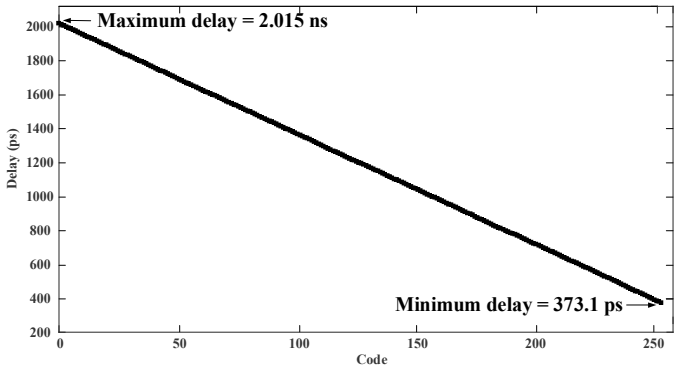

Fig. 7. SAR code-delay curve of the proposed DCDL.

The implantation of the proposed fine delay line (FDL) is illustrated in Fig. 6. This structure is a capacitor-loaded buffer chain. The active transition gates (T-gates) charge the parasitic capacitors at node A, which increases the delay amount of the FDL. The trailing NMOS discharges the node A when the T-gates are turned off. Unlike the presented FDLs in [21],[23], this structure does not employ any complex decoders and binary to thermometer converters, which causes low power consumption and chip area. Table I gives the comparisons between the proposed FDL, current starved FDL [7],[14] and tri-state buffer FDL [21] in terms of power consumption and number of transistors. .

Figure. 7. illustrates the simulated SAR code-delay curve of the proposed ADDLL. According to the maximum and minimum delay value of the DCDL, the delay resolution is 6.44 ps.

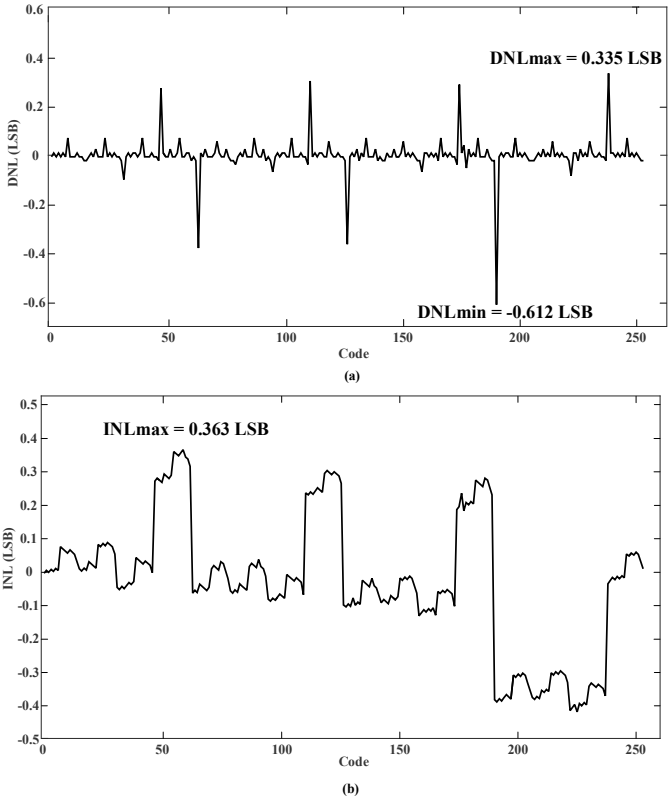

Fig. 8. (a) Simulated DNL of the proposed DCDL. (b) Simulated INL of the proposed DCDL

In order to determine the linearity of the proposed DCDL, the differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed DCDL is shown in Fig. 8. The DNL is defined as:

$$\mathrm{DNL(i)} = \frac{(T_{i-1}-T_i)-\mathrm{LSB}}{\mathrm{LSB}}, 1 \le i \le n \qquad (1)$$

where n is the number of control bits, T_i is the delay amount of the code i, and the LSB value is:

$$\mathrm{LSB} = \frac{(T_{FD}-T_{int})}{2^n-1} \qquad (2)$$

where T_{FD} is the maximum delay value and T_{int} is the intrinsic delay of the DCDL.

TABLE II. DNL VALUES AND LSB OF THE PROPOSED DCDL AT PVT CORNERS.

corner	LSB (ps)	DNL_{max} (LSB)	DNL_{min} (LSB)
SS	8.142	0.66	-0.386
FF	5.119	0.29	-0.726
FS	6.4	0.4	-0.453
SF	6.54	0.48	-0.465
0° C	6.22	0.2	-0.76
85° C	6.89	0.6	-0.289
1.1 V	7.285	0.64	-0.56
1.3 V	5.813	0.36	-0.69

The INL is given as follows:

$$INL(i) = \sum_{k=1}^{i} DNL(k) \quad (3)$$

Based on the DNL and INL results, the proposed DCDL is fully monotonic and shows a good performance in terms of linearity.

Table II shows the DNL values and LSB of the proposed DCDL at PVT corners. According to the results of this table, the DNL values is less than +1 LSB and greater than -1 LSB for all of the PVT corners, which indicates that the proposed DCDL is fully monotonic and exhibits good linearity performance at PVT corners.

C. Digital phase detector

To avoid the jitter and phase noise caused by changing the SAR code between two or three different values in counting mode, the digital phase detector in Fig. 9. is employed [7]. When the signal count arises, the signals CLK_{IN} and CLK_{OUT} are sampled by two DFFs and the output signals U and D are generated. The SAR controller in the counting phase changes its code when the signals U and D are different. If the output signals U and D are identical, the controller holds the current SAR code.

D. Duty cycle corrector

In some DLL applications like double data rate (DDR) DRAMs, in order to improve system throughputs, it is important to achieve a 50% duty-cycle ratio in the output clock signal. The duty cycle corrector (DCC) in Fig. 10. is employed in this work [22]. The signal CLK_{OUT+} turns on the transistors M_1 and M_2 and charges the node X instantly. Afterwards, the rising edge of CLK_{OUT-} discharges the node X and generates the eligible 50% duty-cycle output signal.

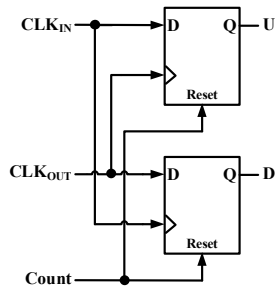

Fig. 9. Implementation of the digital phase detector [7].

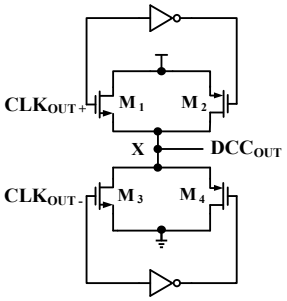

Fig. 10. Schematic of the DCC [22].

III. SIMULATIION RESULTS OF THE PROPOSED ADDLL AND COMPARISONS

The proposed ADDLL has been designed and simulated in a 130 nm CMOS technology using Cadence. Based on the SAR code-delay curve of the proposed DCDL, the ADDLL can work perfectly from 500 MHz to 1.5 GHz. The locking time is 32 clock cycles at all working frequencies. Fig. 11. and Fig. 12 . shows the transient response of the proposed ADDLL at 500 MHz and 1.5 GHz respectively. The total power consumption of the proposed ADDLL is 1.15 mW at 1.5 GHz input clock frequency.

Table III shows a performance summery and comparison between the proposed ADDLL and previous SAR-based approaches. In this table the main characteristic such as frequency range, DCDL resolution, power consumption, etc. are compared. The figure-of-merit for power consumption (FOM_{power}) is defined in [15] as follows:

$$FOM_{power} = \frac{Power\ Consumption\ (\mu W)}{Operating\ Frequency\ (MHz) \times Voltage^2\ (V^2)} \quad (4)$$

where the power consumption is represented in microwatts, the operating frequency is in megahertz and the supply voltage is in square volts.

Compared to the other works, the proposed design presents a good performance especially in terms of power consumption and delay resolution.

As shown in Table III, there is a trade-off between power consumption and frequency range. As the frequency range increases, power consumption increases too. This article emphasizes on low power consumption, which leads to the lowest FOM_{power} compared to the other SAR-based ADDLLs.

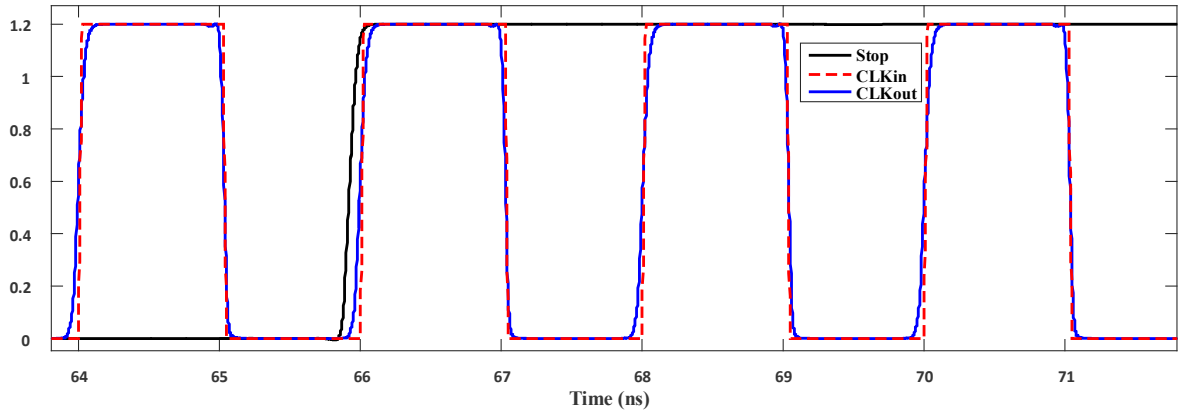

Fig. 11. Transient response of the proposed ADDLL at 500 MHz.

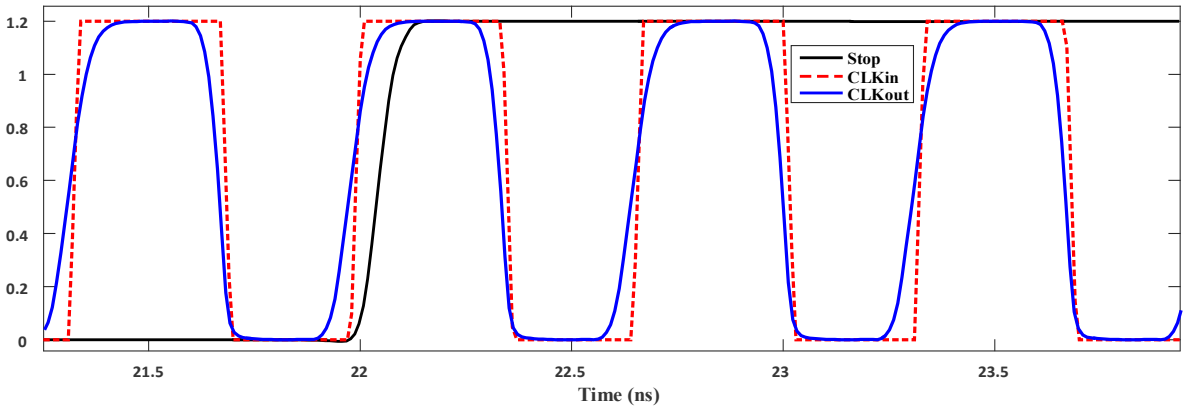

Fig. 12. Transient response of the proposed ADDLL at 1.5 GHz.

TABLE III. PERFORMANCE SUMMERIES AND COMPARISONS

	[7] JSSC 2007	[9] APCCAS 2012	[14] JSSC 2007	[19] ISPACS 2012	[20] VLSI-DAT 2013	[21] TVLSI 2015	[15] TCAS I 2018	This Work
CMOS Technology	130 nm	180 nm	180 nm	180 nm	180 nm	180 nm	130 nm	130 nm
Supply	1.5 V	1.8 V	1.8 V	1.6 V	1.8 V	1.8 V	1.2 V	1.2 V
Frequency Range	1.5 GHz – 2.5 GHz	160 MHz – 900 MHz	40 MHz – 550 MHz	66 MHz – 550 MHz	66 MHz – 1 GHz	60 MHz – 1.2 GHz	1.5 GHz – 3.3 GHz	500 MHz – 1.5 GHz
DCDL Resolution	4 ps	115 ps	10 ps	N/A	10 ps	8.99 ps	N/A	6.44 ps
Power Consumption	30 mW @2.5 GHz	15 mW @900 MHz	12.6 mW @550 MHz	10 mW @550 MHz	22 mW @1 GHz	16.2 mW @1.2 GHz	7 mW @3.3 GHz	1.15 mW @1.5 GHz
Locking Time (Cycles)	24	6	14 – 134	46 – 68	17 – 32	33	16 – 32	32
Number of SAR Bits	6	6	11	11	11	11	7	8
FOM_{power}	5.34	5.144	7.07	7.1	6.79	4.167	1.473	**0.533**
Measurement/ Simulation	M	S	M	M	S	M	M	S

IV. CONCLUSION

A low-power 8-bit SAR-based all-digital DLL is presented in this brief. In the proposed DCDL there is no intricate binary to thermometer converter, which leads to low power dissipation and chip area. The proposed ADDLL is designed and simulated in a 130 nm CMOS technology. Based on the simulation results, the proposed structure locks correctly from 500 MHz to 1.5 GHz in 32 cycles of input clock and consumes 1.15 mW from a 1.2 V supply at 1.5 GHz.

REFERENCES

[1] G.-K. Dehng, J.-M. Hsu, C.-Y. Yang, and S.-I. Liu, "Clock-deskew buffer using a SAR-controlled delay-locked loop," IEEE Journal of solid-state circuits, vol. 35, no. 8, pp. 1128-1136, Aug. 2000.

[2] G.-K. Dehng, J.-W. Lin, and S.-I. Liu, "A fast-lock mixed-mode DLL using a 2-b SAR algorithm," IEEE Journal of Solid-State Circuits, vol. 36, no. 10, pp. 1464-1471, Oct. 2001.

[3] J.-M. Lin, C.-Y. Yang, and H.-M. Wu, "A 2.5-Gb/s DLL-Based Burst-Mode Clock and Data Recovery Circuit With 4× Oversampling," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 4, pp. 791-795, May. 2015.

[4] K. Jongsun , "An anti-boundary switching fine-resolution digital delay-locked loop," Analog Integrated Circuits and Signal Processing, vol. 96, no. 3, pp. 445-454, Sep. 2018.

[5] H.-W. Lee and C. Kim, "Survey and analysis of delay-locked loops used in DRAM interfaces," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 4, pp. 701-711, Apr. 2014.

[6] A. Alvandpour, R. K. Krishnamurthy, D. Eckerbert, S. Apperson, B. Bloechel, and S. Borkar, "A 3.5 GHz 32 mW 150 nm multiphase clock generator for high-performance microprocessors," in IEEE International Solid-State Circuits Conference, Digest of Technical Papers. ISSCC. Feb. 2003, pp. 112-482.

[7] R.-J. Yang and S.-I. Liu, "A 2.5 GHz All-Digital Delay-Locked Loop in 0.13 µm CMOS Technology," IEEE Journal of Solid-State Circuits, vol. 42, no. 11, pp. 2338-2347, Nov. 2007.

[8] M. Estebsari, M. Gholami, and M. J. Ghahramanpour, "A low-power digital DLL-based clock generator in open-loop mode," Analog Integrated Circuits and Signal Processing, vol. 90, no. 2, pp. 427-434, Feb. 2017.

[9] K.-C. Kuo, C.-Y. Chang, and S.-H. Li, "A wide frequency range delay line for fast-locking and low power delay-locked-loops," in IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Dec. 2012, pp. 120-123.

[10] Y. Moon, J. Choi, K. Lee, D.-K. Jeong, and M.-K. Kim, "An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance," IEEE Journal of Solid-State Circuits, vol. 35, no. 3, pp. 377-384, Mar. 2000.

[11] H.-H. Chang, J.-W. Lin, C.-Y. Yang, and S.-I. Liu, "A wide-range delay-locked loop with a fixed latency of one clock cycle," IEEE Journal of Solid-State Circuits, vol. 37, no. 8, pp. 1021-1027, Aug. 2002.

[12] L. Wang, L. Liu, and H. Chen, "An implementation of fast-locking and wide-range 11-bit reversible SAR DLL," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57, no. 6, pp. 421-425, Jun. 2010.

[13] Y.-G. Chen, H.-W. Tsao, and C.-S. Hwang, "A fast-locking all-digital deskew buffer with duty-cycle correction," IEEE Transactions on very large scale integration (VLSI) systems, vol. 21, no. 2, pp. 270-280, Feb. 2013.

[14] R.-J. Yang and S.-I. Liu, "A 40–550 MHz harmonic-free all-digital delay-locked loop using a variable SAR algorithm," IEEE Journal of solid-state circuits, vol. 42, no. 2, pp. 361-373, Feb. 2007.

[15] Bayram, Erkan, Ahmed Farouk Aref, Mohamed Saeed, and Renato Negra. "1.5–3.3 GHz, 0.0077 mm^2, 7 mW All-Digital Delay-Locked Loop With Dead-Zone Free Phase Detector in 0.13 µm CMOS," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, pp. 39-50, Jan. 2018.

[16] S.-K. Kao, B.-J. Chen, and S.-I. Liu, "A 62.5–625 MHz anti-reset all-digital delay-locked loop," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 7, pp. 566-570, Jul. 2007.

[17] F. Lin, J. Miller, A. Schoenfeld, M. Ma, and R. J. Baker, "A register-controlled symmetrical DLL for double-data-rate DRAM," IEEE Journal of Solid-State Circuits, vol. 34, no. 4, pp. 565-568, Apr. 1999.

[18] T. Hamamoto et al., "A 667-Mb/s operating digital DLL architecture for 512-Mb DDR SDRAM," IEEE Journal of Solid-State Circuits, vol. 39, no. 1, pp. 194-206, Jan. 2004.

[19] W.-C. Chen, R.-J. Yang, C.-Y. Yao, and C.-C. Chen, "A wide-range all-digital delay-locked loop using fast-lock variable SAR algorithm," in International Symposium on Intelligent Signal Processing and Communications Systems (ISPACS), Nov. 2012, pp. 338-342.

[20] C.-Y. Yao and Y.-H. Ho, "A fast-locking wide-range all-digital delay-locked loop with a starting SAR-bit prediction mechanism," in International Symposium on VLSI Design, Automation, and Test (VLSI-DAT), Jun. 2013, pp. 1-4.

[21] C.-Y. Yao, Y.-H. Ho, Y.-Y. Chiu, and R.-J. Yang, "Designing a SAR-based all-digital delay-locked loop with constant acquisition cycles using a resettable delay line," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 3, pp. 567-574, Mar. 2015.

[22] J. Lee and B. Kim, "A low-noise fast-lock phase-locked loop with adaptive bandwidth control," IEEE Journal of Solid-State Circuits, vol. 35, no. 8, pp. 1137-1145, Aug. 2000.

[23] P. Raha, S. Randall, R. Jennings, B. Helmick, A. Amerasekera, and B. Haroun, "A robust digital delay line architecture in a 0.13 µm CMOS technology node for reduced design and process sensitivities," in Proceedings International Symposium on Quality Electronic Design, Aug. 2002, pp. 148-153.