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Protection and grounding methods in DC microgrids: Comprehensive review and analysis

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ABSTRACT

DC microgrids (DCMGs) presents an effective means for the integration of renewable-based distributed generations (DGs) to the utility network. DCMGs have clear benefits such as high efficiency, high reliability, better compatibility with DC sources and loads, and simpler control, over its AC equivalent system. While advantages of DCMGs are considerable, of particular concern are the associated protection challenges, such as lack of phasor and frequency information, rapid fault current rise, breaking DC arc and certainly the lack of standards, guidelines and practical experience. This paper presents an extensive review of fault characteristics of DCMGs and the protection challenges. Innovative protection techniques proposed to solve these issues, and comparative analysis of these techniques are presented outlining the strengths and drawbacks of each. Possible improvements to the current technologies and future directions for research, which could enhance the protection of DCMGs, are outlined in this paper.

1. Introduction

Conventional fossil fuel based power generation is one of the largest contributors to the world's greenhouse gas emissions and climate change. A rapid increase in the development of renewable energy sources (RESs) has seen in all parts of the world in recent years as countries endeavor to move towards a sustainable energy supply [1–4]. Efforts to integrate cleaner energy sources has resulted in increasing amount of distributed generators (DGs) based on RESs, such as solar photovoltaic (PV) arrays, micro wind turbines, biomass power plants and fuel cells, being integrated to the utility network. However, the increased penetration of DGs also brings along certain adverse impacts on utility grids, partly due to the intermittent nature of most RESs. The major concerns include voltage rise, power quality, protection coordination and system stability. Therefore, in order to accommodate high penetration of RES, more controllable, reliable, configurable and intelligent energy distribution systems were needed. As a result, microgrids have emerged and become an attractive arrangement for the integration of renewable-based DGs [5,6].

Microgrid is an active distribution network embedding DGs, energy storage (ES) elements and consumer loads, and capable of operating either grid-connected or as an autonomous island system. A microgrid can be carefully designed to achieve high reliability, uninterruptable power supply, increased efficiency, reduced conduction losses and better local voltages [6]. Hence, microgrids are also an effective solution to supply critical loads such as data centers, and rural areas. In addition, microgrids embedding DGs are particularly a relief to the conventional power generation and transmission infrastructure [3,4].

Increasing use of solar PV arrays, electronic loads and electric vehicles (EVs) have prompted the idea of using DC microgrid (DCMG) systems; to achieve increased efficiency due to the reduction of power conversion stages [7]. Innovations in the areas of smart homes/buildings, fast EV charging stations, vehicle to grid (V2G) technology, hybrid energy storage systems, and renewable energy parks, DCMGs are gaining increasing attention [8–11]. Although emerging as an attractive option for future power distribution systems, there are several constraints that hinder the widespread deployment of DCMGs. Protection of DCMGs is one of the key issues [8,11]. Protection challenges associated with DCMGs include [11–15]:

1) Lack of frequency and phasor information making it difficult to detect and locate faults.
2) Absence of natural zero crossings to extinguish the arc that occurs in breaker opening.
3) Fast current rise imposing strict time limits for fault interruption.

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Nomenclature

English symbols

R_f	Fault impedance
V_{dc}	DC bus voltage
V_{an}	AC side line to neutral voltage
I_{vsc}	Current through lower terminal of VSC
V_{pole+}	DC positive pole to the ground potential
I_{dc}	DC line current
I_g	Ground fault current
R_g	Ground fault impedance

Acronyms used

DCMG	DC microgrids
DG	Distributed generator
RES	Renewable energy source
PV	Photovoltaic
EV	Electric vehicle
ES	Energy storage
V2G	Vehicle to grid
PE	Power electronic
G-VSC	Grid-connected voltage source converter
DESAT	Desaturation
ACMG	AC microgrid
CB	Circuit breaker
ACCB	AC circuit breaker
HVDC	High voltage DC
MVDC	Medium voltage DC
IED	Intelligent electronic device
di/dt	Derivative of current
FTT	Fast Fourier transform
STFT	Short-time Fourier transform
WT	Wavelet transform
ANN	Artificial neural network
DWT	Discrete wavelet transform
ETO	Emitter turn off
MMC	Modular multi-level converter
FCL	Fault current limiter
DCCB	DC circuit breaker
SSCB	Solid-state circuit breaker
IGBT	Insulated gate bipolar transistor
IGCT	Insulated gate commutated transistor
ZSCB	Z source circuit breaker
SCR	Silicon controlled rectifier
SiC	Silicon Carbide
GaN	Gallium Nitride
HCB	Hybrid circuit breaker
FMS	Fast mechanical switch
CS	Commutating switch

4) Protection coordination issues due to the intermittent nature of RESs and different modes of operation.
5) Absence of protection standards, guidelines and lack of practical experience.

An adequate level of speed, sensitivity, precision, selectivity, and security, are the key requirements of an effective protection system [16]. Conventional fault detection, localizing and interruption devices are largely inadequate for DCMG protection [15,17–19].

The main objective of this paper is to present a comprehensive and analytical review on the state of the art protection techniques for DCMGs. Furthermore, an in-depth investigation has been made to identify transient fault characteristics, effects of electrical parameters on fault current, and limitations of currently available protection devices. In addition to the post fault behavior of individual converters, simulation studies are presented to investigate the overall DCMG system response under fault events. Grounding configurations utilized in DC networks are detailed, and their advantages and limitations are compared in terms of; personnel and equipment safety, fault detection capability, fault ride-through capability and minimizing stray current induced corrosion. Protection techniques, which appear to be effective and feasible to implement in DC networks are reviewed. Compared with previous review studies in Refs. [20–23], this paper presents a more detailed study into the adoption of novel data-driven DCMG protection schemes. Ground fault behavior of the network under different grounding configurations is evaluated under different considerations to provide insights into the DCMG grounding system design. Furthermore, fault current limiting converter architectures and interrupting devices adopted in DC networks are compared in detail, considering several key performance parameters.

Rest of the paper is organized as follows; Section 2 discusses different fault types in DCMGs, and provides an in-depth analysis of fault features of a DCMG. The protection challenges in DCMGs are identified in Section 3. Different grounding arrangements and design considerations in selecting a grounding arrangement for a DCMG are discussed in Section 4. Fault detection and interruption schemes that are employed or proposed for DCMG systems are discussed and compared in Sections 5 and 6, respectively. Finally, the conclusions and future trends are provided in Section 7.

2. Fault characteristics in DC microgrid systems

In this section, the DCMG fault characteristics are analyzed in order to identify the trends of voltage and currents within the network, and to get insights on the protection requirements of a DCMG. In order to analyze the fault characteristics of a DCMG system, consider the notional DCMG network shown in Fig. 1. In a DCMG, the possible fault types are pole-pole, pole-ground and AC grid faults, and are shown in Fig. 1. These faults can occur in the DC bus, within converters, AC grid, DG sources, ESs and load branches [24–26]. Pole-ground faults are the most common type of fault in a distribution network [27]. Often pole-pole faults are low impedance faults, while pole-ground faults can be either low or high impedance faults. These faults are critical for the whole network; in particular, power electronic (PE) converters and battery units [24].

Fault characteristics vary with the fault type and the fault location. Other key factors which influence the fault characteristics are fault impedance $\boldsymbol{R_f}$, microgrid topology, grounding configuration, DG interface converters and types of DG sources [7,25–30]. Under this section, transient and steady-state characteristics of DCMGs during most common faults, pole-pole and pole-ground faults are analyzed based on simulation results. These fault characteristics are important when designing fault detection, interruption schemes and protection coordination [11,25–28].

2.1. Power electronic converter fault response

A fault in the DC network causes the DC side capacitors of the power electronic (PE) converters to discharge rapidly, and DC bus voltage $\boldsymbol{V_{dc}}$, drops as a result. The fault current during the capacitor discharge depends on the total DC side capacitance and the total fault current loop impedance. The DC side capacitance is the total cumulative capacitance of grid-connected voltage source converter (G-VSC) capacitor, other converter capacitors, and line capacitances. Fault loop impedance is

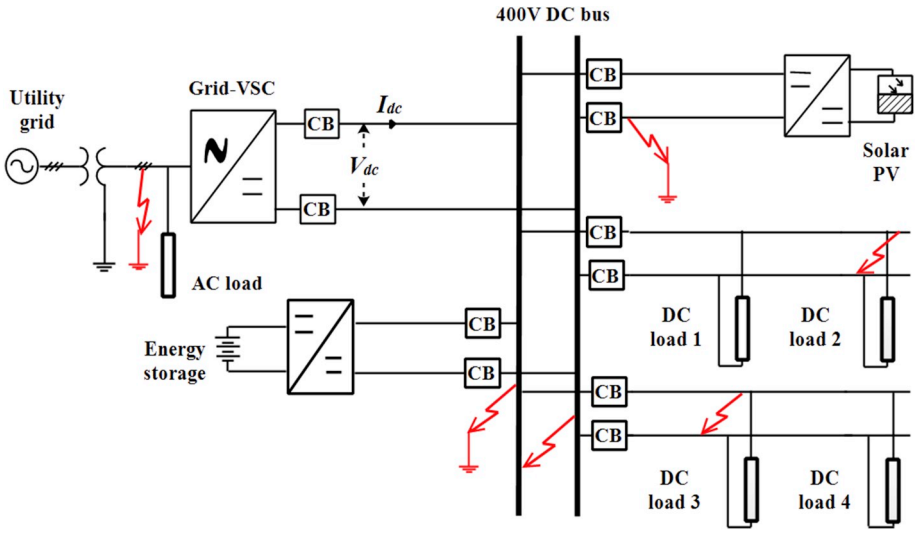

Fig. 1. Schematic diagram of the notional DCMG model.

reliant on fault impedance and fault location.

The healthy operation of an IGBT based converter is assured only when antiparallel diodes across the IGBTs are reverse biased by the DC link voltage of the converter capacitor [13]. DC bus voltage V_{dc}, drops due to initial discharge of DC side capacitance during a fault, and if V_{dc} goes below reverse bias voltage of the freewheeling diodes, PE converters may behave erratically. Fault current flow through the freewheeling diodes, and is only limited by network impedance upstream of the fault.

Commercially available IGBT based converters adopt self-protection schemes for overvoltage and overcurrent protection, and their effects must be considered when analyzing the PE converter behavior during a fault. Typically, desaturation (DESAT) protection activates within 2 μs [31,32]. However, even if the converter operation is cutoff by self-protection, PE converters may continue to conduct fault current through freewheeling diodes of the converter, only to be limited by fault loop impedance, unless fault currents are interrupted [25,26]. These diodes are sensitive to overcurrent, and the current through them must not exceed a certain magnitude, determined based on their ratings [25, 28]. DC network fault response depends on the PE converters interfacing DGs. Pole-pole fault response of two commonly used PE converters in DCMGs, two-level VSC and DC-DC boost converter is examined in the

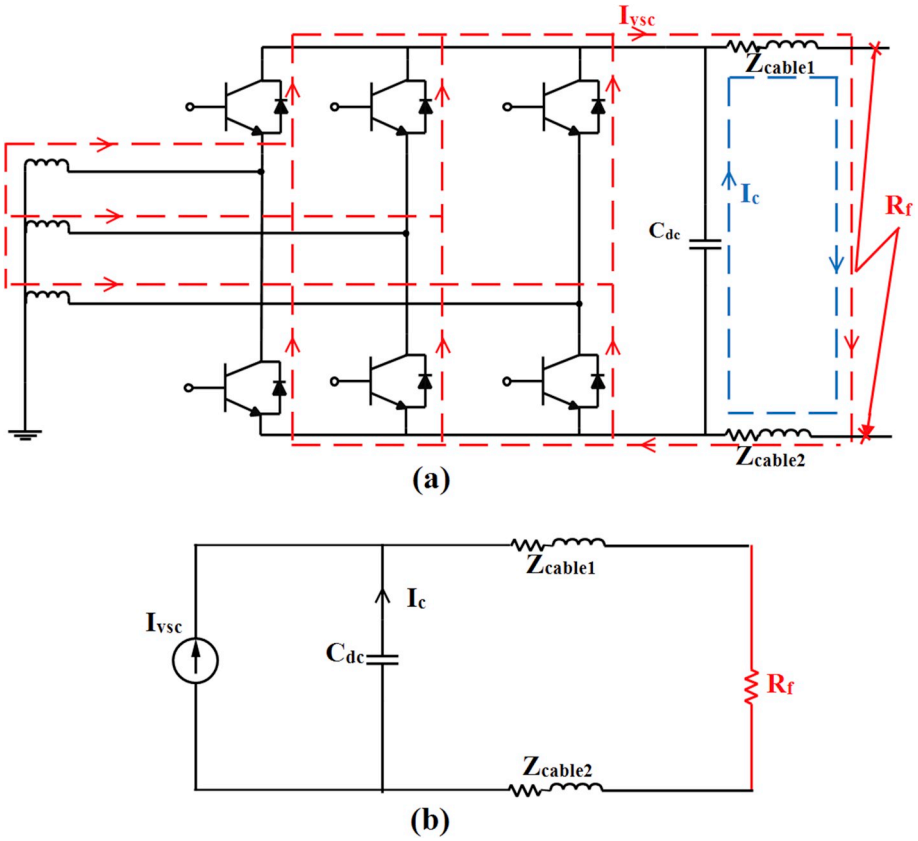

Fig. 2. (a) G-VSC with pole-pole fault, (b) Equivalent circuit for G-VSC fault current feeding through diodes.

following sub-sections.

2.1.1. G-VSC fault response

Fig. 2(a) shows a VSC with a pole-pole fault in the DC side. Low fault impedance, R_f values give rise to higher voltage drops due to DC side capacitor discharge; consequently, VSC loses its control capability [17,25,28].

To analyze the fault characteristics of VSCs, three different stages of fault response; capacitor discharge, diode freewheeling and grid current feeding stage are presented in Ref. [28]. DC link capacitor discharges immediately after a fault resulting in DC bus voltage drop. This capacitor discharge initiates the diode freewheeling and current commutate to the freewheeling diodes. Due to the potential damages to the diodes and other components, it is desirable to interrupt the fault current before the VSC reaches diode freewheeling stage. However, if suitable protective actions are not taken, the VSC will continue to feed grid current to the fault through freewheeling diodes. Fault response of VSC under each stage can be analyzed separately to derive expressions for DC link voltage and cable current; thus provides the theoretical basis for the designing of protection schemes [20,28]. Post fault behavior of a VSC is explained below in order to investigate on overall response of the DCMG system under different fault events.

During a fault, if V_{dc} drops below $1.35\sqrt{3}V_{an}$ (i.e. generated voltage by a diode rectifier), where V_{an} is the phase voltage of VSC input side, freewheeling diodes are forward biased and G-VSC is no longer PWM controlled; hence, VSC starts to work in an irregular way. As a result, DC current fed by VSC I_{vsc}, rise to a considerably higher value, exceeding the converter nominal current. Also, with IGBT control signals being blocked, there is no PWM control action by VSC [25,26], and will continue to feed fault current through diode path. The equivalent circuit for G-VSC fault current feeding, through the diode path, is shown in Fig. 2(b). However, for high R_f values, if V_{dc} is not dropped below $1.35\sqrt{3}V_{an}$, no freewheeling diode conduction occurs, and critical current levels are avoided [25,28].

2.1.2. DC-DC boost converter fault response

DGs connected to the DC bus contribute to the fault through interfacing converters. Fig. 3(a) shows a DC-DC converter with a pole-pole fault. The fault response of a boost converter is similar to that of a VSC with three stages; capacitor discharge, diode freewheeling and DG current feeding stage, and is further discussed in Ref. [20].

Similar to VSCs, DC-DC converter capacitors also contribute to the initial capacitor discharge current resulting in the V_{dc} drop. For low R_f values, if V_{dc} goes below converter input voltage, V_{in}, freewheeling diodes are forward biased. Inductor current will increase, only to be limited by fault current loop impedance. Hence, the fault current through the converter will be higher than the nominal current of the converter. The IGBTs may be blocked leaving the diodes exposed to fault currents. Fig. 3(b) shows the equivalent circuit for fault current feeding from ES through diode path.

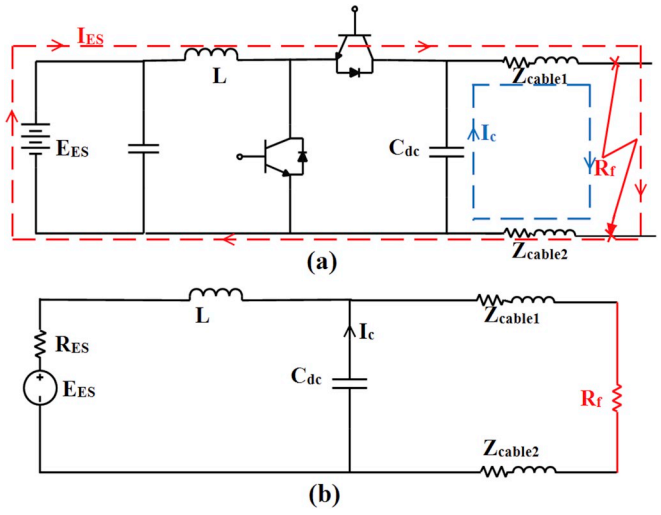

Fig. 3. (a) DC-DC converter with pole-pole fault, (b) Equivalent circuit for DC-DC converter fault current feeding through diodes.

PV interfacing DC-DC converter shows a similar fault response. However, PV plant maximum current is limited; hence, the fault current contribution from the solar PV is limited.

DC-DC buck converters show a similar fault response to that of a boost converter discussed above [20]. Post fault response of dual active bridge based DC-DC converters is presented in Ref. [20].

2.2. Pole-pole fault characteristics

A pole-pole fault is the most critical condition in a DC network, particularly because of the very high fault currents involved. Moreover, pole-pole fault on DC terminals of the network (see Fig. 1), can be considered as an additional load with low resistance [25].

As discussed in Section 2.1, depending on R_f, fault location and fault type, PE converters in a DC network show different fault responses [25,28,29]. Transient and steady-state current paths in the network during a pole-pole fault are shown in Fig. 4. The trend of DC line current, I_{dc} and V_{dc} during a pole-pole fault are shown in Fig. 5. Initially, after the fault, capacitors discharge causing a sudden drop in V_{dc}, and is shown in Fig. 5 (a). DC link capacitor discharge results in a current transient with high amplitude and very low rise time. This capacitor discharge causes a quick rise of I_{dc} and can be seen in Fig. 5(b). Current from DGs increase rapidly and flow to the fault through diode paths [24,25,28]. Pole-pole fault characteristics in a ring-type DCMG are further investigated in Ref. [33].

2.3. Pole-ground fault characteristics

Networks with different grounding configurations show different ground fault characteristics. The notional DCMG (see Fig. 1) under consideration for this analysis has the neutral point of AC side transformer solidly grounded and DC bus ungrounded. During a pole-ground fault on the terminals of the DC bus (Fig. 6), PE converters show a similar response to that of a pole-pole fault discussed in Section 2.1 [25–27,33,34].

During the ground fault V_{dc} drops and forward bias the freewheeling diodes, and AC grid, ES and solar PV plant feed the fault through diode paths as shown in Fig. 6. For the ES and PV plant, a current reclosing path for possible ground fault contribution is absent during high R_g faults [27]. However, if ground fault component through G-VSC is higher than the current flowing in the DC negative pole into the lower terminal of the G-VSC I_{vsc-}, current changes its direction and I_{vsc-} starts to flow through the lower terminal of the VSC into the DC negative pole. As a result, for low R_g values, both PV plant and the ES contribute to the ground fault, as shown in Fig. 6 [25–27].

In case of the activation of IGBT self-protection schemes, the fault current path of ES and solar PV through the VSC lower terminal is blocked off. However, the fault is still fed by the AC grid through the VSC freewheeling diode path.

The trend of DC positive pole to ground potential, V_{pole+} and ground fault current, I_g are shown in Fig. 7. It can be seen that V_{pole+} and I_g have the same frequency and waveform pattern during the fault. Ground fault characteristics of DC networks employing different grounding configurations are further analyzed in Refs. [25–27,34].

3. DC microgrid protection requirements and challenges

Designing a power network protection scheme is a comprehensive task that involves several challenges [16]. Key requirements of DCMG

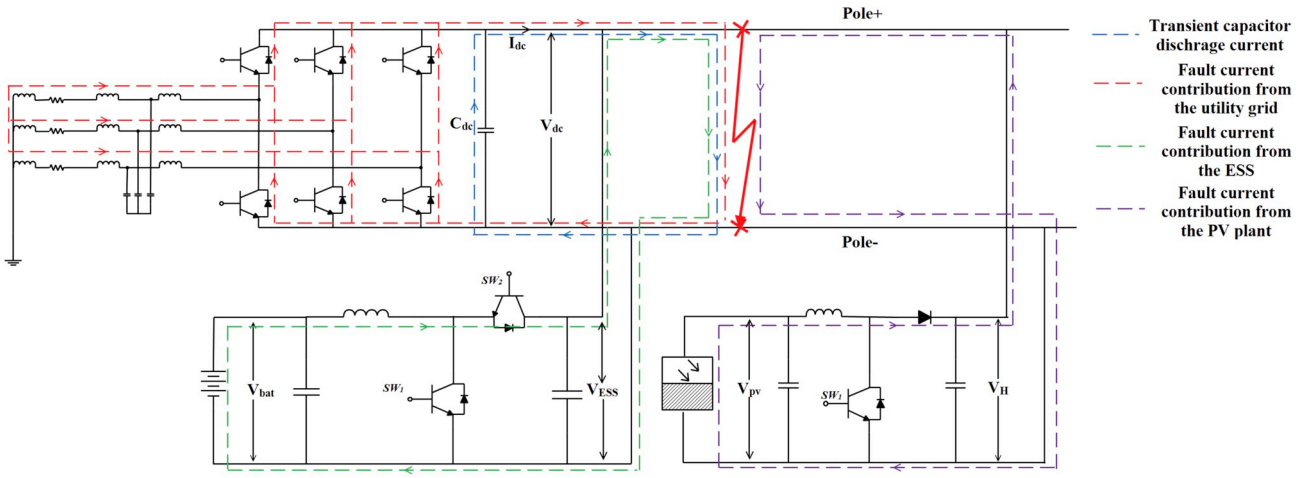

Fig. 4. Fault current flow paths during a pole-pole fault in a DCMG network [25].

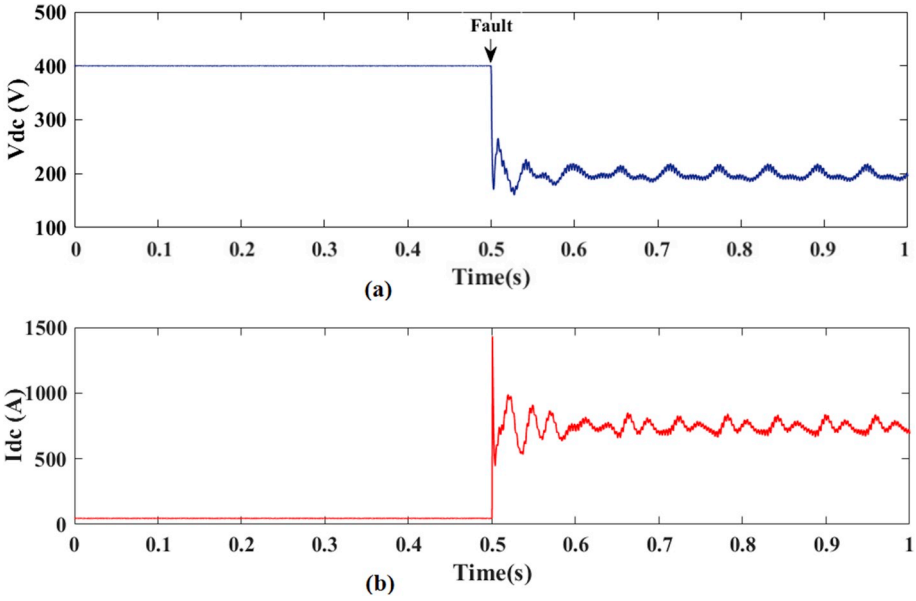

Fig. 5. Trend of (a) DC bus voltage (top), (b) DC line current (bottom), during a pole-pole fault in a DCMG.

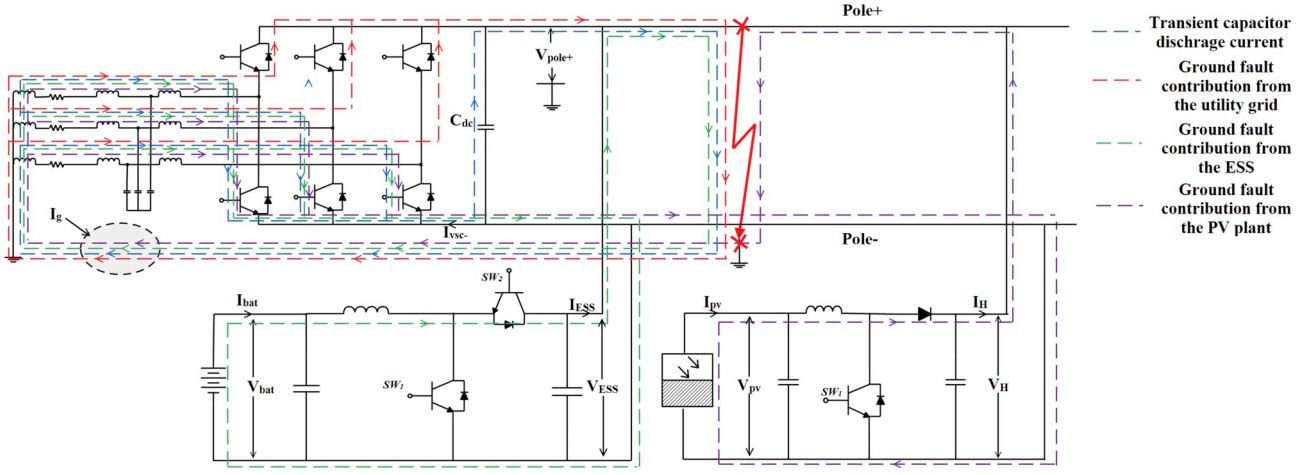

Fig. 6. Pole-ground fault current paths in a DCMG with neutral point of AC side transformer solidly grounded- DC bus ungrounded [26].

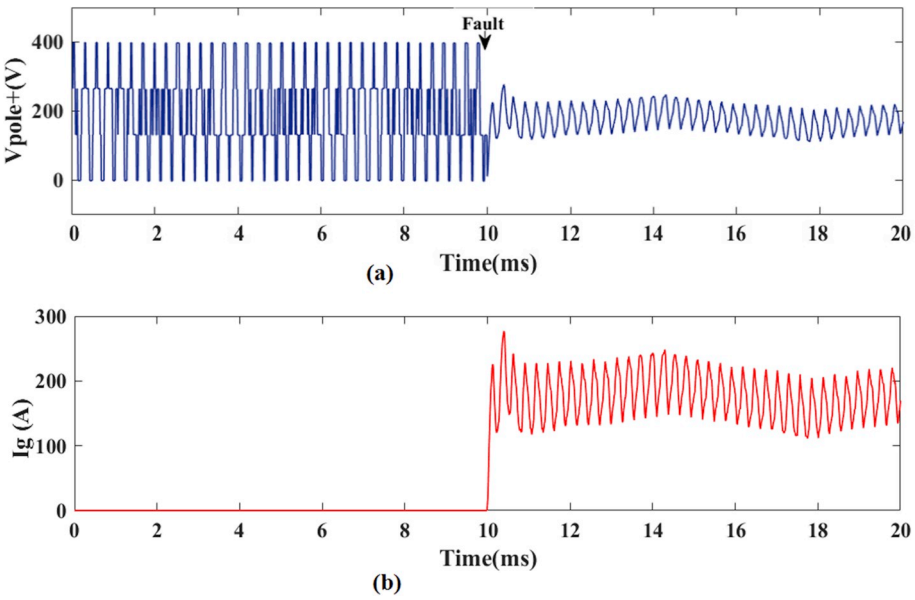

Fig. 7. Trend of (a) positive pole to ground potential (top), (b) ground fault current (bottom), during a ground fault on the DC side, in a DCMG with neutral point of AC side transformer solidly grounded- DC bus ungrounded.

protection and protection challenges are reviewed under this section. The main protection requirements include personnel and equipment safety, reliable fault detection, fast detection, minimum loss of load, fault ride-through capability and backup protection. These must be weighed against the cost of devising a protection scheme [16,19–23].

3.1. *Challenges: fault detection and discrimination*

Lack of effective techniques for fault detection in DC networks represents a major barrier to widespread adoption of DCMGs. Conventionally most of the DC networks are protected by overcurrent and differential elements. However, due to the intermittent nature of DGs connected to the network, different modes of operation and high sensitivity of network response to fault impedance, protection of DCMGs using the above mentioned conventional techniques is not straight forward; changing fault level and changing power flow direction pose challenges to relay coordination [17]. In addition, complex network architectures may lead to suboptimal fault discrimination, resulting in disconnection of healthy sections of the network. Hence, the conventional fault detection schemes have become largely inadequate [17, 20–24], and there is a need for sensitive, intelligent and adaptive DC fault detection and discrimination schemes.

Fault localizing is a crucial requirement, as quick isolation of the faulty section of the network is essential for fast recovery of the network. Line impedance and traveling wave methods have been adopted as an industry standard for fault localization in AC networks [35]. However, the inherent absence of frequency and phasor information prevents the direct adoption of line impedance based methods in DC systems [36,37]. In addition, due to the short length of distribution cables, it is difficult to obtain exact time difference, which rules out the possibility of using traveling wave methods for fault location.

AC power system protection has plenty of standards, guidelines, and experience, which can be easily translated to AC microgrids (ACMGs). Standards for protection are absent when it comes to DC systems [21,35, 36]. In addition, protection devices for AC systems are very mature and commercially available. Conversely, DC protective devices are costly, as they are specialty devices to-date. DCMG fault detection and localization techniques are discussed in Section 5.

3.2. *Challenges: fault current interruption*

AC currents naturally cross zero at every half cycle, causing the self-extinction of the arc between parting contacts of electromechanical breakers. In a DC system, however, there is no zero-crossings and demands the current to be forced to zero by additional mechanism [14,20, 38,39]. Traditional AC circuit breakers (ACCBs) have been employed for DC fault interruption, with considerable voltage and current derating [18,40]. In addition, specially designed mechanical CBs with arc chutes can be used to dissipate and cool the arc [38]. However, these require large and expensive arrangements.

DCMGs rely on PE converters for the integration of DGs and battery units. PE converters have a limited fault current withstand capability, typically in the range 2–3 times nominal load current for few tens of microseconds. In addition, DC systems have very short current rise time resulting in a rapidly increasing fault current transient. Consequently, a fault in a DCMG must be detected and interrupted quickly before reaching critical fault current levels [40]. Electromechanical CBs have a long interruption time due to their mechanical restrictions, and cannot interrupt DC fault current within the required time and current limits [37,41]. Fast breaker designs based on solid-state switches have become widely popular for DC protection [42]. However, due to their high costs, high on-state losses, large volume and weight, and susceptibility to overvoltage, it is still questionable whether they offer an effective solution [42,43]. DCMG fault interruption schemes are discussed in Section 6.

4. DC microgrid grounding

System grounding is an important factor for safe and stable operation of a power distribution network [44]. Grounding aspects of DC networks have not been fully explored, and there are still concerns about safety [42,45]. Hence, it is important to address the grounding issues and identify the grounding configurations that enable safer and more reliable operation of the network.

Grounding is a complex topic involving several design considerations and tradeoffs [45–47]. In order to contribute to a better understanding of DCMG grounding, this section will review different grounding configurations adopted, based on the following considerations [26,45];

1) Facilitation of reliable ground fault detection.
2) Fault ride-through capability during ground faults.
3) Limiting touch voltages and fault currents to safe levels.
4) Immunity to disturbances and noise in the network.
5) Minimizing stray current induced corrosion.

Safety of both personal and equipment is the main objective when designing a grounding scheme. Fault current magnitudes, fault detection capability, susceptibility to faults and voltage surges are the factors to be considered in this regard.

Compatibility of a ground fault detection scheme for a particular network depends on the grounding configuration [26,45]. In addition, the grounding configuration endows the ground fault ride-through capability to the network. While solidly grounded networks have certain positive attributes, their inability to ride-through faults and maintain service in the presence of a ground fault, outweighs in certain applications. Conversely, ungrounded or high resistance grounded systems offer good fault ride-through capability, but the network is prone to disturbances. Especially during a fault transient, aggregate pole to ground capacitance and cable inductance may lead to underdamped oscillatory overvoltages with respect to ground, that potentially cause insulation and equipment damage [47].

Corrosion due to stray current is a major problem associated with DC networks [48,49]. Structural damages to the network components due to corrosion can be avoided, by taking measures to reduce the stray current [48–51]. In a high resistance grounded or an ungrounded network, stray current will be minimized, but the network is prone to transient overvoltages, as discussed above. On the contrary, if the network is solidly grounded, transients will be quickly absorbed, but there will be high stray current. Hence, when designing a grounding scheme, considerations to be prioritized are decided according to the specific application the network being used for.

The following grounding configurations have been proposed in the literature for DCMG system grounding [20,31,47–51];

1) Ungrounded DC bus
2) High resistance grounding
3) DC bus solid grounding
4) DC bus midpoint solid grounding
5) Reconfigurable grounding

In general, a DCMG is interfaced to the AC utility grid [31]. AC grid can have different grounding configurations such as TN, TT, IT [52]. AC grid side grounding arrangement of a network has its impacts on selecting the DC side grounding arrangement [20,21,25–27].

In IEC 60364-1 grounding configurations for the grounding of DCMG components are categorized as TT, TN-S, TN-C, TN-C-S and IT, and are further reviewed in Ref. [20]. However, in this study, we mainly focus on DCMG system grounding configurations, and design considerations in the selection of DCMG system grounding configurations.

Under this section, solidly grounded AC grid and ungrounded AC grid systems are considered separately to investigate the possible DCMG system grounding configurations, and features of a DCMG network with these grounding configurations. For better comparison and to summarize the discussion below, comparative analysis of different DCMG grounding configurations and their features are provided in Table 1.

Table 1
DC microgrid grounding configurations, and their characteristic features.

DC bus grounding configuration	Fault detection schemes applicable	Fault ride-through capability	Ground fault current magnitude	Stray current	Transient over-voltages	Remarks
Neutral point of AC side transformer **solidly grounded**, DC bus **ungrounded.**	• Ground current monitoring. • Insulation monitoring	No	High	High	Low	• Fault detection is relatively easy.
Neutral point of AC side transformer **ungrounded**, DC bus **solidly grounded.**	• Ground current monitoring. • Insulation monitoring	No	High	High	Low	• Fault detection is relatively easy.
Neutral point of AC side transformer **ungrounded**, DC bus **ungrounded.**	• Insulation monitoring.	Yes	Very low	Low	High	• Ground faults should be cleared to prevent subsequent ground fault creating a pole-pole fault.
Neutral point of AC side transformer **ungrounded**, DC bus **high resistance grounded**.	• Ground current monitoring. • Insulation monitoring.	Yes	Moderate	Moderate/ low	High/ Moderate	• Low resistance grounding is proposed to mitigate high transient overvoltages during disturbances.
Neutral point of AC side transformer **ungrounded**, DC bus **midpoint grounded**.	• Detection of pole voltage shift. • Ground current monitoring. • Insulation monitoring	Yes	low (only a transient I_g)	High	Low	• Reduces insulation requirements as touch voltage is half the nominal voltage. • Protection of both poles required.
Neutral point of AC side Transformer **ungrounded**, DC bus midpoint **high resistance grounded**.	• Detection of pole voltage shift. • Ground current monitoring. • Insulation monitoring	Yes	Low	High	High	• Limits the transient capacitor discharge/ charge current.
Neutral point of AC side Transformer **ungrounded**, DC bus **reconfigurable grounding.**	• Ground current monitoring. • Insulation monitoring	No	High	Moderate/ low	Moderate/ low	• Diode grounding does not completely eliminate the stay current induced corrosion. • Reverse diode grounding can eliminate the issue of stray current. • Thyristor grounding scheme provides the flexibility to operate in both ungrounded and grounded configurations.

4.1. Solidly grounded (TT/TN) AC grid network

In a network with solidly grounded AC grid, solid grounding of the non-isolated DC bus creates a permanent fault. Hence, AC grid network with solidly grounded neutral, preclude the possibility of solid grounding of the DC bus, unless the network is electrically isolated using an isolation transformer, as in Fig. 8(a). However, the use of isolation transformers increases the installation costs, and not used often [53,54].

Another possible grounding arrangement without using an isolation transformer is to keep the DC bus ungrounded as shown in Fig. 8(b). As discussed in Section 2.3 ground current level in this network could be considerably higher than the permissible level of 30 mA, as in IEC 60479-1 [44]. Therefore, it is required to implement appropriate ground fault protection measures [25,45].

Fault detection in this grounding configuration is fairly easy, as it typically gives rise to significantly high I_g, and ground current monitoring based ground fault detection schemes are adequate. However, high impedance faults which result in significantly low I_g require more sensitive fault detection scheme, such as insulation monitoring [25,26].

4.2. Ungrounded (IT) AC grid network

Networks with AC side transformer neutral point ungrounded provides more flexibility in selecting DC bus grounding configuration.

Possible DC bus grounding configurations are; 1) DC bus solid grounding 2) ungrounded DC bus, 3) high resistance grounding, 4) DC bus midpoint solid grounding, 5) DC bus midpoint high resistance grounding and 6) reconfigurable grounding [25,26,45].

4.2.1. DC bus solid grounding

DC bus solidly grounded systems (Fig. 9(a)) give rise to significantly high I_g, as it will effectively create a pole-pole fault during a ground fault. Therefore, the network responds as in a pole-pole fault situation (see Section 2.2), and quick protective actions are required [25,26,55].

Ground current monitoring relays can be employed to detect ground faults in these networks [55]. Ground currents of few milliamperes are easily detected by currently available high sensitive ground current monitoring relays [56,57]. Ability to absorb disturbances in the network, and mitigate voltage spikes from such disturbances, is another advantage of this configuration. However, these networks are subjected to corrosion due to stray current flow [26,50,54].

4.2.2. Ungrounded DC bus

Ungrounded DC bus system (Fig. 9(b)) enables fault ride-through capability during ground faults. It has a zero or very low I_g with a single ground fault [58]. However, subsequent ground faults may create a pole-pole condition and can cause significant system damage. Hence, the initial ground fault should be cleared immediately.

Ground current monitoring schemes cannot detect ground faults in this system, and require more sensitive schemes. One such scheme is insulation monitoring, where AC or DC signal injection is used to monitor the system response, in order to identify the drop in insulation level due to a ground fault [55,59–61].

The main disadvantage of an ungrounded network is, it poses a danger to the public, as the bus voltages may reach an elevated level with respect to the ground. Furthermore, they are very susceptible to the noise, and disturbances in the network could give rise to underdamped transient overvoltages, which could deteriorate insulation and damage the equipment [47].

4.2.3. High resistance grounding

High resistance grounded systems (Fig. 9 (c)), similar to ungrounded networks, enables fault ride-through capability as a low resistance path for the circulation of I_g is absent [45,62–64]. The magnitude of I_g during a ground fault can be controlled at a safe level by careful selection of grounding resistance; certain tradeoffs are made in the selection of grounding resistance [26,45].

Generally, grounding resistance is selected such that, a ground fault causes a modest current flow to facilitate fault detection, but is not high to pose a threat to the personal (should be less than 30 mA to be consistent with IEC 60479-1 standard) [45,45]. Ground current monitoring and insulation monitoring relays can be employed to detect ground faults in these networks. A directional element for localization of ground faults in high resistance grounded networks was proposed in Ref. [63]. In addition, digital signal processing based method has been proposed to locate faults in high resistance grounded networks in Refs. [65–67].

Similar to ungrounded DC networks, in high resistance grounded networks stray current flow is minimized, but are prone to transient overvoltages during disturbances [47,55]. The literature proposes the use of low resistance grounding of DC bus [47,55]. As opposed to high resistance grounding, one commonly perceived benefit of low resistance grounding is the damping of oscillations caused by transient disturbances [47].

4.2.4. DC bus midpoint point solid grounding

In a DC bus midpoint solidly grounded network (Fig. 9(d)), the potential of each pole is half the pole-pole voltage, which reduces the insulation requirements. However, both poles have potential with respect to ground, and necessitate the protection of both poles of the network [26,45,46].

In this configuration, during a ground fault, the network is subjected to I_g caused by DC link capacitor charge-discharge. However, the system is free from I_g in steady-state. Literature suggests DC bus midpoint grounding through a high grounding resistance, in an effort to limit the initial capacitor charge-discharge current magnitude [26,45]. Pole voltage shift indicates the occurrence of a ground fault in these networks and is used for detection [55,59]. However, a voltage shift based ground fault detection has its limitations on detection speed and the ability to locate the faults [26,59].

Also, this grounding configuration endows ground fault ride-through capability to the network. In addition, the inherent drawbacks of high

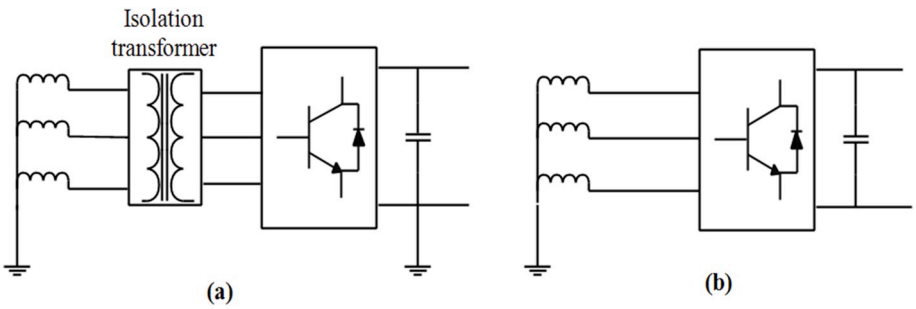

Fig. 8. Possible grounding configurations with neutral point of AC grid transformer solidly grounded networks (a) DC bus solidly grounded with isolation transformer, (b) DC bus ungrounded network [54].

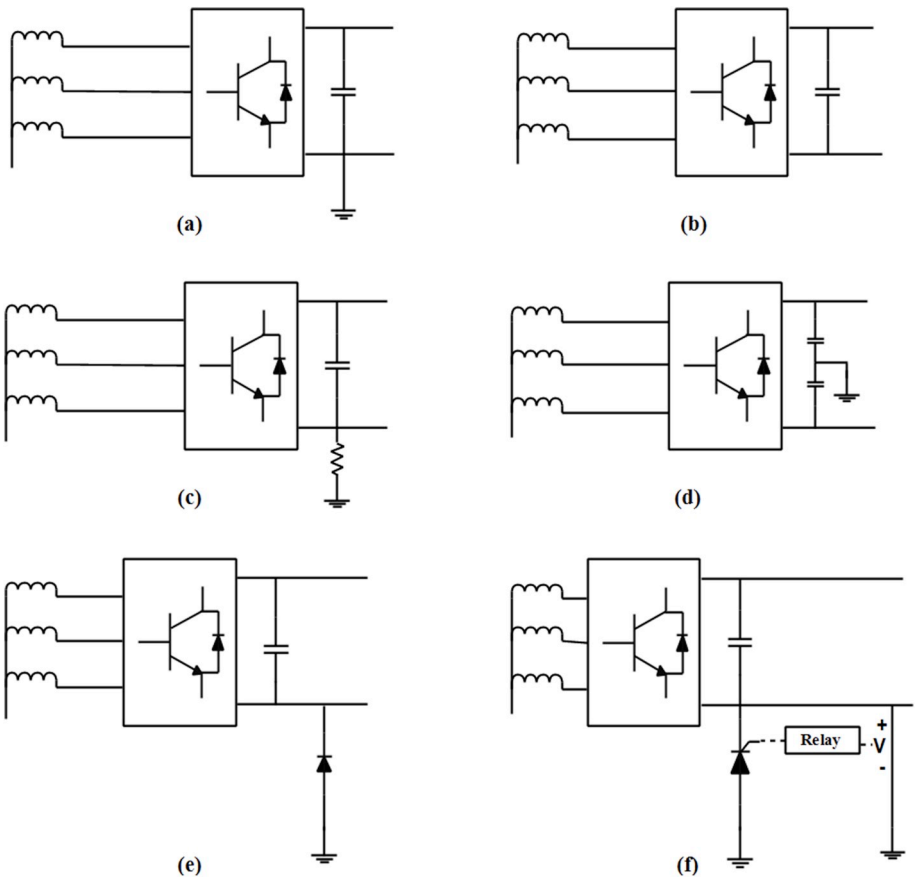

Fig. 9. Possible grounding configurations with neutral point of AC side transformer ungrounded networks, (a) DC bus solid grounding, (b) DC bus ungrounded, (c) high resistance grounded, (d) DC bus midpoint grounding, (e) diode grounding, (f) thyristor grounding [45,50,51].

resistance grounded and ungrounded networks such as bus voltage reaching elevated levels and transient overvoltages caused by disturbances, are eliminated [45].

4.2.5. *Reconfigurable grounding options in DC microgrids*

As discussed earlier, minimizing stray current and avoiding unsafe transient overvoltages are two contradictory requirements, when selecting a grounding configuration for a DCMG. Contrary to the DC network grounding methods discussed earlier, in Ref. [51], it presents reconfigurable grounding methods for DC traction networks, where the network is operated in ungrounded configuration to reduce the corrosion intensity, and upon detection of a high voltage, the network is grounded to reduce the voltages to safe levels.

Reconfigurable grounding options are mainly proposed for DC traction networks as a means of reducing the stray current [49,68]. Use of reconfigurable grounding configurations for DCMGs has not been explored yet.

- Diode grounding

Diode grounding involves solid grounding of DC bus through a diode as shown in Fig. 9(e). Here, the current is allowed to flow from the ground towards the negative bus if the voltage across diode exceeds its forward voltage.

For small magnitudes of voltage between ground and the negative pole, the diodes would conduct, resulting in relatively high stray currents. Hence the problem of stray current induced corrosion is not completely eliminated in this scheme [49–51,68]. In Ref. [48] a reversed diode grounding scheme is proposed to eliminate the issue with stray current. By placing the diode in reverse direction, stray currents are blocked, and at the same time, transient overvoltages created in the network are diminished.

- Thyristor grounding

Unlike diode grounding, thyristor grounding shown in Fig. 9(f) offers more control over the grounding configuration. In this scheme, if the ground to negative bus voltage rises above a threshold value, thyristor gate is triggered to ground the DC bus [49–51]. The main advantage of thyristor grounding over diode grounding configuration is, its ability to maintain DC bus ungrounded, minimizing the stray current [50,51].

From the above discussion, it is clear that different tradeoffs have to be taken into consideration when deciding the grounding configuration for a particular application. A wide system study is required in selecting the appropriate DCMG grounding configuration, and ground fault detection technique should be selected accordingly.

5. DCMG fault detection and localization

Fast and accurate fault detection and localization is an essential requirement for network protection. However, as discussed in Section 3, there are several challenges for the design of DCMG fault detection schemes. Fault detection techniques for DCMGs are still in the early stage of development, compared to ACMGs. Moreover, the absence of frequency and phasor information limit the use of well-established fault detection methods in AC systems [13,24,35].

When designing a DCMG protection system, knowledge of the existing DC power networks such as HVDC, shipboard and traction networks, is of assistance. However, most of these networks utilize converters with current limiting capability. In contrast, DCMG system

needs to be interfaced with AC grid using a bidirectional converter; consequently, different protection schemes are required for DCMGs [24]. Moreover, fault detection in DCMGs has been more challenging due to their small scale, embedding DGs and higher safety requirements. Also, while most of these DC networks are used for point to point applications, DCMGs are by nature multiterminal networks.

There are several factors that should be taken into consideration in the design of fault detection scheme: the type of faults that can occur, the severity of the faults, network arrangement, grounding configuration, fault current flow paths, need for backup protection, protection coordination, types of fault interruption devices, time limits for fault interruption and measures to prevent faulty operation of the protection devices. In addition, component level (eg: - IGBTs), device level (eg: - VSC) and system-level protection schemes should be properly coordinated [16,24,25].

5.1. DCMG fault detection schemes

Currently available techniques for fault detection in DCMG systems, and their performance are reviewed under this section considering the criteria: detection accuracy, fault diagnosis and localization capability, sensitivity, communication and sensory requirements, integration complexity and cost of realization. Fault detection and localizing techniques employed in HVDC, MVDC shipboard, traction networks and ACMGs are also reviewed under this section, to envisage their suitability for DCMGs.

5.1.1. Overcurrent detection

Due to simplicity, overcurrent protection schemes are commonly used in AC as well as DC systems. The objective is to identify abnormal currents flowing in the circuit and identify fault events. However, there are several difficulties to use overcurrent schemes in DCMGs. As discussed in Section 2, fault current parameters, such as magnitude and direction, depends on network architecture, grounding scheme, fault impedance, fault type, fault location, converters used to interface DGs to the DCMG and operating mode of the microgrid. In addition, the fault loop impedance determines the natural frequency and damping factor of the current transient. The simulated fault currents are shown in Fig. 10, in which fault currents with different fault resistances (0.2 and 0.7 Ω) are shown. It clearly shows the influence of fault impedance on fault current magnitude and oscillatory response.

Changing fault levels and changing power flow direction may cause relay coordination issues, delayed and non-operation of relays, and false tripping [17,24]. In Ref. [69] a smart relay utilizing current and voltage levels to detect faults is discussed. If the current through the converters exceeds a threshold value and stays above beyond a certain time, and voltage drops below 0.8 pu, a fault is detected by the relay. Relays are embedded in the converters and DCMG is divided into several zones, which allows the relays to operate autonomously. In Ref. [70] two section current protection scheme is proposed for the protection of MVDC lines. This scheme adopts an instantaneous overcurrent threshold as primary protection, and time limit overcurrent threshold as backup protection. However, the inability to detect high impedance faults and inadequate level of selectivity are major drawbacks of these schemes.

Fault detection technique relying on intelligent electronic devices (IEDs) and communication between IEDs is proposed in Ref. [36]. Current readings from IEDs are used for overcurrent and differential fault detection with predetermined threshold values. This scheme allows the selective isolation of faulted segments. Moreover, differential protection using IEDs enables the detection of high impedance faults. In Ref. [71], a similar approach for fault detection, using IEDs, where current magnitudes, direction and voltage levels are monitored, is proposed.

5.1.2. Derivatives of current

In Ref. [24], the use of derivatives of current (di/dt) for fast detection of faults within DC networks is discussed. Immediately after a fault, the discharge of the DC link capacitors can result in fault current transient, until it is damped by fault loop impedance. In order to interrupt the fault prior to the peak current discharge of DC capacitors a fast fault detection method is required, which makes di/dt based protection schemes more suitable for DC networks [24,72].

Fault detection scheme based on initial di/dt is discussed in Ref. [73]. This initial di/dt fault detection concept utilizes DC link capacitance initial response to a fault to estimate the fault location and relay coordination. This study shows that there is a similarity in the initial response for both low and high impedance fault conditions, although for high impedance faults di/dt decays more rapidly. Hence, detection of high impedance faults is possible by using initial di/dt response [73]. Although di/dt schemes offer very fast fault detection, the accuracy is affected by disturbances and noise in the network [17,24,73].

5.1.3. Differential protection schemes

Differential protection schemes are used to provide zonal protection to predefined protection zones. Varying loading levels, the existence of DGs and different fault levels have no impact on detection accuracy and sensitivity of a differential protection scheme; hence, making it a good option for protection of microgrids both AC and DC [13,17,36]. Fig. 11 shows the schematic diagram for the implementation of a differential scheme to protect a selected DC feeder segment.

In Ref. [74], a differential scheme is proposed, where each protection zone consists of a master controller and two slave controllers. Slave controllers monitor currents at two ends of the protected zone, and send it to the master controller. In case of a fault, the difference of current at two ends exceeds a certain threshold, and the master controller sends a signal to the slave controllers to isolate the faulty section.

Differential schemes rely on communication between protective

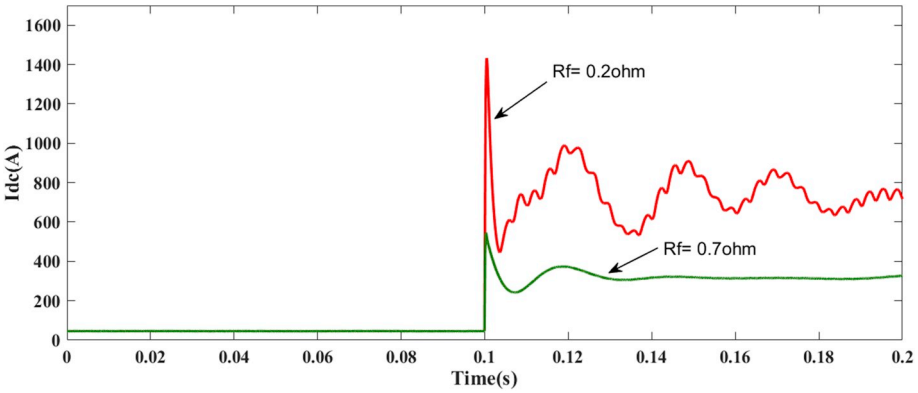

Fig. 10. DC line current waveform during a pole-pole fault (at t = 0.1s), with a fault impedance of 0.2Ω and 0.7Ω.

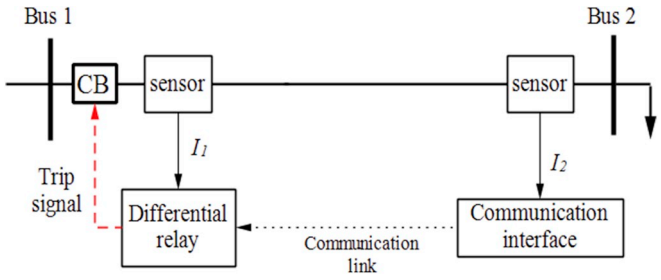

Fig. 11. Differential current scheme for a DCMG distribution feeder protection [13].

devices on both ends of the protection zones for fault detection. Hence, communication delay between protection devices should be taken into consideration, when devising a differential scheme.

5.1.4. Distance protection

Traditional AC networks adopt distance protection schemes, which uses impedance to represent the occurrence of a fault and distance from the relay to the fault location. However, during a fault transient in a DC system, there are rapid oscillations and frequency changes, where no fundamental frequency can be defined. Novel techniques for electrical parameter evaluation to determine the system impedance, which indicates the occurrence and distance of fault in a DC network, have been proposed in Refs. [28,75].

In Ref. [75], distance protection scheme for DC shipboard systems based on active impedance measurement is discussed. The network is injected with a current signal with a wide frequency range and the resultant voltage is measured to calculate the equivalent impedance.

Impedance estimation technique for DC systems without external signal injection is discussed in Ref. [28]. Voltage reference comparison method is used to determine the pole-pole fault location. Moreover, the ground fault location is determined by analyzing the initial fault transient.

5.1.5. Signal processing based fault detection

Lack of time domain information in fast Fourier transforms (FFT) makes it difficult to be used for transient signal analysis. This limits the use of FFT based methods for power system protection [76]. However, short-time Fourier transforms (STFT), which analyses the signal in both time and frequency domains, is being widely studied for power system protection applications [76,77].

Utilization of STFT for quantitative investigation of high frequency harmonics during fault transients in DC networks is presented in Ref. [78]. Various factors that affect the STFT based fault detection, such as sampling frequency, type of window functions, window size, number of FFT points and external factors such as ripple in the voltage and current signals were investigated in Ref. [78]. However, capabilities of STFT for signal processing is limited due to constraints on window size, i.e wide time window will result in particularly good frequency resolution but poor time resolution. Conversely, the narrow time window will result in poor frequency resolution but good time resolution.

Wavelet transform has the capability to decompose a time-frequency signal into specific time-frequency resolutions. Hence, offers better time and frequency resolution compared with STFT and FFT techniques. Wavelet representation of a signal provides a portrayal of the variation of the frequency content with time, and hence reveal when and what type of transients take place in the signal. Wavelet analysis techniques have been proposed extensively for several power system applications, including fault classification and network event recognition [79–87]. Use of Wavelet transform (WT) to capture fault characteristics from monitored signals in DCMGs and MV shipboard networks have been discussed in Refs. [76,79–81] respectively. Simulation studies were carried out to evaluate the effectiveness of using wavelet transforms for DC waveform analysis. Fig. 12 shows the discrete wavelet transformation (DWT) of the DC line current waveform during a ground fault, up to 5 levels of decomposition. In this study, a sampling frequency of 50 kHz and Daubechies 5 (db5) mother wavelet is used. It can be seen that there is a clear increase in magnitudes of the detail coefficients during the fault, especially in detail levels 2, 3 and 4.

The general approach for Wavelet based fault detection is capturing characteristic features of a fault signal by using WT and applying these characteristics to an algorithm as a variable to detect faults. There are different approaches to capture these characteristics. One such approach is to compare the value of detail coefficients. In Ref. [80], fault detection and localization scheme based on detail coefficients of current and voltage signals is discussed.

Adopting the wavelet coefficients directly for fault detection requires large memory space and computing time. WT based technique for fault detection in MV shipboard power systems proposed in Ref. [76] uses the energy variations in detail coefficients. In this approach, Perceval's theorem is used to reduce the quantity of feature vector without losing its original properties, and thus, required memory and processing time has reduced. In addition, several statistical measures for fault feature extraction with reduced quantities have been discussed in the literature [80,82].

In addition, literature proposes the use of signal processing in combination with pattern recognition techniques to detect faults and is discussed in the following section.

5.1.6. Pattern recognition schemes

In recent years a growing interest to employ data-driven or pattern recognition approaches for power system control and protection is seen. Pattern recognition based fault detection overcomes the drawback of having to define hard thresholds, and aids in accurate fault detection unaffected by disturbances and noise. The steps involved in fault detection and classification using pattern recognition techniques are depicted in Fig. 13.

Artificial neural networks (ANN) have already been applied in AC, HVDC and MVDC networks for fault detection and have shown to be accurate, robust and fast in performance [82–87]. Application of ANN for detection and classification of faults according to fault type and location, in DCMG networks have been studied in Refs. [88,89]. An ANN can determine the existence of normal, faulty conditions and different fault locations, fast and accurately. ANNs are trained using post-fault data at different locations and different fault levels to ensure correct

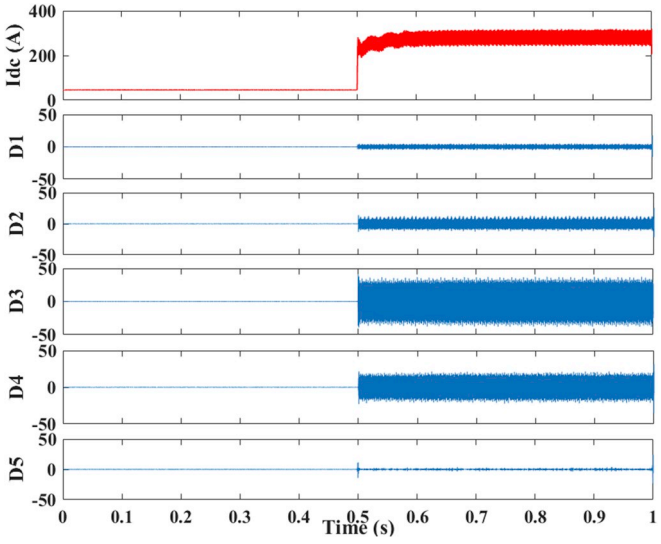

Fig. 12. DWT decomposition of DC line current signal, during a pole-ground fault, up to 5 detail levels.

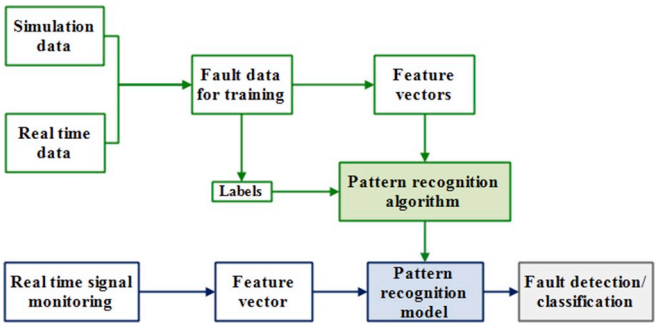

Fig. 13. Steps involved in pattern recognition based fault detection and classification.

fault identification.

In Ref. [90] relative wavelet energy variations in line current are used to construct a feature vector. Fig. 14 shows the relative wavelet energy variations in 6 decomposition levels under different fault and non-fault events. From Fig. 14, it is clear that the capability of the fault detection scheme to identify fault events can be realized by comparing the feature vectors extracted from current signals. The constructed feature vectors are then used to train an ANN for DCMG fault detection and classification.

In Ref. [91] ACMG faults are classified according to fault type, phase, and location. The network line current signals were monitored to extract statistical features using DWT and a statistical feature vector is used as input to a deep neural network to develop a classifier scheme, which achieves a significant level of classification accuracy compared to other schemes.

A preliminary investigation on the use of different classifier techniques including; ANNs, decision trees and support vector machines for fault detection and classification in MVDC shipboard power networks is presented in Ref. [92]. Pattern recognition based fault detection schemes proposed in the literature demonstrate a significant level of effectiveness in terms of classification accuracy, intelligent fault detection capability and robustness to measurement uncertainties. While these pattern recognition techniques show a high level of effectiveness in event classification applications such as HVDC fault detection, AC microgrid fault detection and islanding detection [93–96], the applicability of these classifier techniques for accurate detection of DCMG fault events require further study.

For pattern recognition based fault detection, it is important to determine which classification algorithm provides the best classification performance. Moreover, the required level of accuracy, reliability and speed of classification are the determinant factors when deciding what sampling rates to be used, the processing power required, signals to be monitored and amount of training samples required.

In this section comparative analysis on the performance of each fault detection technique was provided. To summarize the above analysis, strengths and drawbacks of DC fault detection techniques are provided in Table 2.

5.2. *Fault localization and protection coordination requirements*

Fault localization and protection coordination techniques employed in DCMG systems are discussed under the sections below.

5.2.1. *Fault localization*

Fault localization is an essential requirement for the quick isolation of the faulty segment. The absence of frequency and phasor information prevents the use of line impedance based distance protection scheme for locating faults. Furthermore, traveling wave based and signal injection based methods are ineffective since it is difficult to discriminate between reflected waves, as the cables are short in length. Differential protection schemes which protect bounded zones of the network presents an effective solution for fault localization. Differential schemes presented in Refs. [36,74], enables selective fault isolation capability, and were previously discussed in section 5.1.3. Fault location estimation techniques based on local measurements are presented in Refs. [28,73]. Selective positioning of fault interrupting devices working in conjunction with these fault localizing schemes enables selective fault isolation capability, to improve network reliability.

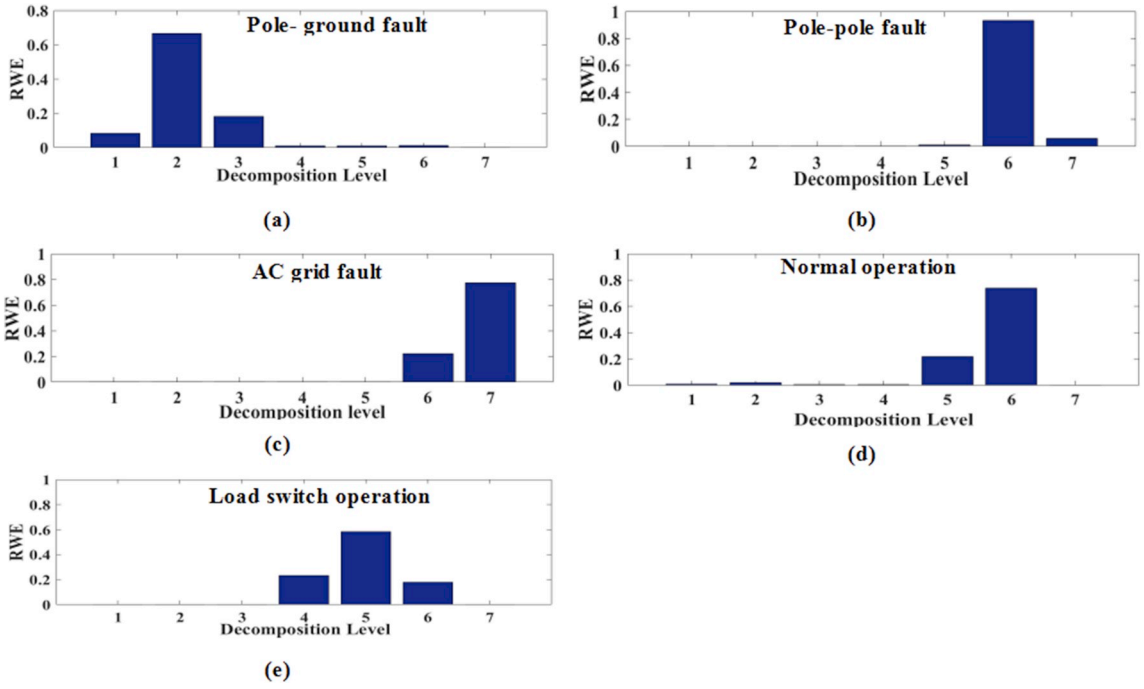

Fig. 14. RWE distribution in decomposition levels of DC line current under normal operation under (a) pole-ground fault in DC side, (b) pole-pole fault in DC side, (c) fault in AC side, (d) normal operation, (e) load switching operation [90].

Table 2
Comparison of strengths and drawbacks of different DC network fault detection schemes.

Detection technique	Strengths	Drawbacks
Overcurrent schemes	• Simple and fast. • Adaptive overcurrent schemes have been developed, to overcome issues due to changing fault levels and current directions. • Easier to implement. • Smart devices (IEDs) have been developed, to provide selective protection.	• Sensitivity and relay coordination issues due to different levels of faults during different modes of operation. • Difficult to detect high impedance faults. • Accuracy will be affected by network disturbances and noise in the measurements.
di/dt based schemes	• Simple and fast. • Not affected by fault impedance. (can detect high impedance faults)	• Accuracy affected by network disturbances in the network. • Mostly used in conjunction with other protection schemes. for backup protection.
Differential schemes	• High sensitivity and precision. • Simple and fast. • Sensitivity not affected by fault impedance. • Facilitates selective tripping, minimizing interruptions to the healthy sections.	• Based on device communication • The requirement of synchronized measurements. • Protects only a bounded zone of the network. • Inability to provide backup protection to the adjacent zones of the network. • Accuracy affected by sensor and communication errors. • The high cost due to additional sensory and communication requirements.
Distance protection schemes	• Simple and fast. • Can provide backup protection to adjacent zones of protection. • More sensitivity to fault resistance and location.	• Mostly relies on the external signal injection for active impedance measurements. • Sensitivity affected by fault impedance. • Affected by network disturbances or noise in the network. • Dependent on network architecture.
Signal processing based schemes	• Accurate and reliable. • The possibility of identifying features of high impedance faults to detect them more accurately. • Signal processing techniques in combination with pattern recognition significantly improve detection accuracy. • Fault diagnosis and localization capability.	• Affected by network disturbances or measurement noise. • Additional sensory and signal conditioning requirements. • Complex algorithms and difficulty to use in real time applications. • High cost of realization. • Mostly non-unit schemes; hence, rely on device communication for selective tripping, upon fault location.
Pattern recognition based schemes	• Accurate and robust. • Intelligent fault detection capability. • Fault diagnosis and localization capability.	• Require large amount of training samples and training time. • Training data not globally available, and difficult to acquire. • Accuracy affected by training data. • Complex structure, thus difficult to use in real time application. • Selection of classification algorithm and feature vectors to meet strict time limits for DC fault interruption is challenging.

5.2.2. *Protection coordination strategies*

Protection coordination strategies are employed to coordinate between primary and backup protection. Primary protection devices act as the main protection device of a particular component or section of the DCMG. Backup protection is implemented in case of failure of primary protection. The selection of primary and backup protection scheme is based on protection component, fault location, required fault clearing time, identification of temporary and permanent faults and fault ride-through capability.

An effective protection coordination strategy minimizes critical fault clearing time, enables quick system restoration and minimizes outages. In Refs. [36,74] differential scheme with non-overlapping zones of protection is adopted. However, the inability to provide backup protection is a major drawback in these schemes.

This Section reviews protection coordination strategies based on time grading of relays and communication between relays, deployed in DC distribution networks.

- Time grading of relays

In order to achieve selective protection capability, relays are time graded. In principle, operating times of the relays are set such that relays closest to the fault operates first. Time grading of the relays enables the backup protection relays to operate if the primary protection fails to operate.

In Ref. [97] protection coordination scheme for a DCMG, employing fast acting fuses and circuit breakers for selective protection is presented. Fast acting fuses used at selected locations provide faster fault clearing capability and are more cost effective compared with circuit breakers. Time graded overcurrent relay embedded into circuit breakers are deployed at selected locations to protect selected zones/components of the network.

Protection coordination scheme between fuses and relays embedded in fault current blocking converters is presented in Ref. [69]. Fast acting fuses which act as the primary protection device of the AC zone of the network are used in this study. Relays which operates much faster than the fuses are employed to interrupt faults in the DC side, thereby preventing the fuses to blow off for faults in the DC side.

- Communication based relay coordination

DCMG protection coordination based on communication between devices offers a reliable solution. In Ref. [32] Intelligent electronic devices (IEDs) are installed at different zones of the network, and communication link between IED is used to maintain proper coordination. The embedded sensors in IEDs monitor real time current measurements and communicates the information between IEDs, which determines the faulted section and send trip signals. In Ref. [11] DCMG protection scheme in which voltage and current information at different relay locations are communicated between relays to determine fault occurrence and fault locations is presented. The communication link is of crucial importance for these protection schemes; hence, severely affected by communication delays and failures.

5.2.2.1. DC microgrid fault interruption schemes. An effective protection scheme requires the availability of fault interruption devices, which can block or limit fault currents and isolate faulty sections of the network. As discussed in Section 3, very fast current rise and absence of natural zero crossing impose very critical time limits for fault current interruption in a DC network. Hence, DC network switchgear is required to operate very fast, and special measures are adopted for DC current breaking and extinguishing the arc [24,36,37].

In Refs. [24,37], limits for fault current interruption in a VSC based

DCMG network is investigated. Current handling capabilities of PE devices were considered mainly in these studies. Restraining transient overvoltages, coordinated operation, fault detection time, power losses, cost of implementation and ability to minimize outages are important considerations in the choice of fault interruption devices for DCMGs. In this section, currently available switchgear and proposed schemes for DC fault interruption are discussed.

5.3. Converter blocking and current limiting schemes

Most HVDC and MVDC applications including shipboard power systems and traction networks use PE converters with fault current blocking capability. It allows the fault current to be interrupted quickly through converter blocking. As discussed in Section 2, typical IGBT based converters are equipped with IGBT self-protection schemes such as DESAT protection, to protect against fault current [31,32]. However, the fault current will continue to flow through freewheeling diodes with no possible means of limiting. Hence, it is not possible to employ converter blocking schemes with conventional VSC and buck/boost architectures, and require modifications to the converter architecture to achieve current blocking capability [24,98].

Conventional converters, although limits maximum current flow during normal operation, are incapable of limiting fault current. However, specially designed converters which have the current limiting capabilities during a fault in the network are discussed in Refs. [98–105]. Fault current limiting converters adopt multi-mode control schemes, and changes the control scheme to limit current upon detection of a fault. These converters working in coordination with protection devices minimizes the risk of damages to the network, and increase the resilience and fault ride-through capability of the network. Loss of power to the healthy sections of the network is a major drawback in this scheme. Fault current blocking converter architectures for DC distribution networks are discussed below.

5.3.1. ETO thyristor based converters

In order to achieve fault current blocking capability, replacing the freewheeling diode of the VSC by ETO thyristors is proposed in Ref. [69], and is shown in Fig. 15. The ETOs typically have a higher voltage and current handling capability, and switching requirements are quite lenient compared to IGBTs. Once the fault is detected, soft shut down technique is used, and ETO gate voltage is reduced dynamically to limit the fault current [69,98,99]. For permanent faults gate voltage is reduced until the device is completely turned off.

5.3.2. Back-to-back voltage source converters

Back-to-back VSCs configuration (see Fig. 16) provides full voltage and current regulation capability on either side of the converter. This converter assembly is capable of blocking fault current, and prevents DC link capacitor discharge [100,101]. Once the fault is cleared, the converter is capable of immediate power supply once the fault is cleared, because the DC link capacitor remains charged.

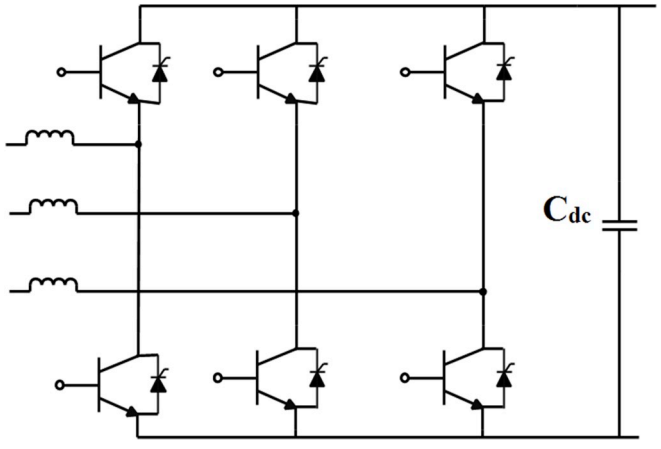

Fig. 15. Modified ETO based VSC architecture, replacing freewheeling diodes [69].

The requirement of two active VSCs which consequently increases the converter size and installation costs is a main drawback. In addition, two conversion stages increase the power loses compared to single VSC configuration.

5.3.3. Isolated DC-DC converter

Isolated DC-DC converter architectures capable of controlling current under fault events are discussed in Refs. [100,103–105]. Dual active bridge (DAB) converter architecture employing two full-bridge converters connected through a high frequency transformer is shown in Fig. 17. DC Fault characteristics of a DAB converter is discussed in Ref. [20]. DAB converter has an inherent capability of limiting fault current during a fault in either side of the converter [20,100].

For high power applications, several modular multilevel DAB architectures are proposed in literature [100,102,106]. Although traditionally modular multilevel converters are employed in HVDC networks, as they require high number of active switches and have several conversion stages; Hence are not cost effective for LVDC and MVDC applications. However, recent developments in the wideband gap devices (WBG) devices such as silicon carbide (SiC) and Gallium nitride (GaN) presents a viable option to fully exploit the advantages of these converter architectures for LVDC and MVDC distribution networks [20,107,108].

Fig. 18 shows a modular multilevel DAB architecture, which comprises of several submodules. These submodules can be actively controlled to limit the fault current. Since the submodule capacitors are decoupled from the output, transient fault current due to capacitor discharge can also be actively limited. Furthermore, submodule capacitors act as an energy buffer, enabling fault ride-through capability against temporary faults [100,106].

5.3.4. Modular multilevel converter architectures

The literature proposes several multilevel converter architectures capable of blocking DC side fault currents [100,109,110]. Fig. 19 shows an alternate arm multilevel converter to be employed at AC-DC interface. During a fault, all the IGBTs are blocked off, cutting off the fault current through the converter.

With the fault current blocking converter action, the faulty segment of the network can be isolated without breaking large currents. Hence, the strategic positioning of fast-acting DC breakers operating in coordination with fault current blocking converters can facilitate quick fault isolation, minimize damages to the network components and minimize interruptions. Protection scheme based on coordinated control between power supply converters and contactors for faster extinction of fault current and to minimize outage time is presented in Ref. [111].

5.4. Fault current limiters (FCLs)

Limiting the fault level can protect DCMG components against high fault currents. Fault current limiter (FCL) can be used in DC networks to limit fault currents as soon as a fault is detected [112]. FCL has an effective impedance of zero at normal operation, but increases upon detection of a fault in order to limit the fault current. Strategic positioning of FCLs is analyzed in Refs. [112,113], which shows the point of integration of DG source to the network is the best position to place the FCL.

The possibility of installing protective inductors at the converter terminals to limit fault current transients in an HVDC network is investigated in Ref. [114]. However, the requirement of a large size iron core, which consequently increases the size, weight and cost of installation, is the main disadvantage of this scheme. In addition, this FCL is

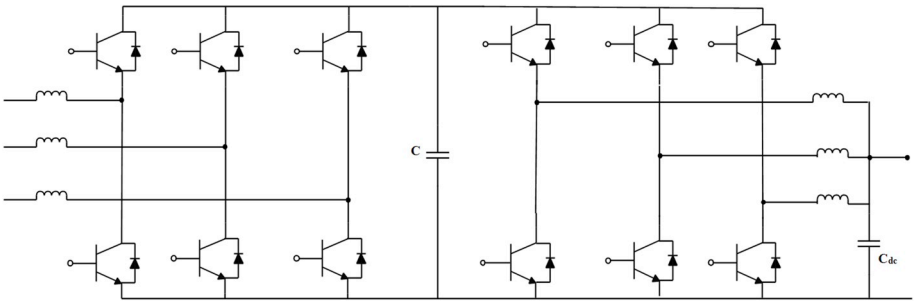

Fig. 16. Modified back-to-back VSC architecture, employing two active VSCs [100].

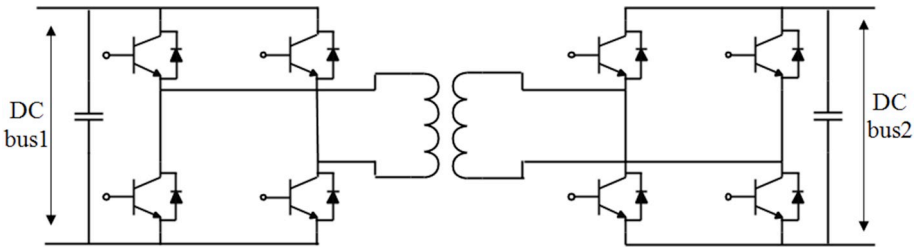

Fig. 17. Dual active bridge converter architecture with fault current blocking capability [20].

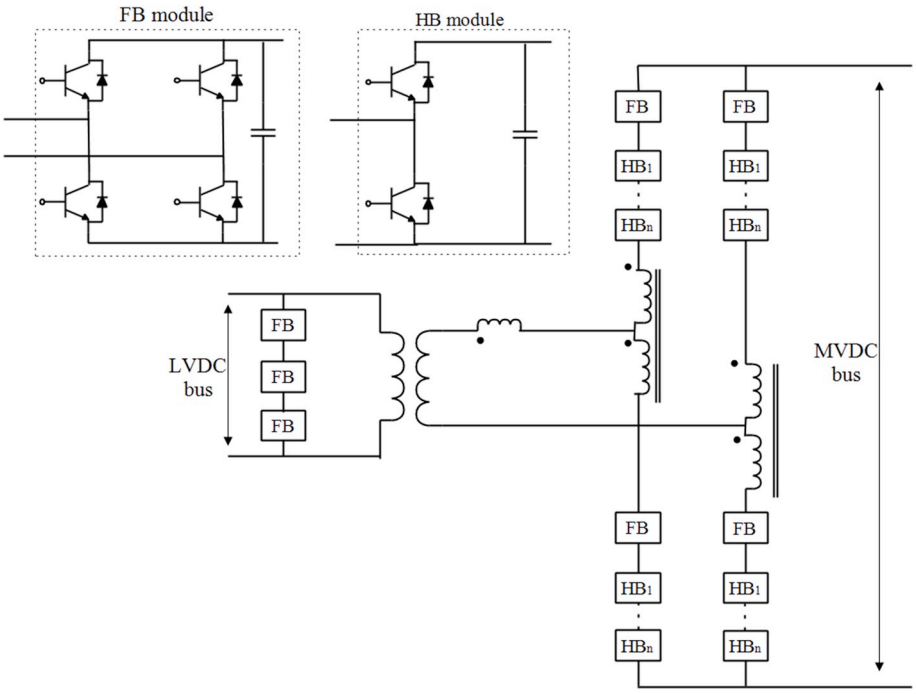

Fig. 18. Modular multilevel dual active bridge converter architecture with fault current blocking capability [100].

only capable of limiting rising currents which makes it effective only during transient stages.

Use of FCLs based on superconducting materials in DC networks is studied in Ref. [115]. The FCL operates in the superconducting mode under normal conditions, and loses its zero resistance if the current density reaches a critical value. Design criteria and parameter selection in superconducting FCLs, based on power networks requirements are analyzed in Ref. [115]. Practical realizations of superconducting FCLs are discussed in Refs. [116,117]. The main disadvantage of this type of FCL is the requirement of long lengths of superconducting materials, which makes FCL large, heavy and expensive. In addition, it requires an additional cooling system.

Several solid-state FCL designs for DC networks have been discussed in Refs. [118,119]. Solid-state FCL has its advantages, such as small size, fully controllable and fast response times. The main drawback of solid-state FCL is having high conducting losses.

Solid-state FCL topology which consists of SCR and IGBT assembly is shown in Fig. 20. Under normal operation, FCL is operating in the conducting state. i.e T_1 is turned ON and T_2 is turned OFF. Load power is supplied through T_1. Since SCR T_1 is a semi controlled device, has a low conducting loss compared to IGBTs. Capacitors C_0 and C_1 are also charged until C_0 and C_1 equals DC bus voltage. Load current flow

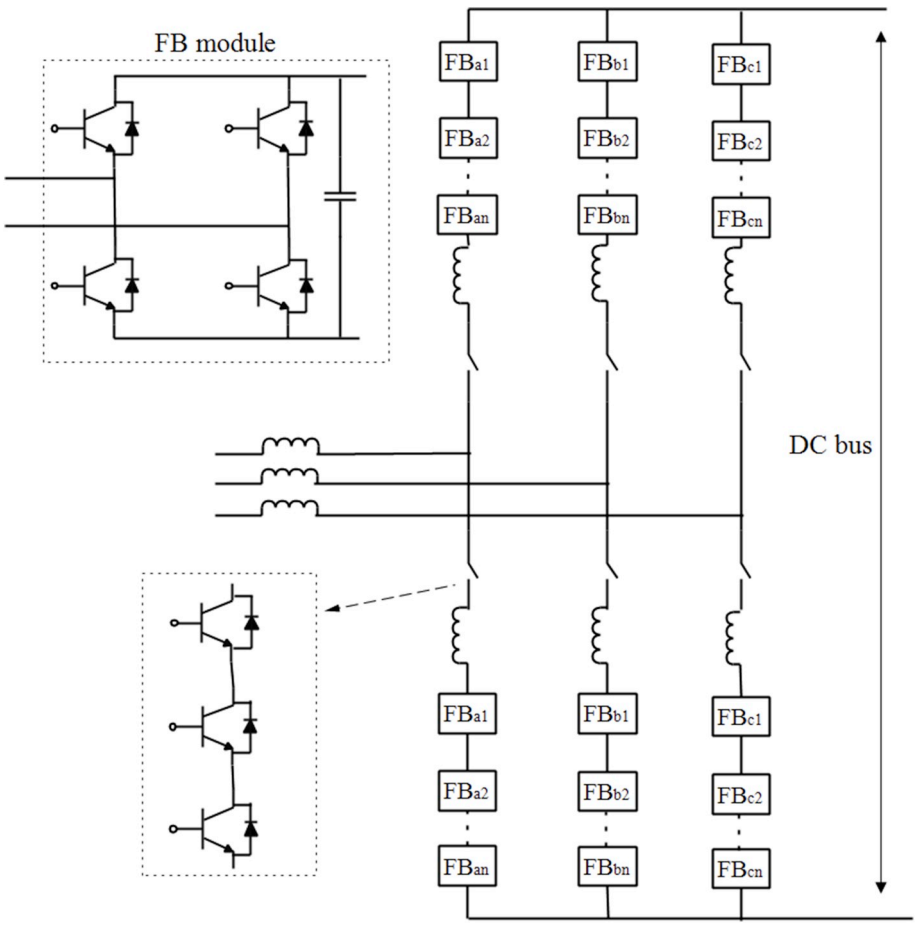

Fig. 19. Alternate arm multilevel converter architecture with fault current blocking capability [100].

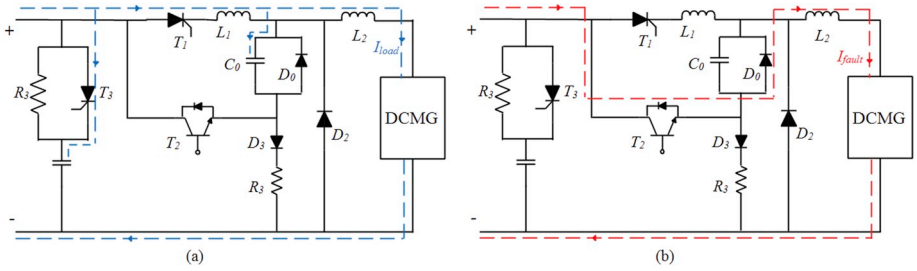

Fig. 20. Current flow path though FCL during (a) normal operation of the DCMG, (b) after a fault is detected in the DCMG [118].

through FCL under normal operating conditions is shown in Fig. 20 (a). When a fault is detected, T_1 is turned OFF and T_2 is triggered. Components R_1, C_1 and T_3 act as an input buffer to absorb energy to prevent T_2 being exposed to overvoltages during triggering. C_0, D_0, R_3, and D_3 form a forced turnoff circuit. During turnoff of T_1, C_0 applies an inverse voltage to the T_1 for forced turnoff. After T_1 is turned off, the FCL becomes a buck converter and current through T_2 (see Fig. 20 (b)) can be controlled [118].

5.5. Fault current blocking with DC side CBs

DC network fault interrupting schemes employing DC side CBs have been proposed in Refs. [37,40,120,121]. These schemes offer selectivity in interrupting faulted section of the network, thereby allowing healthy sections of the network to operate normally.

With the absence of a zero-crossing in the current waveform, DC switchgear faces a unique challenge of no natural method for quenching the arc that occurs during current breaking. Protection of DC networks is done with specially constructed DC circuit breakers (DCCBs) as well as with oversized ACCBs.

Use of ACCBs in series with a reactor in DC networks is discussed in Ref. [120]. However, ACCBs cannot meet strict time limits for fault current interruption in DC networks due to their mechanical restrictions. Even though AC devices have advantages such as low cost, DCCBs are always the better option to be used in DC networks, as they have fast constant current interruption capability [37]. Several mechanical, solid-state and hybrid (solid-state and mechanical) breaker designs for DC network protection have been developed over the past few years.

5.5.1. Mechanical DC breakers

Resonance based principle is generally applied in mechanical DC breakers where oscillator circuits are used to generate a current zero-crossing point. The general circuitry of a mechanical DCCB with both passive and active commutation are shown in Fig. 21 [14,122,123]. It

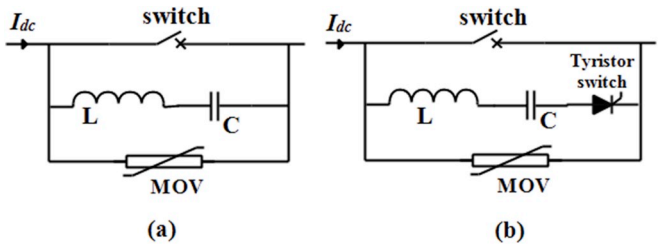

Fig. 21. Mechanical DC circuit breaker, with (a) passive commutation, (b) active commutation [20].

generally comprises of a mechanical switch, commutation circuit, and MOV for absorption and dissipation of energy after the interruption. Once a fault occurs, the mechanical switch opens and arc voltage is created which commutates the current through the commutation circuit. The series arrangement of capacitor and inductor generates an oscillating current, thus creating zero-crossing points between mechanical switch, and the mechanical switch completely interrupts the current [20]. However, response time is much slower (~30 ms) than DC link capacitor discharge speed, and the network is subjected to very high fault current transient, under severe fault conditions.

5.5.2. Solid-state circuit breakers (SSCBs)

SSCBs offer a promising solution for DC fault interruption with its high speed fault current interruption and high fault current handling capability. There are several SSCB designs available based on GTO thyristors, ETO thyristors, IGBTs and IGCTs [20,40]. A detailed survey into the solid-state technology for the SSCBs considering the switching frequency and voltage/power level the SSCBs are being used for, is provided in Ref. [20].

An improved bidirectional SSCB design is shown in Fig. 22. The breaker comprises of series string of solid-state switches to safely handle the DC voltage and it is not possible for transients to exceed the withstand levels of the individual components. IGBTs are often the common choice because of their commercial availability, low power requirement to drive the gate and short response time. However, for high power applications, IGCTs are preferred due to their low conduction losses [40].

SSCB design shown in Fig. 22, provides the functionality of complete CB assembly, where local fault protection is provided through control system of the breaker itself, and external fault detection is not required. Current sensors feed current measurements to the control unit. In case of a fault in the network, the control unit activates the gate drive circuit and turns off active switches. Snubber elements and freewheeling diodes absorb the residual energy at the time of current interruption [14,40,124].

In SSCB design discussed above, solid-state switches must be actively driven to reverse bias before fault current exceeds the interrupt capability of the switch. Hence, timely fault detection is a crucial requirement. In addition, fault detection, processing, and control system required increases response time and cost. To address these issues, Z source circuit breaker (ZSCB) which autonomously responds to faults (see Fig. 23) is proposed in Ref. [14]. ZSCB creates a current zero-crossing by absorbing part of the large transient fault current and once the zero-crossing is created the silicon control rectifier (SCR) is naturally switched off. This natural commutation of the solid-state switch allows the fault to be interrupted, without having to apply signal to disable gate pulses to SCR. Additionally, passive elements used in ZSCB limit peak current in solid-state device. Hence, it is not required to withstand high fault currents.

Inability to provide overload protection and being able to interrupt faults with high fault transients only are some of the inherited drawbacks of ZSCB design proposed in Ref. [14]. For less severe faults, transient fault current may not be sufficient to naturally commutate. New series ZSCB design which adopts a separate force commutation circuitry is proposed in Ref. [125]. In addition, ZSCB circuitry has been modified to achieve bidirectional power flow capability in Ref. [111].

Although SSCBs has its advantages, they require additional sensing, processing, control circuitry. In addition, they require an additional cooling system and have high power loss at semiconductor junctions. In order to address the issue of power loss, use of SiC and GaN, WBG devices are been investigated [14,20,125,126]. It is expected the performance of SSCBs can be significantly improved by using WBG devices, once they become available and economically feasible.

5.5.3. Hybrid CBs (HCBs)

An alternative to the lack of steady-state efficiency of SSCB is Hybrid CBs (HCBs). As depicted in Fig. 24 HCB is a combination of SSCB, and bypass branch consisting of commutating switches (CSs) in series with FMS. During the normal operation, current flows through the bypass branch only [127–132]. To interrupt fault current, CSs are turned *OFF* to commutate all the current through SSCB branch, allowing FMS to be opened at zero current. Then the current is blocked by the SCCB assembly. Since low voltage CSs are adequate to commutate current, low conduction losses are achieved. Possible transient interrupt voltage is prevented by MOVs, which also absorb stored inductive energy in the line. Several practical realizations of this concept are presented in Refs. [128–131].

For use in HCBs, IGBTs and IGCTs are particularly more suitable due to its quick response times and availability for high voltage and current applications [43]. Due to the short *ON* state, solid-state devices do not require any additional cooling, allowing HCBs to be built compactly. Although HCBs offer advantages of both mechanical and solid-state breaker technologies combined, due to mechanical restrictions, HCBs have limited response speeds compared to SSCBs [43,132].

From the above discussion, it is clear, there has been significant progress made in the DC fault interruption technology. It is however, acknowledged that technical and economic issues associated with these

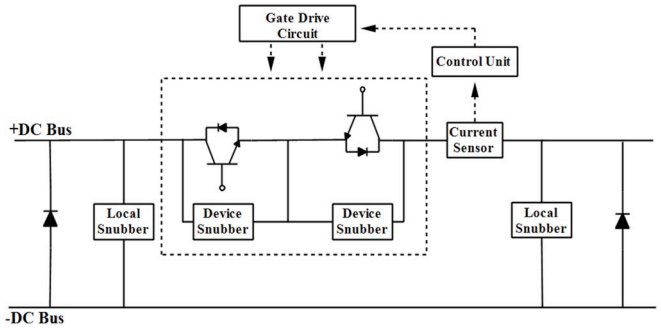

Fig. 22. Bidirectional solid-state circuit breaker, general circuitry [40].

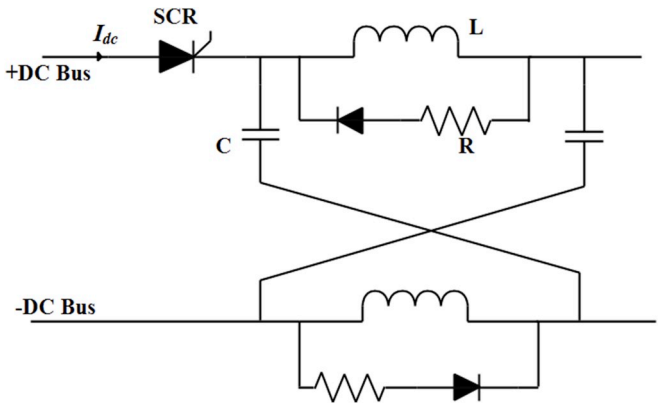

Fig. 23. Z source circuit breaker, general circuitry [14].

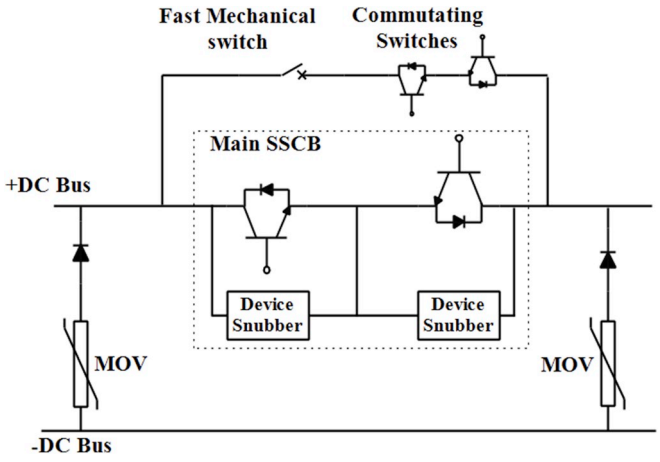

Fig. 24. Hybrid circuit breaker, general circuitry [129].

schemes require further investigation.

To summarize the above discussion, a comparison of the performance of DC fault interruption schemes, and their operational features are provided in Table 3.

6. Conclusions and future trends

This paper analyzed the fault characteristics of DCMGs and explored the current status of protection devices and challenges associated. Moreover, the protection techniques adopted in ACMGs, HVDC and MVDC networks were compared, and it is fair to mention protections aspects of DCMGs are still less explored in research. In conclusion, this study shows that fault detection, localization and interruption schemes for DCMGs require further improvements, especially in terms of speed, accuracy and cost effectiveness.

The following are the specific conclusions and recommendations of this study:

- Fault features of a DCMG were analyzed using a notional DCMG model, employing conventional converters. Limitation of DC fault current utilizing the fast clearance action of fault current blocking converters significantly improve the post-fault behavior of the DC network. However, the use of fault current blocking converters for fault current interruption in DC distribution networks is an under researched topic that requires further investigation.
- Careful selection of grounding configuration enables the safety of personnel and equipment, facilitate reliable fault detection and fault ride-through capability.
- Fast capacitor discharge and the current rise in DC systems impose strict time limits for fault detection and interruption; in this respect, it is important to consider the speed of fault detection, communication delays and response time of protective switchgear.
- The absence of frequency and phasor information makes fault detection and localization challenging, compared to its AC counterpart. Conventional protection schemes such as overcurrent, differential and distance protection require modifications to suit DCMG fault characteristics. Advanced machine learning and signal

Table 3
Performance and operational features of DC Fault interruption schemes.

Interruption scheme		Operating principle	High speed fault detection required?	Response time	On state losses	selectivity	Remarks
Fault current blocking with AC side CBs		• ACCBs operate cutting off fault current from utility grid.	No	~30 ms–100 ms	Negligible (<0.1%)	No	• Low cost
Converters with current blocking and limiting capability		• Utilizes the current blocking and limiting capability of solid-state switches.	No	<10 μs	Very high (depend on the converter architecture)	No	• Very High cost. • Uses self-protection schemes, external triggering not required.
Fault current limiters	Protective inductors at the converter terminals	• Limiting fault current transients to mitigate fast rising fault current	No	–	–	No	• Only effective in the transient stage of the fault.
	Semi- conductor FCL	• Operates in superconducting mode under normal operation, non-superconducting mode under fault current conditions.	No	<2 ms	Low (<0.1%)	No	• Unable to completely interrupt fault current, hence require series connected switches.
	Solid-state FCL	• Utilizes current limiting capabilities of solid-state switches.	Yes	<100 μs	High (~0.1–2%)	No	• Lower power loss, compared to converters with FCL capability.
Fault current blocking with DC side CBs.	Mechanical DCCB	• Creating a zero-crossing point by an oscillating circuit, to open the mechanical switch at zero current.	No	~40 ms	Negligible (<0.1%)	Yes	• Provides galvanic isolation. • Low cost.
	SSCB	• Utilizes the current blocking capability of solid-state devices.	Yes	<100 μs	High (~0.1–2%)	Yes	• Bulky cooling system required. • High cost. • No galvanic isolation capability.
	ZSCB	• Creating a zero-crossing point by absorbing part of transient energy to naturally commutate SCR.	No	<100 μs	High (~0.1–2%)	Yes	• Bulky cooling required. • High cost. • No galvanic isolation capability.
	HCB	• Creating a zero-crossing point by parallel solid-state devices to open fast acting switches at zero current.	Yes	500μs-2ms	Low (<0.1%)	Yes	• Very high cost. • Relatively small size. • No galvanic isolation capability.

processing based protection schemes were identified as a solution for DCMG protection with its ability for fast, accurate and adaptive fault detection.

- Determinant factors in selecting a DC breaker technology were identified: 1) Response time of the breaker, 2) Ability to break transient fault current and withstand interrupt voltages, 3) On state losses, 4) The costs and physical volume of the breaker and 5) Bidirectional power flow capability. In addition, provides an analytical review on each breaker design for DC applications.
- Although SSCB technology shows a promising solution for DC fault protection, high on-state losses, high costs and physical volume preclude widespread use. In the future by applying next generation WBG devices such as SiC and GaN, the properties of SSCBs may improve due to their low conduction loses, higher junction temperature and superior avalanche breakdown capability.
- A fault discrimination scheme, alongside fault interruption with a minimum opening approach, is an essential requirement to minimize the loss of power to the healthy sections of the network. The strategic positioning of fast-acting DC circuit breakers operating in coordination with fault current blocking converters can facilitate quick fault isolation, minimize damages to the network components and minimize interruptions.

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