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A New Configurable Topology for Multilevel Inverter With Reduced Switching Components

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ABSTRACT Multilevel inverters (MLI) are now becoming an important element for medium-voltage high-power applications. A low switch count MLIs are more popular due to their high efficiency, low cost, and easy control for the output having a higher number of levels. A new MLI topology for single-phase applications based on switched dc voltage source with reduced switch count is proposed in the paper. The presented topology is developed with the constraints of lesser blocking voltage of the switches with a higher number of levels at the output using a lower number of components. The proposed topology can also work in the symmetrical and asymmetrical configuration. Selective harmonic elimination (SHE) technique is applied to synthesize the staircase output voltages with eliminations of lower order harmonics by optimized computation of angles for switching operation. The comparative studies with the MLIs recommended in recent times show the importance of the proposed MLI structure in terms of reduced switch count and lower voltage stresses across switches in both asymmetrical and symmetrical configurations. The experimental results are presented to confirm the performance of the proposed topology.

INDEX TERMS Multilevel inverter, reduced semiconductor devices, symmetrical sources, asymmetrical sources, selective harmonics elimination, total standing voltage.

I. INTRODUCTION

Multilevel inverters (MLIs) are the smart arrangements of dc voltage sources with or without using capacitors and power semiconductor devices to achieve high-quality output voltage. MLIs have been widely studied and are gaining importance in the medium and high voltage power applications. This is due to several important features of MLI such as good output voltage waveforms with a lesser amount of total harmonic distortion (THD), enhanced efficiency, reduced voltage stresses across power devices and better electromagnetic compatibility [1]–[5]. Cascaded H-Bridge (CHB), flying capacitor (FC) and neutral point clamped (NPC) are the three basic structures of MLIs. NPC and FC require a higher number of components and issues of capacitor voltage balancing as the number of levels increases. Therefore, many researchers are focusing on the reduction of component count while maintaining a higher number of levels [4], [6].

The design of MLIs depends mainly on the number of voltage levels to be generated. The number of dc voltage sources/links in a topology determines the number of output levels. The magnitude of these dc voltage sources can be obtained in two configurations i.e. symmetrical and asymmetrical. In symmetrical configurations, all dc voltages have the same magnitude whereas, in the asymmetrical configurations, the magnitude of dc voltages is of different values. Therefore, a higher number of levels can be generated with the same number of dc voltage sources and power devices in an asymmetrical configuration compared to the symmetrical mode of operation [7], [8]. In recent years, topologies in both symmetrical and asymmetrical configurations have been reported in several papers. A new symmetrical cascaded MLI has been presented in [9]. It uses 10 switches for 7 levels and 16 switches for 13 levels. With more number of switches, the topology suffers from higher blocking voltages across the

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switches. A cascaded MLI using novel H-bridge has been reported in [10]. In the symmetrical configuration, topology uses lower count of power electronic devices for the same output levels as compared to NPC and CHB. Likewise, some other symmetrical topologies have been discussed in [11]–[15].

Asymmetrical topologies like E-type [16] and ST-type [17], each module uses four dc voltage sources for 13 and 17 output voltage levels, respectively. A cascade MLI has been conferred in [18] which can produce 25 levels by using 10 switches and 8 power diodes. In [16]–[18], the suggested topologies can be linked in cascade to realize an additional voltage level. Furthermore, $4\times m$ number of dc voltage sources are required for m modules connected in cascade. Such selection of dc voltage sources limits the applications of MLIs. A modular MLI using H-bridge have been reported in [19], however, it produces less number of levels using higher input source count. Moreover, it requires higher voltage rating of switches used in H-bridge. Few structures based on H-bridge have been presented in [13], [20]–[24] for asymmetrical configurations. All of these topologies have high voltage stresses on switches which is equal to the sum of all dc voltage sources.

In this paper, a new multilevel inverter topology based on switched dc voltage sources is proposed. By adding a multiple number of switched dc voltage sources, the proposed topology can produce more levels at the output. This paper is organized as follows. Section II describes the basic unit of the proposed topology along with the generalized structure with the working principle in the symmetrical and asymmetrical mode of operation. The mathematical formulations for total standing voltage (TSV) in both configurations are also presented in this section. SHE-PWM technique is described in Section III. Sections IV deals with the comparative study with some recent and popular topologies in both configurations. Results and discussion are given in Section V. An application of the proposed topology for the utility grid has been explained in Section VI and the conclusion is drawn in Section VII.

II. PROPOSED MULTILEVEL INVERTER

In this section, the operating principle of the proposed multilevel inverter topology is discussed in detail. This section also describes the different modes of configuration together with the total standing voltage calculations.

A. PROPOSED TOPOLOGY

The basic unit for the suggested MLI is illustrated in Fig. 1. It contains four dc voltage sources, two bidirectional switches (S_1, S_2) along with six unidirectional switches (S_3, S_4, S_5, S_6, S_7, *and* S_8). The bidirectional switch is made of two unidirectional switches configuration in common emitter connection, which needs only one gate driver circuit. The basic unit produces 9 levels in symmetrical configuration and 13 levels with asymmetrical configuration. For the safe operation of the proposed basic module, the pair of switches (S_1, S_2), (S_1, S_3), (S_2, S_4), (S_3, S_4), (S_5, S_6), and (S_8, S_9) should be worked in complementary mode, to prevent short-circuiting of the dc input voltage sources. Table 1 shows the different switching combinations of the basic unit together with their respective voltages at the output.

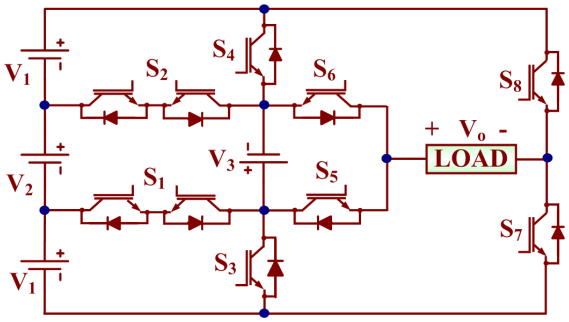


FIGURE 1. Power Circuitry of the Basic unit of proposed topology.

TABLE 1. Different switching states for proposed basic unit.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o
0	0	1	0	1	0	1	0	0
1	0	0	0	1	0	1	0	V_1
0	0	0	1	1	0	0	1	V_3
0	1	0	0	0	1	1	0	$V_1 + V_2$
0	0	0	1	0	1	1	0	$2V_1 + V_2$
0	1	0	0	1	0	1	0	$V_1 + V_2 + V_3$
0	0	0	1	1	0	1	0	$2V_1 + V_2 + V_3$
0	0	0	1	0	1	0	1	0
0	1	0	0	0	1	0	1	$-V_1$
0	0	1	0	0	1	1	0	$-V_3$
1	0	0	0	1	0	0	1	$-(V_1 + V_2)$
0	0	1	0	1	0	0	1	$-(2V_1 + V_2)$
1	0	0	0	0	1	0	1	$-(V_1 + V_2 + V_3)$

B. GENERALIZED STRUCTURE OF THE PROPOSED BASIC UNIT

To attain more voltage levels at the output, the basic module/unit can be expanded by connecting multiple switched dc voltage sources. One switched dc voltage source consists of two unidirectional switches and one dc voltage source. The generalized structure of the proposed multilevel inverter is shown in Fig. 2. The switched dc voltage sources i.e. from V_4 to V_m are used to generate a higher number of voltage levels with the addition and subtraction of different combinations of $V_1$and V_2. These voltage sources i.e. V_4 to V_m are connected in such an arrangement that all these switched dc voltage sources can be linked in series with additive polarity. For this, the polarity of the switched dc voltage source is opposite to the previously connected one. Accordingly, the connections for different power semiconductor switches are changed. All the IGBTs are connected in a topology such that none of their anti-parallel diodes become forward biased, which can be the reason for the short-circuiting of the dc voltage sources.

C. MULTILEVEL INVERTER CONFIGURATIONS

Based on the appropriate magnitude selection of different dc voltage sources, the proposed topology can work in the

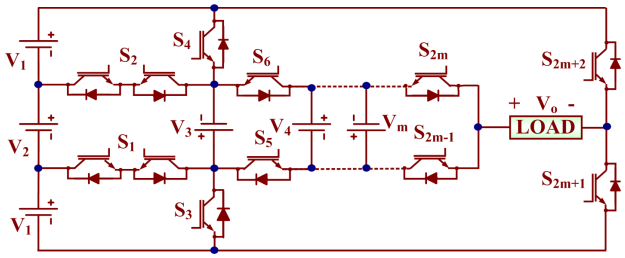


FIGURE 2. Power circuitry of the generalized structure of the proposed MLI topology.

asymmetrical and symmetrical configured sources. The number of dc voltage source decides the voltage levels for symmetrical configurations. The magnitude of different dc voltage sources used in an MLI is important to attain a higher voltage level at the output. Both configurations for the proposed structure of the MLI are discussed below.

1) SYMMETRICAL CONFIGURATION

In this mode of operation, the magnitude of all the dc voltage sources connected to the proposed inverter has a similar magnitude, i.e.

$$V_1 = V_2 = V_3 = V_m = V_{dc} \tag{1}$$

The equations for the proposed structure with $(m+1)$dc input voltage sources are given as:

$$N_{sw} = 2m + 4 \tag{2}$$
$$N_{driver} = 2\,(m+1) \tag{3}$$
$$N_{Levels} = N = 2m + 3 \tag{4}$$

where N_{sw}, N_{driver}, and N_{Levels} are the number of power semiconductor switches, the required number of the driver circuit, and levels generated in the proposed MLI, respectively.

2) ASYMMETRICAL CONFIGURATION

In the asymmetrical mode of operation, by utilizing the same number switches increases the count of voltage levels at the output. The selection of magnitude of dc voltage sources in asymmetrical configurations determines the number of levels. The equation for the maximum number of levels in the asymmetrical case is given as,

$$N_{Levels} = 2^{(m+1)} - 3 \tag{5}$$

For the proposed basic unit, by selecting the magnitude of dc voltage sources as $V_1 = 2V_{dc}$, and $V_2 = V_3 = V_{dc}$, 13 levels at the output is achieved. The equations for N_{sw}, and N_{driver} remains the same as that of symmetrical configuration.

D. DETERMINATION OF TSV

Total standing voltage (TSV) is the term which is determined as the sum of the peak magnitude of the blocking voltages across all the switches with all voltage levels considered and is given as:

$$V_{S_x}TSV = \sum_{x=1}^{2m+2} V_{S_x} \tag{6}$$

where V_{S_x} is the maximum blocking voltage of the switch S_x. TSV is one of the important factors that determine the cost of the inverter. In the proposed topology, the voltage stress across each complimentary switch is the same i.e.,

$$\begin{aligned} V_{S_1} &= V_{S_2} \\ V_{S_3} &= V_{S_4} \\ V_{S_{2m-1}} &= V_{S_{2m}} \\ V_{S_{2m+1}} &= V_{S_{2m+2}} \end{aligned} \tag{7}$$

The maximum voltage stress across switch S_1 appears when switch S_4 is conducting. In this condition, voltage stress of is experienced by switch S_1. Therefore,

$$V_{S_1} = V_{S_2} = V_1 + V_2 + V_3 \tag{8}$$

Similarly,

$$V_{S_3} = V_{S_4} = 2V_1 + V_2 + V_3 \tag{9}$$
$$V_{S_{2m-3}} = V_{S_{2m-2}} = V_{m-1} + V_m \tag{10}$$

The voltage stress across S_{2m-1} and S_{2m} is fixed by the magnitude of V_m. Hence,

$$V_{S_{2m-1}} = V_{S_{2m}} = V_m \tag{11}$$

The voltage stress across S_{2m+1} and S_{2m} is fixed by $2V_1$+V_2 and is not affected by other switched dc voltage sources connected to the topology. Therefore,

$$V_{S_{2m+1}} = V_{S_{2m+2}} = 2V_1 + V_2 \tag{12}$$

Accordingly, from (6) to (12)

$$\begin{cases} TSV = 2\left(V_{S_1} + V_{S_3} + V_{S_5} + \ldots + V_{S_{2m}}\right) \\ TSV = 2\,(5V_1 + 3V_2 + 3V_3 + 2V_{m-1} + 2V_m)\,V_{dc} \\ TSV = 2\,(3V_1 + V_2 + V_3) + \left(4 \times \sum_{1}^{m} Vm\right) \end{cases} \tag{13}$$

III. SHEPWM TECHNIQUE

THD is the main deciding factor for describing the quality of the output voltage which is given by,

$$THD = \frac{\sqrt{\sum_{i=1}^{x} V_i^2}}{V_F} \tag{14}$$

where V_i is the magnitude of i^{th} harmonic order and V_F represents a fundamental component of the output voltage. To generate a better output voltage waveform with reduced THD, numerous PWM techniques have been reported in the literature, and are categorized as fundamental switching frequency PWM (FSF-PWM) and high switching frequency PWM (HSF-PWM). The major difference in both techniques is the number of switching performed by a switch i.e. turn ON and OFF in a complete fundamental cycle of the output

voltage. In FSF-PWM, the number of turn ON and OFF has a lower number, resulting in reduced switching losses. Commonly used FSF-PWM is the nearest level control (NLC), and selective harmonic elimination (SHE-PWM). In HSF-PWM, the number of turn ON and OFF is much higher than FSF-PWM, resulting in the shifting of harmonics at a higher frequency but with higher switching losses. Sinusoidal PWM and space vector PWM are some examples of HSF-PWM [2], [25]–[27].

SHEPWM is used in this paper to achieve staircase output voltage as shown in Fig. 3. In SHEPWM, the lower order harmonics can be eliminated from the output voltage by selecting the optimized switching angles which are calculated at offline stage for each modulation index (MI) and saved in the form of lookup table in memory. In real-time, the calculated optimized switching angles based on the modulation index are recalled from memory to operate MLI.

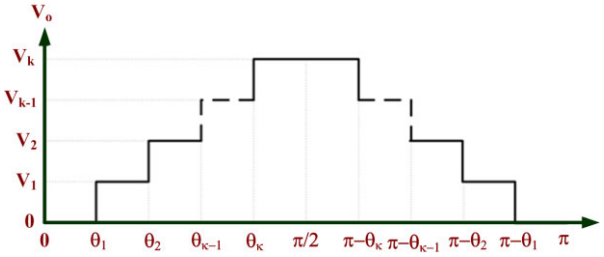


FIGURE 3. Staircase output voltage.

The output voltage can be expressed mathematically by using the Fourier series expansion and is given in (15),

$$v_o(t) = \frac{a_o}{2} + \sum_{i=0}^{n}\left(a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right)\right) \quad (15)$$

where n is the harmonic order, a_o is the dc components of the output voltage and a_n represent the even harmonic components and b_n denotes the odd-numbered harmonics in the output voltage waveform. However, due to quarter-wave symmetry of the output voltage, dc component along with all even harmonics and sine terms of odd harmonics become zero. Consequently, $v_o(t)$ simplifies as,

$$v_o(t) = \sum_{i=1,3,5....}^{n} b_n \sin(n\alpha_i) \quad (16)$$

For a staircase output voltage, b_n can be expressed as,

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{i=1,3,5,..}^{n} \cos(n\alpha_i) \quad (17)$$

In this paper, the proposed single-phase topology is used to generate 9 and 13 levels at the output with symmetrical and asymmetrical configuration respectively. For 9 levels, the harmonic orders eliminated are the 3^{rd}, 5^{th}, and 7^{th}. The equations for different harmonic orders are given as,

$$\left.\begin{array}{l} m_a = \frac{1}{S}\left[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)\right] \\ \cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) + \cos(3\theta_4) = 0 \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) = 0 \end{array}\right\} \quad (18)$$

where M_a is

$$m_a = \frac{\pi \times V_{Desired}}{4 \times k \times V_{dc}} \quad (19)$$

where V_{dc} is the nominal dc voltage, $V_{Desired}$ is the required fundamental voltage and S is the number of DC sources or optimized switching angles. For 13 levels, the harmonic orders eliminated are the 3^{rd}, 5^{th}, 7^{th}, 9^{th} and 11^{th}. The equations for different harmonic orders are given as (20), shown at the bottom of the page.

All the above equations (18) and (19) for 9 levels and equations (18) and (20) for 13 levels are solved with the condition of $\left(0 < \theta_1 < \theta_2 \ldots < \theta_s < \frac{\pi}{2}\right)$ using the PSO method as described in [28]. The feasible solutions that eliminate unwanted harmonics do not exist for the whole range of MI. Therefore, the primary objective of the SHEPWM method is to achieve the fundamental at the desired voltage with the additional benefit of removing the unwanted harmonics if realistic solutions exist. The fitness function given in (21) is used to find the optimized switching angles.

$$f = min\left[\left|100\frac{V_{Desired} - V_1}{V_{Desired}}\right|^4 + \sum_{s=2}^{S}\frac{1}{h_s}\left|50\frac{V_{h_s}}{V_1}\right|^2\right] \quad (21)$$

The order of specific harmonic is represented by h_s e.g. $h_2 = 3$ and $h_3 = 5$, and V_1 is the fundamental voltage.

In PSO, ring topology based particles are arranged that update their velocity and location using (22) and (23) respectively.

$$v_{i,j}^{t+1} = \left(v_{i,j}^{t} \times w^{t+1}\right) + \left[\begin{array}{l} C_1 + r_{1j}^{t} \times \\ \left(P_{Best,i}^{t} - x_{i,j}^{t}\right) \end{array}\right]$$

$$\left.\begin{array}{l} m_a = \frac{1}{S}\left[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) + \cos(\theta_6)\right] \\ \cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) + \cos(3\theta_4) + \cos(3\theta_5) + \cos(3\theta_6) = 0 \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) + \cos(5\theta_6) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) + \cos(7\theta_6) = 0 \\ \cos(9\theta_1) + \cos(9\theta_2) + \cos(9\theta_3) + \cos(9\theta_4) + \cos(9\theta_5) + \cos(9\theta_6) = 0 \\ \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) + \cos(11\theta_6) = 0 \end{array}\right\} \quad (20)$$

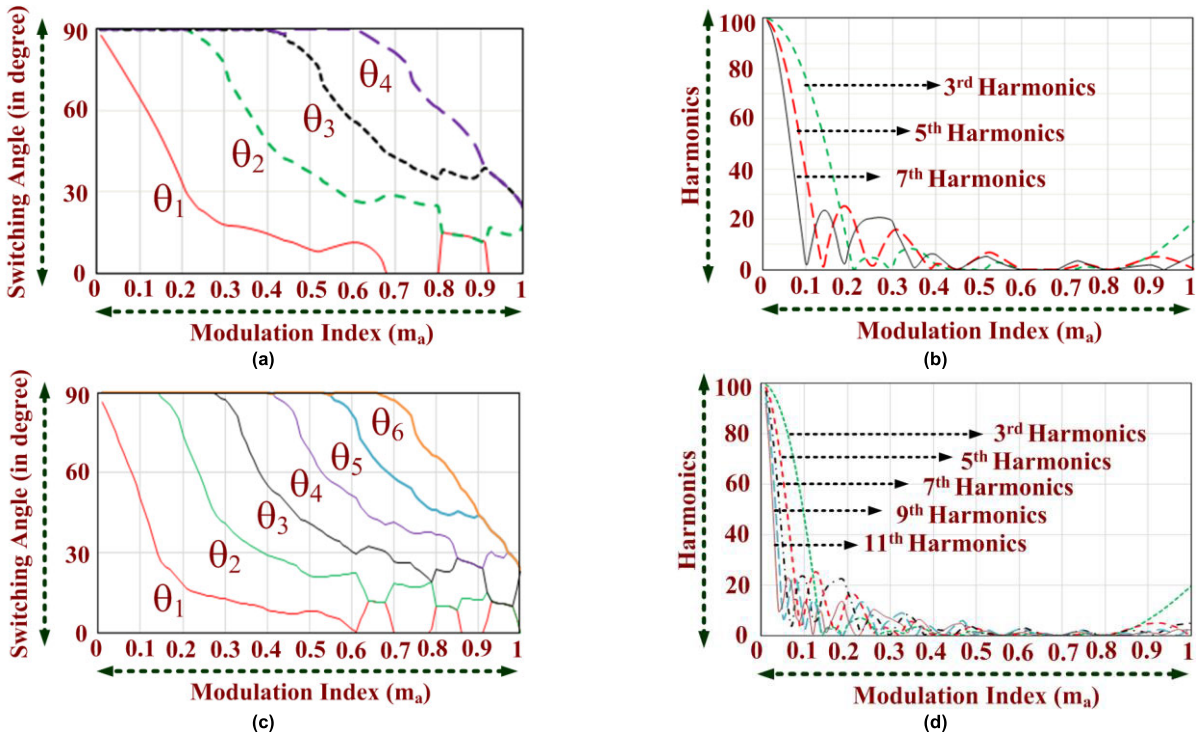


FIGURE 4. Switching angle and Harmonics (a) Optimized switching angles for 9 levels and (b) Variation of harmonics with modulation index for 9 level, (c) Optimized switching angles for 13 levels and (d) Variation of harmonics with modulation index for 13 level.

$$+\left[\begin{array}{c} C_2 + r_{2j}^t \times \\ \left(L_{Best} - x_{i,j}^t\right) \end{array}\right] \tag{22}$$

$$x_{i,j}^{t+1} = x_{i,j}^t + v_{i,j}^{t+1} \tag{23}$$

The local best particle among $i-1$, i, $i+1$ is represented by L_{Best}, the personal best location of the particle is represented by $P_{BEST,i}^t$, and inertia weight is represented by w^{t+1} and calculated using (24).

$$w^{t+1} = w_{\max} - \left(\frac{w_{\max} - w_{\min}}{\text{Total number of iterations}} \times \text{current iteration}\right) \tag{24}$$

The control parameter values selected for the PSO algorithm is given in Table 2.

Fig. 4 (a) gives the variation of angles with respect to the modulation index for 9 levels. Furthermore, Fig. 4 (b) displays the variation of 3^{rd}, 5^{th}, and 7^{th} harmonic components regarding the modulation index as a percentage of the fundamental component. For 13 levels inverter, 3^{rd}, 5^{th}, 7^{th}, 9^{th} and 11^{th} harmonics order are chosen to be eliminated from the output voltage. The solution of (20) gives the results for different angles. Variations for angle and harmonic order associated with a M_a for 13 levels is demonstrated in Fig. 4 (c) and 4 (d), respectively. Table 3 gives the optimized switching angles for two different modulation indexes for 9 and 13 levels.

TABLE 2. Control parameter value selected for PSO.

Symbol	Quantity	Values
C_1, C_2	Acceleration Coefficient	2.0
P	Swarm Size	100
w_{min}	Minimum inertia	0.4
w_{min}	Maximum inertia	0.9
$Iter_{Pmax}$	Maximum number of Iterations	500
β	Initialization of swarm	$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \theta_6$
MI	Modulation Index	$0<m_a<1$

TABLE 3. Optimized switching angles (degree).

m_a	N	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6
0.65	9	8.66	26.82	49.57	85.96	-	-
0.8	9	0.001	24.91	35.13	60.90	-	-
0.69	13	6.61	15.47	29.12	40.94	59.40	87.42
0.8	13	10.20	10.20	23.87	36.70	46.00	66.10

IV. COMPARATIVE STUDIES

The main intention of the proposed inverter is to generate more voltage levels by using a lower switch and source

TABLE 4. Comparison of proposed topology with symmetrical configuration.

Topology	Number of Switch	Number of Driver	Number of dc Sources	TSV ($\times V_{dc}$)	Negative Level
NPC	$2(N-1)$	$2(N-1)$	$(N-1)/2$	$2(N-1)$	With at least two arms
CHB	$2(N-1)$	$2(N-1)$	$(N-1)/2$	$2(N-1)$	With H-Bridge
FC	$2(N-1)$	$2(N-1)$	$(N-2)$	$2(N-1)$	With at least two arms
[9]	$(N+3)$	$(2N+7)/3$	$(N-1)/2$	$19(N-1)/6$	Inherent
[10]	$3(N-1)/2$	$3(N-1)/2$	$(N-1)/2$	$2(N-1)$	With H-Bridge
[18]	$3(N-1)/2$	$5(N-1)/4$	$(N-1)/2$	$9(N-1)/4$	Inherent
[19]	$(N+1)$	N	$(N-1)/2$	$(5N-18)$	With H-Bridge
Proposed	$(N+1)$	$(N-1)$	$(N-1)/2$	$2(N+1)$	Inherent

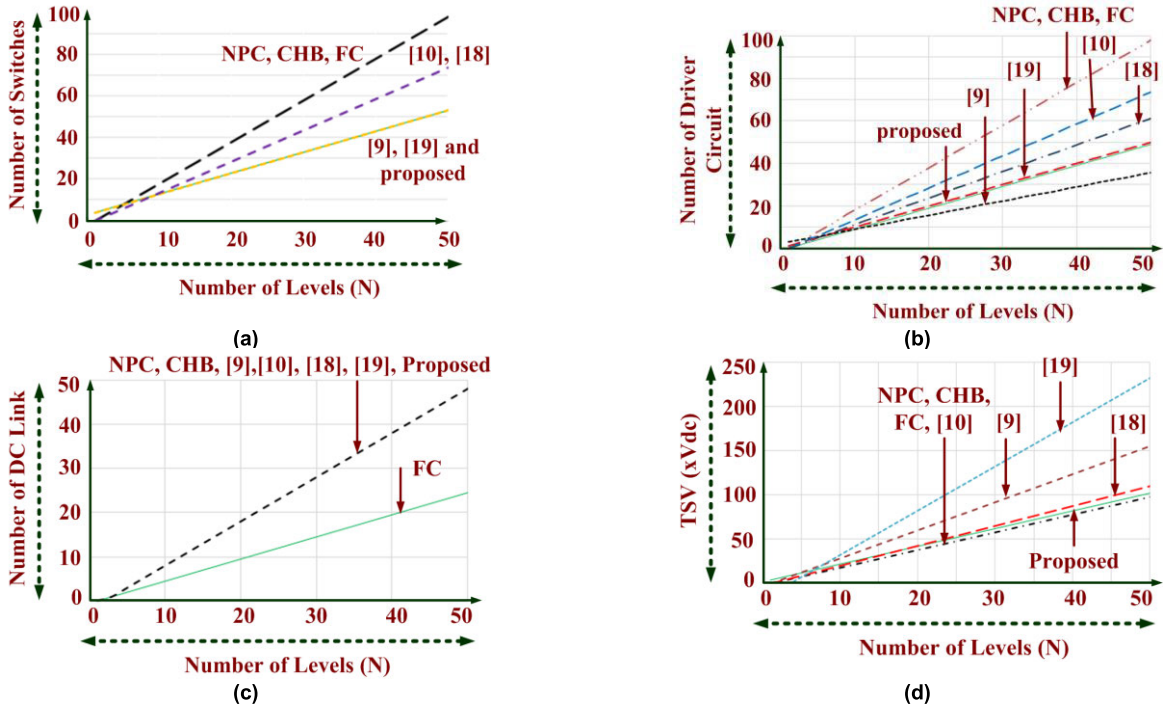


FIGURE 5. Comparison of symmetrical configurations (a) number of levels, (b) number of driver circuits required, (c) number of dc voltage sources and (d) TSV with respect of number of levels for symmetrical mode of operation.

count. To examine the performance of the proposed inverter in both configurations, a comparative investigation is carried out based on the number of switches, number of driver circuits required, TSV with respect to the voltage levels generated at the output, and dc voltage sources.

A. COMPARISON IN SYMMETRICAL CONFIGURATION

Table 4 compares the proposed inverter with other structures of the MLI topologies in a symmetrical configuration. Fig. 5 (a) compares the number of switches with the number of levels for different structures. As illustrated in Fig. 5 (a), the proposed inverter involves the least switch count along with [19]. Fig. 5 (b) gives the comparison of number of driver circuits used in a topology with respect to the number of levels. The switches used in NPC, CHB and FC are unidirectional. Therefore, the number of driver circuit required is equal to the switch count used. In some topologies, bidirectional switches are used. If bidirectional

TABLE 5. Comparison of proposed topology with asymmetrical configuration.

Topology	Number of Switch	Number of Driver	Number of dc Sources	TSV	Negative Level
[13]	$(N+19)/4$	$(N+19)/4$	$(N+7)/4$	$13(N-1)/4$	With H-Bridge
[17]	$3(N-1)/4$	$2(N-1)$	$(N-1)/4$	$5(N-1)/2$	Inherent
[18]	$5\log_5 N$	$5\log_5 N$	$2\log_5 N$	$9(N-1)/4$	Inherent
[20]	$(N+13)/2$	$(N+25)/4$	$(N+1)/4$	$7(N-1)/2$	With H-Bridge
[22]	$\frac{8\ln(N)}{\ln(7)}$	$\frac{8\ln(N)}{\ln(7)}$	$\frac{2\ln(N)}{\ln(7)}$	$5(N-1)/2$	With H-Bridge
[24]	$\frac{10\ln(N)}{\ln(17)}$	$\frac{8\ln(N)}{\ln(17)}$	$\frac{4\ln(N)}{\ln(17)}$	$9(N-1)/4$	With H-Bridge
Proposed	$\frac{2\ln(N+1)}{\ln 2}+2$	$\frac{2\ln(N+1)}{\ln 2}$	$\frac{\ln(N+3)}{\ln 2}$	$5(N-1)/2$	Inherent

switches are connected as common emitter configured, only one driver circuit is required for two switches connected to work as a bidirectional switch. From Fig. 5 (b), the proposed inverter uses less number of driver circuit compare to other structures excluding [9]. Fig. 5 (c) shows the number of dc sources essential to produce N voltage levels. The proposed structure needs the same number of dc voltage sources as other structures except for FC. The TSV of different structures in contradiction of the voltage levels is presented in Fig. 5 (d). Also, the proposed topology has lower TSV than [9], [18] and [19]. Therefore, combining all these merits makes the proposed inverter suitable for low and medium voltage operations in a symmetrical configuration.

B. COMPARISON IN ASYMMETRICAL CONFIGURATION

A comparative study is carried out among the proposed topology and recently introduced asymmetrical MLI topologies in terms of the required dc voltage sources, driver circuit, number of switches, and TSV for N number of level generation. This comparison is presented in Table 5. Topologies [22] and [24] used for comparison are selected with an optimized design which generates the highest number of voltage levels using the least source and switch count. Fig. 6 (a) - (d) graphically compares the variation of the driver circuit, number of switches, TSV, and dc voltage sources, in terms of the resulting number of levels generated at the output. The proposed MLI involves less number of switches compared to other structures except [18]. Furthermore, based on Fig. 6 (c), the proposed topology requires less number of dc voltage sources compare to [13], [17] and [20]. Likewise, the proposed topologies give a lower amount of TSV compare to others except [24]. Furthermore, without any additional circuit, the negative voltage levels can be generated. So along with this ability, in addition to requiring a lower number of switches, dc voltage sources and TSV confirm that the proposed topologies can perform better than other existing topologies in the asymmetrical configuration.

V. RESULTS AND DISCUSSION

The operation of the proposed MLI structure is validated by various experimental results. The simulation work has been performed for both symmetrical and asymmetrical configurations. The experimental setup for the proposed topology is shown in Fig. 7. TOSHIBA IGBT GT50J325 switch is used in the laboratory prototype. The gate pulses for the power switching devices are generated using Vertix-5, XC5VLX50T controller, Field Programmable Gate Array (FPGA) with SHEPWM. To avoid the DC sources being from short circuit, a delay of 2μs has been introduced between complementary switches. The experimental results have been carried out for two modulation indexes using the angles given in Table 3 for both symmetrical and asymmetrical modes of operation.

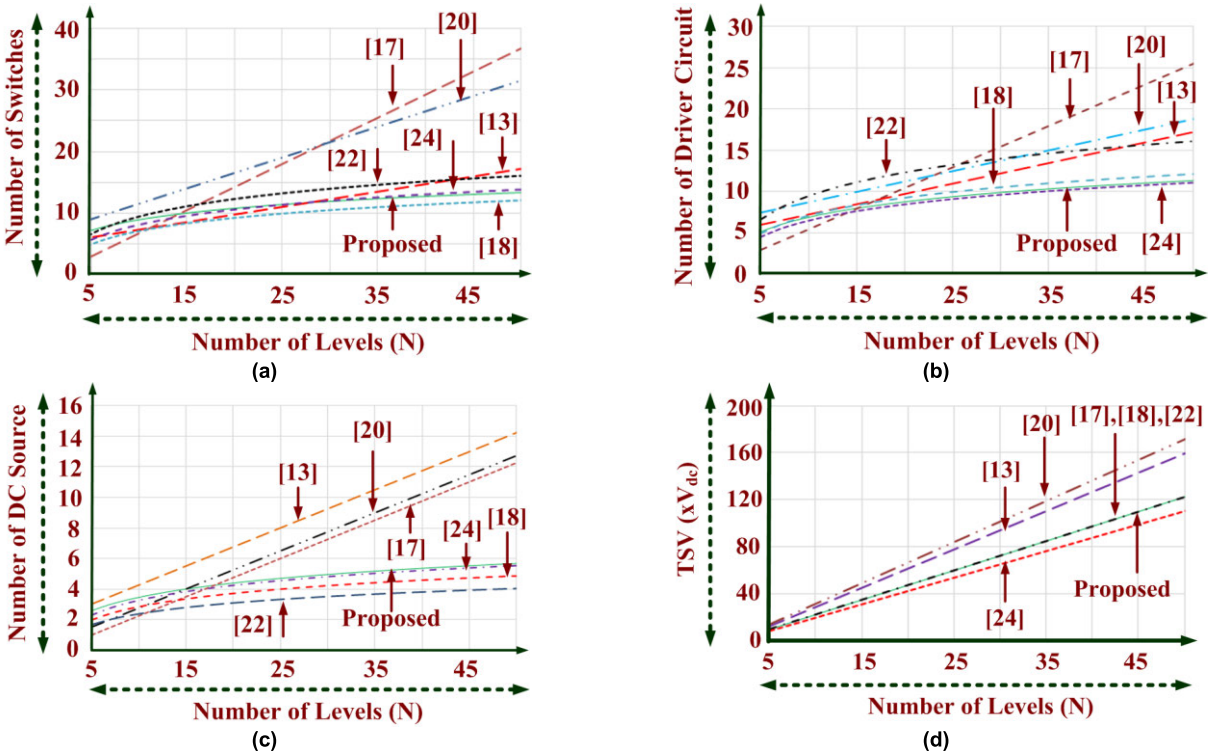


FIGURE 6. Comparison of asymmetrical configurations (a) number of levels, (b) number of driver circuits required, (c) number of dc voltage sources, and (d) TSV with respect of number of levels in asymmetrical mode of operation.

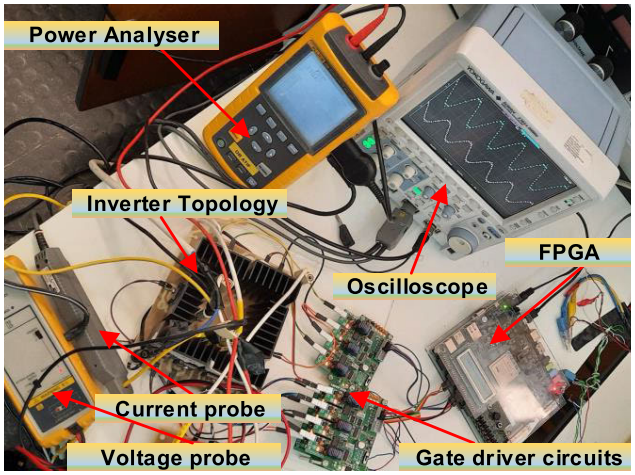


FIGURE 7. Hardware setup of the proposed MLI.

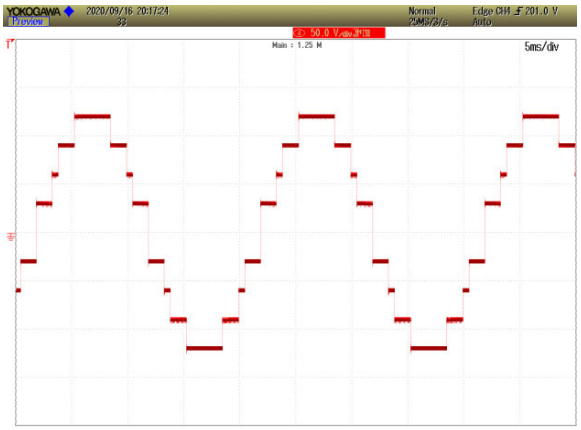
A. SYMMETRICAL OPERATION

For the symmetrical configuration, the voltage magnitude of dc voltage sources is set to 30V. The peak output voltage is 120V for 9 levels at the output with four dc voltage sources. Fig. 8 (a) and 8 (b) show the waveforms of the output voltage at the modulation index 0.80 and 0.65 respectively. Their respective harmonic spectrums are shown in Fig. 8 (c) and (d). The eliminated harmonics for 9 levels have been selected as 3^{rd}, 5^{th}, and 7^{th}. These three harmonic orders are zero as shown by the harmonic spectrum in Fig. 8 (c) and (d).

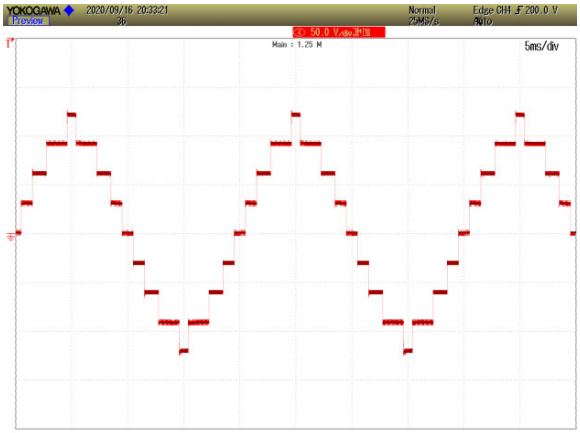
With the symmetrical configuration, the proposed topology has been tested with different loading conditions. Fig. 9 (a) and (b) shows the waveforms of load voltage and current with resistive (R) and resistive-inductive (RL) loads respectively. A 150Ω resistor has been used as an R-load and for RL load, the load parameters are 150Ω and 120mH. Furthermore, the dynamic performance of the proposed topology has also been tested. Fig. 10 (a) depicts the output waveforms of voltage and current with a change of load from no-load condition to 150Ω and from 150Ω to 75Ω. A similar waveform with RL has been shown in Fig. 10 (b) where the load is changed from no load to (150Ω+ 120mH) to (75Ω+ 120mH). In addition, the change of load type has also been considered for evaluating the performance of the proposed topology in symmetrical configuration. Fig. 11 shows the waveforms with a change of load from 150Ω to (150Ω+ 120mH).

B. ASYMMETRICAL OPERATION

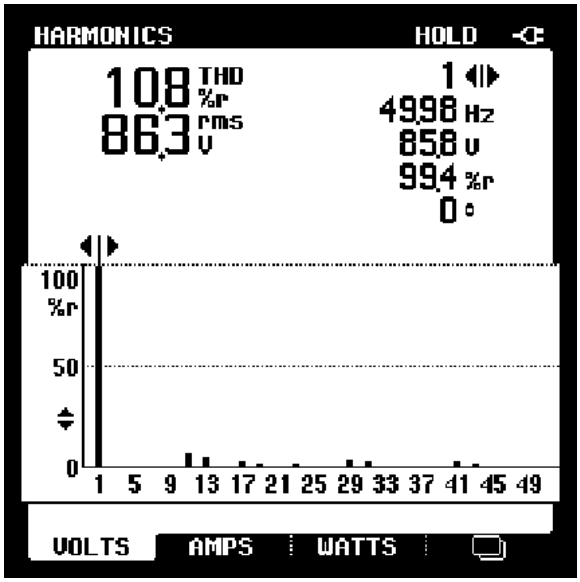
Similarly for 13 levels, the magnitude of V_1, V_2 and V_3 are selected as 60V, 30V, and 30V, respectively. Fig. 12 (a)-(d) demonstrates the experimentally obtained output voltage and their harmonic spectrum for the 13 levels output voltage at m_a of 0.8 and 0.69 respectively. The optimized angles are used to synthesize the output voltage for 13 levels. The harmonic order 3^{rd}, 5^{th}, 7^{th}, 9^{th}, and 11^{th} are removed from



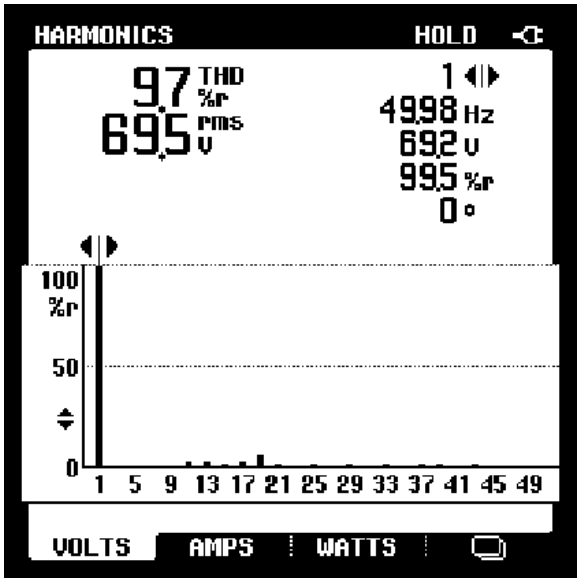
(a) Output voltage with m_a= 0.80



(b) Output voltage with m_a=0.65

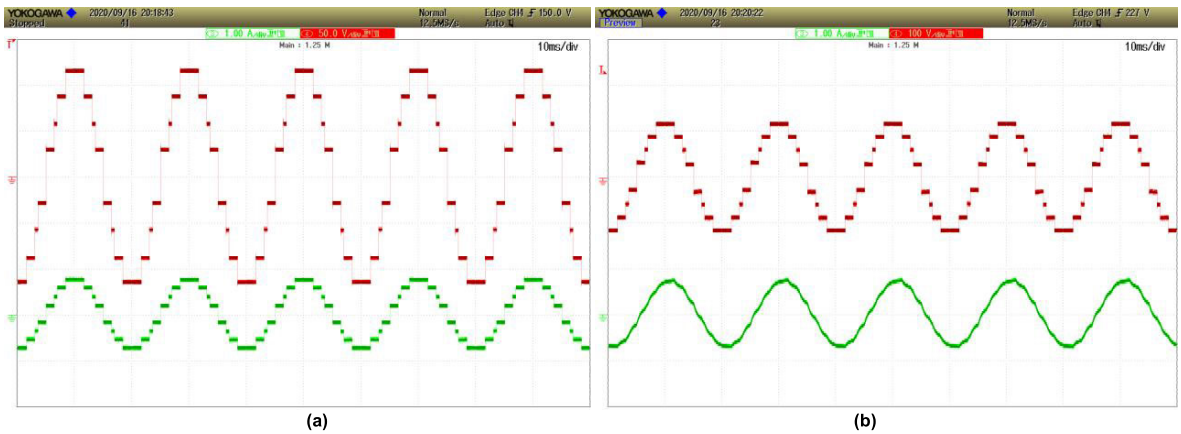


(a) Harmonic spectrum of output voltage with m_a= 0.80



(b) Harmonic spectrum of output voltage voltage with m_a=0.65

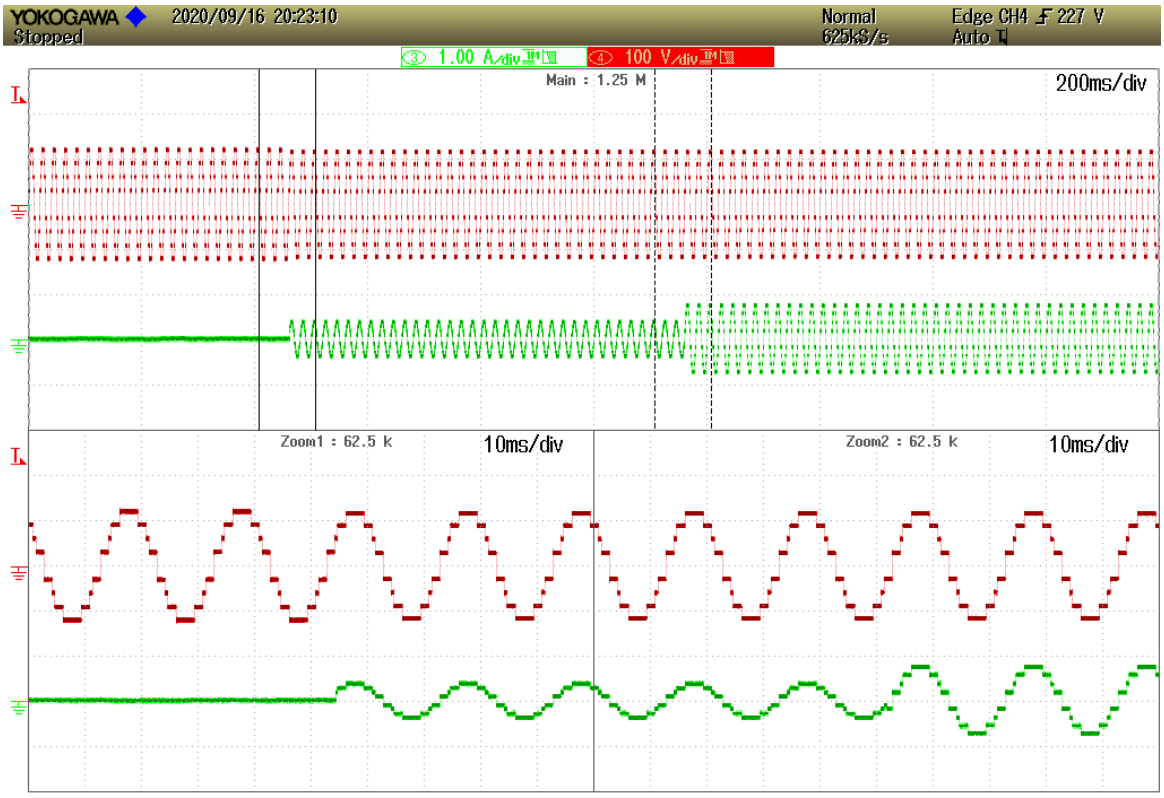
FIGURE 8. Output voltage waveform and their respective harmonic spectrums for 9 levels in symmetrical configuration.



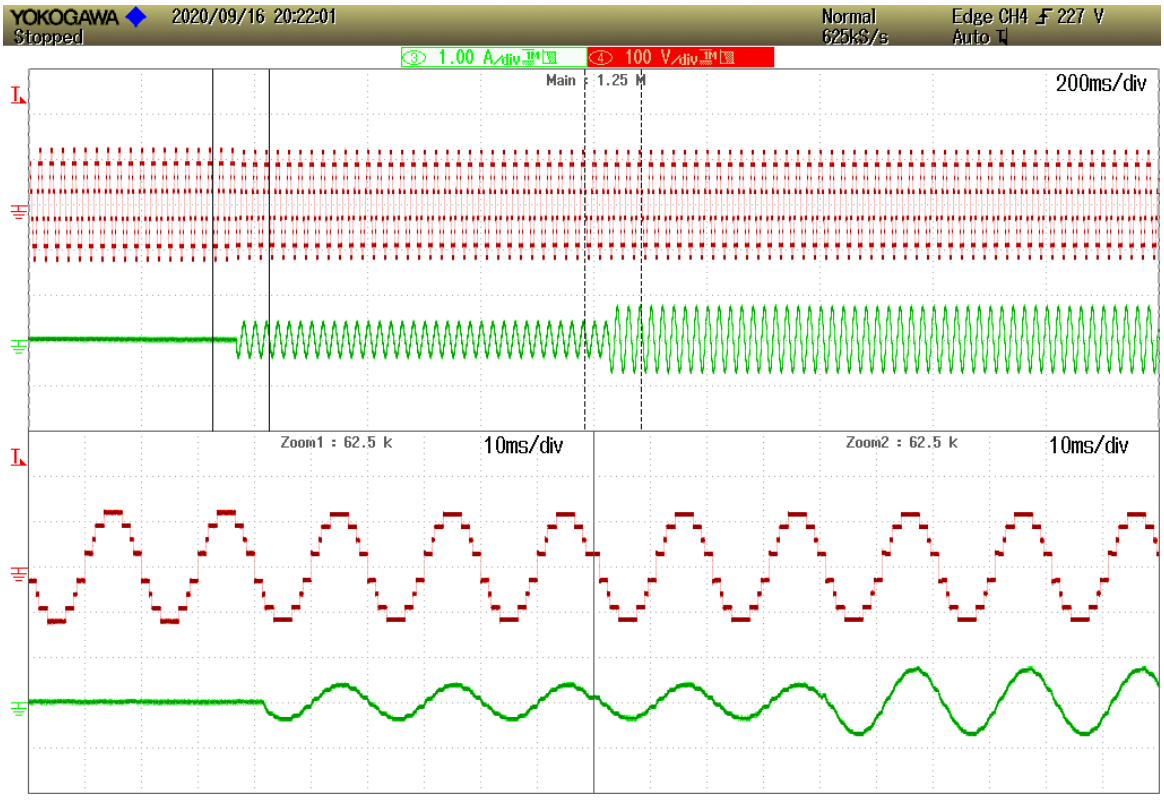
(a) (b)

FIGURE 9. Output voltage and current with symmetrical configuration (a) R load and (b) RL load, and with asymmetrical configuration.

the output voltage and is verified by the harmonic spectrums shown in Fig. 12 (b) and (d). Furthermore, the performance of the proposed structure is also examined for the dynamic change of resistive (no-load, R=150Ω, 75Ω) and series-connected resistive-inductive load (no-load, 150Ω+ L=120mH and 75Ω+ L=120mH) have been demonstrated



(a)



(b)

FIGURE 10. Output voltage and current waveform with change in (a) R load and (b) RL load with symmetrical configuration.

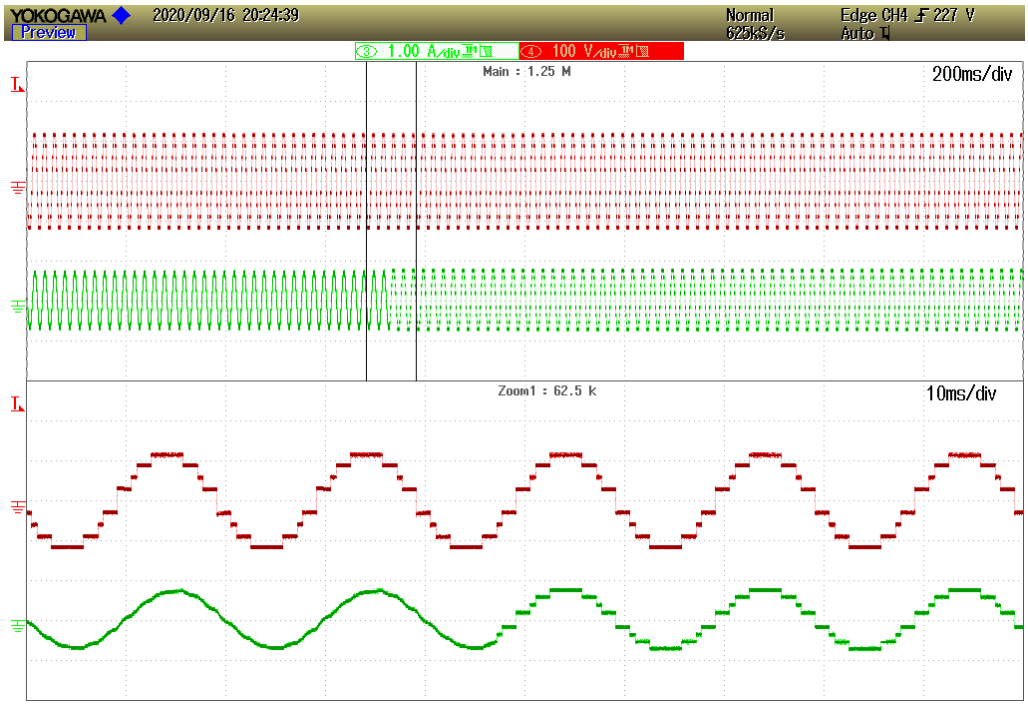
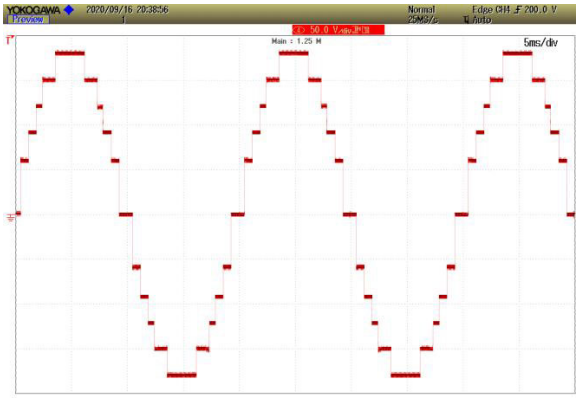
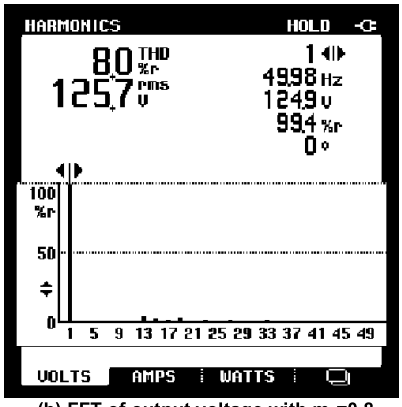


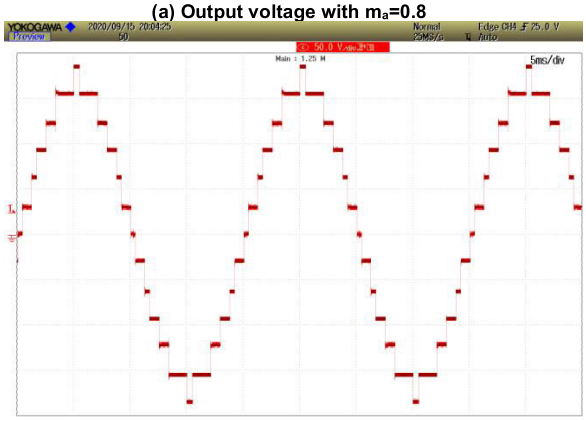
FIGURE 11. Output voltage and current waveform with change in load from RL to R load with symmetrical configuration.



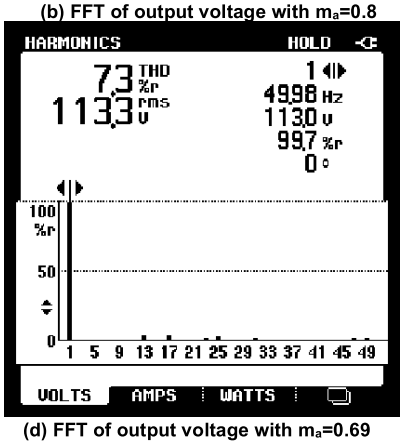
(a) Output voltage with m_a=0.8



(b) FFT of output voltage with m_a=0.8



(c) Output voltage with m_a=0.69



(d) FFT of output voltage with m_a=0.69

FIGURE 12. Output voltage and FFT of output voltage for asymmetrical configuration.

in Fig. 13 (a) and (b) respectively. In addtion, the change of load type from 150Ω to (150Ω+ L=120mH) has been demonstrated in Fig. 14 (a). The frequency of the output voltage has also been changed at the modulation index of 0.69 with a load parameter of (150Ω+ L=120mH). The output frequency has been changed from 25Hz to 100Hz

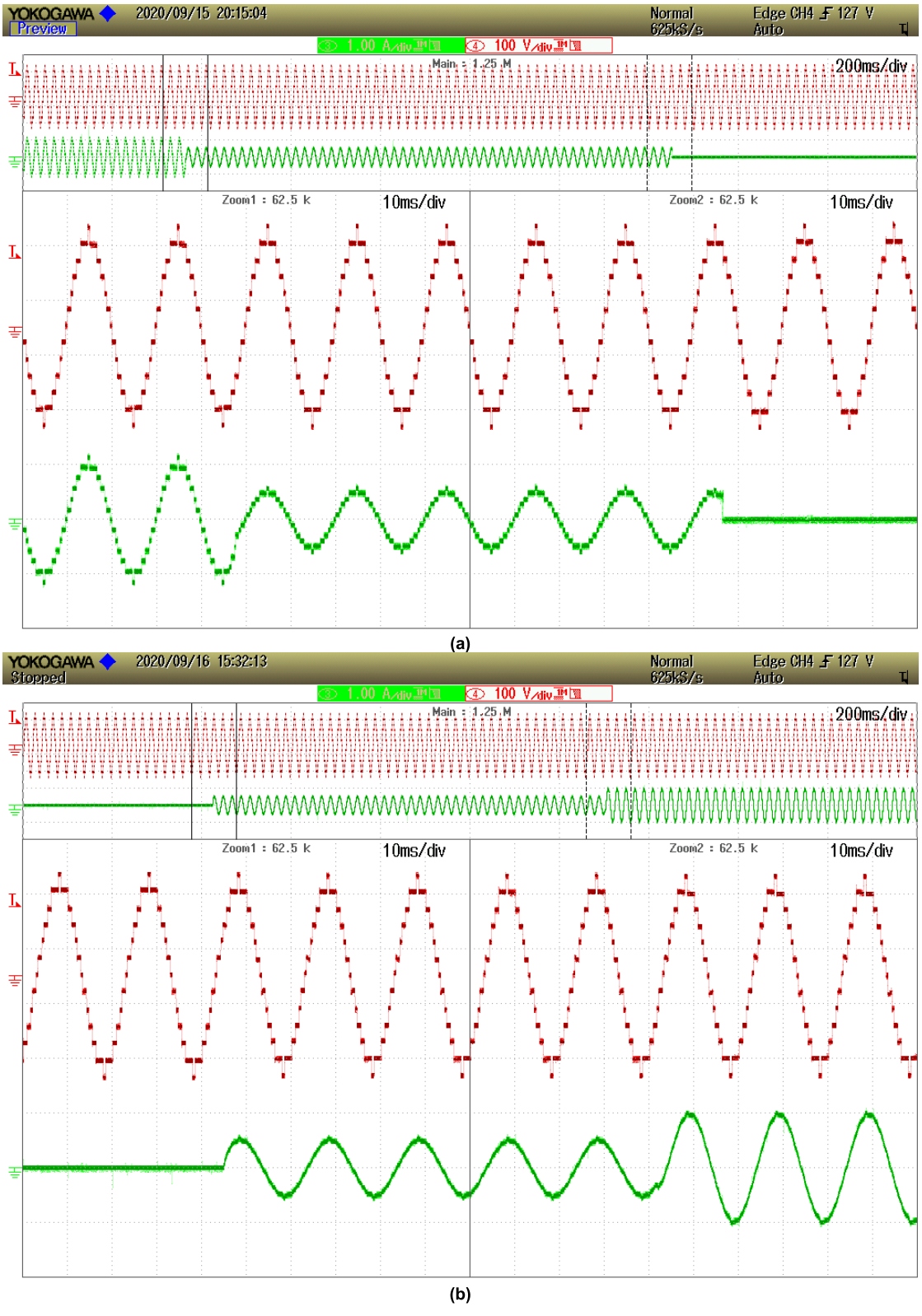


FIGURE 13. Output voltage and current waveform with change in (a) R load and (b) RL load with asymmetrical configuration.

as illustrated in Fig. 14 (b). The harmonic spectrum for the output frequency of 25Hz and 100Hz is provided in Fig. 15 (a) and (b) respectively. From all these waveforms, it can be concluded that the performance of the proposed topology is satisfactory with different real-time operating conditions.

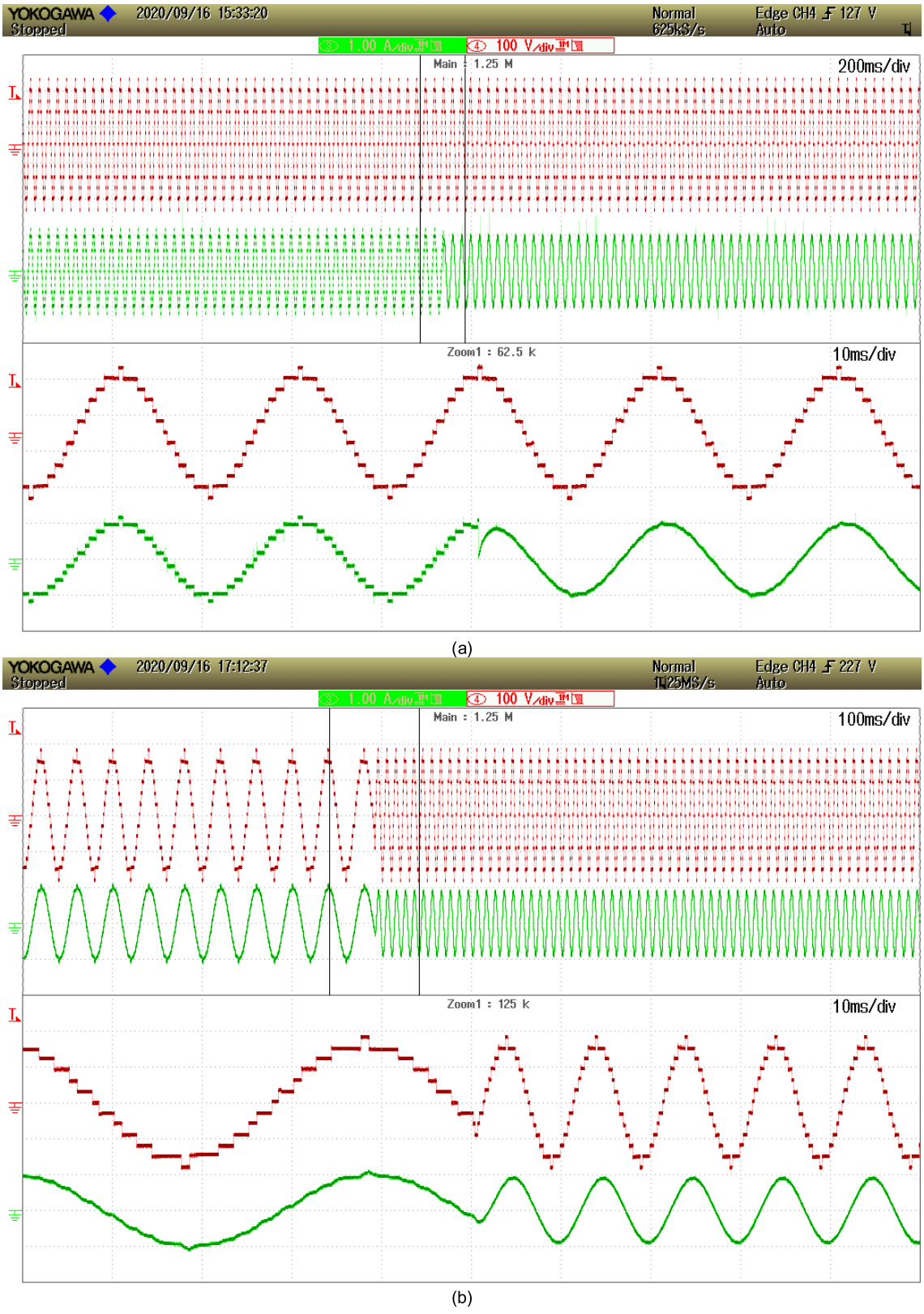


FIGURE 14. Output voltage and current waveform with change in (a) load type and (b) frequency with asymmetrical configuration.

VI. APPLICATION OF THE PROPOSED TOPOLOGY

The main contribution of the proposed topology is the reduction in the number of components which is essential for the grid-tied applications as shown in Fig. 16. Further, for the power quality improvement, the selective harmonic elimination pulse width modulation (SHEPWM) technique has been

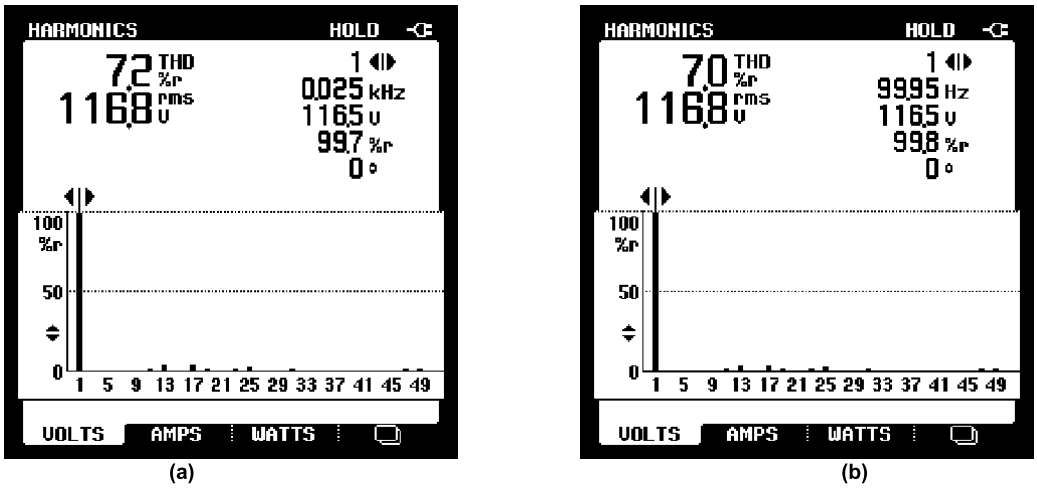


FIGURE 15. Harmonic spectrum of 13 level output voltage at modulation index of 0.69 at output frequency of (a) 25Hz and (b) 100Hz.

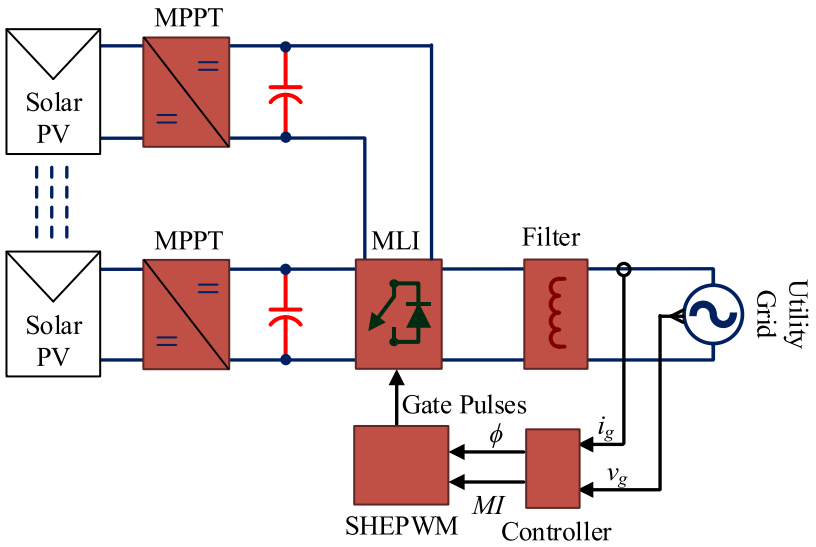


FIGURE 16. Application of the proposed topology.

used for the gate pulse generation as shown in Fig. 16. The accessible solar energy from solar PV panels is in the form of dc and a dc/dc converter is used to tracks its maximum power point (MPP). The output of the dc/dc converter forms the dc-link for the inverter. Several combinations of solar panels with MPPT can be used for the isolated dc voltage sources of the proposed topology with different magnitude. These dc-links are used as an input for the multilevel inverter MLI. The output of the inverter is ac and is suitable to feed to the utility grid through an output filter. For the control of the power, the grid voltage and current (v_g, i_g) is tracked and based on the available power, the modulation index (MI) is selected to control the output voltage of the inverter. The phase angle ϕ is used for the phase-locked loop (PLL) which is necessary to synchronize the inverter output voltage with the utility grid.

VII. CONCLUSION

A new MLI structure is suggested, which can work in both symmetrical and asymmetrical modes. The proposed structure comprises several features including lower switch count with lesser voltage stress across them. Moreover, the proposed topology uses a lower number of dc voltage sources for a certain voltage levels compared to other MLIs used for comparison. SHEPWM method is used to improve the output voltage by removing the lower order harmonics. Experimentation for both symmetrical and asymmetrical is carried for two different modulation indexes. For both modulation indexes, the selected harmonic orders are eliminated from the output voltage. Finally, the proposed topology is tested under different combinations of loads and gives satisfactory results.

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