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A multi-input, multi-stage step-up DC-DC converter for PV applications

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KEYWORDS

Step up dc/dc converter;
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Abstract The paper introduces a step-up multiple-input multi-stage dc-dc converter with a soft-switching for Photovoltaic (PV) applications. The proposed topology is constructed from series connection of switched capacitor circuits to minimize the effects of partial shading and mismatch between PV modules. A soft switching is achieved for the entire switches in the converter with no need for additional components. The applied technique utilizes the stray inductance of PCB traces to create a LC circuit so that the zero current switching is achieved for all switches. Moreover, the converter will take advantage of the superior features of Wideband gap devices in order to operate at high switching frequency. As a result, bulky capacitors in switched-capacitor circuits are significantly reduced, hence, small size multilayers ceramic capacitors with high temperature capability will be employed. Furthermore, with the lower losses and the higher temperature capability of Wideband gap devices, the thermal requirements will be reduced and with fast reverse recovery time, the snubber circuit are not required. Simulation results are presented, laboratory prototype is constructed, and experimental results are given at rated power to validate the feasibility of proposed dc-dc converter under soft switching operation.

1. Introduction

Non-conventional energy sources such as photovoltaics (PV) and wind energy become very attractive around the world due to the environmental pollution, depletion of fossil fuels, and the increase demand of electrical energy [1]. However, these sources are not continuously available in nature, and for better utilization, a power electronics interface is required [2]. For instance, the partial shading and mismatches between PV modules have a significant impact on output power of series connected PV systems [3–5]. The step up dc-dc converters are essential part in PV energy systems [6–7]. Transformerless based dc–dc converters are widely employed to achieve high voltage gain with small size, light weight and volume resulting in system with higher efficiency and higher power density. The conventional boost dc-dc converter has several drawbacks. Due to the parasitic components of power MOSFET, diode, inductor and capacitors, the voltage gain is limited to 5 times and the system efficiency is significantly reduced [8–10].

In applications where high gain dc-dc converters are needed, isolation based dc/dc converters [11–20] will be employed. However, these converters require large transformer

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turns ratio in order to achieve high voltage gain. In [13], a boost-type input inductor is proposed to overcome the drawbacks of traditional isolated converter. This type provide high voltage gain with no need for large transformer turns ratio. However, the additional inductor together with the transformer will increase the size and weight of these converters. Furthermore, due to the associated leakage inductance, active snubber circuits are required to suppress the voltage spikes.

The dc/dc converter-based voltage multiplier cell is proposed in [21]. The topology runs with relatively small duty ratio and multiple cells need to be connected together to achieve high voltage gain. Two types are recognized in literature, in [21–23] switched capacitor and switched inductor circuits are proposed. However, these converters require large number of switched capacitor cells and switched inductor cells to perform the energy transfer tasks and it can be considered the main drawback of these converter.

Nowadays, with the development of multiple-input converters, PV systems are gaining more attention. The multiple input voltage sources converters are proposed to fully utilize the advantages of PV modules [24–25]. A basic circuit of multiple DC source with modular structure is shown in Fig. 1. A single dc-dc converter is assigned for each module to regulate the output voltage. The modules are connected in cascaded manner to increase the output voltage gain. Comparing to the conventional centralized and multistring structure, the multiple-input converters systems are more efficient. Advantages of multiple-input converters to PV modules are, 1) modular and flexible structure 2) independent control, 3) better maximum power point tracking, 4) less partial shading effect and mismatch losses and 5) higher reliability, safety, and protection 6) lower maintenance and cost.

In this paper, a numerous effort has been made to develop a step up, multi-stage dc-dc converter based switched capacitor with reduced voltage stress on all power devices. The semiconductor devices and capacitors are the only components in the circuit. The soft switching operation for all switching devices at both turning on and turning off time is the main advantage of the proposed converter resulting in converter with low electromagnetic interference (EMI) and low switching loss. Furthermore, the soft switching operation enable the converter to operate with high switching frequency and thus lead to smaller size passive components and higher power density. Additionally, the superior feature of high switching frequency operation of GaN devices provide several advantages to the proposed converter. Smaller size multilayers ceramic capacitors with high temperature capability can be employed instead of large electrolytic capacitors, and with the lower losses and the higher temperature capability, the thermal requirement will be significantly reduced, and with fast reverse recovery, the snubber circuit are not needed.

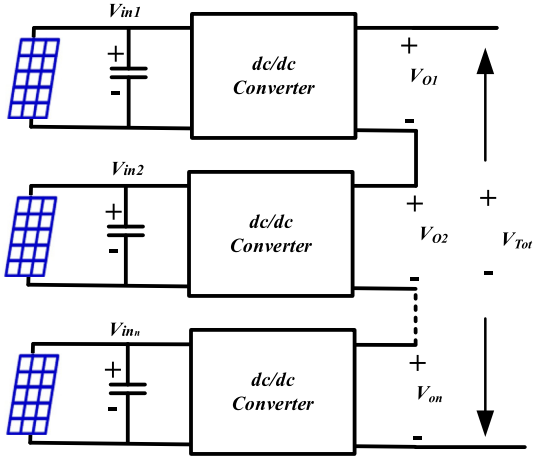


Fig. 1 General circuit structure of the proposed multi-input multi-sage dc/dc converter.

2. The proposed multi-input converter

The diagram of the proposed converter is shown in Fig. 1. The converter provides boost functionality and has multistage circuit structure which make the system more flexible to integrate different voltage sources and to increase the overall system's power generating capacity [26]. These stages are connected in series to build up a string of dc/dc converters, therefore, the output voltage of all stages is added up and the total output voltage V_{Tot} equal to the sum of the output voltages for N number of stages. The output voltage for N number of stages is described in the following equation:

$$V_{Tot} = \sum_{i}^{N} V_{oi} i = 1, 2, 3, ..., N \tag{1}$$

2.1. Circuit overview

The proposed multi-input converter extracted from general structure is shown in Fig. 2. The soft-switching realization and the high switching frequency operation is the most distin-

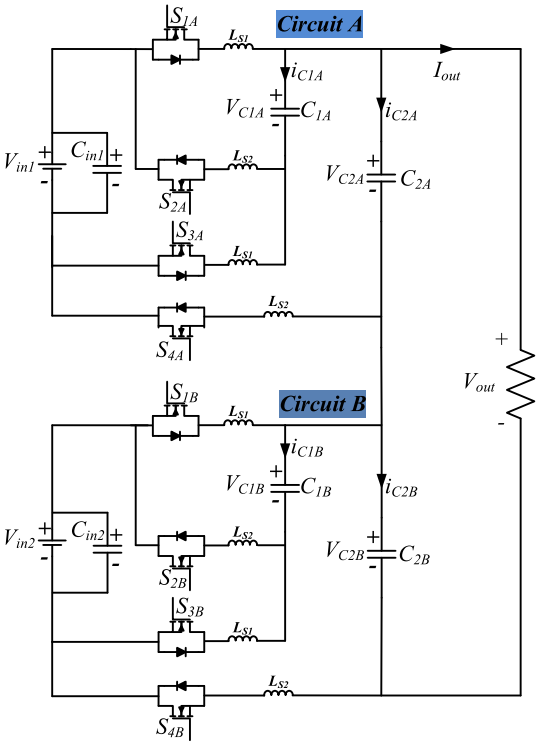


Fig. 2 The proposed two-stage step-up dc/dc converter.

guished feature of the proposed converter. As can be seen in Fig. 2, two separate switched capacitor circuits, circuit A and circuit B, with two input sources, V_{in1} and V_{in2}, are connected in parallel to increase the transferred power to the load and can generate four times voltage gain. The first input voltage source (V_{in1}) is connected to circuit A. Circuit A consists of four power switching devices ($S_{1A} \sim S_{4A}$), two capacitors (C_{1A}, C_{2A}) and two intentionally created stray inductances L_{S1} for charging loop of C_{1A} and L_{S2} for charging loop of C_{2A}. Similarly, the second power source (V_{in2}) is connected to circuit B that consists of four power switching devices ($S_{1B} \sim S_{4B}$), two capacitors (C_{1B}, C_{2B}) and the stray inductance L_{S1} and L_{S2}. By connecting these two circuits in series, the total output voltage across the output load is the sum of voltages across the output capacitors C_{2A} and C_{2B}. In Fig. 2, the passive components in circuit A (C_{1A}, C_{2A}) and in circuit B (C_{1B}, C_{2B}) become a serious problem to further reduce size, weight, and cost of the converter. However, by using the wide bandgap devices and the small size multilayer ceramic capacitors, the switched capacitor circuit can be a good option in low power and high switching frequency applications.

2.2. Circuit operating principle

Since the converter has an identical structure, the following analysis will be only for the circuit A. Circuit B can have the same circuit analysis. The schematic of circuit A is shown in Fig. 3. It has four power switches and two capacitors. The L_{S1} represents the stray inductance of PCB traces when the capacitor C_{1A} is being charged with input voltage V_{in1}. However, L_{S2} represents the stray inductance loop of PCB circuit traces as the capacitors C_{2A} is being charged when C_{1A} and V_{in1} are connected in series. Also, S_{1A} and S_{3A} are the switching devices in charging loop of capacitor C_{1A} and controlled in complementary with switches S_{2A} and S_{4A} in charging loop of capacitor C_{2A}. Both stray inductances L_{S1} and L_{S2} represent the the package inductance of the MOSFETs, capacitor, and the stray inductance of the PCB traces. For the sake of analysis, one assumes that the stray inductance in both charging loops are equal, and that is $L_s = L_{s1} = L_{s2}$. Circuit A in Fig. 3 has two operating switching states. The first switching states is shown in Fig. 4(a), when switches S_{1A} and S_{3A} are turned ON simultaneously, the voltage source V_{in1} charges the intermediate capacitor C_{1A} through S_{1A} and S_{3A}, energy is transferred to the intermediate capacitor (C_{1A}) and in this time the output capacitor C_{2A} is being discharged to the load and provide the required load current I_{out}. In the second switching state as shown in Fig. 4(b), switches S_{1A} and S_{3A} are turned OFF, S_{2A} and S_{4A} are turned ON, the voltage source V_{in1} and capacitor C_{1A} are connected in series and capacitor C_{2A} is charged through S_{2A} and S_{4A}. The total current through S_{2A} and S_{4A} equals the sum of both I_{out} and I_{C2A}. And in order to achieve ZCS for the switches S_{1A}, S_{2A}, S_{3A}, and S_{4A}, the stray inductance of charging loop L_{s1} and L_{s2} are utilized to create a resonant LC circuit with a sinusoidal shape charging current. The details of ZCS operation principle will be studied in Section 3.

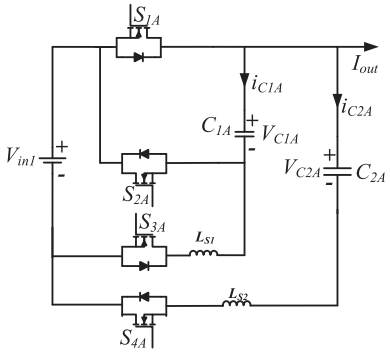
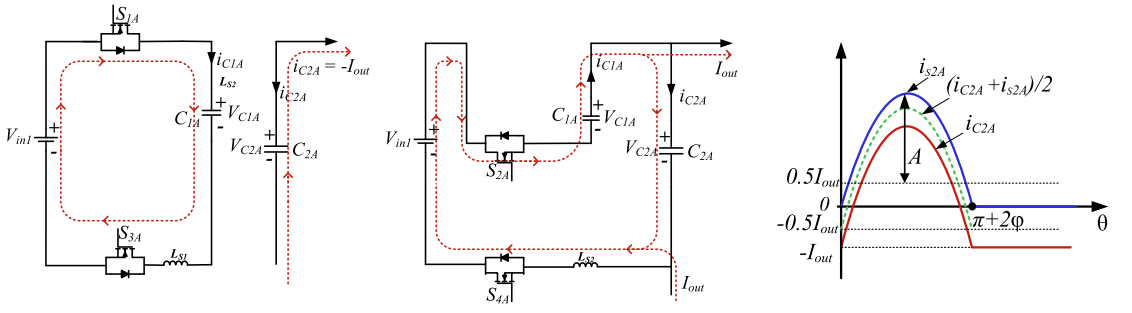


Fig. 3 Schematic of Circuit A.

3. Realization of soft-switching in the proposed DC/DC converter

3.1. Soft switching

By analyzing the operating principle of circuit A, the switching state 1 as shown in Fig. 4(a) and switching state 2 as shown in Fig. 4(b) has two differences in their circuit structure. The first difference, during switching state 1, only capacitor C_{1A} resonates with the stray inductance L_{S1}. However, during the switching state 2, the intermediate capacitor C_{1A} and output capacitor C_{2A} resonate with the stray inductance L_{S2}. Therefore, the total capacitance of the switching state 2 is a result of two capacitors C_{1A} and C_{2A} connected in series, which cause a larger oscillation frequency than that of switching state 1. The second difference, during switching state 2, input dc source V_{in1} and capacitor C_{1A} are connected in series to charge



(a) Switching states 1 (b) Switching states 2 (c) Current waveforms of S_{2A} and C_{2A}

Fig. 4 (a). Switching states 1 Fig. 4(b) Switching states 2 Fig. 4(c). Current waveforms of S_{2A} and C_{2A}.

capacitor C_{2A} and in the same time provide load current I_{out}. Therefore, if switches S_{2A} and S_{4A} is required to to realize ZCS, the conduction angle of switching *state 1* must be larger than the conduction angle of switching *state 2*.

Fig. 5 shows the ideal waveforms of the proposed dc-dc converter under steady-state condition. V_{gS1A} and V_{gS3A} are the gate signals of switches S_{1A} and S_{S3A} with duty cycle D_1 and V_{gS2A} and V_{gS4A} are the gate signals of switches S_{2A} and S_{4A} with duty cycle D_2. V_{DS1A}, V_{DS3A} and V_{DS2A}, V_{DS4A} are the drain source voltage of the switches S_{1A}, S_{3A} and S_{2A}, S_{S4A}, respectively. I_{S1A}, I_{S3A} and I_{S2A}, I_{S4A} are the drain-source currents of the switches S_{1A}, S_{3A} and S_{2A}, S_{S4A}. When the switches S_{1A} and S_{3A} in the first switching state are turned on, the current through the switches starts to resonate from zero with sinusoidal shape, and when the switching frequency matches the resonant frequency, the switches will be turned OFF at zero current. Therefore, ZCS for switches S_{1A} and S_{3A} are realized. Similar current waveforms and ZCS operation will occur for switches S_{2A} and S_{4A} during switching state 2. In Fig. 5, I_{C1A} and I_{C2A} are the current through capacitor C_{1A} and C_{2A}. Capacitor C_{1A} is charged with sinusoidal current shape waveform whereas capacitor C_{2A} is charged with linear current waveform. V_{C1A}, V_{C2A} are the voltage across the capacitor C_{1A} and C_{2A} with a dc offset equal to the input voltage for capacitor C_{1A} and twice the input voltage for capacitor C_{2A}.

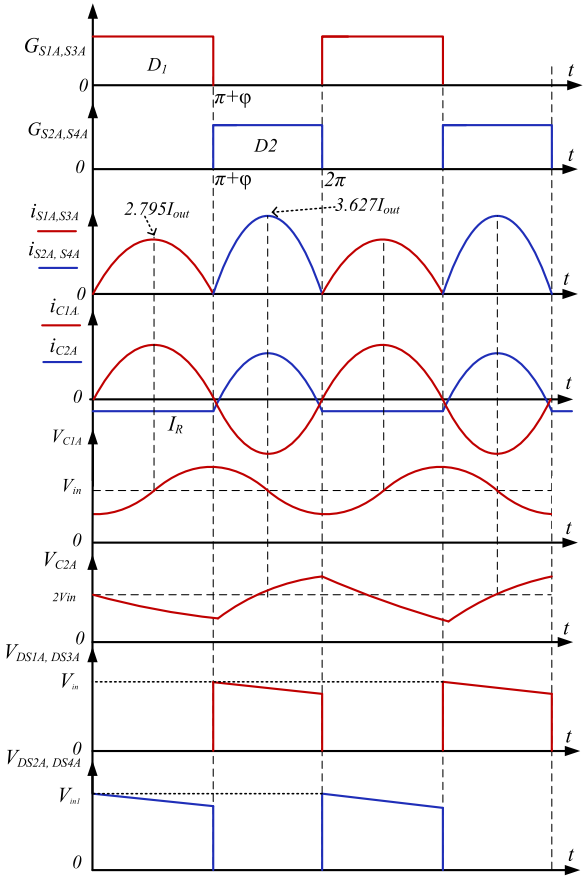


Fig. 5 Ideal voltage/current waveforms of proposed dc/dc converter.

3.2. Duty ratio calculation for the purpose of soft switching

The circuit parameters in Fig. 5(b) and the predicted current waveforms of switching states in Fig. 5(c) are utilized to find the exact value of the duty ratio in order to realize soft switching in the proposed circuit. In this analysis, the stray inductance in the charging loop of the switching state 2 is defined as L_{S2}. So, if S_{2A} and S_{4A} are turned on, Eq. (2) can be established:

$$V_{in} + V_{C1A}(t) - V_{C2A}(t) = L_{S2}\frac{d}{dt}i_{S2A}(t) \tag{2}$$

get the derivative of Eq. (2)

$$\frac{d}{dt}\left(V_{in} + V_{C1A}(t) - V_{C2A}(t)\right) = L_S\frac{d^2}{dt^2}i_{S2A}(t) \tag{3}$$

where, $L_S = L_{S1} = L_{S2}$

During switching state 2, the current through switch S_{2A} will provide the current to load and at the same time charges the capacitor C_{2A}, so,

$$i_{S2A}(t) = i_{C2A}(t) + I_{out} \tag{4}$$

another current expression can be derived for switch S_{2A},

$$i_{S2A}(t) = -C\frac{d}{dt}V_{C1A}(t) \tag{5}$$

Where $C = C_{1A} = C_{2A}$. The current in the output capacitor C_{2A} can be derived as,

$$i_{C2A}(t) = C\frac{d}{dt}V_{C2A}(t) \tag{6}$$

Eqs. (5) and (6) are substituted into (3), and Eq. (7) can be derived:

$$\frac{i_{C2A}(t) + i_{S2A}(t)}{C} = L_{S2}\frac{d^2}{dt^2}i_{S2A}(t) \tag{7}$$

If the output current has always constant value, the following expression can be obtained,

$$\frac{d^2}{dt^2}i_{S2A}(t) = \frac{d^2}{dt^2}\,i_{C2A}(t) \tag{8}$$

From (7) and (8), the currents sum of switch S_{2A} and output capacitor C_{2A} can be rewritten as

$$i_{C2A}(t)+i_{S2A}(t) = \frac{1}{2}CL_{S2}\frac{d^2}{dt^2}(i_{C2A}(t) + i_{S2A}(t)) \tag{9}$$

The expected output result from Eq. (9) is sinusoidal current shape and each of $i_{S2A}(t)$ and $i_{C2A}(t)$ has the following expression

$$\begin{aligned} i_{S2A}(t) &= A\sin(\omega_2 t + \phi) + \tfrac{I_{out}}{2} \\ i_{C2A}(t) &= A\sin(\omega_2 t + \phi) - \tfrac{I_{out}}{2} \end{aligned} \tag{10}$$

Where ω_2 is the oscillation frequency and can be calculated using the circuit starry inductance L_s and the capacitor C, so

$$\omega_2 = \frac{\sqrt{2}}{\sqrt{L_S C}} \tag{11}$$

Eq. (10) shows that both current flow with a sinusoidal shape, hence, the current is starting/ending the charging process with zero value, therefore,

$$\begin{aligned} A\sin(\phi) &= -\tfrac{I_{out}}{2} \\ A\sin(\omega_2 T_2+\phi) &= -\tfrac{I_{out}}{2} \end{aligned} \tag{12}$$

It can be concluded from Eq. (12) that, the phase angle ϕ has negative value ($\phi < 0$), and the switching turn on time T_2 of second switching state for switches S_{2A} and S_{4A} is bounded by

$$\frac{\pi}{2} \le \omega_2 T_2 + \phi \le \pi \tag{13}$$

Thus, the two equation in (12) can be solved if

$$\omega_2 T_2 + \phi = \pi - \phi \tag{14}$$

Using Eqs. (11) and (14), the turn on time of second switching state is calculated as (let $\varphi = -\phi$)

$$T_2 = (\pi + 2\varphi)\frac{1}{\omega_2} = (\pi + 2\varphi)\frac{\sqrt{L_S C}}{\sqrt{2}} \tag{16}$$

The switching turn-on time T_1 for the first switching state can be calculated by:

$$T_1 = \pi\sqrt{L_S C} \tag{15}$$

From (15) and (16), the total switching time T_S is derived as,

$$T_S = T_1 + T_2 = \sqrt{LC}\left(\frac{1}{\sqrt{2}}(\pi + 2\varphi) + \pi\right) \tag{17}$$

the duty ratio of switching state 1 (D_1) and switching state 2 (D_2) in order to realize ZCS operation for all switches can be calculated by

$$\begin{aligned} D_1 &= \tfrac{T_1}{T_S} = \tfrac{2\pi}{2\pi+\sqrt{2}(\pi+2\varphi)} \\ D_2 &= \tfrac{T_2}{T_S} = \tfrac{\sqrt{2}(\pi+2\varphi)}{2\pi+\sqrt{2}(\pi+2\varphi)} \end{aligned} \tag{18}$$

To find the exact value of ϕ, the current second balance of output capacitor C_{2A} is applied, therefore,

$$\frac{D_2}{\pi + 2\varphi}\int_0^{\pi+2\theta}\left(A\sin(\theta+\varphi) + \frac{I_{out}}{2}\right)d\theta = I_{out} \tag{19}$$

Solving Eq. (19), and substituting the result in Eq. (10), noticing that ($\varphi = -\phi$), the value of amplitude A and phase angle ϕ is obtained as

$$\begin{aligned} A &= 3.128 I_{out} \\ \varphi &= 9.20^{\circ} = 0.161\text{rad} \end{aligned} \tag{20}$$

Substitute theses values in Eq. (18), the duty ratio D_1 and D_2 of the two switching states becomes

$$\begin{aligned} D_1 &= 0.562 \\ D_2 &= 0.438 \end{aligned} \tag{21}$$

Based on (21), the conduction angle of switches S_{1A} and S_{3A} in the switching state 1 and the switches S_{2A} and S_{4A} in the switching state 2 can be estimated as

$$\begin{aligned} \gamma_1 &= 1.124\pi \\ \gamma_2 &= 0.876\pi \end{aligned} \tag{22}$$

The current flow in switches S_{2A}, S_{4A} and output capacitor C_{2A} is described as follow:

$$i_{S2A}(t) = i_{S4A}(t) = 3.625 I_{out}\sin\left(\omega t - 9.20^{\circ}\right) \tag{23}$$

So, the peak current amplitude of switches S_{2A} and S_{4A},

$$I_{S2A\_peak} = I_{S4A\_peak} = 3.625 I_{out} = \frac{3.625 P_o}{4 V_{in}} \tag{24}$$

However, to find the peak amplitude of switches S_{1A} and S_{2A}, the current second balance of capacitor C_{1A} is applied,

$$\int_0^{1.124\pi}\left(B\sin\left(\frac{\theta}{1.124}\right)\right)d\theta = 2\pi I_{out} \tag{25}$$

And this will result in the peak current amplitude of switches S_{1A} and S_{2A}, B = 2.795Iout, therefore,

$$I_{S1A\_peak} = I_{S3A\_peak} = 2.795 I_{out} = \frac{2.795 P_o}{4 V_{in}} \tag{26}$$

4. Efficiency analysis

Because the soft switching operation of the circuit, the switching losses on switches $S_{1A} \sim S_{4A}$ and $S_{1B} \sim S_{4B}$ of the proposed converter are not considered. Therefore, the power loss analysis includes three parts: conduction losses in the power devices, and losses in the capacitors.

4.1. Conduction losses in semiconductor devices

The conduction loss in semiconductor devices can be estimated from their RMS current value calculated in previous section. Fig. 6 shows the current profiles of the switches in the circuit A. S_{1A}. S_{3A} together only conduct in the first switching state, and S_{2A}, S_{4A} conduct in the second switching state. S_{1A} and S_{2A} carry only the charging current of capacitor C_{1A}. However, in the second switching state, switches S_{2A} and S_{4A} carry the charging current for output capacitor C_{2A} and provide the load current I_{out}. The current of the switches S_{1A} and S_{2A} can be expressed using:

$$I_{S1A} = I_{S3A} = \begin{cases} B\sin\left(\frac{\theta}{1.124}\right) 0 \le \theta \le 1.124\pi \\ 0 \quad 1.124\pi \le \theta \le 2\pi \end{cases}$$

So, the RMS current value of switches S_{1A} and S_{2A} can be calculated as

$$I_{S1A\_RMS} = I_{S3A\_RMS} = 1.482 I_{out}$$

The power conduction losses in switches S_{1A} and S_{3A} can be estimated as

$$P_{con\_S1A} = P_{con\_S3A} = 2.196 {I_{out}}^2 R_{ds\_on}$$

The current flow in the switches S_{2A} and S_{4A} of circuit A can be expressed using

$$I_{S2A} = I_{S4A} = \begin{cases} 0 \quad 0 \le \theta \le 1.124\pi \\ A\sin\left(\frac{\theta}{0.876}\right) + I_{out} 1.124\pi \le \theta \le 2\pi \end{cases}$$

The RMS current value of switches S_{2A} and S_{4A} can be calculated from the following equation

$$I_{S2A_{RMS}} = I_{S4A_{RMS}} = 1.696 I_{out}$$

And the power conduction losses in switches S_{2A} and S_{4A} can then be calculated as

$$P_{con\_S2A} = P_{con\_S4A} = 2.876 {I_{out}}^2 R_{ds\_on}$$

The four switching devices $S_{1B} \sim S_{4B}$ of circuit B in Fig. 3 can experience the same current profile and power conduction losses.

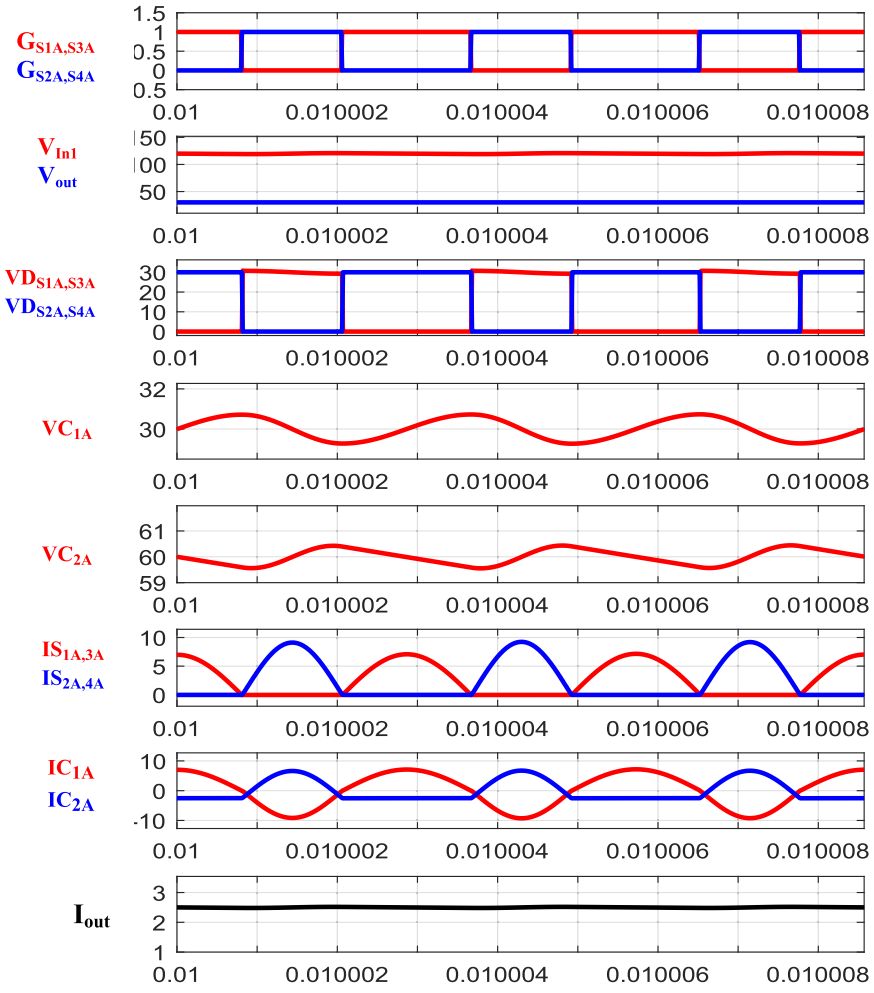


Fig. 6 Simulation Results of 300 W ZCS of Power Switch Waveforms.

4.2. Conduction losses in the main capacitors

The two main capacitors C_{1A} and C_{2A} can experience different current stress, as the current shown in Fig. 6, the current of capacitor C_{1A} is the currents sum of S_{1A} and S_{2A}. The current on the capacitor C_{1A} can be expressed using

$$I_{C1A} = \begin{cases} B\sin\left(\frac{\theta}{1.124}\right) 0 \le \theta \le 1.124\pi \\ A\sin\left(\frac{\theta}{0.876}\right) + I_{out} 1.124\pi \le \theta \le 2\pi \end{cases}$$

So, the RMS current on the capacitor C_{1A} can be calculated as in (34)

$$I_{C1A\_RMS} = 2.253 I_{out}$$

Then, the power losses in the capacitor C_{1A} can be estimated as

$$P_{con\_C1A} = 5.076 {I_{out}}^2 R_{ESR}$$

As for capacitor C_{2A}, the current flow is the sum of switch S_{2A} and load I_{out}. The current on the capacitor C_{1A} can be expressed as follow,

$$I_{C2A} = \begin{cases} -I_{out} 0 \le \theta \le 1.124\pi \\ A\sin\left(\frac{\theta}{0.876}\right) - I_{out} 1.124\pi \le \theta \le 2\pi \end{cases}$$

So, The RMS current of the capacitor C_{1A} can be obtain from the following

$$I_{C2A_{RMS}} = 1.363 I_{out}$$

Then, conduction power losses in the capacitor C_{2A} can be estimated as

$$P_{con\_C2A} = 1.858 {I_{out}}^2 R_{ESR}$$

4.3. Conduction losses in the input capacitor

For the first switching state, the value of input current I_{in1} is the total sum of of switches current I_{S1A} and I_{S2A} and its average value is 2 I_{out}. The ac components of the input current flows into the input capacitor and generates loss. The current on the input capacitor C_{in1} can be expressed using:

$$I_{Cin1} = \begin{cases} B\sin\left(\frac{\theta}{1.124}\right) - I_{out} 0 \le \theta \le 1.124\pi \\ A\sin\left(\frac{\theta}{0.876}\right) 1.124\pi \le \theta \le 2\pi \end{cases}$$

The RMS value of ac ripple in the input current is

$$I_{Cin1\_RMS} = 1.014 I_{out}$$

The power losses in the input capacitor C_{in1} can be obtained as

$$P_{con_{CinA}} = 1.028 I_{out}^2 R_{ESR}$$

Table 1 lists the converter design parameters. The parameters are used to estimate the converter's efficiency during normal conditions. GaN-FET (TP65H035WSQA) is used for all power devices and five 100-V 1-μF ceramic capacitors (C3225X7R2A105K200AE) are connected in parallel as the main circuit capacitors. R_{ds_on} represents the on-state resistance of the switch, and R_{ESR} is the equivalent series resistance of the main capacitors.

Table 2 illustrates the power losses comparison between the proposed voltage multiplier and the conventional voltage multiplier proposed in [27] with soft-switching operation. P_{loss_Switch} and $P_{loss\_Capacitor}$ represent the total conduction loss on switches and main capacitors. The proposed topology shows a fewer number of power switching devices and capacitors compared with traditional converter. Furthermore, the proposed voltage multiplier experiences a much smaller power conduction loss when compared to the traditional voltage multiplier.

Table 2 Comparison between the proposed voltage multiplier and the conventional Voltage multiplier.

Conduction Loss	Proposed Multiplier	Conventional Multiplier
P_{loss_Switch}	$20.29 I_R^2 R_{ds\_on}$	$29.46 I_R^2 R_{ds\_on}$
$P_{loss\_Capacitor}$	$13.86 I_R^2 R_{ESR}$	$19.6 I_R^2 R_{ESR}$
No of power devices	8	10
No of Capacitors	2	4

5. Simulation and experiment results

5.1. Simulation results

Simulation has been performed using MATLAB to validate the operating principle of the proposed high step up dc/dc converter with four times conversion ratio. Table 3 shows the simulation parameters. The simulated circuits have a common output voltage (120 V) with two-input voltage each with 30 V and output power 300 W. Since the circuit A and B are identical, therefore, the presented simulation waveforms will be only for circuit A.

Fig. 6 illustrate the gate control signals, currents and voltage waveforms of switches and capacitor for circuit A. Circuit B can have similar waveforms. $G_{S1A,S3A}$ are the gate drive signals of switches S_{1A} ans S_{3A} with duty cycle D = 0.562 and whereas $G_{S1A,S3A}$ is gate drive signals of switches S_{2A} ans S_{4A} with duty cycle D = 0.438. $VD_{S1A,S3A}$ and $VD_{S2A,S4A}$ are the drain source voltage of switches with dc voltage stress equal to the input voltage 30 V. The output load current I_{out} is equal to 2.5 A. $IS_{1A,S3A}$ are the switches drain-source current of switches S_{1A} and S_{3A} whereas $IS_{2A,4A}$ are the switches drain-source current of switches S_{2A} and S_{4A}. When the power switches S_{1A} and S_{3A} are turned on, the current through capacitors and switches starts from zero. And because the switching frequency is set equal to resonance frequency, the current will decrease to zero when switches are turned off. Therefore, the ZCS of switches S_{1A} and S_{3A} are realized in turn on and turn off. However, in the second switching state, when switches S_{2A} and S_{4A} are turned on, ZCS is also realized in both turn on and turn off. Fig. 7 also illustrates the current and voltage waveforms of capacitors C_{1A} and C_{2A}. IC_{1A} and IC_{2A} are the current through capacitor C_{1A} and C_{2A} respectively. The capacitors C_{1A} is charged in the first switching state with the sinusoidal current waveform and discharged in series with input voltages V_{in1} in the second switching state. VC_{1A} and VC_{2A} are the voltage across the capacitor C_{1A} and C_{2A}. V_{in1} is the input voltage for circuit A and set to be 30 V. V_{out} is the output load voltage. Switching frequency is 350 kHz. Capacitance C_{1A} and C_{2A} are 5 μF and stray inductance L_S is 52 nH. The simulation results verify the theoretical analysis presented in Section 3.

Table 3 Simulation parameters.

Description	Items	Values
Output Power	P_o	300 W
Input voltage	V_{in}	30 V
Output Voltage	V_{out}	120 V
Resonant capacitor	C_{1A}, C_{2A}, C_{1B}, C_{2B}	5 μF
Resonant Inductor	L_S	52 nH
Resistor Load	R_{Load}	48 Ω
Switching frequency	f_s	350 kHz

Table 1 Parameters used in converter design.

Items	Values
V_{in}	30 V
V_{gs}	12 V
Q_s	24 nC
C_{oss}	196 pF
R_{ds_on}	35 mΩ
R_{ESR}	15 mΩ
f_s	350 kHz

5.2. Experimental results

A 300-W, 4 times voltage gain ratio dc/dc converter prototype has been built to validate the theoretical analysis experimentally using two switched-capacitor testing boards. The prototype is shown in Fig. 7. The figure shows two general test boards each contains six switches and two capacitors. Only four switches are used in this experiment. The converter run at a high switching frequency (f_s = 350 KHz), hence, very small value of multilayer ceramic capacitors are used for C_{1A} and C_{2A} (as shown in Fig. 2). The resonant capacitor is five 100 V 1 μF from TDK connected in parallel. Therefore, C_{1A} and C_{2A} have an equivalent of about 5 F. thus, the utilization of a fast switching speed GaN device is very important to the proposed converter.

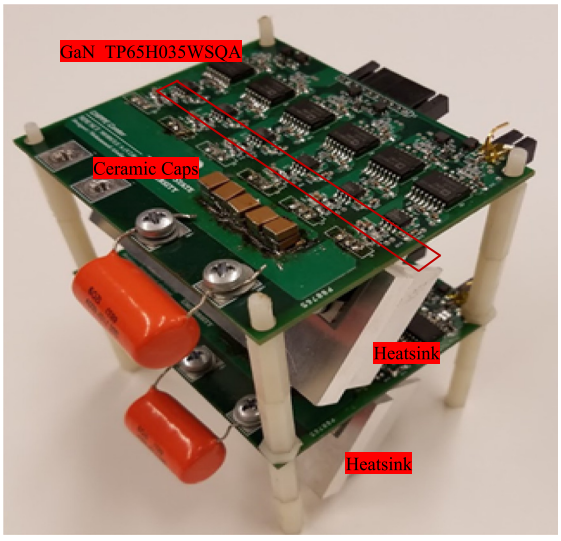


Fig. 7 Prototype of the proposed dc/dc converter.

The experimental results for the 300 W test are shown in Fig. 8 and Fig. 9. Fig. 8 shows the input voltage, output voltage and current through switch S_{1A} in circuit A and S_{1B} in circuit B and a load current. It can be seen from the figure that the input voltage is set at 30 V and output voltage is 120 V which is four times the input voltage. Also the figure shows that switch S_{1A} in circuit A as well as switch S_{1B} in circuit B turn on and turn off at zero, thereby realizing ZCS. It can be noticed that the charging currents of two two switches are not exactly equal in their peak values since the test setup are built from two different circuit boards, also, the wires between the two circuit boards are not identical in length, which results in different values for the inductances. Furthermore, these wires can add more resistance which cause the system to be less efficient, so the results can be improved if the converter is integrated onto one single PCB layout. Fig. 9 shows the zoomed in drain– source voltage waveforms of switch S_{1A}, the input voltage of circuit A V_{in1} , the input voltage of circuit B V_{in2} and the output voltage V_{out}. It shows that the voltage stress over the device S_{1A} is the same as the input voltage 30 V and all the power switching devices in the converter can experience the same voltage stress.

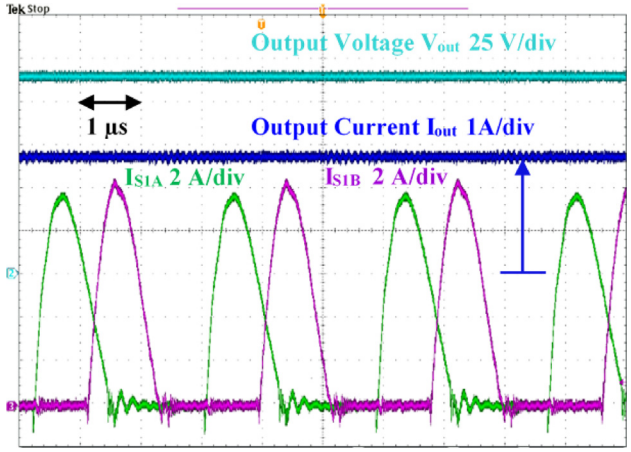


Fig. 8 Experimental result of switches current s_{1a} and s_{1b} output current and output voltage.

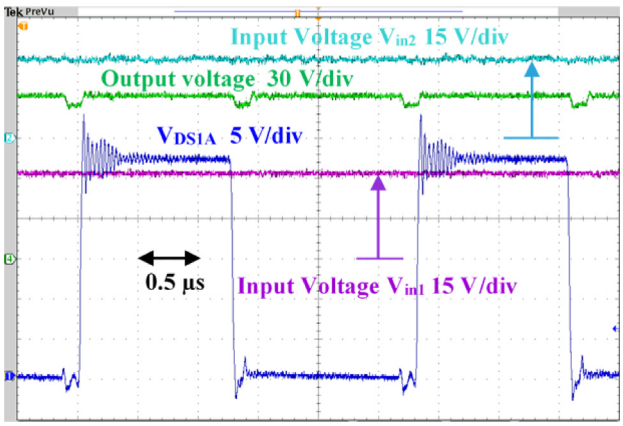


Fig. 9 Experimental result of zoomed in drain source-voltage waveforms of switch $s_{1a,}$ input voltage and output voltage.

Fig. 10 shows the experimental results of the output voltage of the proposed converter. the output capacitor voltage of circuit A $V_{C\ 2A}$. The waveform in the top is the total output voltage with a voltage ripple less than 1 V.

And the two waveforms in the bottom illustrate the output capacitor voltage of the top stage ($V_{C\ 2A}$) and bottom stage ($V_{C\ 2B}$) as shown in Fig. 2, respectively , and they have a maximum voltage ripple of 4.5 V.

Fig. 11 shows the measured efficiency curve from 30 W to 300 W with 30-V fixed input voltage for each circuit board. The test shows maximum efficiency was obtained for an output of 120 W at 98.3%. The overall measured efficiency is above 97% for the whole test range. The difference between measured and calculated efficiency curves because the two testing boards are connected with two different cables, adding more resistance to the circuit. Furthermore, the stray inductance loops are not optimized and cause oscillation with soft switching operation, and this add more switching loses (not considered in calculated curve) and hence lead lower measure efficiency curve. And this is more obvious in Fig. 9 when the current in the switches are having different peak current values. An integrated design circuit can help to increase the total efficiency of the proposed converter.

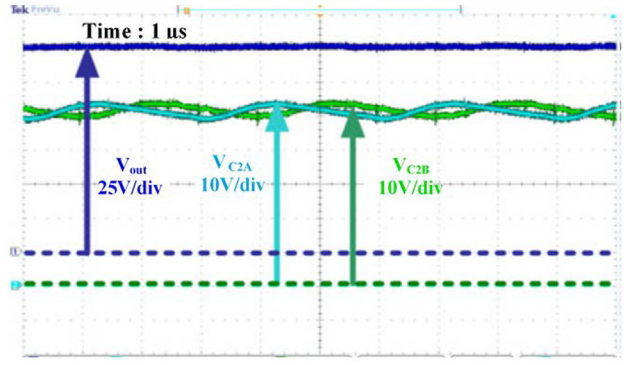


Fig. 10 Experimental result of output of capacitor $v_{c2a,}v_{c2b}$ and output voltage v_{out}.

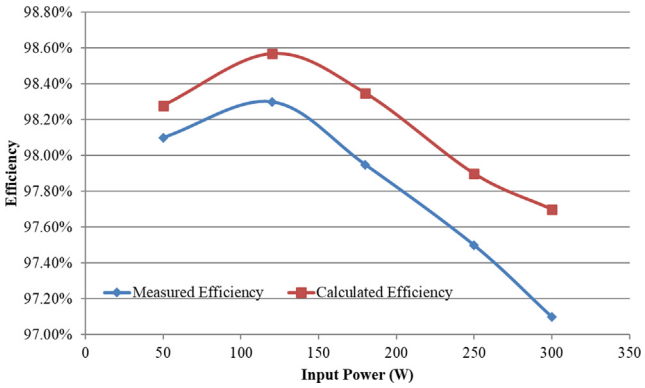


Fig.11 Measured and calculated efficiency Efficiency curve of the proposed dc/dc converter curve.

6. Conclusion

A high step up dc/dc converter based switched capacitor circuit is proposed in this paper to achieve higher efficiency and smaller size circuit structure with ZCS operation. A multi input dc-dc converter is introduced instead of conventional dc/dc converter for PV applications. The proposed converter can help to increase the extracted PV power when partial shading or mismatch is considered. Utilization of fast switching speed of WBG devices enable the converter to use small size multilayer ceramic capacitor instead of large electrolytic capacitors to achieve high power density. Although the dc/dc converter operates at higher switching frequency (fs = 350 k Hz), ZCS can be achieved for all the switching devices, which eliminates the switching loss. In order to design the dc/dc converter for ZCS operation, layout stray inductance is used, hence, the system design targets, high efficiency and small size are achieved. A 300-W prototype with ZCS operation has been built and tested, a peak efficiency of 98.3% have been obtained.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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