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A Reconfigurable Passive RF-to-DC Converter for Wireless IoT Applications

Ulkuhan Guler *Member, IEEE,* Yaoyao Jia, Student *Member*, IEEE, and Maysam Ghovanloo, *Fellow, IEEE*

***Abstract*—In this paper, we present a reconfigurable rectifier, which makes it feasible to harvest energy with net-zero energy consumption, i.e. without draining power from battery, in a wide input power range. The proposed topology can operate with low input power signals and can be fine-tuned for a specific operating frequency in a wide frequency range from several MHz to GHz in remotely-powered systems. A prototype is fabricated in 0.35-µm standard CMOS process and occupies 0.019 mm^2. Although the proposed rectifier supports four different rectifier topologies, on silicon it only occupies the footprint of a single rectifier. At 13.56 MHz with 2.2 mW input power, the four-switch rectifier topology yields 82% power conversion efficiency (PCE), while the hybrid topology (diodes + switches) provides 81% PCE at 11.2 mW input power. The rectifier operates with input power as low as 1.1 mW, at which level the PCE is still reasonable at 65.2%. This allows a wireless device at low power level to operate at extended read range. This reconfigurable rectifier is especially suitable for Internet of Things (IoT) mobile application, where the power of the incoming signal changes by the distance between the power source and the device.**

***Index Terms*— RF-to-DC converter, CMOS rectifier, wireless power transfer, energy harvesting, Internet-of-Things, IoT.**

I. Introduction

EXPONENTIAL growth in the demand for next-generation sensors and actuators in Internet-of-Things (IoT) applications increases the need for highly efficient energy harvesting systems [1]. The problems associated with wired and battery-powered solutions in IoT applications make wireless solutions more attractive [2]. Accessibility to device locations in various environments strictly limits the use of wires, which also suffer from cost and bulky connectors. Moreover, the size of a battery is a bottleneck to further decrease the footprint of a sensor [3]. The need for replacement of batteries is yet another problem that can be counted as downside of battery solutions. It has been speculated that ultra-low power systems, which do not require battery charging more frequently than once a week can potentially, be recharged or directly powered wirelessly from RF sources [4].

In wireless IoT applications, challenges include reducing the cost of sensors, maintaining sustainable energy harvesting, wireless power transmission (WPT), compact energy storage, and efficient power conversion methods [5]. Along with the sustainability of harvested energy, the efficient conversion of harvested power plays a critical role in the long-term and continuous monitoring of the environment. Especially, this has become more important for personal health monitoring with wearables and implantable medical devices (IMD), in which the inconvenience of a battery solution is clear [6], [7].

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Y. Jia and M. Ghovanloo are with GT-Bionics Lab, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30308, USA. Ulkuhan Guler was also with GT-Bionics Lab. She is now with Department of Electrical and Computer Engineering, Worcester Polytechnic Institute, Worcester, MA 01609, USA. (e-mail: uguler@wpi.edu)

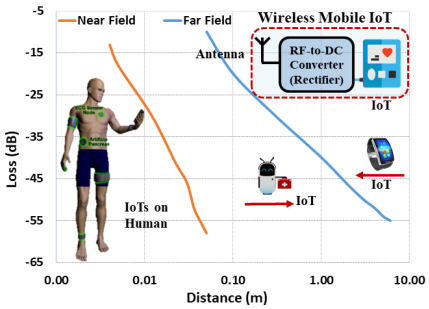

Fig. 1. The power loss of a far field [10] and a near field [11] signals versus distance from the source.

Efficiency of an RF-to-DC converter for a wide range of input power heavily depends on the distance between the harvester and the source [8], [9]. This dependency is presented in Fig. 1, which demonstrates the near- and far-field power loss which vary with distance from an RF source [10], [11]. In mobile applications, this is a real problem, because of the large variability in available power at the input of the energy harvesters. Conventional RF-to-DC converters that can only achieve high power conversion efficiency at a particular power range are not preferred in this kind of applications [12], [13]. Although a few examples are available in the literature [14], [19], RF-to-DC converters, capable of reconfiguring themselves according to power and/or amplitude of the incoming RF signal to maintain high PCE from available power, while not increasing the chip area, is a need for IoT.

In this paper, we have proposed a reconfigurable passive RF-to-DC converter, designed for 13.56 MHz operating frequency and several mW power delivery. However, with proper choice of fabrication process, the proposed architecture can be optimized for a specific operating frequency ranging from MHz to GHz and for a specific power delivery ranging from µW to mW levels. Section II presents the operating principle behind the reconfigurable rectifier and the details of its implementation. In order to conduct an accurate AC power measurement and give insight about the measurement method, Section III describes some of the AC power measurement methods utilized for PCE calculations. Section IV discusses the measurement results and performance parameters, followed by concluding remarks.

II. Operation Principles and Implementation

As reported in [6], changes at the input power strongly affect the PCE of conventional rectifiers, which are tuned to operate at a specific power level. A rectifier that works with high PCE

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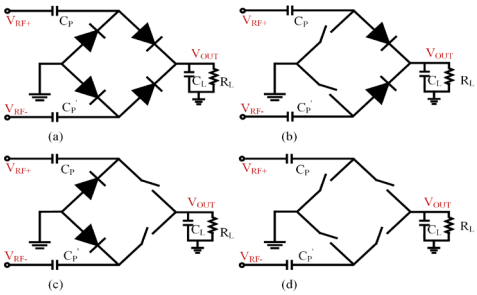

Fig. 2. (a) The four-diode topology (ALL-D), (b) the two-switch (NMOS) and two-diode (PMOS) hybrid topology (NS-PD), (c) the two-diode (NMOS) and two-switch (PMOS) hybrid topology (ND-PS), and (d) the four-switch topology (ALL-S), which are used in the reconfigurable rectifier.

at a higher power level may not operate efficiently at a lower power level, or vice versa. To overcome this problem, researchers have proposed employing two rectifiers, which are optimized separately to maintain efficient operation at a wide power range [15]. However, the occupied large area on the chip with large power transistors and pump capacitors makes this an expensive solution. Another method of cost reduction is using standard CMOS process for manufacturing to eliminate the cost of additional devices and processing steps. Here, we focused on a solution that is standard CMOS-compatible and compact rectifier which operates effectively in a wide input power range.

Bridge and cross-coupled rectifiers are two of the widely used rectifier topologies [12]-[16]. In this reconfigurable rectifier, we employ four well-known types of rectifier topologies illustrated in Fig. 2. As diodes and switches can also be implemented with standard CMOS transistors by configuring the gate connection of each transistor, all these topologies are compatible with standard CMOS. When these rectifiers are implemented with transistors, they utilize the same number of four power transistors. We realized that by only changing the gate biasing of power transistors, a transition among these types of rectifiers is possible, thus altering the transistors from diode to switch and vice versa.

To obtain higher PCE, power losses in the rectifier should be kept low as much as possible. The main two mechanisms which cause power losses are forward dropout voltage and reverse leakage current. The contribution of these two mechanisms on signal paths determines the efficiency of a rectifier. Since forward dropout voltage and reverse leakage current have different behaviors and values in diodes and switches, the number of switches and/or diodes on one path affect the PCE. While the four-diode (ALL-D) topology has two diodes, the four-switch (ALL-S) topology has two switches on one signal path. Similarly, two-diodes two-switches (hybrid) topologies (ND-PS and NS-PD) have one diode and one switch on the main current path.

The ALL-D topology has two high dropout voltages in each signal path, which is directly related to the threshold voltage, V_{th}, of diode-connected transistors. On the other side, as explained in [6], a common-mode gate voltage accumulates on internal nodes of the ALL-S topology, which reduces the required effective V_{th}. Therefore, this rectifier operates efficiently with lower input voltages than what is required for the other rectifiers. We can conclude that the ALL-S topology operates more efficiently below the threshold voltage level. On the other hand, as the input voltage increases above the threshold voltage, reverse leakage current starts to increase

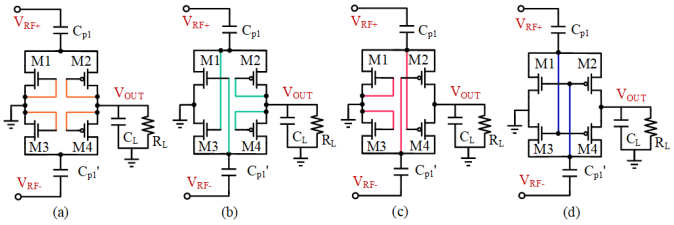

Fig. 3. Transistor-level implementation of rectifiers given in Fig. 2. (a) ALL-D, (b) NS-PD, (c) ND-PS, and (d) (ALL-S).

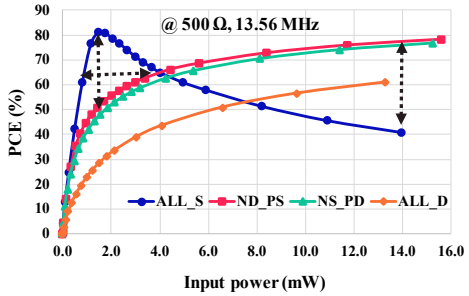

Fig. 4. Simulated PCE of four types of rectifiers vs. input power.

rapidly in this topology unlike the ALL-D topology.

In fact, the hybrid topologies combine the advantages of the ALL-S and the ALL-D topologies within a certain input voltage range. They have less dropout voltage than the ALL-D topology and less reverse leakage current than the ALL-S topology. The dropout voltage is less than two V_{th}, but only slightly more than one V_{th} in hybrid topologies. When there are one diode and one switch on a signal path in series, the reverse leakage current of the diode, which is smaller than that of the switch, determines the value of reverse leakage current in that path.

Fig. 3 illustrates the transistor-level implementation of the topologies, given in Fig. 2. The main difference between different topologies is in their gate connections, using which we can reconfigure the rectifier. For the sake of simplicity, all power transistors have been designed with the same aspect ratios chosen as $(\frac{W}{L} = \frac{1.5\ mm}{0.35\ \mu m})$ for NMOS and PMOS transistors, pump capacitors are 1 nF, and the load capacitance is 100 nF. It is possible to further improve the PCE by optimizing each of these parameters [17]. We have performed our analysis for each topology at 13.56 MHz under a 500 Ω loading condition. Simulations are conducted in SPECTRE from Cadence Design Systems (San Jose, CA). We have swept the input power by changing voltage of the input signal, and calculated the PCE of each rectifier topology.

As expected, Fig. 4 shows that ALL-S rectifier achieves the highest PCE up to 4 mW at low input power levels, where it has a peak PCE of 82% at 1.5 mW. Around 4.2 mW input power, the hybrid rectifiers start to have greater PCE than the ALL-S rectifier. The purpose of proposed reconfigurable rectifier topology is to obtain high PCE in a wide input power range, regardless of the power level of the incoming signal. The analysis proved that with the input power below 2 mW, with a configurable rectifier, PCE improves 30% in comparison with a fixed hybrid one. Indeed, this idea increases the availability of power with a PCE higher than 65% from 0.9 mW to 4 mW, which leads to operability of an IoT device at much lower power levels. Similarly, with the input power more than 12 mW, yet again 30% more PCE is obtained with a configurable rectifier than a fixed one with ALL-S and ALL-D topologies.

Arrows in Fig.4 show above mentioned enhanced regions. At the start-up, the power level might not be high enough to operate efficiently with the ALL-D or hybrid rectifiers. Hence, the proposed rectifier starts up with the ALL-S configuration.

III.AC Power Measurement Methods for Rectifiers

The performance metrics, used to evaluate a rectifier, includes PCE, voltage conversion efficiency (VCE), sensitivity, and output voltage. Indeed, the preeminent metric among all is PCE, which is expressed as,

$$PCE = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT}+P_{loss}}, \quad (1)$$

where P_{OUT} is the average DC output power, estimated as $P_{OUT} = \frac{V_{OUT}^2}{R_L}$, where V_{OUT} is output DC voltage of the rectifier and R_L is the rectifier loading, and P_{IN} is the average input power, estimated as $P_{IN} = \frac{1}{T}\int V_{IN} I_{IN}$, where V_{IN} is the input AC voltage of the rectifier, and I_{IN} is the input AC current of the rectifier. In fact, the difficulty of determining the PCE of a rectifier arises from the measurement of AC power. In this section, to guide to an accurate measurement, we discuss some of the AC power measurement methods.

A. Current Probe

By attaching its clamp to a cable/wire, the current flowing from a cable/wire can be measured with current probes. AC current at the input of the rectifier is measured by a current probe and displayed on an oscilloscope screen. Along with AC current, AC voltages are also measured by an oscilloscope. Later on with post processing tools, such as MATLAB, input AC power is calculated by integrating and averaging of multiplied AC voltage and AC current. Even though using current probes seems to be a simple method, the calculation of AC power still needs to be precise. The type of the current probe should be capable of measuring the minimum value of current flowing into the rectifier with sufficient accuracy. Moreover, the calibration of a current probe is vital for accurate measurements. Finally, the cost of wideband current probes compared to regular voltage probes limits the availability of these devices to average designer.

B. Current Sensing Resistor

Measuring PCE of a rectifier by a current sensing precision resistor, deployed at the input of the rectifier, is a widely used method especially at relatively low frequencies [12]. The value of the resistor should be small, 1 Ω – 10 Ω, depending on the sensitivity of the instruments, mainly the oscilloscope. AC input current is measured by differentiating the voltage across the current sensing resistor and dividing the difference voltage to the precision resistor value. Although increasing the resistor value helps to increase sensitivity, it adds an undesired voltage drop and RC delay at the input of the rectifier, which should be accounted for. Lowering the input voltage lowers the PCE compared to its actual value.

To increase the sensitivity of the measured current, another method uses an external differential amplifier, which amplifies the voltage difference across the precision resistor. By employing this method, a small resistor would be sufficient to achieve the desired sensitivity in the current measurement. Moreover, if the amplifier output is properly buffered, it will reduce the effect of oscilloscope parasitic capacitance. However, the design of the external amplifying stage associated with the IC should be considered.

C. Vector Network Analyzer (VNA)

Another commonly used method is measuring S-parameters with a network analyzer to determine the actual power delivered to the rectifier. By applying a single tone, the frequency at which the rectifier operation is being measured, the reflected power can be calculated. In [16], by using measured mixed-mode S-parameters, P_{IN} is calculated as,

$$P_{IN} = P_S(1 - |S_{dd11}|^2 - |S_{cd11}|^2), \quad (2)$$

where S_{cd11} is differential-to-common and S_{dd11} is differential-to-differential mode reflection coefficients, both are derived from the main S parameters, and P_S is the source power supplied from the network analyzer. A simplified but accurate version of the input power calculation is given as,

$$P_{IN} = P_S(1 - |S_{11}|^2), \quad (3)$$

where S_{11} presents reflection losses at the input of the rectifier.

Limitations associated with this method are due to limitations of the vector network analyzer (VNA), such as frequency and power levels that the device can support. For example, most VNAs supply 15 dBm maximum power, which corresponds to 31.6 mW, at low frequency (kHz – MHz) range. Therefore, the rectifier can be tested with a maximum P_{IN} = 31.6 mW. Since, this method does not require any additional device and/or instrumentation, which may affect the measurements, it is one of the most reliable methods for AC power measurement.

D. Power Analyzer

In general, power meters and power sensors are used for radar and wireless communication applications. We found that they are also useful tools for PCE measurements. A power sensor is connected between the AC signal source and the rectifier. The power sensor is a splitter type device, which reflects precisely the same value of power drawn by the rectifier. Similar to the VNA method, the power level and the operation frequency are limited by the device capability. Power levels higher than the power meter's rating may damage the power meter. The measurable frequency is also limited by the frequency range of the power meters. Although this method also gives accurate results, these devices are not as widely available as the devices used in the abovementioned methods.

IV.Measurement Results and Discussion

The reconfigurable rectifier in Fig. 3 was fabricated in the TSMC 0.35-µm standard CMOS process. The measurement setup with the chip micrograph is presented in Fig. 5a, and a simplified block diagram of this setup is depicted in Fig. 5b. Among methods in section III, we conducted measurements with a VNA (Rohde & Schwartz, ZVB 4). P_{IN} is calculated using (3). An oscilloscope (Tektronix, DPO 4034) is used to measure the rectifier AC input voltage. A multimeter is used to measure the DC voltage at the rectifier output. Measurements were conducted under a 500 Ω load at 13.56 MHz. Measurements of all four rectifier topologies were conducted under the same conditions. Switching between different topologies took place by controlling the gate biasing of power transistors manually by a custom design PCB and proper wire

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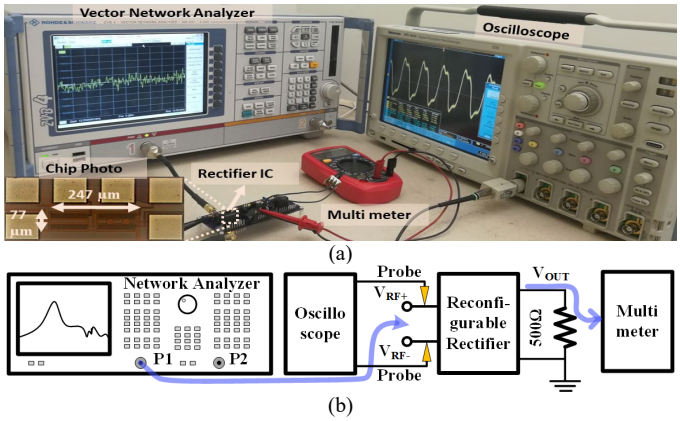

Fig. 5. (a) Measurement setup with the reconfigurable rectifier chip photo, (b) the block diagram of the measurement setup.

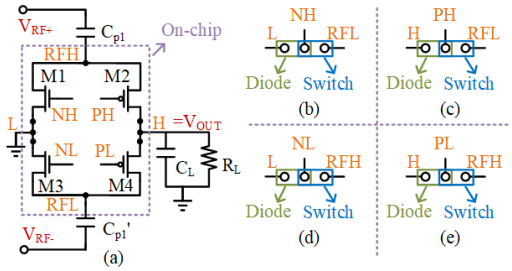

Fig. 6. Reconfiguration mechanism on the PCB. (a) On-chip part of the rectifier, on-PCB jumper sets for (b) M1, (c) M2, (d) M3, and (e) M4 power transistors.

bondings, which allows the reconfiguration operation as demonstrated in Fig.6. We measured the PCE, output voltage, and output power of the rectifiers with input power in the range of 0 dBm to 14 dBm, which corresponds to 1 mW to 25.11 mW. 14 dBm is the maximum level that VNA ZVB 4 can properly supply.

Fig. 6 presents the PCE performance of four configurations with varying input power. The ALL-S rectifier exhibits the highest PCE until 4.4 mW input power. The PCE of the ALL-S rectifier at 2.2 mW is ~82%. However, it deteriorates immediately from both sides. Actually, we observed a deviation in power at the peak PCE compared to simulations. This high PCE is achieved because of the low on-resistance of switches on the current path, which in turn reduces the dissipated power on the switches. For example, if M2 transistor in Fig. 2d is considered, when V_{RF+} is positive, the gate of M2 is connected to V_{RF-} which is at a negative voltage. The higher over drive voltage (V_{GS} -V_{th}), the lower R_{on}, where V_{GS} is the gate source voltage and R_{on} is the on-resistance of the transistor. On the other hand, M1 transistor in Fig. 2d is on the reverse bias path and gate biasing at negative voltage reduces the reverse current leakage, as well. Around 4.5 mW of input power, the ALL-S rectifier with decreasing PCE and the hybrid rectifiers with increasing PCE have met around 70% PCE. We also noticed that the PCE of the ALL-S rectifier does not drop as sharply as in simulations. With increasing input power, the amplitude of V_{RF+} increases, which also raises drain source voltage (V_{DS}) of M1. As higher V_{DS} causes a stronger electric field between the drain and the source, even when V_{GS} of M1 is at a considerable low value, a significant reverse current starts to flow from M1.

Beyond 4.5 mW of input power, the PCE of hybrid rectifiers keep increasing, which confirms that the reverse current is substantially reduced with these topologies. When $V_{DS} > V_{GS} - V_{th}$, reverse current becomes proportional to $(V_{GS} - V_{th})^2$. As

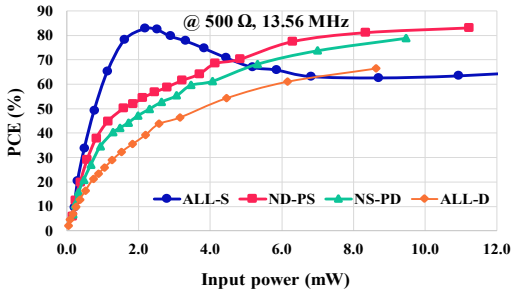

Fig. 6. Measured PCE of four types of rectifiers vs. input power.

in the case of Fig. 2c and d, M1 transistor has less reverse current when it is diode connected due to less $(V_{GS} - V_{th})^2$, in which $V_{GS} = 0, and\ V_{DS} > 0$. The hybrid rectifier ND-PS has slightly better PCE than that of NS-PD, because of the less V_{th} of NMOS, which reduces the forward loss. On the other hand, employing a PMOS transistor degrades the performance of a switch at low power range. Even though, not obvious from the graph, the hybrid rectifier NS-PD has slightly better PCE than that of ND-PS at low-power range up to 0.35 mW input power. The ALL-D rectifier has a similar behavior as hybrid rectifiers. However, it exhibits the worst PCE performance among all four topologies. We also examined that simulations and measurements are in a good agreement, as can be seen from Figs. 4 and 6.

Fig. 7a presents the PCE of all four rectifier topologies by varying the loading. For the ALL-S configuration, from VNA we have applied 7 dBm (-5 mW), where the ALL-S topology has its highest PCE according to Fig. 6. While, for the other topologies, from VNA we have applied 13 dBm (-20 mW), where they are close to their highest PCE. All topologies retain their high PCEs in a range of output loads from 300 Ω to 1200 Ω. However, the PCE of the ALL-S decreases by 13%, when the load changes from 500 Ω to 1200 Ω, as the percentage of reverse current increases. It is also important to note that, when the load decreases below 300 Ω, the decreasing slope of PCE is faster for the ALL-S topology than that of in the other rectifiers.

The PCE change vs. operating frequency starting from 150 kHz to 40 MHz is shown in Fig. 7b. All topologies reach their highest PCE around 3 MHz, except the ALL-S topology which has its highest PCE at 9 MHz. The ALL-D topology and hybrid topologies have greater PCE between 3 MHz – 5 MHz than that of between 6 MHz - 13.56 MHz. Above 15 MHz, the PCE of all rectifiers decrease, except at 30 MHz, where a small peak occurs, which might be because of resonance with parasitics.

The output DC voltages (V_{out}) of rectifiers vs. input AC power are depicted in Fig. 7c. The ALL-S topology achieves the highest output DC voltage until the input power range of 4.15 mW, which is followed by the hybrid ND-PS rectifier. After that point, the hybrid ND-PS rectifier exhibits the highest output DC voltage, which is closely followed by the other hybrid rectifier. When the input power is more than 8 mW, V_{out} of the ALL-S rectifier drops behind the other three types.

Fig. 8a presents the transient view of the measured output DC voltage of rectifiers with 1 Vpeak input voltage at 500 Ω load and 13.56 MHz. These waveforms are presented to demonstrate the behavior of rectifiers with low input power. According to the figure, at low input power, the ALL-S rectifier achieves the highest output DC voltage. It is followed by hybrid rectifiers ND-PS and NS-PD, and the ALL-D topology, respectively. The

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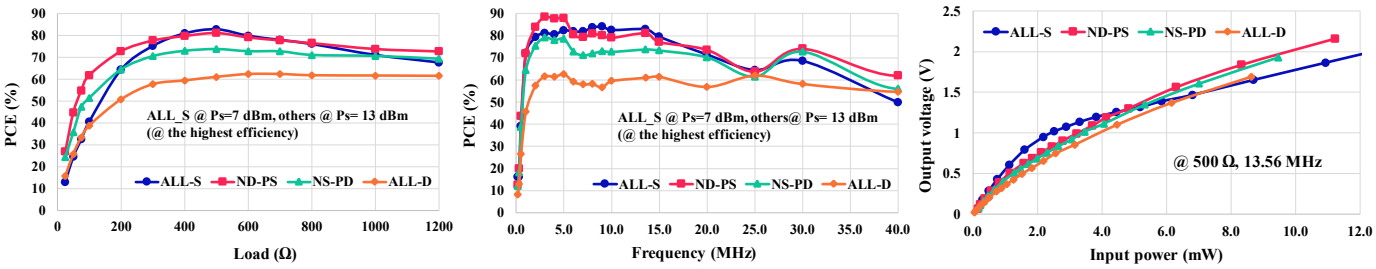
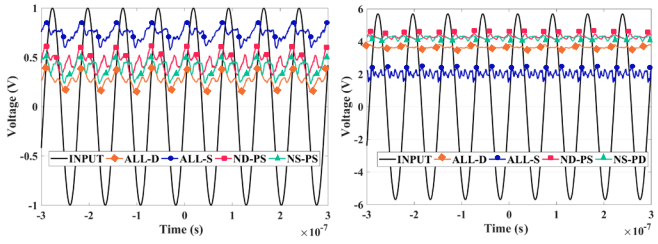


(a) (b) (c)

Fig. 7. (a) Measured PCE of four type rectifiers with varying output load. (b) Measured PCE of four type rectifiers with varying operating frequency. (c) Measured output voltage of four type rectifiers with varying input power.



(a) (b)

Fig. 8. The transient view of the measured output voltage of rectifiers with (a) 1 Vpeak at 500 Ω load and (b) 5.7 Vpeak input voltage at 5 kΩ load.

TABLE I. COMPARISON OF PERFORMANCE PARAMETERS

Parameters	[12]	[13]	[18]	[19]	This work
Peak Efficiency (%)	80.2	~50	92.6	65	82
Frequency (MHz)	13.56	900	13.56	1000	13.56
Load (Ω)	500	125 k	127	100k	500
Structure	Active hybrid	Two stg. ALL-S	Active hybrid	Recon-figurable	Reconfi-gurable
Area (mm^2)	0.18	NA	NA	0.00845	0.019
Technology (nm)	500	180	350	180	350

results are in a good agreement with Fig. 7c. We chose a 5.7 V_{peak} input voltage scenario to demonstrate the high input power behavior of rectifiers. In Fig. 8b, to clearly address the behavior of topologies, we increase the output load from 500 Ω to 5 kΩ. By this, we aimed to reveal the differences of output DC voltages of each rectifier at the same input power by reducing the ripples at the output. According to Fig. 8b, the highest output DC voltage is attained by the ND-PS topology, which is followed by the NS-PD, the ALL-D, and ALL-S topologies. Table I compares the proposed rectifier with those in literature. This rectifier drives 200 times heavier load than the one in [19], but only occupies 2.25 times larger area without capacitors and control circuit, which are simple logic gates. While this rectifier and the one in [12] operate at the same frequency, under the same loading, this has 9.47 times smaller area with higher PCE.

V. CONCLUSION

This paper points out that the only difference among four rectifier topologies is their gate biasing. We propose to combine these topologies into one reconfigurable rectifier. The measurement results prove the analysis results. According to the measurement results the ALL-S rectifier generates the highest output DC voltage with the highest PCE of 82% at the lower power levels in the given range. When the input power increases, where the ALL-S topology deteriorates, hybrid type rectifiers start to perform better than the ALL-S topology and ND-PS type topology obtains the PCE of 81%. We have proved that considerable amount of energy can be saved with the proposed reconfigurable rectifier topology by selecting the best topology according to the received input power.

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