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Efficient CNTFET-based design of quaternary logic gates and arithmetic circuits

Seyyed Ashkan Ebrahimi [a], Mohammad Reza Reshadinezhad [a,*], Ali Bohlooli [a], Mahyar Shahsavari [b]

[a] Faculty of Computer Engineering, University of Isfahan, Isfahan, Iran
[b] University of Lille, LIFL, CNRS, UMR 8022, F-59650 Villeneuve d'Ascq, France

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ABSTRACT

A new voltage mode design is presented for quaternary logic using CNTFETs. This architecture with presentation of a new structure for voltage division can be applied on any four-valued logic implementation. To ensure the functionality of this promising proposed architecture, basic gates, half-adder, and full-adder are implemented using voltage divider. Moreover, a decoder is considered to enhance the parameters of half-adder such as power consumption, delay, and number of transistors. The designs are simulated using Hspice simulation tool. In comparison with prior works, our half-adder design is optimized by 75.2%, 7.8% and 77% in power consumption, delay and PDP parameters, respectively.

1. Introduction

Multiple-valued logic (MVL) is studied extensively as an appropriate alternative to binary systems [1,2]. The MVL is able to solve and optimize the complexity in interconnection problems introduced by binary systems in VLSI circuits [3,4]. In MVL platform, fewer digits are required to save, display or compute data. Other advantages of applying MVL are higher speed computation, more dense data storage memory, applying more optimized connection routes, higher capability of transferring and receiving data, and simplification in testing and evaluating [5–9]. However, MVL systems apply signals with more levels compared to that of a binary system. This phenomenon is more vulnerable to manufacture variation and system signal noise, that is, the noise margin shrinking. If these issues are not dealt with in a proper manner they prevent the application of MVL circuits.

Shrinking scalability of MOSFETs is the main factor encouraging the scientists to design their fabrications using CMOS technology. Now, the question is to what extent would this shrinking process continue? The miniaturizing of transistor faces serious challenges and restrictions such as the quantum effects, high lithography costs, ICs heating, increased leakage currents, on-current increase difficulty, large parameter variations, low reliability and yield as well as an increase in manufacturing cost [10]. To overcome these challenges and restrictions and develop a sustainable future in replacing of CMOS technology, introduction of new alternatives is inevitable. The implementation of the first nano-computer in Stanford University can be regarded as a breakthrough in replacing of CMOS through CNTFET [11]. At present many researchers are dealing with the following challenges with respect to the applicability of CNTFET: CNT density, diameter and doping variations, miss-position and misplacement of CNT and presence of metallic CNT [12,13].

Voltage-mode MVL circuits can be obtained through multi-threshold transistors [2]. Raychowdhury and Roy [14] designed a complex set of circuit arithmetic for MVL operators by using CNTFETs and resistors. They developed multi-threshold CNT transistors, which could control the threshold voltages through controlling the nano-tube diameter. In another study [15], authors have eliminated the bulky resistors by applying active load *p*-type CNTFETs and developed their next work by designing logic gates, decoder, half-adder and multiplier through the three-valued logic [2]. Two different three-valued adders, are introduced by applying the complex circuit design in [16], where the researchers applied different diameters for the CNT transistors, and capacitors. In [17], the capacitors are omitted, leading to considerable optimization in power consumption and PDP. A dynamic structure for implementing a dynamic ternary logic based on the complete model technique is proposed in [18], where clock signal is applied to evaluate and pre-charge. The reliability of three- and four-valued logic gates is investigated in [19]; where, the voltage-mode multi-

* Corresponding author.
E-mail addresses: ebrahimi@eng.ui.ac.ir (S.A. Ebrahimi), m.reshadinezhad@eng.ui.ac.ir (M.R. Reshadinezhad), bohlooli@eng.ui.ac.ir (A. Bohlooli), mahyar.shahsavari@lifl.fr (M. Shahsavari).

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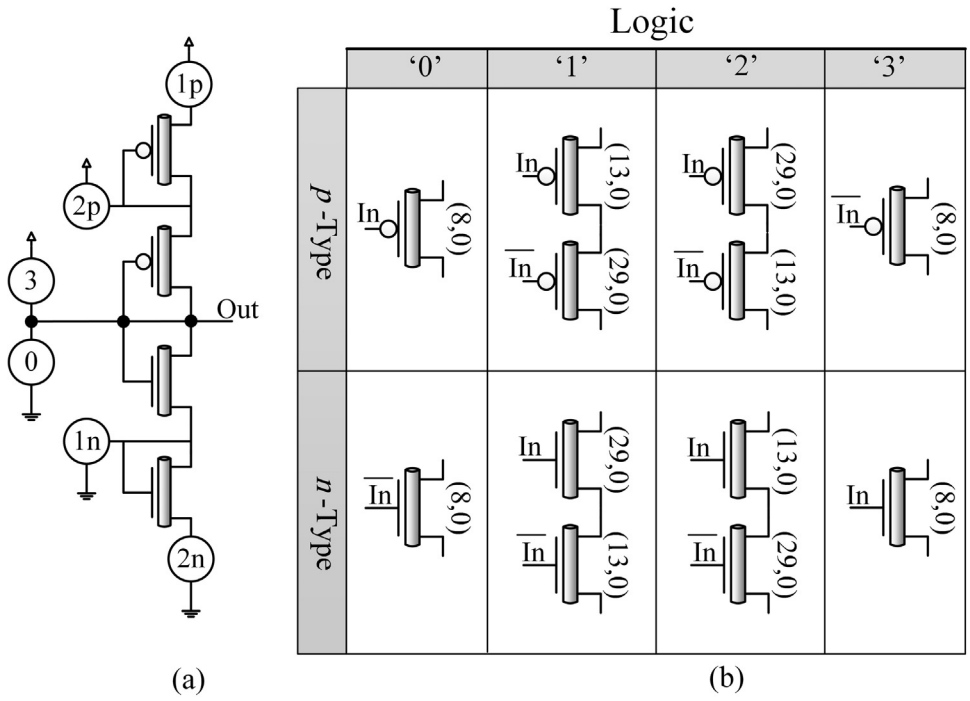

Fig. 1. (a) Proposed voltage division circuit, and (b) route controlling CNTFETs.

Table 1
Corresponding voltages for logic values.

Scale	Logic	Voltage (V)
Vdd	'3'	0.9
2Vdd/3	'2'	0.6
Vdd/3	'1'	0.3
GND	'0'	0

valued circuit design is obtained through pseudo complementary implementation. The complete set of quaternary logic gates, decoders and multiplexers are designed and described in [20]. In their work, the authors applied separate power supplies for each logic value. The universal designs of ternary-valued logic (TVL) with high-speed, low-power and full swing output using CNTFETs are presented in [21]. All TVL functions can be implemented by the method presented in [21], where, a power supply for each logic value is required. These studies are theoretical investigations under ideal conditions.

Table 2
Truth table of *B2Q*.

In1	0	0	1	1
In2	0	1	0	1
Out	0	1	2	3

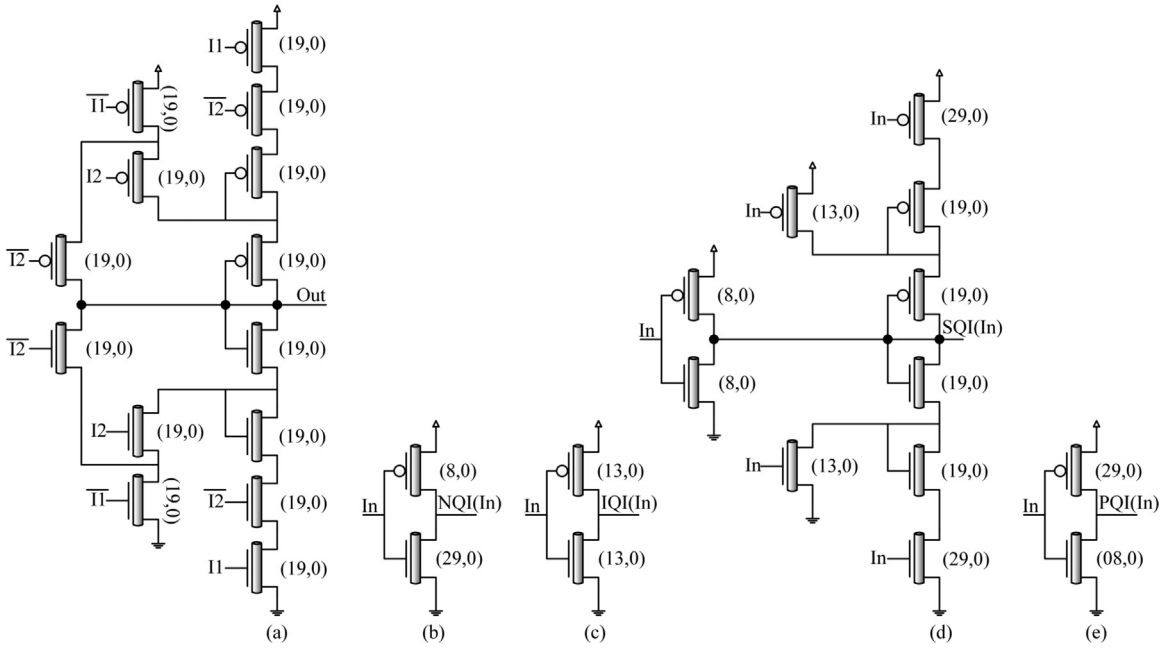

Fig. 2. Proposed implementation of (a) *B2Q*, (b) *NQI*, (c) *IQI*, (d) *SQI* and (e) *PQI*.

Table 3
The truth table of quaternary inverters.

IN	Out			
	NQI	*IQI*	*PQI*	*SQI*
0	3	3	3	3
1	0	3	3	2
2	0	0	3	1
3	0	0	0	0

Table 4
Truth table of two inputs *QNAND* and *QNOR*.

QNAND					*QNOR*				
B					*B*				
A	0	1	2	3	*A*	0	1	2	3
0	3	3	3	3	0	3	2	1	0
1	3	2	2	2	1	2	2	1	0
2	3	2	1	1	2	1	1	1	0
3	3	2	1	0	3	0	0	0	0

The main contribution of this study is to introduce a new architecture for implementing 4-valued circuits, using CNTFET technology. In this architecture, each one of the 4-value functions can be directly implemented through the truth table. This architecture would lead to simplification in the design process, since its implementation resembles the designing of the binary circuits. Moreover, the architecture is introduced according to the trade-off between delay and power consumption in comparison with the previous works. Here only one power supply would be suffice. An intriguing point here is that for implementation of MVL circuits there exists the possibility of its expansion, e.g. to 5 valued logic circuits.

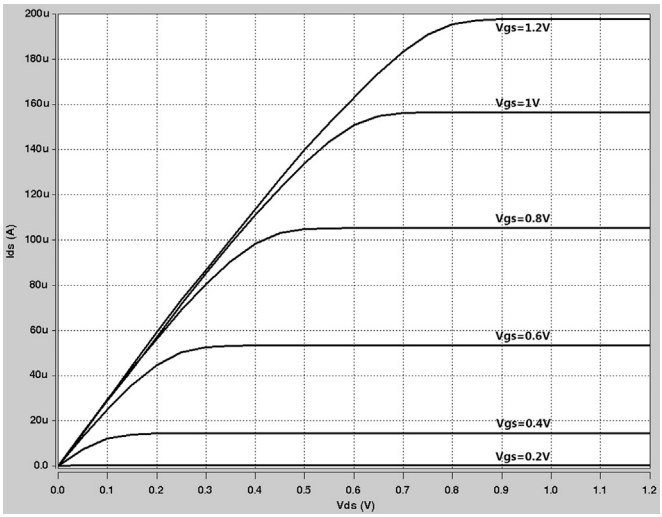

Fig. 4. *I–V* Characteristics of an *n*-type CNTFET based on Stanford model.

2. Carbon nanotube FET (CNTFET)

Carbon nanotubes are considered as a graphene tab rolled into a cylindrical structure. The direction of the rolling is called chirality vector. Due to the chirality vector and the arrangement of hexagonal honeycomb lattice of carbon atoms, the carbon nanotubes could be a conductor or semiconductor. The semiconductor single wall carbon nanotubes (SWCNTs) are applied as a channel of CNTFET [22]. By applying CNT as a transistor channel, a new device is yielded which generally known as CNTFET [23]. The chirality vector is defined by (n_1,n_2) pair named chiral number, which specifies the physical and electrical characteristics of the CNT. Chirality vectors are determined by the equation $ch=a_1n_1+a_2n_2$ where, a_1 and a_2 are the unit vectors of the hexagonal honeycomb lattice. Like MOSFETS, CNTFETs are divided into *n*- and *p*-type. However, compared to MOSFETs, the size and mobility of *n*- and *p*-

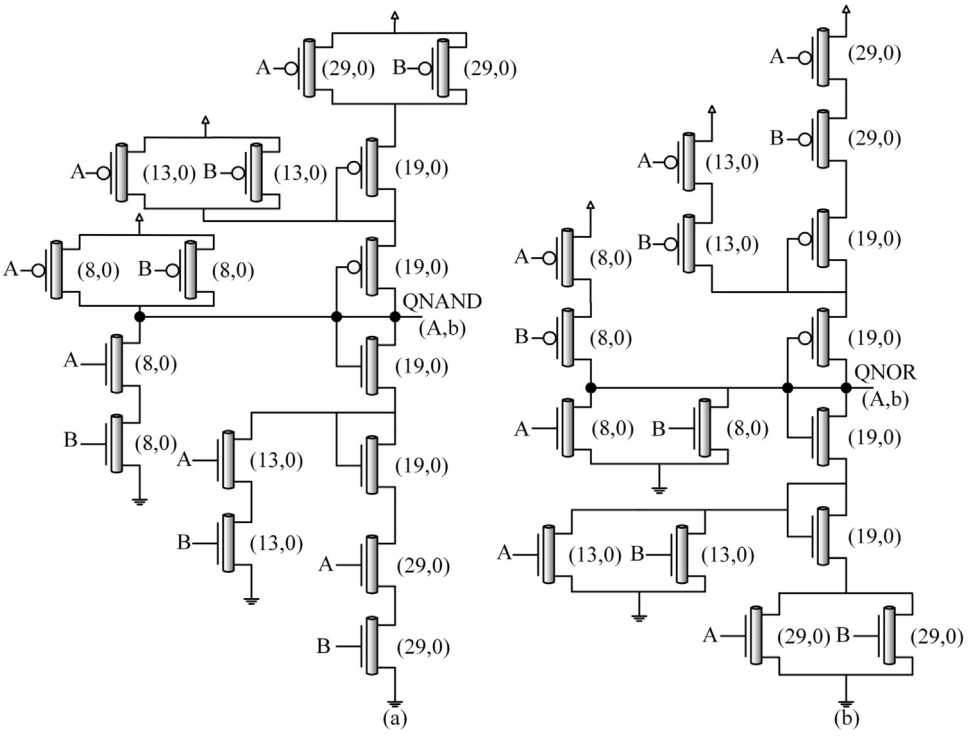

Fig. 3. Implementation of (a) *QNAND* and (b) *QNOR*.

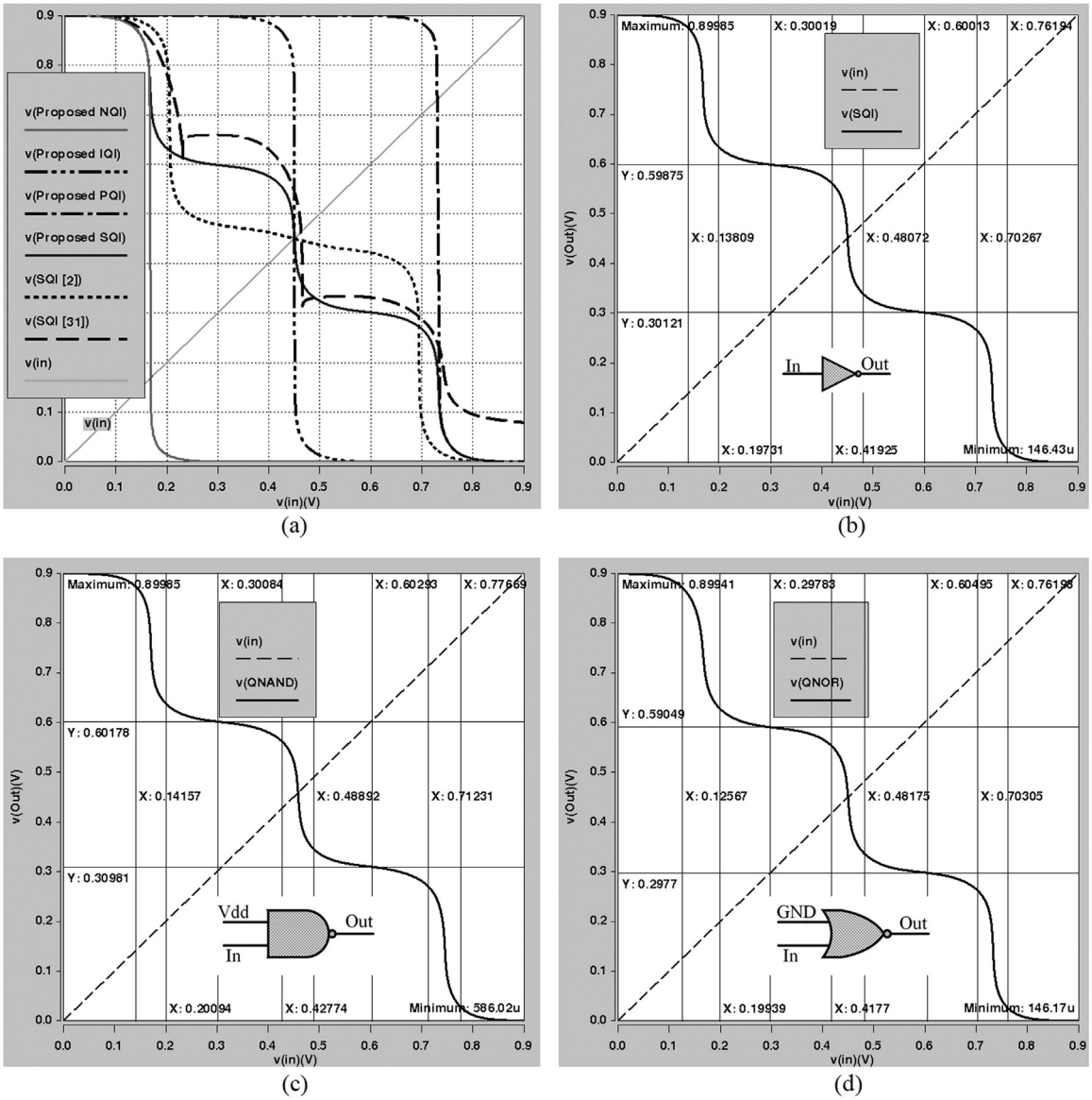

Fig. 5. VTC diagram for (a) quaternary inverters, (b) proposed *SQI*, (c) proposed *QNAND* and (d) proposed *QNOR*.

Table 5
Noise margin values for proposed 4-valued designs.

Noise margin (V)	Logic	*SQI*	*QNAND*	*QNOR*
High	2,3	0.104	0.1	0.11
	1,2	0.117	0.105	0.11
	0,1	0.139	0.136	0.141
Low	2,3	0.138	0.142	0.126
	1,2	0.119	0.127	0.12
	0,1	0.102	0.109	0.1

types in CNTFETs do not differ [24]. The diameter of CNTs is calculated by the following [20]:

$$D_{CNT}=\frac{a\sqrt{n_1^2+n_1n_2+n_2^2}}{\pi}\simeq 0.0783\sqrt{n_1^2+n_1n_2+n_2^2} \quad (1)$$

where, $a=2.49$ Å ($\sqrt{3}a_0$ *and* $a_0\simeq 0.144$ nm) is the interatomic distance between two carbon atoms. The operation principle of carbon nanotube field-effect transistor is similar to that of traditional silicon devices. Therefore, to turn ON a transistor, there is a need to define a threshold voltage. The threshold voltage of a CNT channel is approximated as the inverse function of its diameter [20]:

$$V_{\text{th}}\simeq\frac{E_{bg}}{2e}=\frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}}\simeq\frac{0.436}{D_{CNT}\,(\text{nm})} \quad (2)$$

where, e is the unit electron charge, $V_\pi = 3.033$ eV is a carbon π–π bond energy in the tight bounding model and E_{bg} is the band gap energy.

3. Proposed CNTFET-based design

In general, the multiple-valued logic circuits can be implemented using one [17,2], or more than one power supply source [18,20]. Increasing the number of power supplies in a circuit causes an overall distribution at the whole circuit since more sources than that of the two necessary *Vdd* and *GND* sources are required; therefore, increase in the number of power supply sources would lead to complexity in interconnections, more energy consumption and higher fabrication cost. Here, one power supply source is applied for multiple-valued logic circuits;

Table 6
The result of simulation of quaternary inverters and *QNAND* and *QNOR*.

C-Load	Parameter	Proposed Designs						Designs presented in [4]			[29]	[2]	[20]
		NQI	*IQI*	*SQI*	*PQI*	*QNAND*	*QNOR*	*SQI*	*QNAND*	*QNOR*	*SQI*	*SQI*	*SQI*
0e-15f	Power(uW)	0.009	0.0131	0.9556	0.0087	0.5531	0.5539	1.3579	1.6775	1.5531	1.7595	1.2198	41.731
	Delay(ps)	1.3	0.91	1.7393	1.2258	3.1309	3.3049	19.067	24.552	26.527	3.6617	1.9553	5.0936
	PDP(e-19J)	0.12	0.1193	16.621	0.1067	18.279	18.308	258.91	411.86	411.99	64.427	23.85	2125.6
1e-15f	Power(uW)	0.08	0.0849	0.9958	0.0785	0.5699	0.5796				1.7798		41.749
	Delay(ps)	113.5	69.1	39.766	118.44	80.522	79.504				68.901		7.8268
	PDP(e-19J)	90.3	58.696	395.99	92.983	458.9	460.78				1226.3		3264.6
2e-15f	Power(uW)	0.19	0.1576	1.0359	0.1493	0.5868	0.6158				1.7995		41.765
	Delay(ps)	224.6	132.35	77.668	224.78	155.5	157.53				132.9		10.479
	PDP(e-17J)	3.33	2.0858	8.0456	3.356	9.1247	9.7007				23.915		43.765
3e-15f	Power(uW)	0.22	0.2241	1.0758	0.2159	0.6037	0.6307				1.8192		41.783
	Delay (ps)	333.1	199.21	116.01	336.5	233.03	234.21				198.9		13.153
	PDP(e-17J)	7.32	4.4643	12.018	7.265	14.068	14.772				36.183		54.957
4e-15f	Power(uW)	0.29	0.2978	1.1156	0.2885	0.6207	0.6787				1.8393		41.797
	Delay(ps)	444.9	263.55	153.76	443.72	310.54	300.6				257.13		15.823
	PDP(e-17J)	12.6	7.8485	17.154	12.801	19.242	20.402				47.94		66.135
Transistor Count		2	2	10	2	16	16	9	15	15	6	10	16

Malfunction

Table 7
Truth table of *QHA*.

Sum *B*					Carry *B*				
A	0	1	2	3	*A*	0	1	2	3
0	0	1	2	3	0	0	0	0	0
1	1	2	3	0	1	0	0	0	1
2	2	3	0	1	2	0	0	1	1
3	3	0	1	2	3	0	1	1	1

therefore, the voltage division rule is applied to produce different voltages for different logic values.

The proposed design in this architecture for creating voltage divider is shown in Fig. 1(a), where, four CNTFETs are applied with the chirality vector of (0, 19). These transistors operate in a state of intermediate conductance. There are six routes from either *Vdd* or *GND* to the output in Fig. 1(a) presented as 3, 2*p*, 1*p*, 0, 1*n* and 2*n*. The route 0 is used to create logic '0', which is controlled by the *n*-type transistors network. In the same manner, the route 3 is to produce logic '3', which is controlled by *p*-type transistors. The routes 1*x* and 2*x* ($x \in \{p, n\}$) are connected to the output using voltage divider that creates logic '1' and '2', respectively. Consequently, to produce logics 0, 1, 2 or 3 in the output, the corresponding route should be connected to the output. For example, if logic '1' is needed, the route 1*p* is connected to *Vdd* using the *p*-type CNTFETs and the route 1*n* is connected to *GND* through the *n*-type CNTFETs as well, in order to perform the voltage division. The corresponding voltage for each logic value is presented in Table 1. In this article, four different chirality vectors are used to control the routes. These chirality vectors are applied in previous articles [4,2,20,19] as well.

The required *p*-type and *n*-type CNTFETs for controlling the routes are shown in Fig. 1(b), where the chirality value is placed in front of each transistor. The input signals in Fig. 1(b) are 4-valued. If the primary input signals are binary, the 4-valued signals can be generated through an encoder (*B2Q*). As it is observed in Fig. 1(b), a reverse voltage of inputs is required to control and detect the routes as well. By applying Standard Quaternary Inverter (*SQI*), the inverse operation is generated. These newly designed *SQI* and *B2Q* circuits are introduced in Section 4.

In the next sections two selected implementing methods for each 4-valued logic circuits are presented by *QNAND*, *QNOR*, *QHAs* and *QFA* based on the results obtained from simulations. The wholeness of this proposed architecture is revealed in the first selected method and the circuit parameters are optimized in the second selected method.

4. Designing quaternary universal gates

The basic gates such as two-input quaternary NAND/NOR (*QNAND*/*QNOR*) and quaternary inverters are designed and verified; moreover, the appropriation of voltage division functionality for this proposed designs is evaluated.

4.1. Inverters & encoder

The proposed *B2Q* circuit design based on this proposed architecture is shown in Fig. 2(a), the input/output correlations are tabulated in Table 2. The following four types of quaternary inverters: Negative (*NQI*), Intermediate (*IQI*), Standard (*SQI*) and Positive Quaternary Inverter (*PQI*) are introduced and implemented. The correlations among the inputs and outputs of these inverters are presented by (3). The truth table of each inverter is represented in Table 3 and implementation of each one of them is illustrated in Fig. 2.

$$
\begin{aligned}
NQI &= \begin{cases} 3 & if\ in = 0 \\ 0 & if\ in \neq 0 \end{cases} \\
IQI &= \begin{cases} 3 & if\ in = 0\ or\ 1 \\ 0 & if\ in = 2\ or 3 \end{cases} \\
SQI &= 3 - in \\
PQI &= \begin{cases} 3 & if\ in \neq 3 \\ 0 & if\ in = 3 \end{cases}
\end{aligned} \tag{3}
$$

Here, how the SQI works is assessed. When the input has the value '0', with respect to (1) and (2), three *p*-type transistors in routes 1*p*, 2*p* and 3 are switched ON while three *n*-type transistors in routes 0, 1*n* and 2*n* are switched OFF. Consequently, the logic '3' appears in the output. After changing the input value to '1' (0.3 V) the *p*-type transistor in route 3 will be switched OFF while the *n*-type transistor of route 2*n* will be switched ON. Other transistors remain in their previous states; thus, in this state, as to voltage division, the output voltage will change to logic '2'. A change from

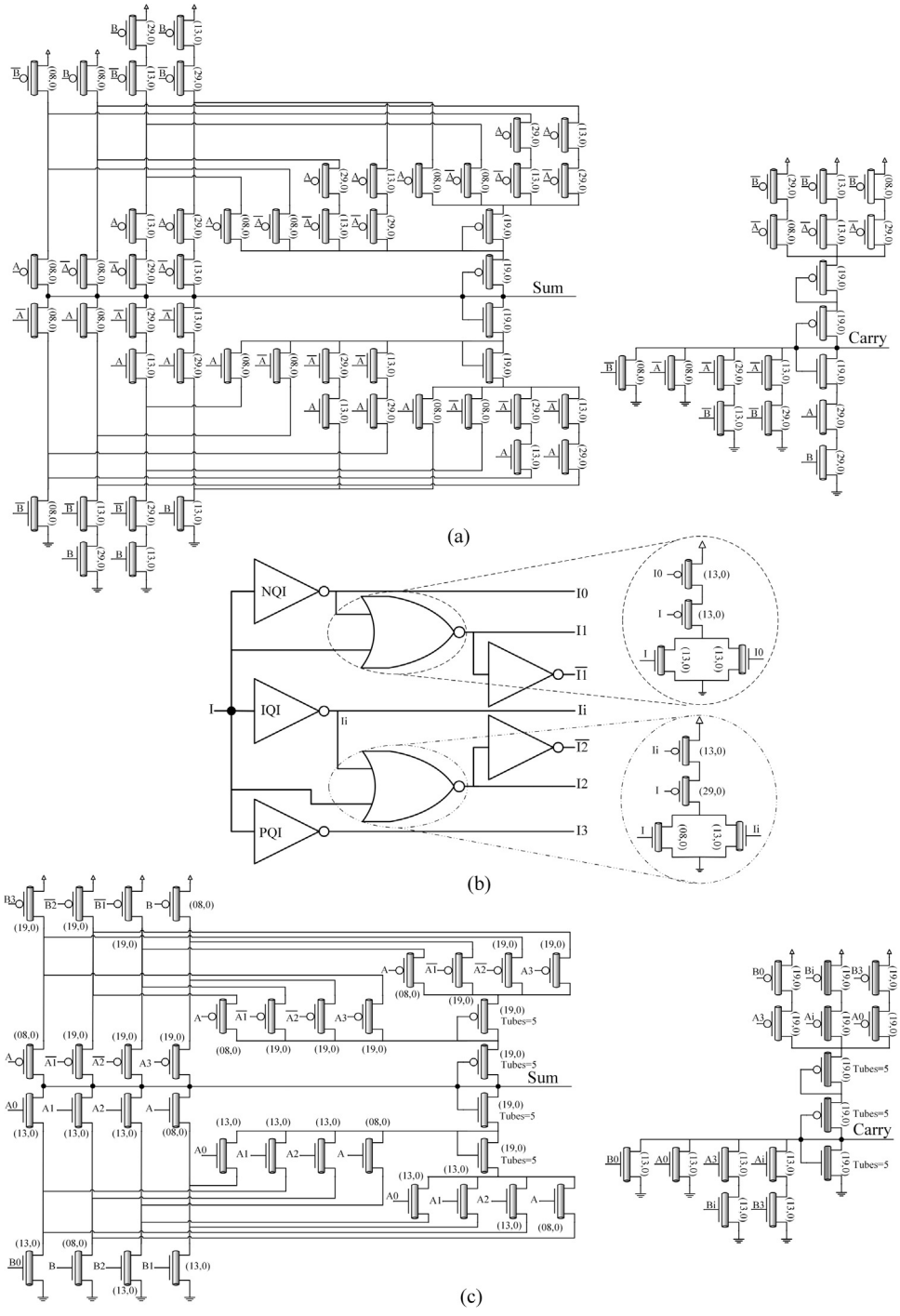

Fig. 6. (a) First proposed *QHA*, (b) proposed *Q-DEC* and (c) second proposed *QHA*.

Table 8
The output values of *Q-DEC* for different inputs.

I	*I*0	*I*1	$\bar{I}$1	*Ii*	$\bar{I}$2	*I*2	*I*3
0	3	0	3	3	3	0	3
1	0	3	0	3	3	0	3
2	0	0	3	0	0	3	3
3	0	0	3	0	3	0	0

logic '1' to logic '2' leads to turning the *p*-type CNTFET OFF in route 2*p* while turning the *n*-type CNTFET ON in route 1 n, simultaneously. In this case, only route 1*p* is closed in the pull-up network of the circuit; in the pull-down network of this proposed circuit, route 1n and route 2n are closed and route 0 is open. Similar to the previous state, here, the voltage division occurs and the output is diverted to the state of logic '1'. When the input value is '3', all pull-down routes are closed and all pull-up routes are open; hence, the output drops to *GND* ('0').

4.2. NAND and NOR gates

The truth table of *QNAND* and *QNOR* is tabulated in Table 4. The correlation between inputs and output of each gate is determined through the followings:

Table 9
The value of chirality vectors and required gate signals for route controlling for different inputs.

Logic	*p*-Type		*n*-Type	
	Gate signal	Chirality vector	Gate signal	Chirality vector
0	*I*	(08,0)	*I*0	(13,0)
0 or 1	*I*	(13,0)	*Ii*	(13,0)
0 or 1 or 2	*I*	(27,0)	*I*3	(13,0)
3	*I*3	(19,0)	*I*	(08,0)
3 or 2	*Ii*	(19,0)	*I*	(13,0)
3 or 2 or 1	*I*0	(19,0)	*I*	(27,0)
2	$\bar{I}2$	(19,0)	*I*2	(13,0)
1	$\bar{I}1$	(19,0)	*I*1	(13,0)

$$QNAND = \overline{\text{Min}\ (A \text{ and } B)} \tag{4}$$

$$QNOR = \overline{\text{Max}\ (A \text{ and } B)} \tag{5}$$

The implementation of *QNAND* and *QNOR* based on this proposed architecture are shown in Fig. 3. The designs of this proposed *QNAND* and *QNOR* are obviously symmetrical and similar to conventional CMOS technology circuit design.

The Stanford University SPICE model [25] that include non-idealities, like channel elastic scattering, the doped source/drain region, Schottky barrier (SB) resistance, multiple CNTs per device and other non-idealities, is adopted to simulate these circuits consisting of the ones introduced here and the ones of to be compared with. This SPICE model is explained in [26–28] in a comprehensive manner. Fig. 4 illustrates the $I-V$ characteristics of the *n*-type CNTFET applied in this article employing the Stanford University model. In this architecture three CNTs are applied in constructing each transistor (tubes $=3$), where pitch $=30\text{E}-9\text{m}$ and gate length $=32\text{E}-9\text{m}$ while the other parameters remain fixed and the default values are applied. The simulations are performed using same parameters model for circuits introduced here and the ones of to be compared with, at 27 °C with 0.9 V power supply. All changes in outputs are considered and the worst delay case is addressed. For circuits which have two outputs, their maximum delay is reported as the worst delay. The time between 50% of change at the input up to 50% of the change at the corresponding output is considered as the delay. The Voltage Transfer Characteristics (VTC) of this proposed *SQI* is compared to the previous works, Fig. 5(a). The noise margin for these proposed *SQI*, *QNAND* and *QNOR* are illustrated in Fig. 5(b)–(d), respectively. The noise margin of these three gates are listed in Table 5. Functionality of these proposed gates prove that this architecture functions in a correct manner in addition to facilitating the designs.

The results obtained from the simulation of these introduced gates are tabulated in Table 6. As observed, in VTC (Fig. 5(a)), the reaction of this proposed *SQI* against input voltage changes is more rapid in comparison with the previous works. This architecture has

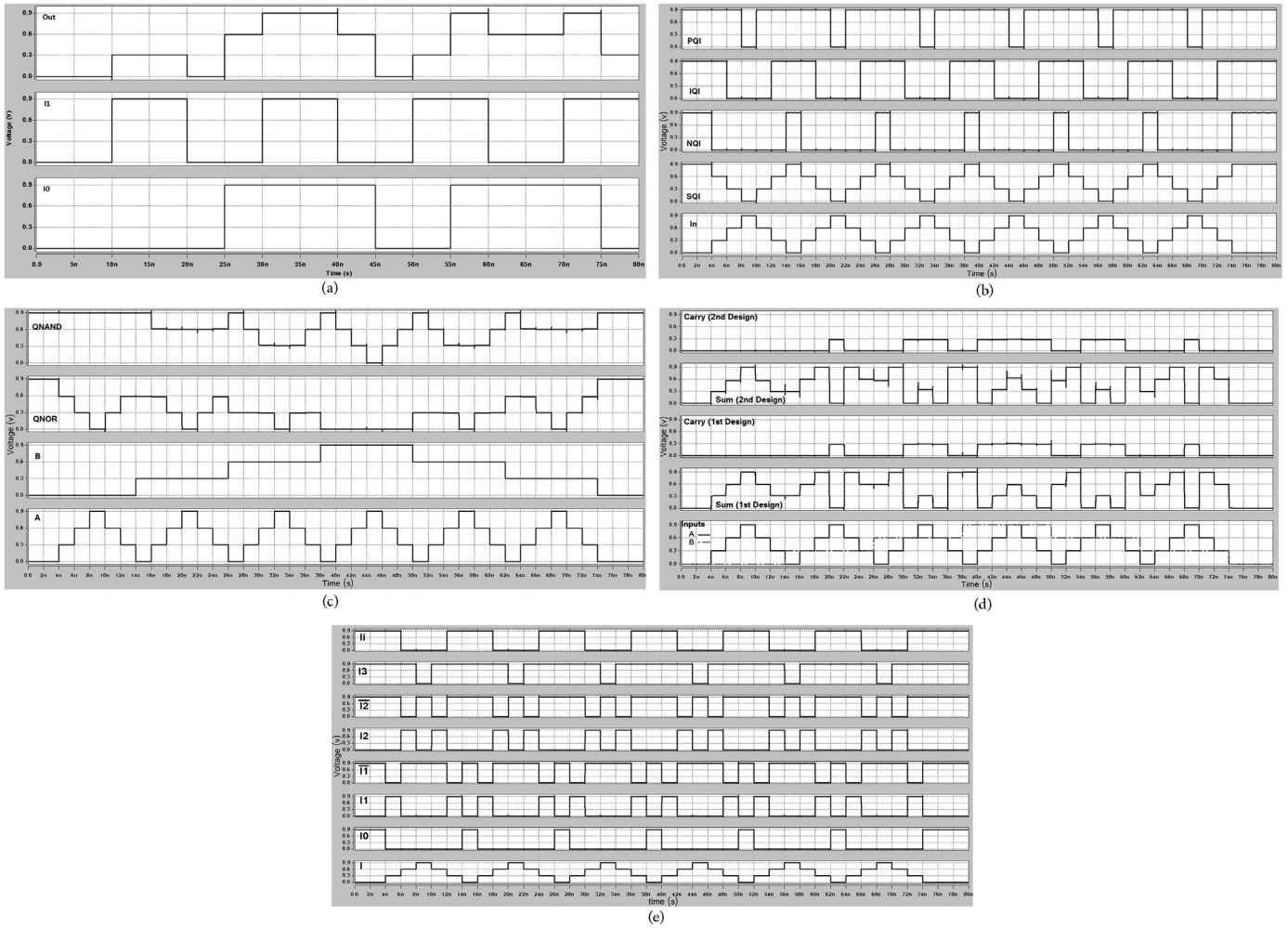

Fig. 7. Transient response of proposed (a) *B2Q*, (b) Q-inverters (c) *QNAND* and *QNOR* (d) *QHAs* and (e) *Q-DEC*.

Table 10
Truth table for *QFA*.

$\sum in=A+B$	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3	4	4	4	4	5	5	5	5	6	6	6	6
C	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
Sum	0	1	2	3	1	2	3	0	2	3	0	1	3	0	1	2	0	1	2	3	1	2	3	0	2	3	0	1
Carry	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	2	1	1	2	2

Table 11
The possible values of *A* and *B* to generate valid *A*+*B*.

A+*B*	0	1		2			3				4			5		6
A	0	0	1	0	1	2	0	1	2	3	1	2	3	2	3	3
B	0	1	0	2	1	0	3	2	1	0	3	2	1	3	2	3

an appropriate noise margin since at the output there is no voltage swing problem. By comparing the circuits here with that of the [4] it is observed that they have voltage swing problem in the presence of capacitance load. (e.g. if the C-Load =1*e*–15f at the output, the voltage of each logic (except '0') is reduced by 0.3 V and any increase in C-Load makes this problem worse). In this architecture, when C-Load =0 the PDP parameter outperforms the findings in [4] by 94.2%. The output nodes in [29] have the voltage swing problem and due to constant ON state of the pull-up network, the static power is high. Moreover, the PDP parameter in *SQI* implementation at C-Load =2e–15f is optimized by 66.4%. The major problem in the findings of [20] is the application of three different power supplies for implementing 4-valued logic circuits. This method introduced complexities in the interconnection with a high power consumption. In this study at C-Load =2e–15f the PDP parameter outperforms that of the [20] by 81.6%. In designing 4-valued circuits based on the method introduced by [2] and illustrated in Fig. 3(d) in [29] the output does not have a correct function per C-Load over 0e–15 and in logic 1 and 2 it is troublesome (Fig. 5(a)). Compared with [2] the PDP parameter in this proposed architecture at C-Load =0 has a better performance by 30.31%.

Producing intermediate logics in MVL circuit designs through the proposed voltage divider and that of [2,29,14] encounter a short circuit in certain output situations. Here, there exists a direct relation between power consumption and the standby energy consumption increase.

5. Quaternary half-adder (QHA)

Any enhancement in adding operation leads to enhancement of other operations [30]; since, they generate more complex operations like multiplication, division and exponentiation [31,32]. This addition operation is widely applied in arithmetic logic unit (ALU), floating-point unit, and address calculation in the main and cache memories [33].

The Sum and Carry functions of *QHA* are represented by (6) and (7). The truth table of *QHA* is tabulated in Table 7. In (6) and (7), A_i, B_i $\epsilon\{0, 1\}$ are obtained through decoding the signals *A* and *B* as follows:

$$\text{Sum}=3.(A_0B_3+A_1B_2+A_2B_1+A_3B_0)+2.(A_0B_2+A_1B_1+A_2B_0+A_3B_3) +1.\ (A_0B_1+A_1B_0+A_2B_3+A_3B_2) \quad (6)$$

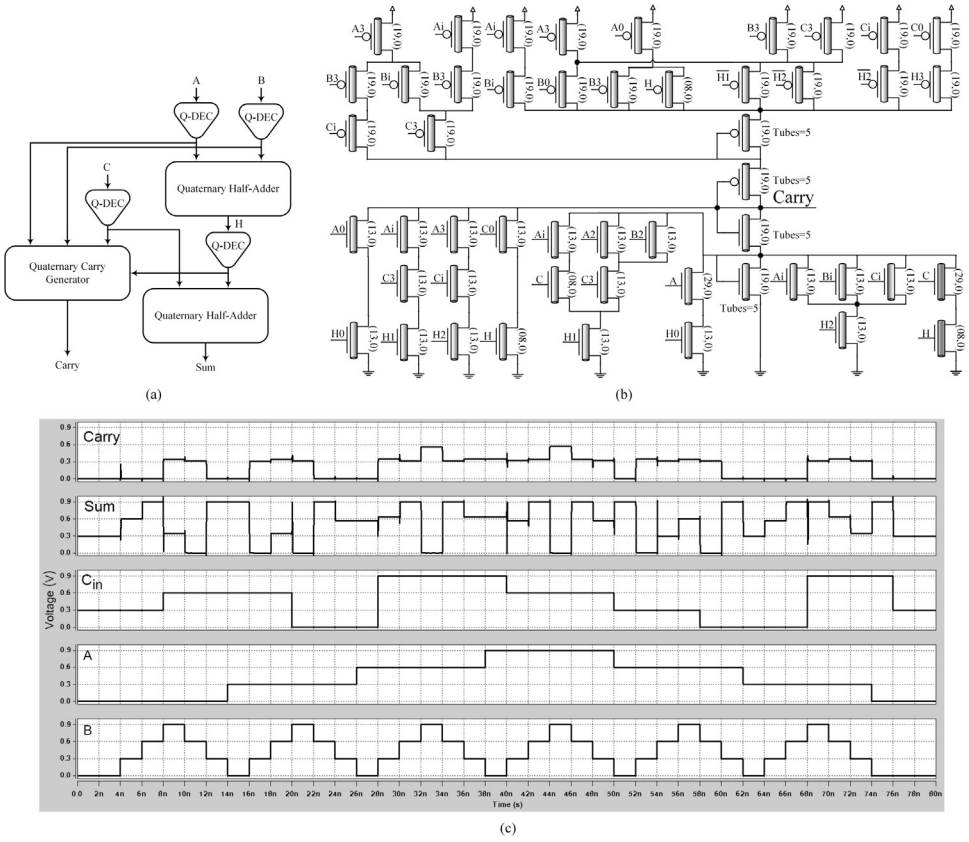

Fig. 8. (a) The schematic diagram of this proposed *QFA*, (b) transistor level structure of Carry generator and (c) the transient results of proposed *QFA*.

Table 12
The simulation results.

C-Load	Parameter	Proposed					*QFA* [35]	*QHA* [20]	*BFA*-based *QFA*
		Q-DEC	*B2Q*	1st *QHA*	2nd *QHA*	*QFA*			
0e–15f	Power (uW)	0.3337	0.8684	1.7557	1.4563	2.4766	98.36	5.882	2.868
	Delay (ps)	7.61	2.561	49.892	18.972	71.728	109.23	20.573	43.01
	PDP (e-16J)	0.0254	0.022	0.876	0.276	1.178	107.439	1.2101	1.2337
2e–15f	Power (uW)	1.827	0.906	1.908	1.6193	2.6579	102.43	5.961	3.7
	Delay (ps)	390	51.11	251.334	74.941	107.994	122.36	42.459	80.1
	PDP (e-16J)	7.125	0.464	4.7955	1.21352	2.871	125.333	2.531	2.96
Transistor count		18	18	89	87	195	163	106	190
Power supply count		1						3	1

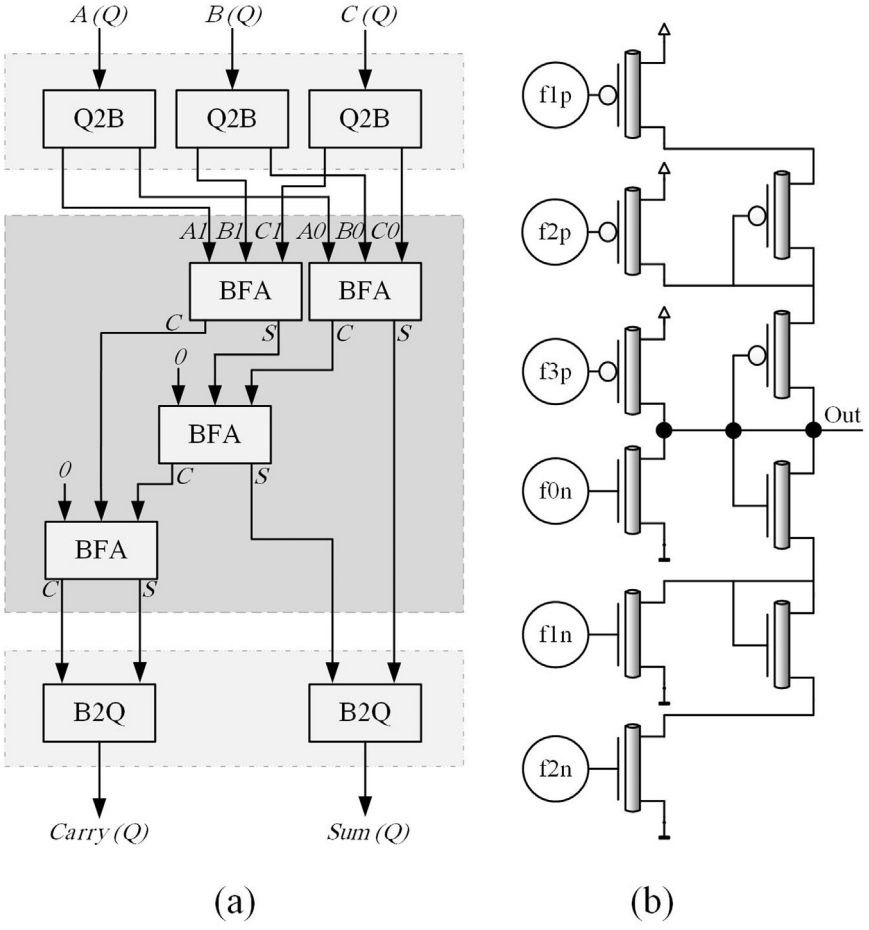

Fig. 9. (a) BFA-based QFA, and (b) third method to implement 4-valued circuit based-on this proposed architecture.

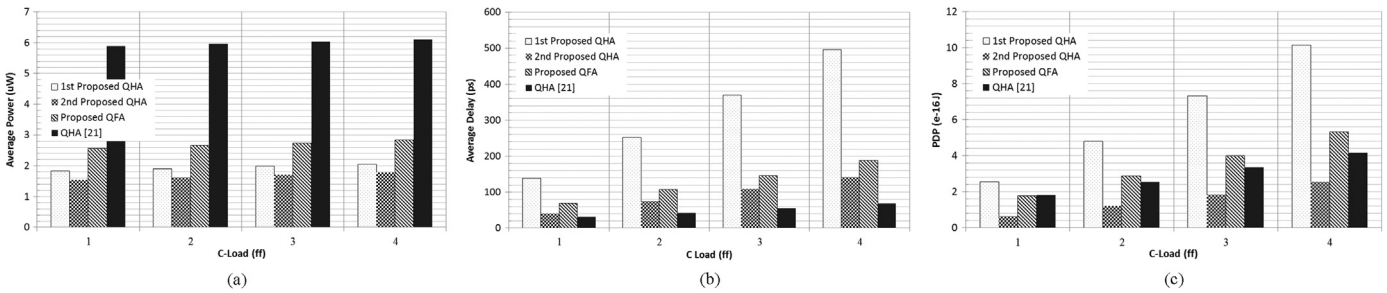

Fig. 10. (a) Average power consumption (b) Average delay and (c) PDP variations versus C-Load variation.

Carry=1. $(A_1B_3+A_2B_2+A_2B_3+A_3B_1+A_3B_2+A_3B_3)$ (7)

For example, if A has logic value of '2' then: $A_0=0$, $A_1=0$, $A_2=1$ and $A_3=0$ can be written.

5.1. First proposed QHA design in this architecture

Here, two circuits are applied separately to calculate the Sum and Carry. According to Table 7, logic '2' and '3' do not appear on the Carry output; hence, there is no connection in Carry circuit design for routes 2*n*, 2*p* and 3. The first proposed *QHA* is shown in Fig. 6(a), where, the two inverters are required to generate $\bar{A}$ and $\bar{B}$, which are not shown in the Fig. 6.

5.2. Second proposed QHA design in this architecture

In the first proposed design for *QHA*, there exist relatively higher number of transistors between output with either *Vdd* or *GND*. To remove this issue, a second design is being suggested here. In this case, the value of each input should be specified. To determine the value of each input a decoder is necessary. This proposed quaternary decoder (*Q-DEC*) is shown in Fig. 6(b), with one input and 7 outputs. The outputs of this decoder for any logic in the input are tabulated in Table 8.

After determining the logic value of the input, the suitable transistor based on Table 9 is chosen and the correct route connects to the output subsequently. The chirality and required signal connected to the gate of the applied transistors are tabulated in Table 9. The required controlling signals for transistor gate are provided directly by the input or by a decoded input.

In Table 8, *I* is the input signal, *Ix* and $\overline{Ix}$ ($x\in\{0, 1, 2, 3, i\}$) are the outputs of the decoder. For instance, if one of the pull-up route in Fig. 1(a) is to be connected to *Vdd*, while, the input logic value is '2' or '3', the *p*-type transistor with chirality (19, 0) is applied. In this case, gate is connected to *Ii*. Yet, another example, when an input has logical '0' and it needs to be connected to one of the pull-down routes to the *GND*, one *n*-type transistor with chirality (13, 0) is chosen. The gate of this transistor is connected to *I0*.

In [20] authors introduced a quaternary decoder with 16 transistors and 3 computing levels. To control the *p*-type transistors they used four extra inverters (Fig. 8 in [20]). Consequently, the number of transistors and computing levels increases to 24 and 4, respectively. In this proposed *Q-DEC*, the number of required transistors is 18 and the computing levels is 3.

There are three main power consumption states: P_{static}, $P_{dynamic}$ and $P_{short\text{-}circuit}$ [34]. The $P_{short\text{-}circuit}$ state is when the pull-up and pull-down transistors are ON simultaneously. In other to reduce $P_{short\text{-}circuit}$ in the second proposed design, the chirality of pull-up transistors, which is controlled by decoder's outputs, is considered as (19, 0); while the chirality for pull-down transistors is (13, 0). The circuit of the second proposed design is shown in Fig. 6(c). For simplicity, the decoders are not shown in Fig. 6.

The transient response of these proposed *B2Q*, inverters, *QNAND* and *QNOR*, first and second *QHA* and *Q-DEC* in this article are shown in Fig. 7(a)–(e), respectively. The results of simulations are listed in Table 12.

In the second proposed *QHA* design, with no load capacitance, the power consumption, delay, and PDP are 75.2%, 7.8% and 77%, respectively, indicating a better result in comparison to [20]; moreover, the implementation of this design only needs one power source while the number of transistors are decreased and no voltage swing problem occurs at 500 MHz frequency with C-Load up to 6e–15f.

6. Quaternary full-adder (*QFA*)

The *QFA* is presented by using the second proposed *QHA* and decoder in Section 5.2. The Sum and Carry values are tabulated in Table 10. The possible values of *A* and *B* for $A+B=X$ ($X\in\{0, 1, 2, 3, 4, 5, 6\}$) are listed in Table 11. The characteristics of this proposed architecture contribute to implementation of the common FA through the *QHA* blocks. This is one of the reasons based on which it is claimed that, adopting of this architecture leads to simplicity in designs. This *QFA* shows the ability of cascading circuits which are implemented based on this proposed architecture with acceptable and correct functionality.

The schematic diagram of this proposed *QFA* is shown in Fig. 8 (a). This *QFA* circuit consists of four decoders, one Carry generator, and two *QHA*. There is no Carry unit computing in both the *QHAs* in Fig. 8(a). The inputs of Carry generator are the decoded values of *A*, *B*, *C* and *H*. The results of simulations are tabulated in Table 12 and the transient response of the *QFA* is shown in Fig. 8(c).

A thorough analysis of Table 12 would indicate the fact that these proposed power consumption, delay and PDP outperform the available findings in [35]. Moreover, the malfunctions at the two states when the input summation is 2 or 3; and when the summation of the inputs change from 4 or 5 to 6 or 7 are observed in *QFA* presented in Fig. 6 of [35].

In order to estimate the efficiency level of the introduced QFA it is compared with CNTFET implementation of static CMOS full-adder (BFA-based QFA). For this purpose, the circuit shown in Fig. 9(a) is designed, simulated and the results of which are tabulated in Table 12.

It should be mentioned that such circuit implementation based-on this architecture are not merely limited to these two presented methods, for example the following model (Fig. 9(b)) can be adopted as well to improve the drive capability. This claim is justified by the fact that a reduction of connections in the output node leads to a reduction in the capacitance of output capacitor, while the number of transistors between the output with either *Vdd* or *GND* remains constant regardless of the number of inputs.

The evaluations of power consumption, delay and PDP are shown in Fig. 10(a)–(c), respectively, for the first and the second proposed *QHA* and *QFA* designs against C-Load variations from 1 to 4e–15f.

7. Summary

Due to the advantages over binary logic in designing digital systems the MVL is of great importance. For example, it is possible for the MVL logic to simplify and cause energy efficiency in digital design since it reduces the complexity of interconnections and chip area. This article presents the new quaternary designs of MVL circuits based on CNTFETs. Applying different chirality vectors in CNTFET contributes in designing a voltage divider to generate the required 4-valued logics. The universal functionality complete digital gates are designed and tested with appropriate results. Two types of half-adders are proposed here and by applying the optimized half-adder, the full-adder design is implemented. The quaternary CNTFET-based circuits are implemented and the results of simulations confirm the true functionality of the operations. With respect to the previous implementations, the designs presented here demonstrate improvements in the critical circuit characteristics. In comparison with the available PDPs, (as the term presents a trade-off between delay and power consumption) this newly designed PDP outperform other competitive designs. The obtained results indicate that this design approach is a viable solution for high-performance VLSI design in nanotechnology.

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