A New Modeling Technique for Microwave Multicell Transistors Based on EM Simulations

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***Abstract*— Dealing with high-power operation (i.e., >100 W) is extremely critical to power-amplifier designers due to the lack of accurate transistor models of multicell (i.e., powerbar) devices. The reason is twofold: from one side, it is extremely difficult to characterize high-power transistors (e.g., device instability, thermal issues, microwave instrumentation costs, and measurement uncertainty that drastically increases with the investigated power level); and from the other side, the scaling proprieties of the model, moving from the unit-cell device to the multicell one, are inherently poor due to the different passive access structures to the active-device area. In this article, for the first time, an accurate modeling technique oriented to multicell devices is described, which allows one to extract a compact model of a multicell transistor showing similar prediction accuracy of the unit-cell one. Our assumptions have been widely demonstrated in the manuscript by a comprehensive characterization campaign from small- to large-signal operations carried out on both the unit- and multicell devices.**

***Index Terms*— Field-effect transistors (FETs), GaN, high-electron-mobility transistor (HEMT), high-power amplifiers, microwave amplifiers, microwave measurement, multicell transistors.**

I. Introduction

MULTICELL transistors represent a valid solution to push up the power limits of the hybrid or quasi-MMIC power amplifiers, preserving very compact circuit size [1]–[4]. In fact, multicell devices are offered by the most important foundries as the preferred solution for very high-power transistor operation, since they show significant advantages in terms of circuit manufacturing and end-user customization. Nevertheless, multicell dimensions and, consequently, their power handling capability are inherently limited by the different thermal and electrical conditions existing between the central and peripheral cells. As a matter of fact, when these differences become significant, it is meaningless to increase the multicell dimension, since the expected improvements are inhibited by the device nonideal behavior. Such considerations directly apply also to the possibility of extracting the accurate models of the multicell devices. Indeed, the extraction of an accurate model of the unit-cell does not allow one to achieve a suitable model of the multicell by simple scaling rules, since not only the passive access structures of the multicell, i.e., the gate and drain manifolds, must be correctly modeled accounting for the differences existing among the signals exciting the different cells but also a dedicated, distributed, and thermal model may be required [5].

Nevertheless, multicell transistors can be designed with the aim of minimizing some of the aforementioned problems. First, the design of the unit- and multicell layouts, i.e., via-holes, air-bridge, and cell distance, can be performed to minimize the thermal-state differences existing among the different cells in the multicell structure; this is evidently accomplished at the expense of the structure occupation area but strongly simplifies the required thermal model and clearly improves multicell performance. A smart design of a multicell device that minimizes thermal influence on the multicell performance is reported in [5].

Different from [5], our aim is to extract a compact model having the same accuracy and computational efficiency of the unit-cell model. The unit-cell is usually sufficiently small to avoid any possible issues in the characterization phase, e.g., the adoption of a GaN unit-cell with a periphery of 1 mm does not pose any issues in characterizing the transistor under small- and large-signal operations in both on-wafer and connectorized environments. From a modeling perspective, starting from a reliable and complete set of measurements allows extracting a very accurate model of the unit-cell and this clearly represents a great advantage. Finally, it is worth noting that, once an accurate compact model of the multicell structure is obtained, it can be also used as the "unit-cell" model for correctly designing a higher power device structure.

The proposed approach found its roots in the scalable model proposed in [6], where electromagnetic (EM) simulations were adopted for extracting a compact description of a multifinger device [7]. In this article, that approach is extended to the modeling of the multicell devices.

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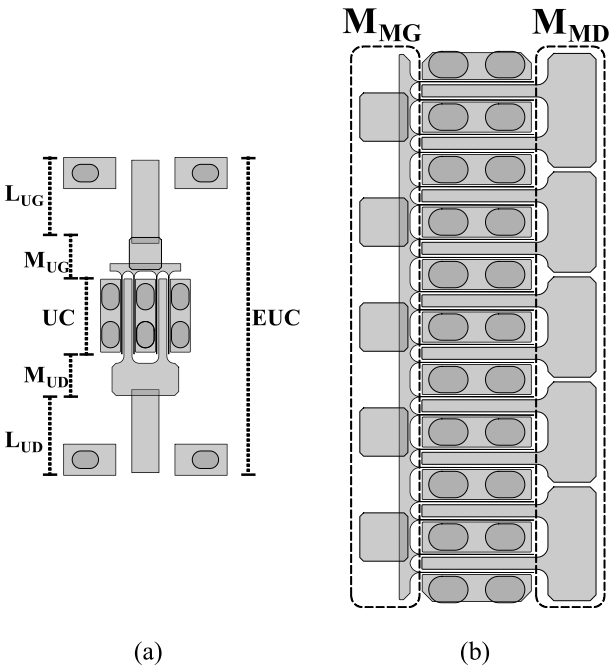

Fig. 1. Layouts of (a) empirical unit-cell and (b) multicell devices.

This article is organized as follows. Section II presents the proposed multicell modeling technique, describing how it can be used for device engineering and circuit design. Section III focuses on the EM simulations, discussing the simulation steps required for correctly extracting the models of the unit- and multicell transistor access structures. In Section IV, the described modeling technique is applied to a 50-W multicell transistor. The achievable accuracy level is demonstrated by means of a comprehensive characterization involving the different transistor operating conditions from small- to medium- and high-power levels for both the unit- and multicell devices. Finally, Section V concludes this article.

II. Multicell Modeling Technique

The proposed multicell modeling technique is fully based on the EM simulations that are a very useful tool for the design of complex devices involving more than one transistor; this is the case of multicell transistors but also of cascode [8] and stacked devices [9].

The first and fundamental step consists in properly calibrating the EM simulator [10] for the optimum tradeoff between the accuracy and the simulation time and for verifying the achievable accuracy. In order to do this, suitable on-wafer test structures can be realized, e.g., lines, for comparing the measurements and the EM simulations.

The second step concerns the EM simulations that are carried out on the passive access structures of the empirical unit-cell, i.e., gate and drain launchers and manifolds, and of the multicell, i.e., gate and drain manifolds. Fig. 1 shows the layouts of the empirical unit-cell and multicell devices, putting in evidence the contribution of the launchers and manifolds. In particular, L_{UG} and L_{UD} are the launchers of the empirical unit-cell, M_{UG} and M_{UD} are the manifolds of the empirical unit-cell and, finally, M_{MG} and M_{MD} are the manifolds of the multicell. It should be pointed out that the reference planes of the unit-cell [UC in Fig. 1(a)] clearly identify the elementary device that is repeated to compose the multicell active area, whereas the empirical unit-cell [EUC in Fig. 1(a)] represents the empirically characterized device. Finally, it is worth noting that the diverse access structures of the unit- and multicell transistors are correctly accounted for by EM simulations.

The next step is the complete experimental characterization of the empirical unit-cell device. More precisely, we performed: dc measurements, low-frequency large-signal measurements, microwave S-parameter measurements, and microwave load–pull measurements. Then, by using the EM simulations of the empirical unit-cell access structure, it is possible to refer all the measurements to the unit-cell reference planes [see Fig. 1(a)]. The deembedded measurements are then used for the extraction and validation of the unit-cell nonlinear model.

It should be put in evidence that, differently from [6], in the present case, all the parasitic phenomena related to the device active and passive areas are correctly considered, including the ones associated with the doped layers (e.g., contact resistances). Indeed, in the present case, measured S-parameters, which fully account for the parasitic effects, are used for the identification of the unit-cell extrinsic parasitic network (EPN). In order to clarify the differences existing between the proposed approach and the one described in [6], it should be pointed out that, in this article, EM simulations are used for the accurate descriptions of the multicell manifolds and to correctly refer the measurements to the unit-cell reference planes, whereas no EM simulation is carried out on the device active area represented by the different unit-cells. Therefore, in the proposed modeling approach, EM simulations are carried out only on the access structures of the multicell device, avoiding all the approximations related to the description of the device active area in EM simulations (e.g., doping concentrations and profiles).

Once the unit-cell model is available, it is possible to generate the multicell distributed (MCD) model by connecting N unit-cells to the EM simulations of the multicell gate and drain manifolds. The distributed nonlinear model is a $(2N+2)$-port circuit element that can be efficiently used for studying the impact of the distributed effects related to the different attenuations and delays in the signals exciting the single cells. This article can be extremely useful for engineering the multicell by considering the aforementioned distributed effects but also for scaling up the multicell dimensions. To this end, a possible strategy consists of using the N-unit-cell structure as the new unit-cell, providing sufficient separation in the layout definition between the new unit-cells to make the distributed thermal effects still negligible, and, eventually, designing the manifolds of the scaled device in order to consider the distributed electrical effects.

The MCD model can also be used to simulate the multicell behavior in CAD environments; nevertheless, for improving the computational efficiency, a simplification can be performed by considering the N unit-cells equally excited, i.e., neglecting the differences existing in attenuation and delay in the signals

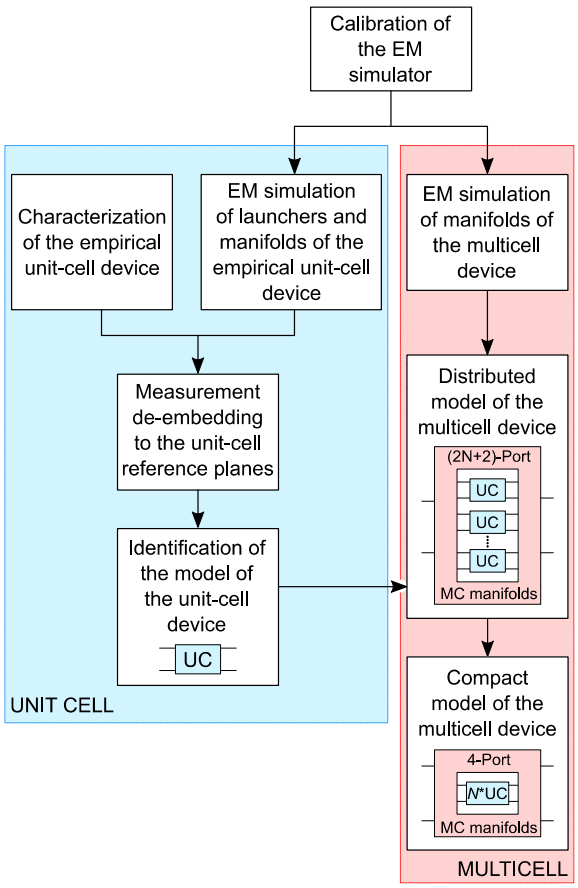

Fig. 2. Flowchart describing the extraction procedure of the MCC model.

exciting the different cells. Under this hypothesis, a multicell compact (MCC) model can be easily generated by considering that the coupling effects are correctly accounted for by the gate and drain manifold EM simulations and that the different cells are strictly in parallel. It is worth noting that the unit-cell model contains both EPN and intrinsic device descriptions, though, being the N unit-cells identical, the unit-cell scaling procedure simply consists of dividing by N the series elements and multiplying by N the parallel elements.

As will be shown in Section IV, the MCC and MCD models show a very similar level of accuracy. Nevertheless, the differences are in their usage: the MCC model is oriented to circuit design, whereas the MCD model can be exploited for power-device design optimization. It should not be surprising that the two models show similar prediction accuracy, since the multicell device was originally designed in order to minimize the thermal and electrical distributed effects. The frequency at which the predictions of the two model formulations start to deviate is an efficient indicator of the frequency (drop of) performance of the multicell device with respect to the unit-cell one. Such an information can be efficiently used for properly selecting the optimum layout of the multicell manifolds. As a matter of fact, the proper design of the multicell device requires that the predictions of the two models practically coincide for the entire fundamental-frequency range of the selected technology.

Fig. 2 reports the flowchart that summarizes the steps of the described modeling technique.

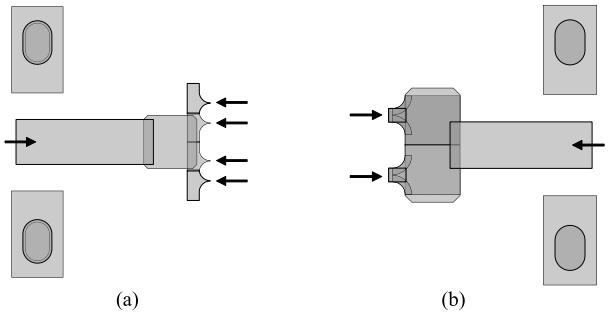

Fig. 3. EM simulated layouts of the empirical unit-cell manifolds and launchers. (a) Gate side. (b) Drain side. The arrows indicate the ports for EM-simulation.

III. EM Simulations

In this section, we describe the EM simulations required for the correct scaling from the unit-cell to the multicell structure.

Fig. 1(a) shows the layout of the empirical unit-cell field-effect transistor (FET) used for modeling. The empirical unit-cell has a total gate periphery of 1.04 mm, which consists of four gate fingers, each having width of 260 μm. To accomplish a robust scaling technique, we divided the layout structure into three areas: the gate and drain passive access structures and the unit-cell. The passive structures consist of gate and drain manifolds and launchers, which are required for on-wafer transistor characterization. The unit-cell, i.e., the elementary device that will be actually replicated in the multicell structure, is defined by its cross-sectional design such as the dimensions of the electrodes, epitaxial structure, and substrate.

The RF characteristics of the passive access structures do not scale linearly with the gate periphery, because they heavily depend on the layout of the manifolds, e.g., the number of the gate fingers, bus lines, and bonding pads. On the other hand, the RF characteristics of the unit-cell linearly scale with the gate periphery, providing that the cross-sectional design of the FET is identical in the unit- and multicell structures. This is the main reason for which the passive access structures and the unit-cell are separately modeled. For the modeling of the passive access structures, EM simulations are exploited in this article.

A. EM Simulations of the Empirical Unit-Cell Manifolds

Fig. 3 shows the simulated layouts of the empirical unit-cell passive access structures. Keysight's Momentum [10] has been used for the manifold modeling as a 3-D planar EM simulator. This simulator is based on the frequency-domain method of moments to simulate accurately the layered structures. Throughout the simulation, the boundary condition was set to open, which means the layered substrates are infinitely extended all the way in the horizontal direction. A 3-D distributed model is exploited for the definition of thick conductors. Regarding the mesh density, the number of cells per wavelength is set to 50 for the maximum frequency. The feed type of ports at the manifold side is appropriately defined as the direct feed. They correspond to the contact area of the ground-signal-ground probes for the unit-cell device and the ones of the bonding wires for the multicell device, respectively.

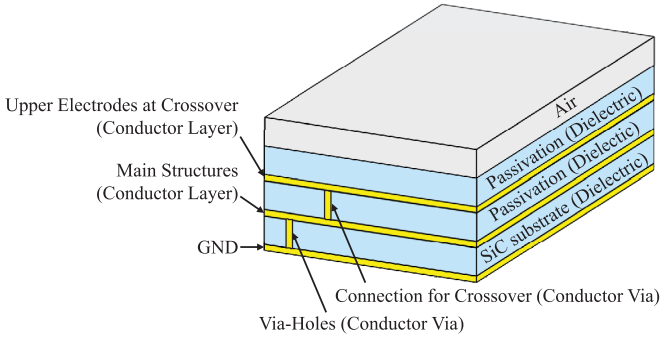

Fig. 4. Layered structure used for EM simulations. Dielectric types are reported, as well as the structures between the layers.

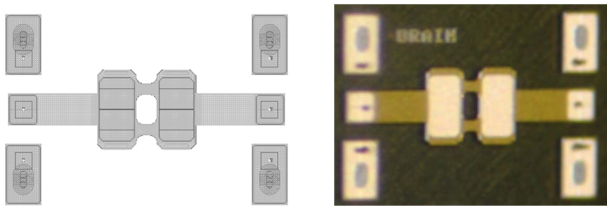

Fig. 5. Test structure of the EUC drain passive access. (a) Layout. (b) Realized structure.

In contrast, the transmission line (TML) feed type is applied to the ports at the finger side. The TML calibration technique removes self-inductance, capacitance-to-ground, and mutual inductance and capacitance between the adjacent fingers.

The layered structure used in EM simulations is described in Fig. 4. It was slightly simplified in order to improve the simulation speed by reducing the number of dielectric layers. The material properties (e.g., permittivity and losses of substrate, and conductivity of metal) are carefully adjusted from the measured S-parameters of the TMLs having different lengths.

The optimized definition of the setup is then used for the EM simulations of the manifold layouts.

To confirm the quality of our EM simulations, we designed and realized dedicated test structures that reproduce the gate and drain passive access structures of the empirical unit-cell device. One example is illustrated in Fig. 5, where the test structure is realized with the drain passive access structure connected face to face to its mirrored structure. Such a structure allows for directly measuring the two-port S-parameters. Fig. 6 shows the comparison of the measured results and the EM-simulations and clearly demonstrates that our EM simulations are in good agreement with the measurements. Similar results were also obtained on the test structure of the gate manifold. Obviously, the realization of the test structure in Fig. 5 is not required to apply our modeling approach; comparisons are here reported only for quantifying the accuracy level of the EM simulations.

The obtained EM-based models of the passive access structures are then used to deembed the measurements (e.g., multibias S-parameters) to the unit-cell reference planes [see Fig. 1(a)]. As shown in Fig. 3, the EM-ports, which are indicated by arrows, are set at the edge of each gate and

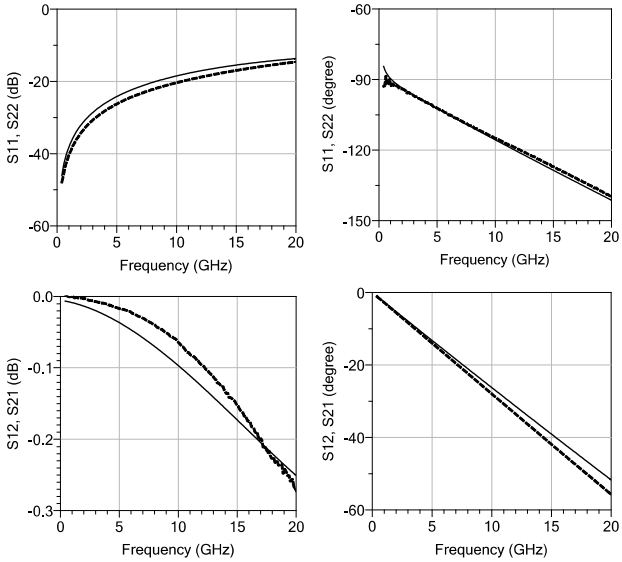

Fig. 6. Comparison between S-parameter measurements (dashed lines) and EM-simulations (continuous lines) of the test structure shown in Fig. 5.

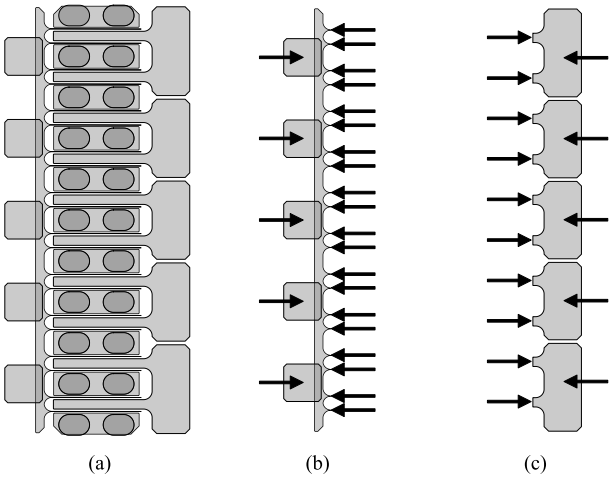

Fig. 7. Layouts of (a) multicell FET, (b) gate manifold, and (c) drain manifold.

drain finger. For the purpose of deembedding, EM multiport S-parameters are converted into two-port S-parameters by treating the ports at the unit-cell side (four ports for the gate and two ports for the drain) as two unique ports at the gate and the drain, respectively.

B. EM Simulations of the Multicell Manifolds

Fig. 7(a) shows the layout structure of the multicell FET, which has five unit-cells. Fig. 7(b) and (c) reports the simulated structures for the gate and drain manifolds, respectively.

Like the unit-cell manifolds, EM-simulated S-parameters are converted into $(N+1)$-port S-parameters, where N denotes the number of unit-cells. For example, looking at Fig. 7(b), the EM simulation of the gate manifold has 25 ports, which consist of 5 ports at the input side and 20 ports at the unit-cell side. For the multicell modeling, the five input ports are connected and treated as one port and, at the unit-cell side, the 20 ports

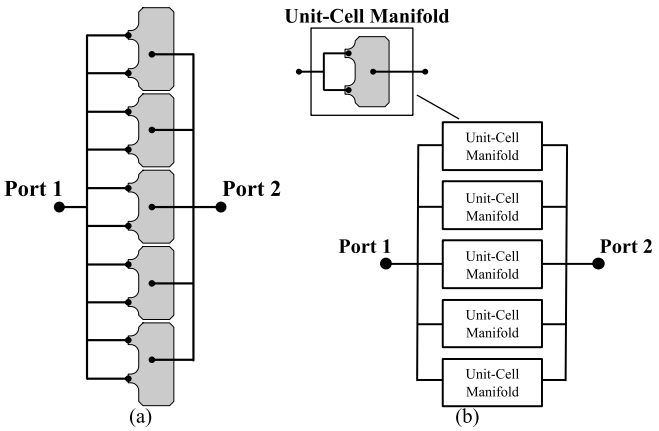

Fig. 8. Layout structures of the multicell drain manifold. (a) Actual multicell manifold. (b) Scaled manifold from the unit-cell manifold.

are treated as five ports, each one representing the four gate fingers of the unit-cell (see Fig. 3).

C. Nonscalability of the Manifolds

One of the main reasons that justify the use of the EM-based approaches for obtaining accurate scalable models is the nonscalability of the manifolds. In order to confirm this assumption, we carried out S-parameter simulations of the two multicell manifold structures. In particular, we performed a comparison of the simulated results between the actual multicell manifolds and the ones obtained by directly parallelizing the unit-cell manifolds. Fig. 8 clarifies the two simulated structures: the actual layout of the multicell drain manifold [see Fig. 8(a)] and the one obtained by simply scaling the unit-cell drain-manifold [see Fig. 8(b)].

Both the considered structures are obtained by EM simulations, although the information concerning the coupling effects of the multicell access structure is properly accounted for only simulating the actual layout of the multicell manifolds. In the other case, where only the EM simulation of the unit-cell device access structure is used, clearly no coupling effect is considered. It should be noted that by performing the simulations of the actual manifolds, as reported in Fig. 8(a), for the drain side, the coupling and distributed effects among the different unit-cell manifolds are automatically averaged. This procedure is similar to what typically happens when one measures the transistor S-parameters, which fully account for the aforementioned effects, and use these data for extracting a conventional lumped-element EPN. The actual advantage of the proposed approach is that, when multicell devices are considered, it is complex to perform accurate measurements (e.g., sample and calibration standard availability, instrumentation power limitations, and stability issues), so EM simulations represent an advantageous and valuable alternative.

Fig. 9 reports the simulated results that clearly demonstrate the assumption that the RF characteristics of the manifolds do not scale linearly with the gate periphery. It should be pointed out that high-power amplifier operation heavily excites the transistor nonlinearity, so, in order to obtain models with

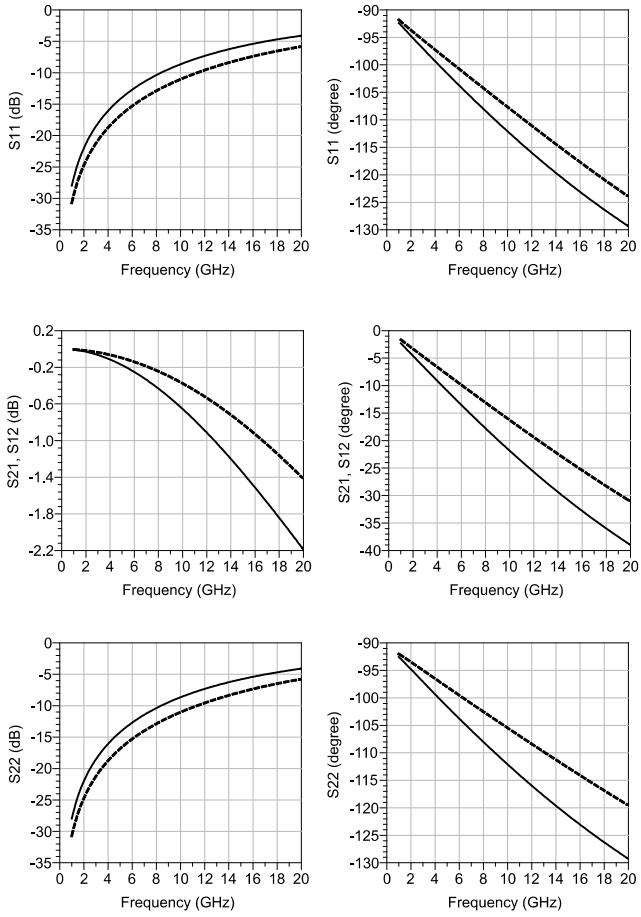

Fig. 9. Simulated S-parameters of the actual multicell drain manifold (continuous lines) and the ones obtained by scaling the unit-cell manifold (dashed lines). Input reflection coefficient (S11), forward and reverse transmission coefficients (S21 and S12), and output reflection coefficient (S22).

adequate prediction capabilities, also the device behavior at harmonic frequencies needs to be correctly accounted for.

Finally, it is worth noting that the simplified procedure for scaling the unit-cell manifold reported in Fig. 8(b) is more accurate with respect to the brutal scaling of the empirical unit-cell model, typically adopted by designers when an accurate multicell model is missing; in fact, in the latter case, the multicell access structure is completely wrong.

IV. Multicell Model Extraction

The modeling methodology described in Section II was applied to a 0.6-μm GaN process, considering a 1.04-mm high-electron-mobility transistor (HEMT) device as unit-cell and then a multicell transistor composed of five unit-cells. The layout of the empirical unit-cell device is shown in Fig. 1(a), and the main foundry specifications are summarized in Table I.

As it can be seen, besides the unit-cell device, indicated as UC, the experimentally characterized device contains also the input and output launchers and the input and output manifolds. The unit-cell can be modeled by using a standard equivalent circuit topology, as shown in Fig. 10. Both launchers and manifolds are modeled by EM simulations, as described in Section III, and properly deembedded from the measurements used during the extraction of the unit-cell model.

TABLE I
0.6-μm GaN HEMT Technology Specifications

Quantity	*Value*
Breakdown Voltage	-200 V
Pinch-off Voltage	-3 V
I_{dss}	1 A/mm
Saturated Output Power	10 W/mm

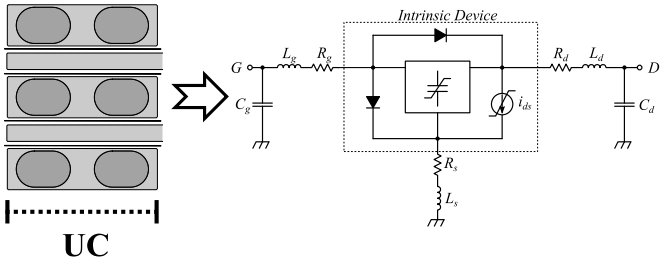

Fig. 10. Equivalent circuit topology adopted for the unit-cell model.

Focusing on the extraction procedure, we used the Angelov model extracted considering as nominal bias point $V_{DS0} = 50$ V and $I_{DS0} = 0.5$ mA. In particular, the dc I/V characteristics and the capacitances are described by means of the standard Angelov equations [11], whereas the linear EPN is extracted by means of the conventional cold-FET S-parameter measurements [12]–[15].

Finally, to correctly account for the thermal and trapping effects affecting the microwave transistor operation [16]–[18], we use the dispersion model proposed in [19], which is based on purely dynamic correction terms modifying the dc I/V characteristics.

For the sake of completeness, we report here the equation of the drain current [19]

$$i_{ds} = F(\underline{v}, V^0, P^0, \vartheta_c) = [1 + \Delta_m(\underline{v}, V^0, P^0)] \cdot F_{\rm dc}(\underline{v}_x, \vartheta_c) \quad (1)$$

$$v_x = \begin{bmatrix} v_{gx} \\ v_{dx} \end{bmatrix} = \begin{bmatrix} v_g(t) + \Delta_g(\underline{v}, V^0, P^0) \\ v_d(t) + \Delta_d(\underline{v}, V^0, P^0) \end{bmatrix} \quad (2)$$

where $F_{\rm dc}$ function is the Angelov drain-current equation [11], $\underline{v}$ is the vector of the instantaneous voltages at the device ports, V^0 is the vector of their average values, P^0 is the average dissipated power, ϑ_c is the case temperature, v_x is the vector of the modified voltages, while the correction terms Δ_m, Δ_g, and Δ_d, account for the dynamic drain-current deviations, related to the trapping and thermal effects, with respect to the device dc I/V characteristics.

To extract the unit-cell model, first, we carried out S-parameter measurements under cold-FET operation, in order to extract the EPN. These measurements are performed in the frequency range from 1 to 40 GHz using TRL calibration and then are deembedded from the EM-simulated input and output manifolds. In this way, the reference planes were shifted from the launcher to the unit-cell reference planes. The deembedded cold-FET measurements were then used to extract the EPN by following well-assessed extraction techniques [12]–[15]. Table II reports the extracted values of the parasitic elements.

TABLE II
Extracted Values of Parasitic Elements

R_g (Ω)	2.70	R_d (Ω)	0.77	R_s (Ω)	0.63
L_g (pH)	63	L_d (pH)	56	L_s (pH)	8
C_g (fF)	0	C_d (fF)	0		

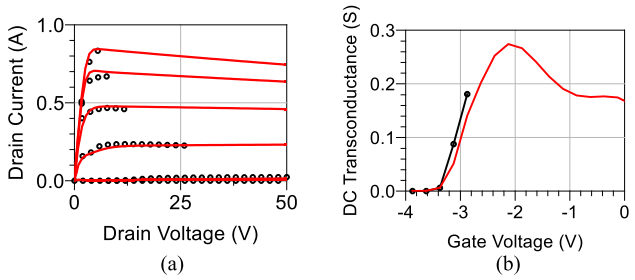

Fig. 11. Measurements (black circles) and simulations (red continuous lines) of the unit-cell model. (a) DC I/V characteristics at $V_{GS0} = -4$–1 V, step 1 V, and $V_{DS0} = 0$–50 V, step 1 V. (b) Transconductance at $V_{DS0} = 50$ V.

After that, the extraction procedure continues with the identification of the Angelov parameters that describe the dc I/V characteristics. We carried out dc measurements over a wide grid of drain and gate biases, as shown in Fig. 11, and we optimized the model parameters against these measurements. Fig. 11 also shows the comparison between the measurements and simulations of the dc I/V characteristics and the dc transconductance at the nominal drain bias voltage.

The resistive gate current is described by means of the Schottky junction conventional formulation and parameters are extracted by means of dc measurements performed in the presence of gate-forward conduction [20].

After the extraction of the dc I/V model parameters, we extracted the purely dynamic correction terms (i.e., Δ_m, Δ_g, and Δ_d) [19] accounting for dispersion effects. To do this, we carried out large-signal low-frequency measurements by using the measurement setup described in [21] and [22]. The frequency chosen to perform that characterization (i.e., 2 MHz) guarantees to operate above the cutoff of the low-frequency dispersion effects so that the trap and thermal behavior of the device is correctly gathered [23] and properly exploited in the extraction of the dispersion model.

In order to obtain an accurate description of the thermal and trapping phenomena, for the identification of the purely dynamic correction terms, we used measurements carried out under class-AB, class-B, class-C, and class-F operations at three drain bias voltages, i.e., $V_{DS0} = 45$, 50, and 55 V. For each of these operating conditions, different loads were synthesized at the output of the DUT for several values of input power ranging from low- to high-power operation. Fig. 12 shows the comparison between the measurements and simulations after numerical optimization. In particular, Fig. 12(a)–(d) shows the measurements used in the identification phase, whereas Fig. 12(e)–(h) shows the fitting capability of the model under different operating conditions with respect to the ones used during identification. For the validation of

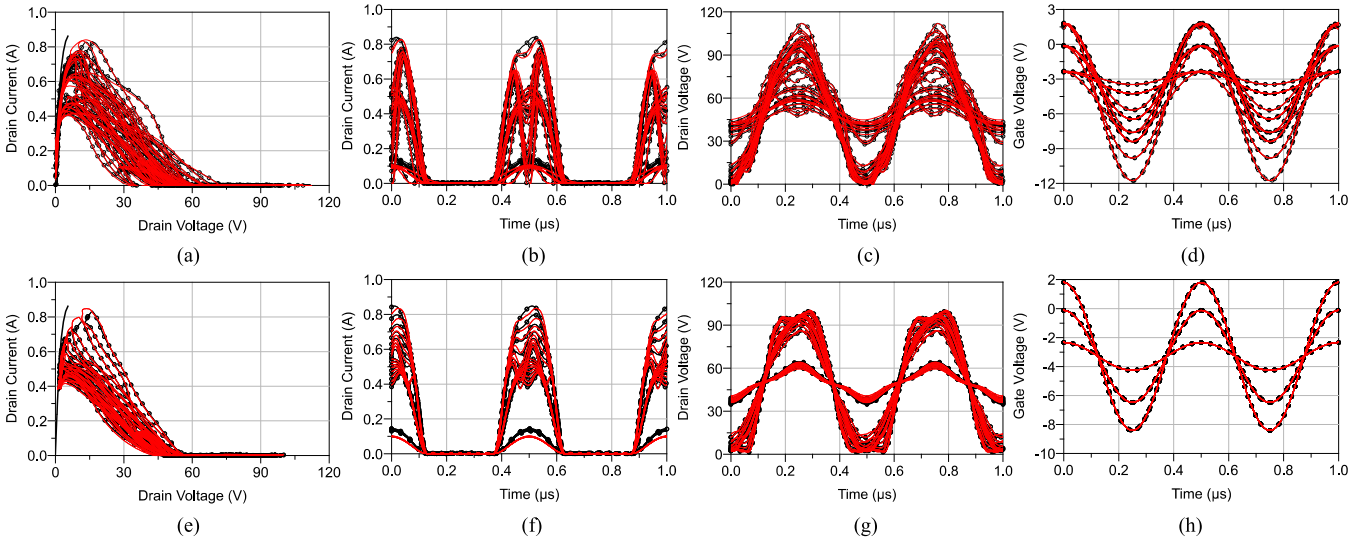

Fig. 12. Measured (black circled lines) and simulated (red continuous lines) load lines, drain current, drain voltage, and gate voltage used in (a)–(d) extraction phase and for (e)–(h) validation of the current-generator dispersion model. Frequency is 2 MHz. (a) and (e) DC I/V characteristic measured at $V_{GS0} = 1$ V.

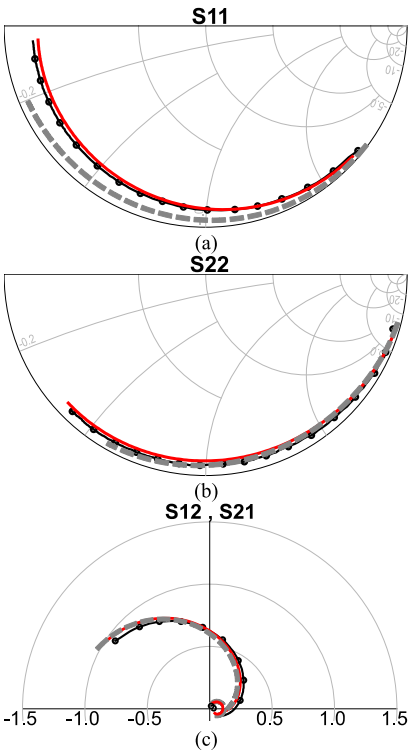

Fig. 13. Empirical unit-cell measured (black circled lines) and simulated (red continuous lines) S-parameters from 1 GHz to 15 GHz at $V_{DS0} = 50$ V and $I_{DS0} = 0.5$ mA at the TRL reference planes. Simulations after the deembedding of the manifolds and EPN are also reported (gray dashed lines). (a) Input reflection coefficient (S11). (b) Output reflection coefficient (S22). (c) Reverse and forward transmission coefficients (S12 and S21).

the dispersion model, we carried out measurements under the inverse class-F operation. As it can be seen in Fig. 12, the accuracy of the model is very good in predicting both the load lines and the voltage and current waveforms.

Finally, the Angelov model parameters describing the intrinsic nonlinear capacitances were identified by following the approach described in [14]. For this purpose, we carried out multibias S-parameter measurements in the frequency range from 1 to 15 GHz, by means of TRL calibration. These measurements are shifted to the unit-cell intrinsic reference plane by deembedding both manifolds and EPN, and then used for the extraction of the capacitance parameters. Fig. 13 shows the comparison between the measurements and the model predictions under small-signal operation for the nominal bias point at the TRL reference planes and after the deembedding of the manifolds and the EPN.

At this point, the model of the unit-cell was further validated by means of load–pull data collected by means of a standard load–pull setup [24] at 4.8 GHz at the nominal bias point. Fig. 14 shows the comparison between the measurements and the unit-cell model predictions. The reference planes of the load–pull measurements lay at the launcher reference planes, so the input and output manifolds and launchers have been also included in the simulations. In order to emphasize the main figures of merit for power amplifier design, i.e., output power and efficiency, the output power load–pull contours are drawn at a constant average drain current I_{DS0}.

In particular, three levels of constant I_{DS0} are shown in Fig. 14: 100, 160, and 200 mA, corresponding to the quasi-linear, medium-power, and saturated-power unit-cell operations. As it can be noted, both optimum values and shape of the contours are well reproduced by the model.

Fig. 14(d) reports the drain efficiency versus the output power over all the input power values for the optimum load. The small discrepancies shown both under small- and large-signal operations confirm the accuracy of the unit-cell model.

Once the accuracy of the unit-cell model is assessed, it is possible to implement the MCD and MCC models. It is worth noting that the MCD and MCC models have been obtained without performing any measurement on the multicell device, i.e., we simply applied the methodology described in Section II based on the EM simulations reported in Section III. To assess the effectiveness of the proposed approach, the modeling procedure is validated by comparing the predictions of the two models with S-parameters and load–pull measurements, carried out at 4.8 GHz under class AB, i.e., $V_{DS0} = 50$ V

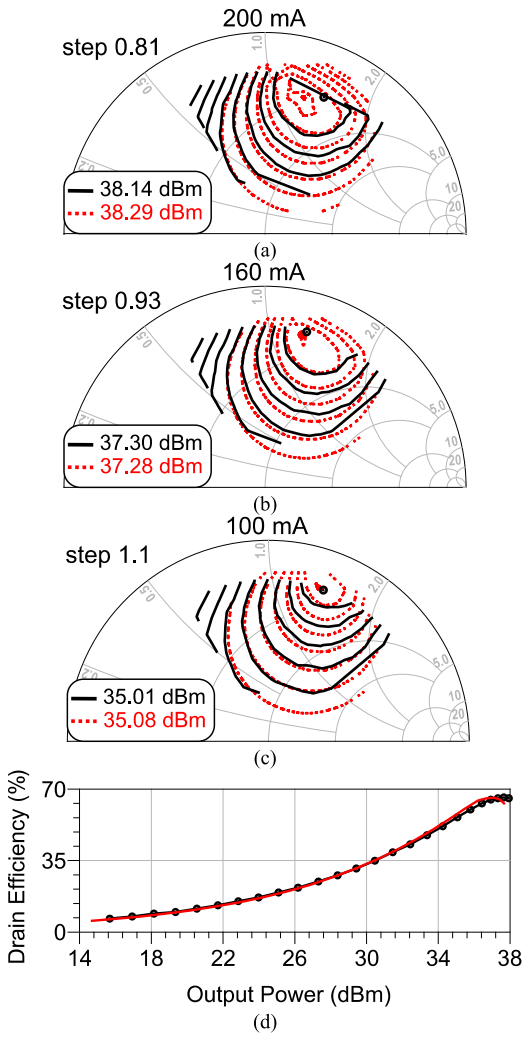

Fig. 14. (a)–(c) Unit-cell measured (lines) and simulated (dotted lines) output power contours at constant I_{DS0} (the maximum values are reported in the boxes). Class-B bias is $V_{DS0} = 50$ V and $I_{DS0} = 0.5$ mA. Frequency is 4.8 GHz. (d) Measured (circled line) and simulated (continuous line) drain efficiency versus output power over all the input power values for the optimum load in (a).

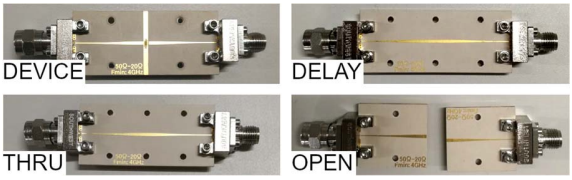

Fig. 15. Test jig with the mounted device and TRL calibration standards used to measure the multicell device. $Z_0 = 20\ \Omega$.

and $I_{DS0} = 20$ mA/mm. In order to perform measurements on the multicell device, a suitable test jig, shown in Fig. 15, was designed and used during the measurements. Fig. 15 also shows the TRL calibration standards designed to calibrate properly the load–pull setup at the die reference plane. Bonding wires, shown in Fig. 16, were correctly accounted for by EM simulations.

Fig. 17 shows the comparison between the multicell measurements and the model predictions under small-signal operation for $V_{DS0} = 50$ V and $I_{DS0} = 20$ mA/mm, at the die

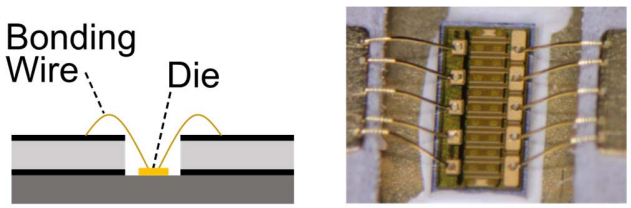

Fig. 16. Cross section of the test jig and detail of the multicell device and bonding wires.

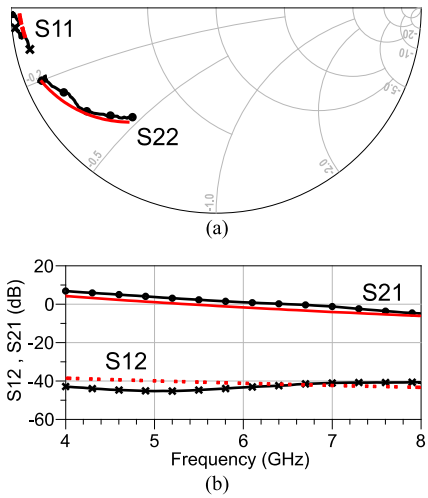

Fig. 17. Comparison between the measured (black circled and crossed lines) and simulated (red continuous and dotted lines) multicell S-parameters from 4 to 8 GHz at $V_{DS0} = 50$ V and $I_{DS0} = 20$ mA/mm. Results are at the die reference planes. (a) Input and output reflection coefficients (S11 and S22). (b) Reverse and forward transmission coefficients (S12 and S21).

reference planes. The bandwidth of the comparison has been limited between 4 and 8 GHz, i.e., the entire fundamental frequency range of the selected technology. As can be seen, the model shows a good level of accuracy in predicting small-signal parameters for the nominal bias point.

Fig. 18 displays the comparisons between the multicell measurements and simulations of the output-power load–pull contours at three levels of average drain current, i.e., I_{DS0}: 800 mA, 1 A, and 1.5 A, corresponding to the quasi-linear, medium-power, and saturated-power multicell operations. In particular, Fig. 18(a)–(c) refers to the MCD model, whereas Fig. 18(d)–(f) refers to the MCC model. As it can be seen, optimum values and shape of the contours are well reproduced by both the distributed and compact models.

Fig. 19 shows the comparison between the multicell measured drain efficiency and the MCC-model simulations versus output power over all the input power values for the optimum load. The accuracy shown both at the small- and large-signal operations confirms the accuracy of the MCC model.

The prediction capability of the two multicell models is comparable and this is mainly due to how the access structures to the multicell device have been designed. As shown in Fig. 16, in the multicell device, we realized five pads that deliver the input signal to the five unit-cells and each pad is connected to the input microstrip line with an identical, dedicated bonding. In this way, we minimize the electrical

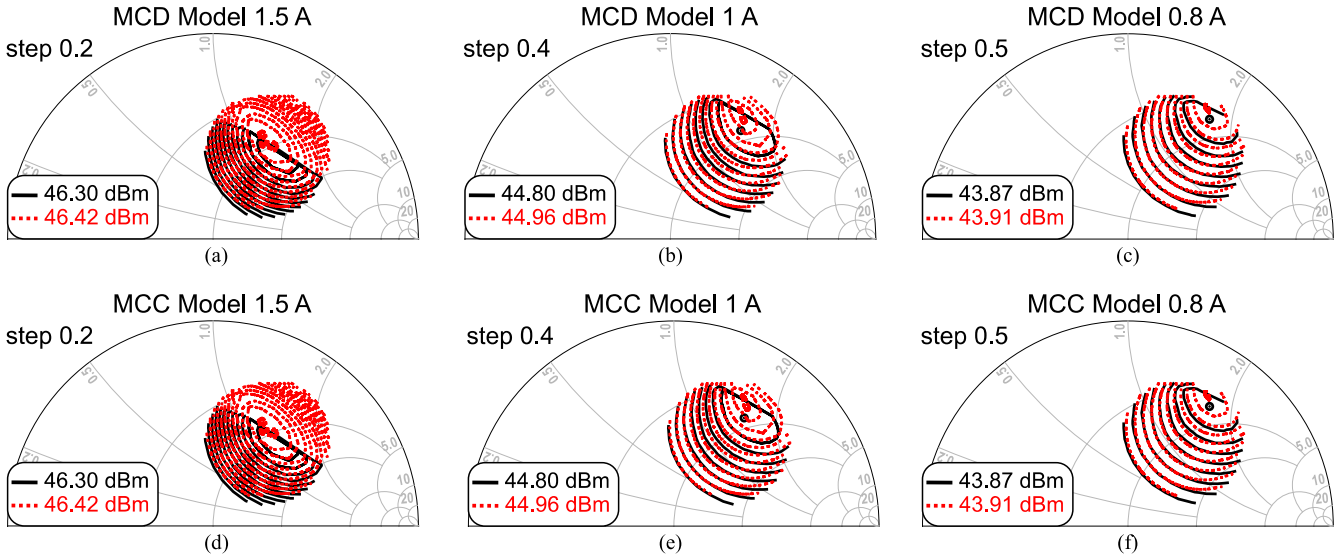

Fig. 18. Multicell measured (black lines) and simulated (red dotted lines) output power contours. (a)–(c) MCD model and (d)–(f) MCC model at constant I_{DS0} (the maximum values are reported in the boxes). Class-AB bias is $V_{DS0} = 50$ V and $I_{DS0} = 20$ mA/mm. Frequency is 4.8 GHz. $Z_0 = 7\ \Omega$.

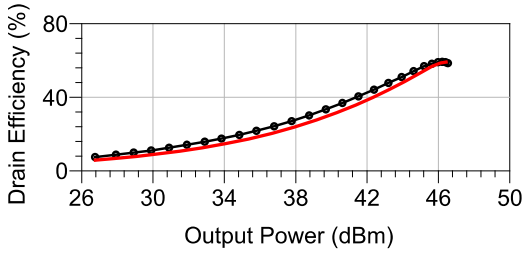

Fig. 19. Measured (circled line) and simulated (continuous line) multicell drain efficiency versus output power over all the input power values for the optimum load in Fig. 18(d).

distributed effects due to the differences in bonding wires and routing of the input signal.

As expected, the MCC model shows better performance in terms of simulation time. Considering the load–pull results reported in Fig. 18, the harmonic balance simulation, performed at 4.8 GHz with a grid of 100 loads and 20 input-power levels, took 15.46 s for the MCC model, which performs over five times faster than the MCD, which took 82.26 s. All simulations are performed by using an Intel Core i5-6200U microprocessor (clock frequency 2.3 GHz) and 8 GB of DDR4 RAM.

V. Conclusion

In this article, we proposed a new modeling technique oriented to multicell power transistors. We performed extensive measurements, from linear to saturated device operation, in order to assess the accuracy of our approach. In particular, we clearly proved how adopting the described approach the accuracy level of the unit-cell model can be transferred to the multicell one.

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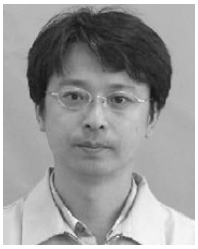

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