Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter With New Method of Capacitor Voltage Balancing

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***Abstract*—This paper presents a three-phase cascaded multilevel inverter that uses five-level transistor-clamped H-bridge power cells. Multicarrier phase-shifted pulse-width modulation method is used to achieve balanced power distribution among the power cells. A new method to balance the midpoint capacitor voltage in each cell is developed and tested. The analysis of the output voltage harmonics and the total power losses covering the conduction and the switching power losses are carried out and compared with the cascaded neutral-point-clamped and the conventional cascaded H-bridge inverters. For verifications, the proposed inverter is experimentally tested on an induction motor. From the results, the proposed inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality.**

***Index Terms*—Cascaded H-bridge, cascaded neutral-point-clamped inverter, five-level inverter, multicarrier phase-shifted pulse-width modulation (CPS-PWM), multilevel inverter, transistor-clamped converter.**

I. Introduction

DEMAND for high-voltage, high-power converters capable of producing high-quality waveforms while utilizing low-voltage devices and reduced switching frequencies has led to the multilevel inverter development with regard to semiconductor power switch voltage limits. Multilevel inverter research is ongoing to further improve its capabilities, to optimize control techniques, and to minimize both component count and manufacturing cost. Owing to voltage limits, to enable high-power conversion, power switches are typically cascaded in series and configured into multilevel structures. The synthesized multilevel outputs are superior in quality which results in reduced filter requirements and overall system size. Switching losses are also reduced, with lower switching frequency operation and maintained high-power quality.

The multilevel inverter has been implemented in various applications ranging from medium to high-power levels, such as motor drives [1]–[3], power conditioning devices [4], [5] also conventional or renewable energy generation and distribution [6]–[8]. There are three major multilevel voltage source inverters topologies, namely neutral-point-clamped (NPC) or the diode-clamped inverter [9], cascaded multilevel [10], and flying capacitor (capacitor clamped) [11]. There are also topologies that have been introduced and have successfully found various industrial applications [12]–[14]. Modulation strategies applied to multilevel inverters are selective harmonics elimination [15]–[17] carrier-based pulse-width modulation (PWM) [18]–[22], space vector modulation (SVM) [23]–[26], and staircase or fundamental frequency modulation [27], [28].

This paper focuses on the cascaded multilevel inverter topology. Generally, among the three topologies, the cascaded multilevel inverter has the potential to be the most reliable and achieve the best fault tolerance owing to its modularity; a feature that enables the inverter to continue operating at lower power levels after cell failure [29]–[31]. Modularity also permits the cascaded multilevel inverter to be stacked easily for high-power and high-voltage applications. The cascaded multilevel inverter typically comprises several identical single phase H-bridge cells cascaded in series at its output side. This configuration is commonly referred to as a cascaded H-bridge (CHB), which can be classified as symmetrical if the dc bus voltages are equal in all the series power cells, or as asymmetrical if otherwise. In an asymmetrical CHB, dc voltages are varied to produce more output levels [2], [32]. Consequently, inverter design becomes more complicated as each power cell has to be sized accordingly to the different power levels, including isolated dc sources. This makes symmetrical CHB modularity advantageous over asymmetrical with regard to maintenance and cost.

For the symmetrical cascaded inverter, voltage level increase is possible without varying dc voltage with the same number of power cells, as proposed by this paper. Recently, the transistor-clamped converter topology has received increased attention as it provides a simpler approach to increase output levels by taking different voltage levels from the series stacked capacitors [12], [33]. In this paper, the proposed new configuration uses a five-level transistor-clamped H-bridge (TCHB) as a power cell that can produce a five-level output instead of three-level as with the conventional H-bridge [33]–[35]. A similar arrangement using a NPC in each power cell has been presented [3]. However, an excessive number of power switches and diodes are required. In [19], though the number of switches for each cell is lower, and to achieve the same output quality, more cells are required, which increases the number of isolated dc sources, as well as bulky transformers.

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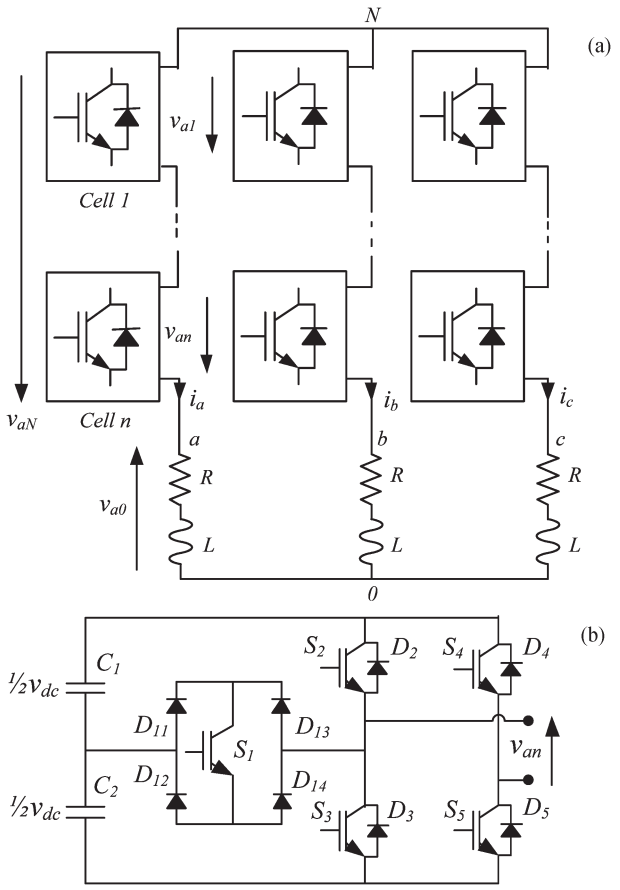

Fig. 1. TCHB: (a) general configuration of the proposed three-phase cascaded multilevel inverter and (b) topology of five-level transistor-clamped H-bridge for each cell.

TABLE I
FIVE-LEVEL TRANSISTOR-CLAMPED H-BRIDGE OUTPUT VOLTAGE

S_1	S_2	S_3	S_4	S_5	v_{an}
0	1	0	0	1	v_{dc}
1	0	0	0	1	$\frac{1}{2}v_{dc}$
0	0 or 1	1 or 0	0 or 1	1 or 0	0
1	0	0	1	0	$-\frac{1}{2}v_{dc}$
0	0	1	1	0	$-v_{dc}$

(Switch ON = 1, Switch OFF = 0)

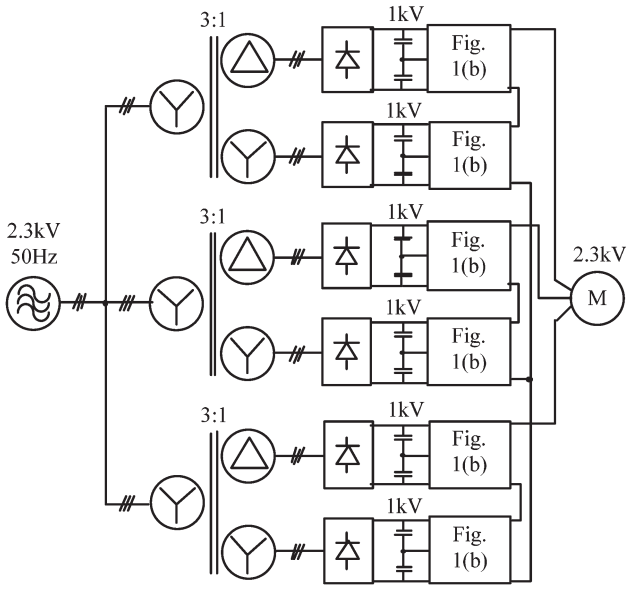

Fig. 2. Basic configuration for medium-voltage drive application.

In this paper, the proposed inverter is evaluated for medium-voltage drive application, in which based on the standard voltages, 2.3 kV to 13.8 kV and the power range 400 kW to 40 MW [36]. With more output levels, in addition to better output quality, the possibility of motor insulation failure as a result of steep voltage wave fronts (dv/dt) across the motor terminals is reduced, compared to the conventional CHB with similar cell configuration [29]. Focus was more on constant-speed drive applications such as fans, blowers, pumps, and compressors, since these comprise 97% of currently installed medium-voltage drives [37]. It is found in various industries such as production plants, process industries, as well as in the oil and gas sectors. Simulation and experimental results are presented for verification. This paper is organized as follows: the inverter's configuration is presented in Section II, the PWM modulation strategy in Section III, analysis of output voltage and harmonics in Section IV, the proposed capacitor voltage balancing in Section V, comparison with several conventional inverters in Section VI, experimental verification in Section VII, and Section VIII is the conclusion.

II. PROPOSED INVERTER CONFIGURATION

Fig. 1(a) is the general configuration of the proposed inverter, comprising N_C series-connected five-level TCHB cells. Fig. 1(b) shows the cell with the additional one bidirectional switch connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels $(\pm v_{\rm dc}, \pm(1/2)v_{\rm dc}, 0)$ to be produced based on the switch combinations given in Table I. The basic configuration for a 2.3-kV medium-voltage drive is shown in Fig. 2 where each power switch is a single 1.7-kV IGBT. The number of power cells required depends mainly on the operating voltage and production cost. In this case, a two-cell configuration is sufficient to produce a high-quality output with up to 17-voltage levels.

In general, the maximum levels in the phase and line voltages of the proposed inverter, based on N_C cells, are given by the following equations:

$$n_p = 4N_C + 1 \tag{1}$$

$$n_l = 8N_C + 1. \tag{2}$$

Based on valid switch combinations, $S_1 - S_5$ in Table I, the cell output voltage v_{an} can be represented by

$$v_{an} = v_{\rm dc}(S_{5n} - S_{4n}) \left\{ \frac{1}{2} S_{1n} + |S_{2n} - S_{4n}|.|S_{3n} - S_{5n}| \right\}. \tag{3}$$

Summation of all the power cell voltages gives the phase-to-neutral voltage, v_{aN} and line voltage, v_{ab}, respectively, as

$$v_{aN} = \sum_{n=1}^{N_C} v_{an} \tag{4}$$

$$v_{ab} = v_{aN} - v_{bN}. \tag{5}$$

III. PWM Modulation Strategy

The modulation index M of the proposed multilevel inverter is defined by

$$M = \frac{1}{2}\frac{V_{\text{ref}}}{V_{Cr}} \tag{6}$$

where V_{ref} is the amplitude of the voltage reference and V_{Cr} is the amplitude of the carrier signal.

Multicarrier phase-shifted PWM (CPS-PWM) modulation is used to generate the PWM signals. The amplitude and frequency of all triangular carriers are the same as well as the phase shifts between adjacent carriers. Depending on the number of cells, the carrier phase shift for each cell $\theta_{Cr,n}$ can be obtained from

$$\theta_{Cr,n} = \frac{2\pi(n-1)}{N_C}, \quad n = 1, 2 \ldots N_C. \tag{7}$$

For signal generation in each cell, two voltage references and one carrier signal are used [18]. The references, v_{ref1} and v_{ref2} are derived from a full-wave voltage reference, v_{ref} defined by

$$v_{\text{ref}} = M \sin \omega t \tag{8}$$

$$v_{\text{ref1}} = |v_{\text{ref}}| \tag{9}$$

$$v_{\text{ref2}} = v_{\text{ref1}} - \frac{1}{2}. \tag{10}$$

Both references are identical but displaced by an offset equal to the carrier's amplitude which is 1/2. When the voltage reference is between $0 < v_{\text{ref}} \leq (1/2)$, v_{ref1} is compared with the triangular carrier and alternately switches S_1 and S_3 while maintaining S_5 in the ON state to produce either $(1/2)v_{\text{dc}}$ or 0. Whereas, when the reference is between $(1/2) < v_{\text{ref}} \leq 1$, v_{ref2} is used and alternately switches S_1 and S_2 while maintaining S_5 in the ON state to produce either $(1/2)v_{\text{dc}}$ or v_{dc}. As for the reference between $-(1/2) < v_{\text{ref}} \leq 0$, v_{ref1} is used for comparison which alternately switches S_1 and S_2 while maintaining S_4 in the ON state to produce either $-(1/2)v_{\text{dc}}$ or 0. For a voltage reference between $-1 < v_{\text{ref}} \leq -(1/2)$, v_{ref2} is compared with the carrier to produce either $-(1/2)v_{\text{dc}}$ or $-v_{\text{dc}}$ alternately switches S_1 and S_3, maintaining S_4 in the ON state. It is noted that two switches, S_4 and S_5, only operate in each reference half cycle. This implies that both switches operate at the fundamental frequency while the others operate close to the carrier frequency. This allows the dc voltage to be switched at a low frequency so as to reduce the switching losses.

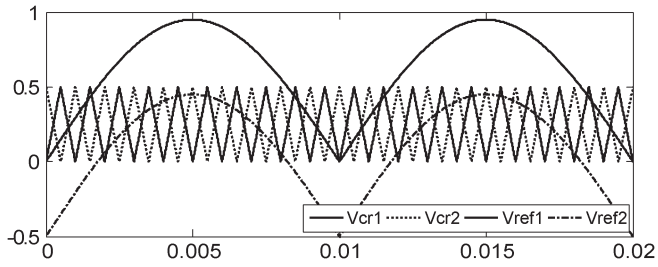

Fig. 3. Multicarrier phase-shifted PWM for two-cell configuration.

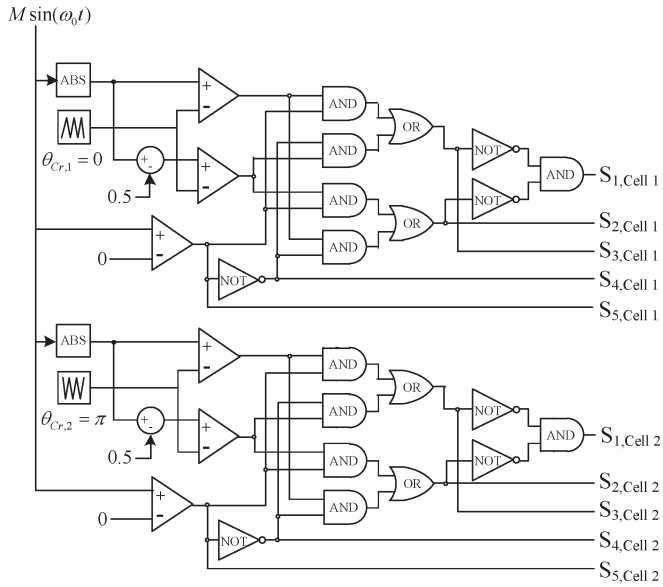

Fig. 4. PWM signal generation with multicarrier phase-shifted modulation for phase a.

TABLE II
PHASE-TO-NEUTRAL VOLTAGE FOR TWO-CELL CONFIGURATION

	v_{a1}	v_{a2}	v_{aN}
$0<v_{ref}\leq{}^1/_2$	0	0	0
	$\frac{1}{2}v_{dc}$	0	$\frac{1}{2}v_{dc}$
	0	$\frac{1}{2}v_{dc}$	$\frac{1}{2}v_{dc}$
	$\frac{1}{2}v_{dc}$	$\frac{1}{2}v_{dc}$	v_{dc}
${}^1/_2<v_{ref}\leq 1$	$\frac{1}{2}v_{dc}$	$\frac{1}{2}v_{dc}$	v_{dc}
	v_{dc}	$\frac{1}{2}v_{dc}$	$\frac{3}{2}v_{dc}$
	$\frac{1}{2}v_{dc}$	v_{dc}	$\frac{3}{2}v_{dc}$
	v_{dc}	v_{dc}	$2v_{dc}$
$-{}^1/_2<v_{ref}\leq 0$	0	0	0
	$-\frac{1}{2}v_{dc}$	0	$-\frac{1}{2}v_{dc}$
	0	$-\frac{1}{2}v_{dc}$	$-\frac{1}{2}v_{dc}$
	$-\frac{1}{2}v_{dc}$	$-\frac{1}{2}v_{dc}$	$-v_{dc}$
$-1<v_{ref}\leq -{}^1/_2$	$-\frac{1}{2}v_{dc}$	$-\frac{1}{2}v_{dc}$	$-v_{dc}$
	$-v_{dc}$	$-\frac{1}{2}v_{dc}$	$-\frac{3}{2}v_{dc}$
	$-\frac{1}{2}v_{dc}$	$-v_{dc}$	$-\frac{3}{2}v_{dc}$
	$-v_{dc}$	$-v_{dc}$	$-2v_{dc}$

Fig. 3 shows the modulation scheme used for the proposed two-cell configuration and Fig. 4 shows a detail block diagram for generating the PWM signals. The phase-to-neutral voltage v_{aN} obtained based on the voltage reference magnitude and the combination of cell voltages, v_{a1} and v_{a2}, are listed in Table II.

From Table II, a total of nine-levels $(\pm 2v_{\rm dc}, \pm(3/2)v_{\rm dc}, \pm v_{\rm dc}, \pm(1/2)v_{\rm dc}, 0)$ phase-to-neutral voltages are produced when both cells are cascaded with CPS-PWM modulation. When $v_{\rm ref}$ is within $0 < v_{\rm ref} \leq (1/2)$, each cell can only produce 0 or $(1/2)v_{\rm dc}$; therefore, v_{aN} has three possible outputs which are 0, $(1/2)v_{\rm dc}$, and $v_{\rm dc}$. In the case of $(1/2) < v_{\rm ref} \leq 1$, each cell can produce either $(1/2)v_{\rm dc}$ or $v_{\rm dc}$ which result in three possible v_{aN} outputs also, $v_{\rm dc}$, $(3/2)v_{\rm dc}$, and $2v_{\rm dc}$. For negative $v_{\rm ref}$, the outputs are similar but with the opposite polarity. As the phase voltages are displaced by $(2/3)\pi$ from each other, higher levels of line voltages will be generated where for v_{ab}, obtainable from (5).

IV. Analysis of Output Voltage and Harmonics

In general, any PWM switched waveform can be expressed in infinite series of sinusoidal harmonics form as

$$\begin{aligned} F(t) = \frac{1}{2}A_{00} &+ \sum_{n=1}^{\infty}\{A_{0n}\cos(n\omega_o t) + B_{0n}\sin(n\omega_o t)\} \\ &+ \sum_{m=1}^{\infty}\{A_{m0}\cos(m\omega_c t) + B_{m0}\sin(n\omega_c t)\} \\ &+ \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\{A_{mn}\cos(m\omega_c t + n\omega_o t) \\ &\qquad + B_{mn}\sin(m\omega_c t + n\omega_o t)\} \end{aligned} \tag{11}$$

where the coefficients A_{mn} and B_{mn} are defined in double integral Fourier form

$$\begin{aligned} A_{mn} + jB_{mn} &= \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} F(x,y)e^{j(mx+ny)}\,dxdy, \\ x &= \omega_c t, \quad y = \omega_o t. \end{aligned} \tag{12}$$

Based on the method developed in [38], the expression for instantaneous v_{aN} and instantaneous v_{ab} of the proposed inverter configuration can be represented by the following equations where J represents the Bessel function of the first kind. From these equations, the harmonic spectrum for both v_{aN} and v_{ab} can be obtained at various operating conditions. Evaluating (14) with $N_C = 2$, $M = 0.95$, $v_{\rm dc} = 1$ kV, $f_0 = 50$ Hz, and $f_c = 1$ kHz results in the line voltage harmonics shown in Fig. 5

$$\begin{aligned} v_{aN}(t) = N_C M v_{\rm dc}\cos(\omega_o t) + \frac{v_{\rm dc}}{\pi} \times \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \\ \times\left\{\frac{1}{m}J_{2n-1}(2N_C m\pi M)\cos\left((2N_C m + n + 1)\pi\right)\right. \\ \left.\times\cos(N_C m\omega_c t + (2n-1)\omega_o t)\right\} \end{aligned} \tag{13}$$

$$\begin{aligned} v_{ab}(t) = \sqrt{3}N_C M v_{\rm dc}\cos\left(\omega_o t + \frac{\pi}{6}\right) + \frac{2v_{\rm dc}}{\pi} \times \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \\ \times\left\{\frac{1}{m}J_{2n-1}(2N_C m\pi M)\cos\left((2N_C m + n + 1)\pi\right)\right. \\ \times\sin\left((2n-1)\frac{1}{3}\pi\right) \\ \left.\times\sin\left(N_C m\omega_c t + (2n-1)\left(\omega_o t - \frac{1}{3}\pi\right)\right)\right\}. \end{aligned} \tag{14}$$

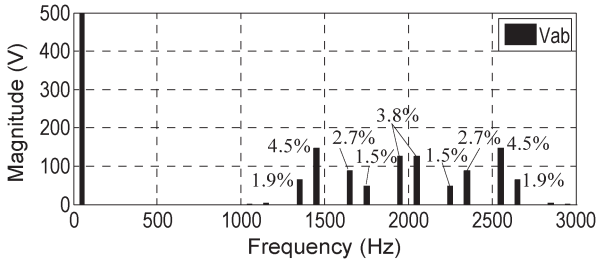

Fig. 5. Harmonic spectrum of line voltage generated using (14).

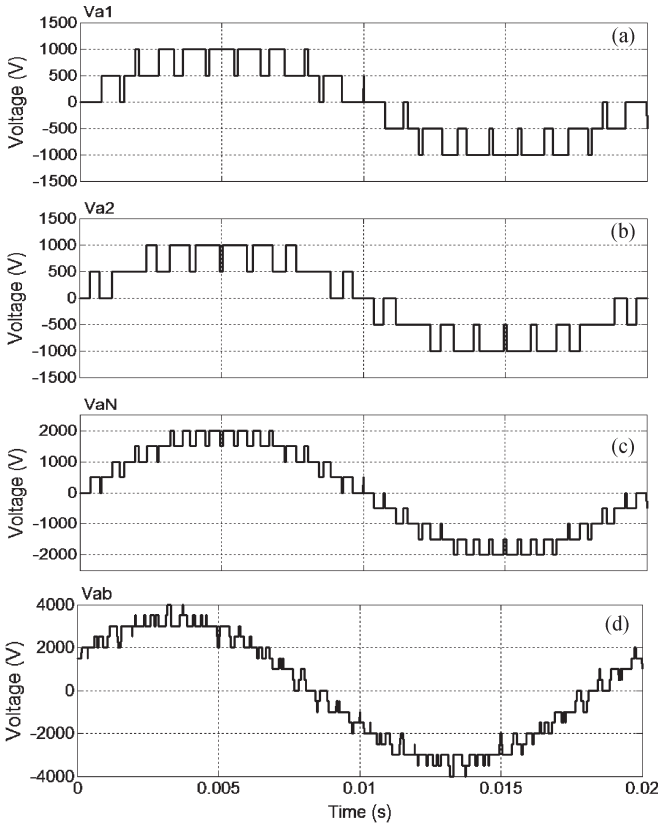

Fig. 6. Simulated output voltage of the proposed inverter. (a) Cell 1 output voltage. (b) Cell 2 output voltage. (c) Phase voltage. (d) Line voltage.

The simulated output voltages for the medium-voltage drive configuration in Fig. 2 are shown in Fig. 6. Test conditions were the same for comparison. Similarly, the modulating signal's frequency and modulation index were 50 Hz and 0.95, respectively. The triangular carriers have a maximum switching frequency of 1 kHz and are phase-shifted 180° to each other. All the cells were supplied by 1-kV dc voltages.

The phase and line voltages have twice the switching frequency of each cell, following the number of cells cascaded. The frequency components of these voltages obtained from Matlab simulation are shown in Fig. 7. The detailed harmonic content of the line voltage versus modulation index is shown in Fig. 8.

V. Proposed Capacitor Voltage Balancing

During normal operation, natural balancing can be achieved in each cell, keeping the midpoint capacitor voltage close to

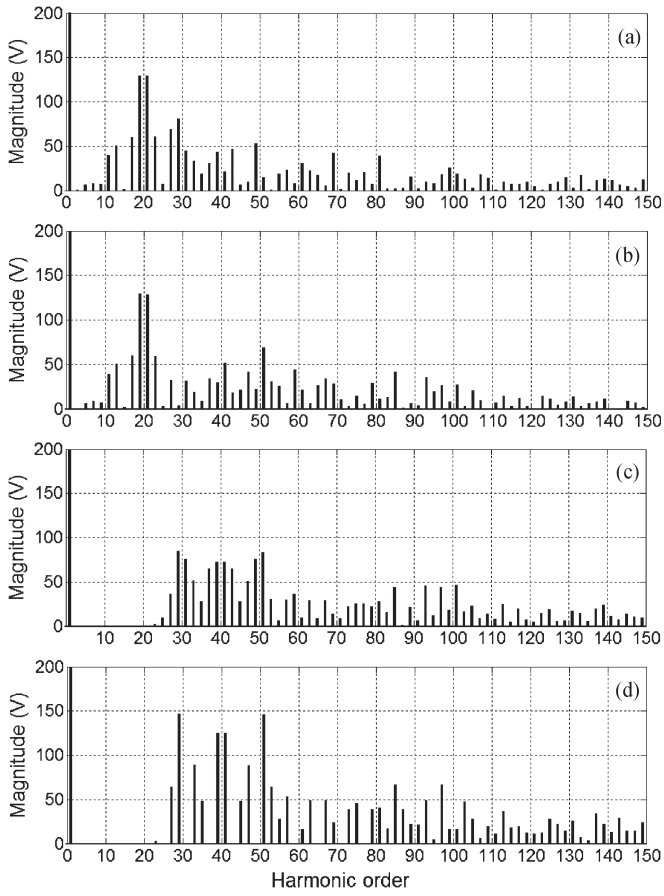

Fig. 7. Harmonic spectrum of the proposed inverter. (a) Cell 1 output voltage harmonics. (b) Cell 2 output voltage harmonics. (c) Phase voltage harmonics. (d) Line voltage harmonics.

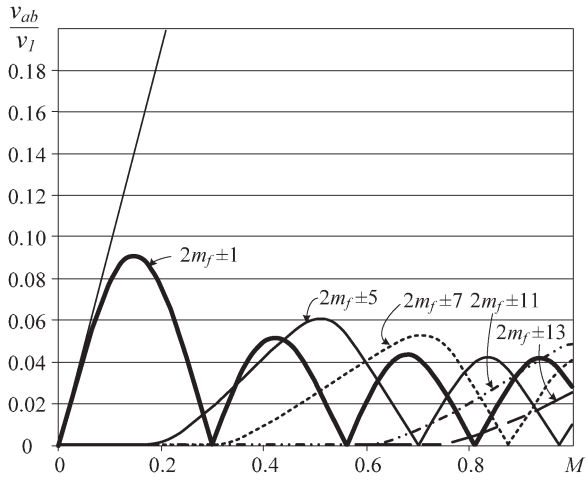

Fig. 8. Line voltage harmonics versus modulation index ($m_f = f_c/f_o$).

$(1/2)v_{\rm dc}$. However, under certain circumstances such as during a transient or sudden large disturbance, cells may become imbalanced, causing the average current drawn from the midpoints to be nonzero, therefore, shifting the midpoint capacitor voltage away from $(1/2)v_{\rm dc}$. In a worst case scenario, this may lead to system instability and cause damage to the whole system. The

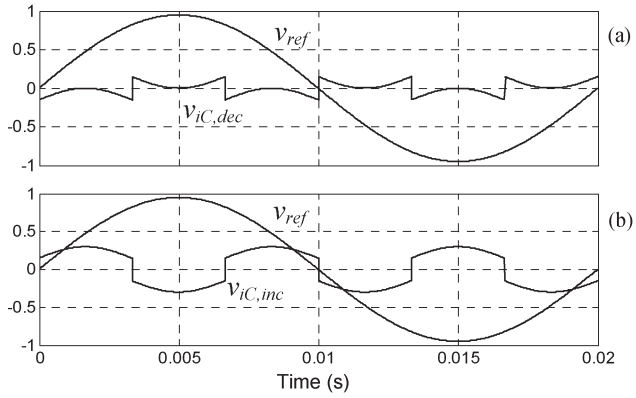

Fig. 9. Third harmonic offsets. (a) Offset voltage to decrease the midpoint capacitor current. (b) Offset voltage to increase the midpoint capacitor current.

average current, $I_{\rm avg}$ can be obtained through integration of the capacitor current over one fundamental period

$$I_{\rm avg} = \frac{1}{2\pi}\int_0^{2\pi} i_C(t)\,dt. \tag{15}$$

In order to ensure reliable and safe system operation, cell balancing control has to be incorporated [39]. In this case, switching state redundancy is not applicable since PWM modulation is used. Moreover, the absence of a bidirectional switch in the second leg of the TCHB limits the cell balancing capability under certain conditions even if the SVM modulation is used. In addition to using balancing circuitry, voltage balancing can be implemented by controlling $I_{\rm avg}$ via a third harmonic offset injection method [40]. This method uses two offset voltages, $v_{i_C,\rm dec}$ and $v_{i_C,\rm inc}$, as shown in Fig. 9(a) and (b). These offset voltages can be represented by the following equations:

$$v_{i_C,\rm dec} = \begin{cases} v_{\rm offset,pk}\sin 3\omega t \\ -v_{\rm offset,dc}, \\ v_{\rm offset,pk}\sin 3\omega t \\ +v_{\rm offset,dc}, \end{cases} \begin{array}{l} \text{if } v_{\rm offset,pk}\sin 3\omega t \geq 0 \\ \\ \text{If } v_{\rm offset,pk}\sin 3\omega t < 0 \end{array} \tag{16}$$

$$v_{i_C,\rm inc} = \begin{cases} v_{\rm offset,pk}\sin 3\omega t \\ +v_{\rm offset,dc}, \\ v_{\rm offset,pk}\sin 3\omega t \\ -v_{\rm offset,dc}, \end{cases} \begin{array}{l} \text{if } v_{\rm offset,pk}\sin 3\omega t \geq 0 \\ \\ \text{If } v_{\rm offset,pk}\sin 3\omega t < 0 \end{array} \tag{17}$$

where $v_{\rm offset,pk}$ and $v_{\rm offset,dc}$ are two variables for controlling its amplitude and dc offset. Adding any of these offsets to the voltage reference changes the duty cycle D of the midpoint capacitor current and also its amplitude

$$D = \begin{cases} 2\left(1 - abs(v_{\rm ref})\right), & \text{if } \frac{1}{2} \leq abs(v_{\rm ref}) \leq 1 \\ 2abs(v_{\rm ref}), & \text{if } 0 \leq abs(v_{\rm ref}) \leq \frac{1}{2}. \end{cases} \tag{18}$$

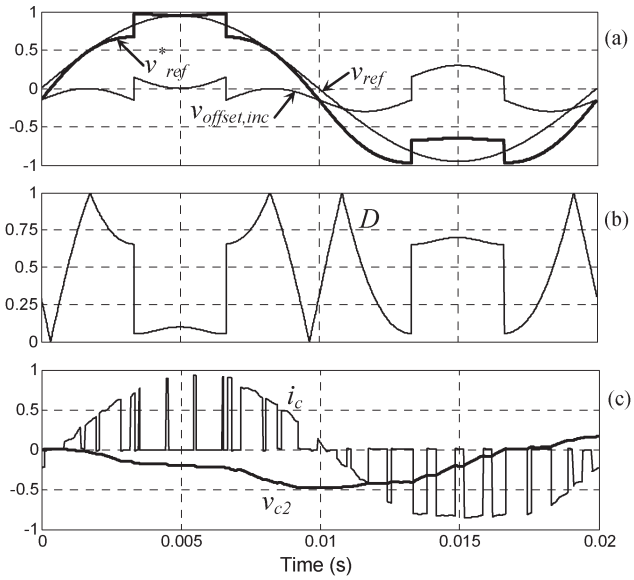

Fig. 10. (a) Proposed offset voltage to increase the midpoint capacitor voltage and the corresponding voltage reference, (b) duty cycle, (c) midpoint capacitor current and voltage.

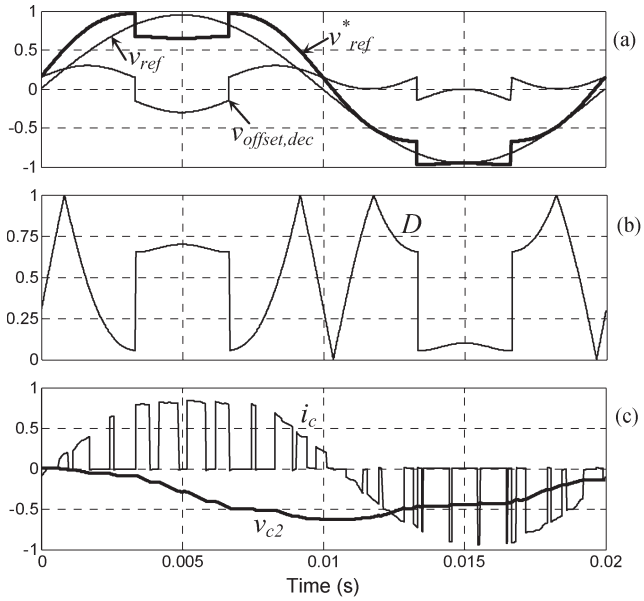

Fig. 11. (a) Proposed offset voltage to decrease the midpoint capacitor voltage and the corresponding voltage reference, (b) duty cycle, and (c) midpoint capacitor current and voltage.

Maximum D occurs when the voltage reference is 1/2 and minimum when the reference is 0 or 1. Adding the offset voltage in Fig. 9(a) forces the voltage reference away from 1/2, reducing the duty cycle and thus the midpoint capacitor current. Whereas, adding the offset voltage in Fig. 9(b) forces the reference close to 1/2 and therefore increases the midpoint capacitor current.

In each cell, to regulate the midpoint capacitor voltage, combinations of these offset voltages are used. Using only one offset voltage in one fundamental period as was done for a diode-clamped back-to-back converter in [40] is not applicable, since the capacitor current varies by the same amount in both half cycles, producing $I_{\text{avg}} \equiv 0$ and therefore resulting in no voltage balancing. Whereas, use of a different offset voltage in each half cycle of the fundamental period as proposed in this paper produces positive or negative I_{avg}, depending on the combination used. For instance, using the combination of $v_{i_C,\text{dec}}$ in the positive half cycle and $v_{i_C,\text{inc}}$ in the negative half cycle produces a negative I_{avg} so as to increase the midpoint capacitor voltage, and vice versa

$$v_{\text{offset,inc}} = \begin{cases} v_{i_C,\text{dec}} & 0 < \omega t \leq \pi \\ v_{i_C,\text{inc}} & \pi < \omega t \leq 2\pi \end{cases} \tag{19}$$

$$v_{\text{offset,dec}} = \begin{cases} v_{i_C,\text{inc}} & 0 < \omega t \leq \pi \\ v_{i_C,\text{dec}} & \pi < \omega t \leq 2\pi. \end{cases} \tag{20}$$

The effective region for controlling the midpoint capacitor current in this approach is $(1/3)\pi \leq \omega t \leq (2/3)\pi$ in the positive half cycle and $(4/3)\pi \leq \omega t \leq (5/3)\pi$ in the negative half cycle. In order to provide an efficient control of cell balancing while keeping the output distortion minimal, $v_{\text{offset,pk}}$ and $v_{\text{offset,dc}}$ are set such that the modulated voltage reference will be close to 1 when the maximum modulation index is applied. Incorporating v_{offset} for cell balancing defines the new voltage reference as

$$v^*_{\text{ref}} = M \sin \omega t + v_{\text{offset(inc or dec)}}. \tag{21}$$

Figs. 10 and 11 show the offset voltages used for both cases with their corresponding voltage references, duty cycles, and midpoint capacitor currents and voltages. From both figures, it is noted that the midpoint capacitor voltage increases or decreases after one fundamental period as a result of adding the corresponding v_{offset}.

The variation of the midpoint capacitor voltage depends on the load current applied to the inverter. For a given power, operating voltage and power factor, the load current I_L can be calculated as follows:

$$I_L = \frac{P}{\sqrt{3} V \cos\theta}. \tag{22}$$

The midpoint capacitor current i_C can be estimated by multiplying the duty cycle D with the instantaneous load current, i_L. Accordingly, this yields capacitor voltage variation as

$$\Delta v_c \approx \frac{1}{C} \int i_c \, dt = \frac{i_L}{C} D T_s = \frac{i_L D}{C f_s} \tag{23}$$

where f_s is the switching frequency, which is also equal to the carrier frequency. The duty cycle is obtained by substituting the corresponding v^*_{ref} into (18), depending on which balancing action is required, either to increase or decrease the midpoint capacitor voltage. Since PWM modulation is used, voltage

variation in each switching cycle can be obtained by rewriting (23) in discrete form as follows:

$$\Delta v_c(k) \approx \frac{i_L(k)}{C} D(k) T_s = \frac{i_L(k) D(k)}{C f_s}. \tag{24}$$

Accordingly, voltage variation in one fundamental period can be obtained from (25), where N_k is the number of switching cycle in one fundamental period defined as f_s/f_0

$$\Delta v_{c,\text{cycle}} \approx \frac{1}{C f_s} \sum_{k=1}^{N_k} i_L(k) D(k). \tag{25}$$

From (25), it is obvious that the voltage variation is directly proportional to the load current while inversely proportional to the capacitance and the switching frequency, for a fixed modulation index. It is interesting to note how the midpoint capacitor voltage varies when a different modulation index of the voltage reference is applied, keeping the same values of offset variables (i.e., $v_{\text{offset,pk}}$ and $v_{\text{offset,dc}}$ are both set to 0.15). For comparison at a different modulation index, the same amplitude of load current is used. The reason is that the new voltage reference defined using different modulation index produces a different duty cycle. As a result, different midpoint capacitor current is obtained in each case, thus indirectly evaluating the performance of the cell balancing mechanism at different loading conditions.

Fig. 12(a) shows the variation of the midpoint capacitor voltage versus modulation index for several capacitance values in one fundamental period at 1-kHz switching frequency and with a unity power factor. Relative comparison is made against the balancing condition at $M = 1$ which represents 1-MW load. This is based on the configuration shown in Fig. 2, and the result is normalized to $v_{\text{dc}} = 1$ kV. The result is applicable to both balancing conditions since the offset voltages are interchanged between the positive and negative half cycle. This means that, the result can be inferred as the amount of voltage increments or decrements, depending on the balancing condition. Fig. 12(b) shows the voltage variation at different switching frequencies; 1 kHz, 1.5 kHz, and 2 kHz when using 3400 μF capacitor. The effect of the cell balancing mechanism at different power factor is shown in Fig. 12(c) for 1-kHz switching frequency with the same capacitance. Based on the results obtained, the highest voltage variation occurs when the modulation index is 0.8. Depending on the depth of imbalance, the balancing time τ_{bal} in terms of the number of cycles required can be obtained by dividing the depth of imbalance ε normalized to v_{dc} with $\Delta v_{c,\text{cycle}}/v_{\text{dc}}$

$$\tau_{\text{bal}} = \frac{\varepsilon}{\frac{\Delta v_{c,\text{cycle}}}{v_{\text{dc}}}}. \tag{26}$$

A hysteresis controller as shown in Fig. 13 is used to realize the voltage balancing mechanism where the control is activated only when the capacitor voltage difference, Δv_C has exceeded the hysteresis band limits. When Δv_C exceeds the

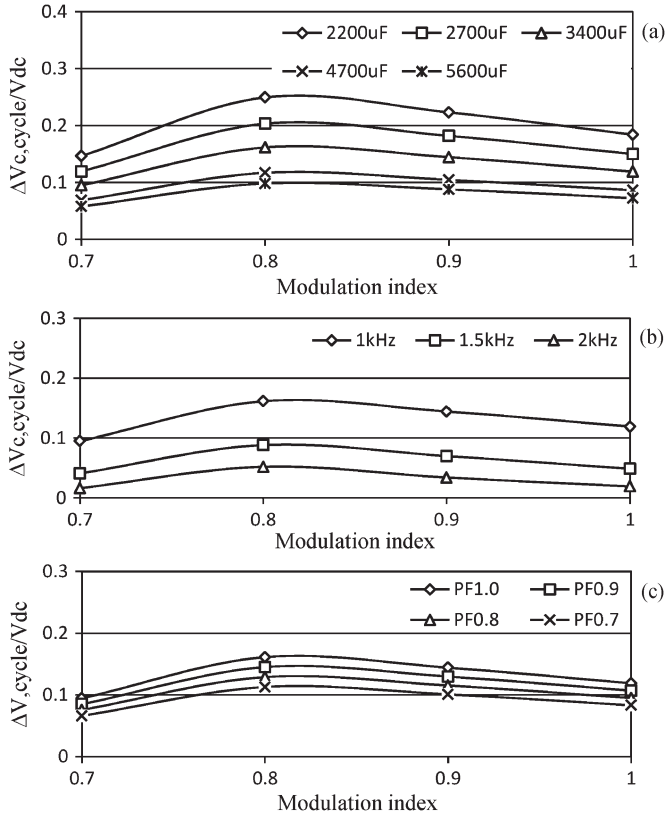

Fig. 12. Simulation results showing the variation of the midpoint capacitor voltage in one fundamental period for different (a) capacitance values, (b) switching frequencies, and (c) power factors.

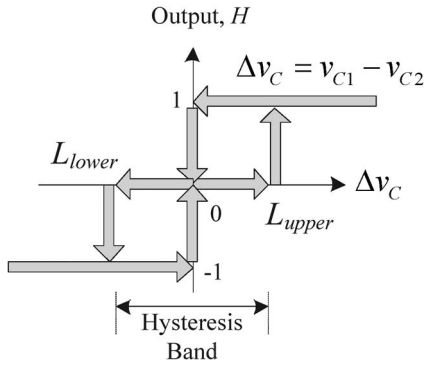

Fig. 13. Hysteresis controller for the cell balancing mechanism.

upper limit, L_{Upper} (i.e., $v_{C1} \gg v_{C2}$) the hysteresis controller sets the output $H = 1$, and therefore $v_{\text{offset,inc}}$ is added to the voltage reference to increase the midpoint capacitor voltage until $\Delta v_C = 0$, and vice versa. Under natural balancing, the midpoint capacitor voltage fluctuates within the band limits, keeping the controller setting $H = 0$, and therefore none of the offset voltages is added to the voltage reference. In summary, v^*_{ref} as the function of H is as follows:

$$v^*_{\text{ref}}(H) = \begin{cases} M \sin \omega t, & H = 0 \\ M \sin \omega t + v_{\text{offset,inc}}, & H = 1 \\ M \sin \omega t + v_{\text{offset,dec}}, & H = -1. \end{cases} \tag{27}$$

The hysteresis band is selected based on the maximum voltage drop due to maximum loading condition in the first half cycle of the fundamental period. Setting appropriate hysteresis band avoids frequent third harmonic offset injection that affects the output quality. The midpoint capacitor voltage normally decreases to a certain level in the positive half cycle and then subsequently increases in the negative half cycle. This condition occurs when the motor is in motoring mode. The opposite condition is expected when the motor is in regenerative braking mode. Evaluating (25) for half cycle, from $k = 1$ to $(1/2)N_k$, yields the minimum limit for the hysteresis band. It is noted that D is evaluated with purely sinusoidal $v_{\rm ref}$ since voltage variation under a natural balancing condition is of interest.

On the other hand, in a case where the maximum voltage drop allowed and the switching frequency are already specified, the minimum capacitance required to fulfill that condition can be obtained as

$$C_{\min} = \frac{1}{v_{\rm dc} f_s \varepsilon} \sum_{k=1}^{\frac{N_k}{2}} i_L(k) D(k). \tag{28}$$

The proposed cell balancing method is recommended for use in the typical operating region (i.e., $M = 0.7$ to 1) or at high speed to ensure that cell balancing works effectively with minimal output distortion. It is expected to work well when operated with full load current at the rated speed. However, its effectiveness might be affected when it is operated with full load current at a low speed down to zero. The reason is that voltage drop is significant at a low speed, and this forces the harmonic offset injection to work continuously, therefore degrading the output quality. Moreover, higher common-mode voltage is expected to appear in the system compared to normal operating conditions due to third harmonic offset injection. Nonetheless, this effect occurs temporarily only when the cell balancing takes place. The common-mode voltage generated by the proposed inverter is defined by (29), and it is measured between the neutral points of the load and the inverter

$$v_{\rm cm} = \frac{1}{3}(v_{aN} + v_{bN} + v_{cN}). \tag{29}$$

VI. Comparison With Other Multilevel Inverters

In order to evaluate the performance of the proposed inverter, comparison was made against the cascaded NPC with similar two-cell configuration. Comparison with cascaded NPC is made since it produces the same number of output levels per cell as that of proposed inverter. In comparison with the conventional CHB, the CHB is arranged into four-cell configuration, forming a nine-level CHB (9L-CHB) so as to produce the same output quality with the other two inverters. The comparison takes into account the output quality of the inverters, total power losses, as well as the inverter specifications. In order to indicate the improvement in output quality and the additional power loss when using power cell with five-level output instead of three-level output, a comparison with the conventional five-level CHB (5L-CHB) in two-cell configuration was made as well.

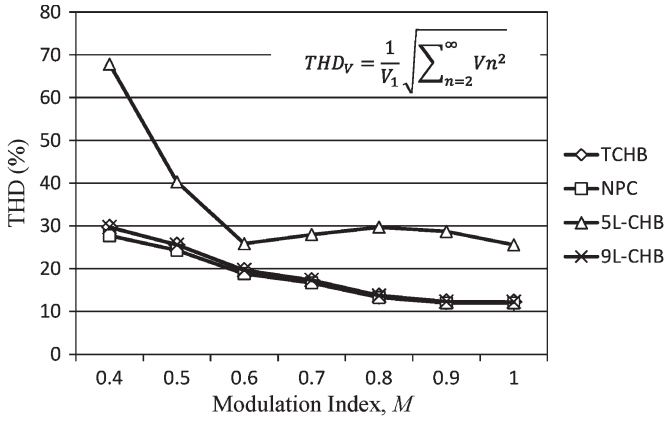

Fig. 14. Line voltage THD of the proposed inverter and other multilevel inverters.

A. Output Voltage Harmonics

Fig. 14 shows the total harmonic distortion (THD) of the line voltage for all inverters at different modulation indices. The THD of the proposed inverter, cascaded NPC, and the 9L-CHB are almost similar since they have the same output levels. However, a slight difference in THD occurs at low modulation indices particularly for the cascaded NPC as compared to the other two inverters. All the three inverters have almost linear relationship between the THD and the modulation indices, unlike the 5L-CHB which is very nonlinear. In general, the difference in THD between the three nine-level inverters and the 5L-CHB is about half, except for the modulation indices in the range of $0.5 < M < 0.7$. In the typical operating region, $0.7 < M < 1$, their THD varies from 12% to 17%, whereas for the 5L-CHB, its THD varies from 25% to 30%. The lower the THD, the lower the requirements of the output filter, thereby minimizing the overall system size.

B. Conduction and Switching Power Losses

Conduction and switching power losses of all inverters were evaluated at three operating conditions (low, medium, and high-power factor). The first operating condition is when the inverters deliver 0.75 MW at 2.3 kV, with a 0.70 lagging power factor, second is when the inverters deliver 1 MW at 2.3 kV, with a 0.80 lagging power factor and the third operating condition is when delivering 1.25 MW at 2.3 kV, with 0.90 lagging power factor. The switching frequency is the same for all inverters for a fair comparison. For this purpose, all inverters were set to produce an effective switching frequency of 2 kHz for the line voltage output.

Conduction losses of IGBT and diode can be approximated from their forward voltage drop, $V_{\rm on,IGBT}$, $V_{\rm on,D}$, and the instantaneous current $i(t)$ as

$$P_{\rm cond,IGBT} = \frac{1}{T}\int_0^T V_{\rm on,IGBT} i(t)\, dt \tag{30}$$

$$P_{{\rm cond},D} = \frac{1}{T}\int_0^T V_{{\rm on},D} i(t)\, dt. \tag{31}$$

The device forward voltage drop is normally given as a function of current and can be obtained from the device's datasheets. They can be modeled using various types of curve fits such as power function $(ax^b + c)$ and exponential function $(ae^{bx} + ce^{dx})$ [41]. In this paper, Matlab Curve Fit toolbox is used for this purpose. The curve fit selection is based on the one that best represents the corresponding function over the desired range. The type of power switches selected for power loss estimation in this case is EUPEC IGBT (BSM300GA170DLC, 1700 V/300 A). It is chosen for its suitability and the availability of the required data. Modeling through the Matlab Curve Fit toolbox yields the forward voltage drop of the IGBT and the freewheeling diode as

$$V_{\text{on,IGBT}} = 2.099e^{0.001394i(t)} - 1.507e^{-0.01467i(t)} \quad (32)$$

$$V_{\text{on},D} = 1.563e^{0.001012i(t)} - 1.041e^{-0.01189i(t)}. \quad (33)$$

Substituting (32) and (33) into (30) and (31), respectively, yields the conduction power loss of IGBT and diode as

$$P_{\text{cond,IGBT}} = \frac{1}{T}\int_0^T \left\{2.099e^{0.001394i(t)} - 1.507e^{-0.01467i(t)}\right\} i(t)\,dt \quad (34)$$

$$P_{\text{cond},D} = \frac{1}{T}\int_0^T \left\{1.563e^{0.001012i(t)} - 1.041e^{-0.01189i(t)}\right\} i(t)\,dt. \quad (35)$$

For switching power loss estimation, voltage drop across the switching device as well as the current flowing through it are sampled at each switching instant. From datasheet, switching energy loss is also given as a function of current for a certain dc-link voltage. Assuming a linear characteristic, the switching energy loss can be modeled proportional to the dc-link voltage in case if the dc-link voltage used in simulation is different from the dc-link voltage provided in the datasheet. Again, by applying the curve fitting method, the equations which represent the switching energy loss for the IGBT, $E_{\text{on,IGBT}}$ and $E_{\text{off,IGBT}}$, and the reverse recovery energy loss during turn-off, $E_{\text{off},D}$ for the diode are obtained as

$$E_{\text{on,IGBT}} = 47.83e^{0.003599i(t)} - 44.79e^{-0.004557i(t)} \quad (36)$$

$$E_{\text{off,IGBT}} = 0.552i(t)^{0.9023} - 0.2783 \quad (37)$$

$$E_{\text{off},D} = 82.99e^{-0.0004465i(t)} - 81.62e^{-0.007217i(t)}. \quad (38)$$

Therefore, switching power losses for the IGBT, $P_{\text{on,IGBT}}$ and $P_{\text{off,IGBT}}$, and turn-off power loss, $P_{\text{off},D}$, for the diode can be obtained by

$$P_{\text{on,IGBT}} = \frac{1}{T}E_{\text{on,IGBT}} = \frac{1}{T}\left\{47.83e^{0.003599i(t)} - 44.79e^{-0.004557i(t)}\right\} \quad (39)$$

$$P_{\text{off,IGBT}} = \frac{1}{T}E_{\text{off,IGBT}} = \frac{1}{T}\left\{0.552i(t)^{0.9023} - 0.2783\right\} \quad (40)$$

$$P_{\text{off},D} = \frac{1}{T}E_{\text{off},D} = \frac{1}{T}\left\{82.99e^{-0.0004465i(t)} - 81.62e^{-0.007217i(t)}\right\}. \quad (41)$$

The bidirectional switch diodes for the proposed inverter and the clamping diodes for the cascaded NPC are assumed to have similar characteristics with the IGBT free-wheeling diodes, and therefore the same equation is applied to estimate its power loss. Since the total power losses and the total output power are known, the inverter's efficiency can be obtained by

$$\text{Efficiency}(\%) = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100\%. \quad (42)$$

Among the three nine-level inverters, at $PF = 0.9$, the highest power loss occurs in the 9L-CHB, followed by the cascaded NPC, and finally the proposed TCHB inverter as shown in Fig. 15(a). As expected, the 5L-CHB has the lowest power loss due to the least component count. Nevertheless, the total power losses of both the cascaded NPC and the 9L-CHB are almost similar at the other two operating conditions. To obtain nine-level output, the proposed inverter requires only 25% additional power switches compared to 5L-CHB, whereas for both cascaded NPC and 9L-CHB, 100%. The blocking voltage of each power switches in the cascaded NPC and 9L-CHB is relatively lower as compared to the proposed inverter due to its component arrangements. For this reason, the switching power losses of both inverters are also lower. However, the conduction power loss depends on the current that flows through power switches. The more power switches are used, the more conduction power loss will be, as experienced by both cascaded NPC and 9L-CHB inverters having four times the number of power switches of the proposed inverter.

The inverters' efficiencies at the corresponding three power factors are shown in Fig. 15(b). As the power factor increases, the efficiency of the inverters also increases as a result of more real power being effectively transferred with respect to the power loss. From the figure, the inverters' efficiencies are found having an almost linear relationship with power factors. Considering a typical operating power factor of an electric motors,

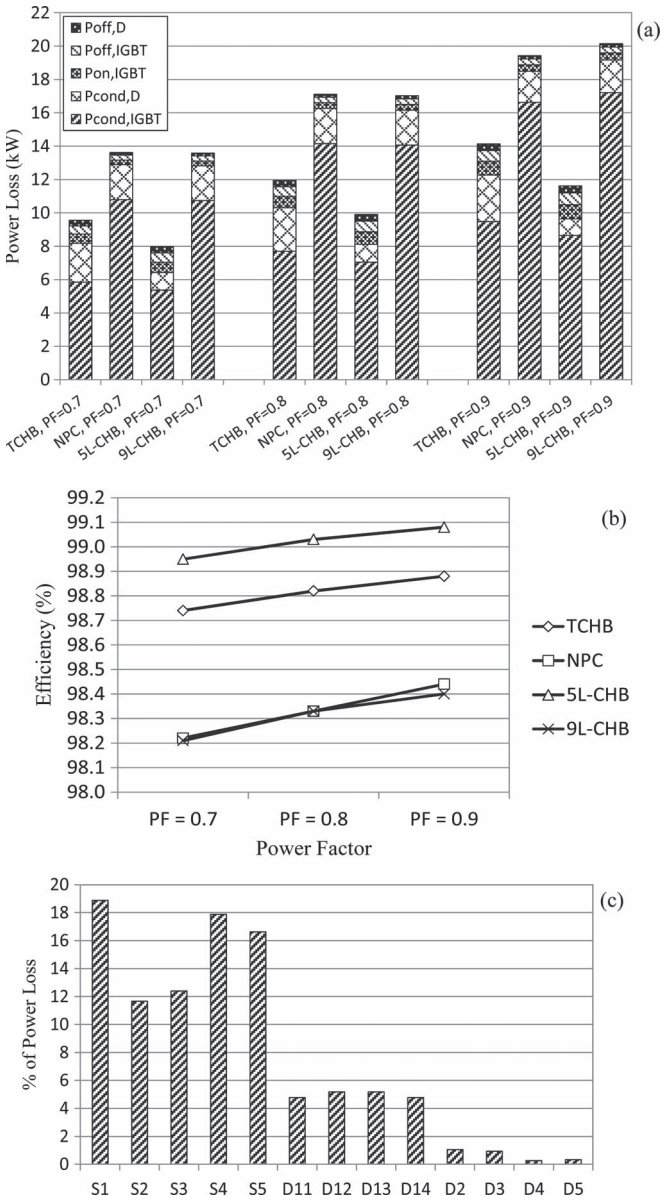

Fig. 15. (a) Comparison of total power losses at different power factors, (b) comparison of the inverters' efficiencies, and (c) detailed power loss distribution among the switching devices in each power cell.

$PF = 0.8$ for comparison, the inverter's efficiency when using the 5L-CHB is 99.03%, the proposed inverter, 98.83%, and for the cascaded NPC and the 9L-CHB, they are both 98.33%. The efficiency's difference for the proposed inverter with respect to 5L-CHB is 0.2% while with the rest is 0.5%. Independent of the accuracy of absolute losses, a relative comparison is valid since the same model is used.

Fig. 15(c) shows the percentage power loss distribution among the switching devices in each power cell based on the average power switches' losses in one phase at $PF = 0.9$. Note that S_2–D_2, S_3–D_3, S_4–D_4, and S_5–D_5 are pairs that reside in one package. Diodes D_{11}, D_{12}, D_{13}, and D_{14} exist either in a discrete form or in a full-bridge package. This information is required in designing the appropriate heat sink as power losses among the devices are not symmetrically distributed. The highest conduction loss occurs in S_1 with 18.88%, followed by S_4 and S_5 with 17.88% and 16.64%, respectively. Next, S_3 and S_2 consume 12.40% and 11.67%, respectively. Bidirectional switch diodes (D_{11}, D_{12}, D_{13}, and D_{14}) contribute to 19.94% of the total losses. This is then followed by D_2 1.04%, D_3 0.94%, D_5 0.34%, and finally D_4 0.27%.

A reduction in conduction power losses for TCHB is possible by using a bidirectional switch topology with two IGBTs connected with in common-emitter configuration [12]. In both directions, the current flows through one IGBT and one diode, rather than one IGBT and two diodes as in the presented configuration. Therefore, lower conduction losses can be achieved with increase in control complexity.

TABLE III
COMPARISON BETWEEN THE PROPOSED INVERTER AND THE OTHER MULTILEVEL INVERTERS

Parameter	*Proposed Inverter*	*Cascaded NPC*	*n_pL-CHB*	*(2n_p-1)L-CHB*
Phase voltage levels	2n_p-1	2n_p-1	n_p	2n_p-1
Line voltage levels	4n_p-3	4n_p-3	2n_p-1	4n_p-3
Power cells per phase	½(n_p-1)	½(n_p-1)	½(n_p-1)	n_p-1
Power switches per phase	2½ (n_p-1)	4(n_p-1)	2(n_p-1)	4(n_p-1)
Bi-directional switch -diodes / phase	2(n_p-1)	-	-	-
Clamping diodes	-	2(n_p-1)	-	-
Capacitors per phase	n_p-1	n_p-1	½(n_p-1)	n_p-1
Isolated dc source per phase	½(n_p-1)	½(n_p-1)	½(n_p-1)	n_p-1
Power per cell	2P$_{nom}$/ (3(n_p-1))	2P$_{nom}$/ (3(n_p-1))	2P$_{nom}$/ (3(n_p-1))	P$_{nom}$/ (3(n_p-1))
Voltage measurement transducers per phase	n_p-1	n_p-1	½(n_p-1)	n_p-1
Maximum voltage	1 *pu*	1 *pu*	1 *pu*	1 *pu*
Modulation method	CPS-PWM	CPS-PWM	CPS-PWM	CPS-PWM
Load voltage THD	Low	Low	High	Low
Efficiency	Medium	Low	High	Low
Output quality	High	High	Low	High

C. Inverter Specifications

The inverter specifications comparing the proposed inverter with the corresponding three inverters are given in Table III. The specifications are formulated in terms of the number of phase voltage levels n_p of the conventional CHB. Since a minimum cascaded configuration requires two cells, therefore n_p counts from five levels onwards. The comparison includes the number of output levels, power switches, diodes, capacitors, isolated dc sources, and the power rating for each cell. The maximum voltage supported for all inverters is the same and so is the modulation method. For better output quality, use of the proposed inverter is better compared to the cascaded NPC and 9L-CHB with regard to the total power losses. The requirements for isolated dc power supply and voltage balancing for the proposed inverter and the cascaded NPC are the same, but the advantage of the proposed inverter is that it has lower total power losses. The use of 9L-CHB on the other hand though requires no voltage balancing, but it requires more isolated dc power supply by means of more transformers and therefore creates higher power losses as a whole.

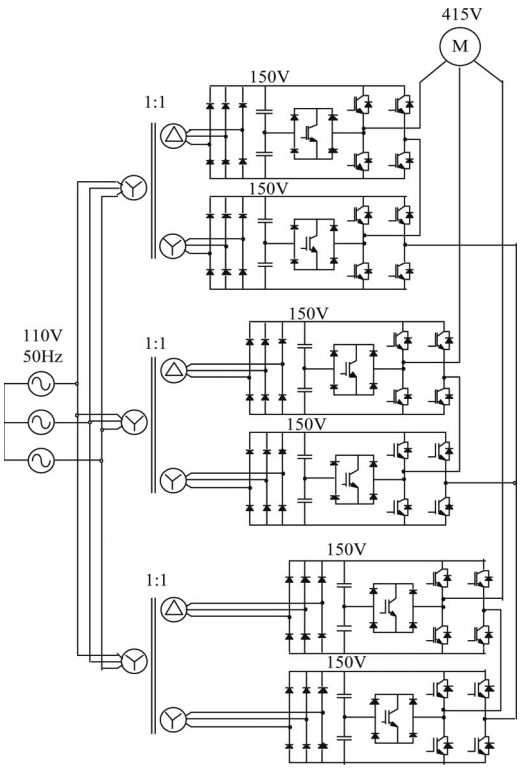

Fig. 16. Scaled-down prototype.

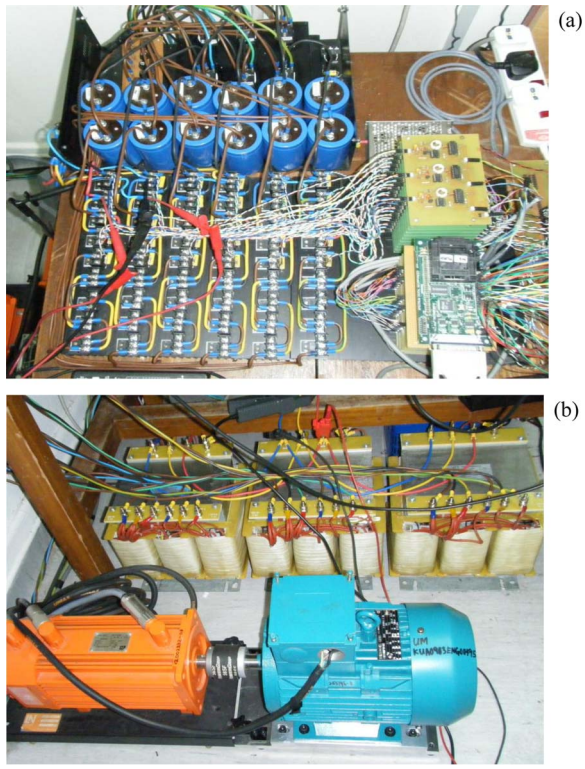

Fig. 17. Hardware implementation: (a) the proposed inverter prototype and (b) phase-shifting transformers, induction motor load, and servo brake system.

VII. Experimental Verification

For verification, experimental tests were carried out where the scaled-down system shown in Fig. 16 used the inverter and load in Fig. 17(a) and (b), respectively. A TMS320F2812 DSP was used to generate the PWM signals and to implement the cell balancing mechanism. The inverter was supplied by a three-phase ac power supply through phase-shifting transformers. Each phase-shifting transformer provided two isolated dc sources with approximately 150-V dc voltage for the upper and the lower power cells. The modulation index was set to $M = 0.95$. The specification of each cell is given in Table IV. Of the 30 IGBTs, six form the bidirectional switches. There are 12 dc capacitors, 24 diodes, six full-bridge rectifiers, and three phase-shifting transformers.

Fig. 18(a) shows the measured output voltage of phase a for each cell and the phase-to-neutral voltage, indicating uniform power distribution between the cells. A nine-level output was produced when the cells were cascaded in series. Full load line voltage and three-phase currents are shown in Fig. 18(b) and (c), respectively. In the line voltage, 17 levels were produced, thus providing high output quality. The output power measured was 1 kW, RMS voltage 355.9 V, RMS current 1.75 A, and frequency 50 Hz. Fig. 18(d) shows the main input current resembles a sinusoidal form as a result of using 12-pulse rectifier and phase-shifting transformer. The phase voltage and line voltage harmonics are shown in Fig. 19(a) and (b), respectively. The details of line voltage harmonics measured up to 50th harmonic order, a maximum order that can be measured using a Fluke 43B Power Analyzer, are shown in Fig. 19(c) with THD $= 9.7\%$. The harmonics were found to be approximately similar with those obtained in Fig. 5, thus validating the results.

TABLE IV
Specification of Each Power Cell for the Scaled-Down Prototype

DC bus voltage, v_{dc}	150 V
Fundamental frequency, f_0	50 Hz
Carrier frequency, f_c	1 kHz
IGBT, S_1-S_5	IRG4PH50UDPBF, 24A, 1200V
Capacitor, C_1-C_2	3400uF, 200V
Diode, D_{11}-D_{14}	30CPF12PBF, 30A, 1200V

In general, the effect of capacitor voltage imbalance in each cell is minimal for fixed frequency motor drive application. Fig. 20(a) shows the midpoint capacitor current i_C and the respective voltages, v_{C1} and v_{C2}, for Cell 1 in a full load constant-speed motor drive condition. The capacitor voltages balance (i.e., close to $(1/2)v_{\rm dc}$) under normal conditions, indicating that $I_{\rm avg}$ from the midpoint node is approximately zero, by means of natural balancing. A case where Cell 1 at first is unbalanced at t_0 and then after applying the voltage balancing mechanism discussed at t_1 gives the result shown in Fig. 20(b). Cell 2 with balancing control balances both capacitor voltages in spite of the Cell 1 initiated imbalanced, therefore validating the balancing mechanism. Another case where the balancing control of Cell 2 disabled is shown in Fig. 20(c). The tests were performed at partially loaded condition where both $v_{\rm offset,pk}$ and $v_{\rm offset,dc}$ were set to 0.15.

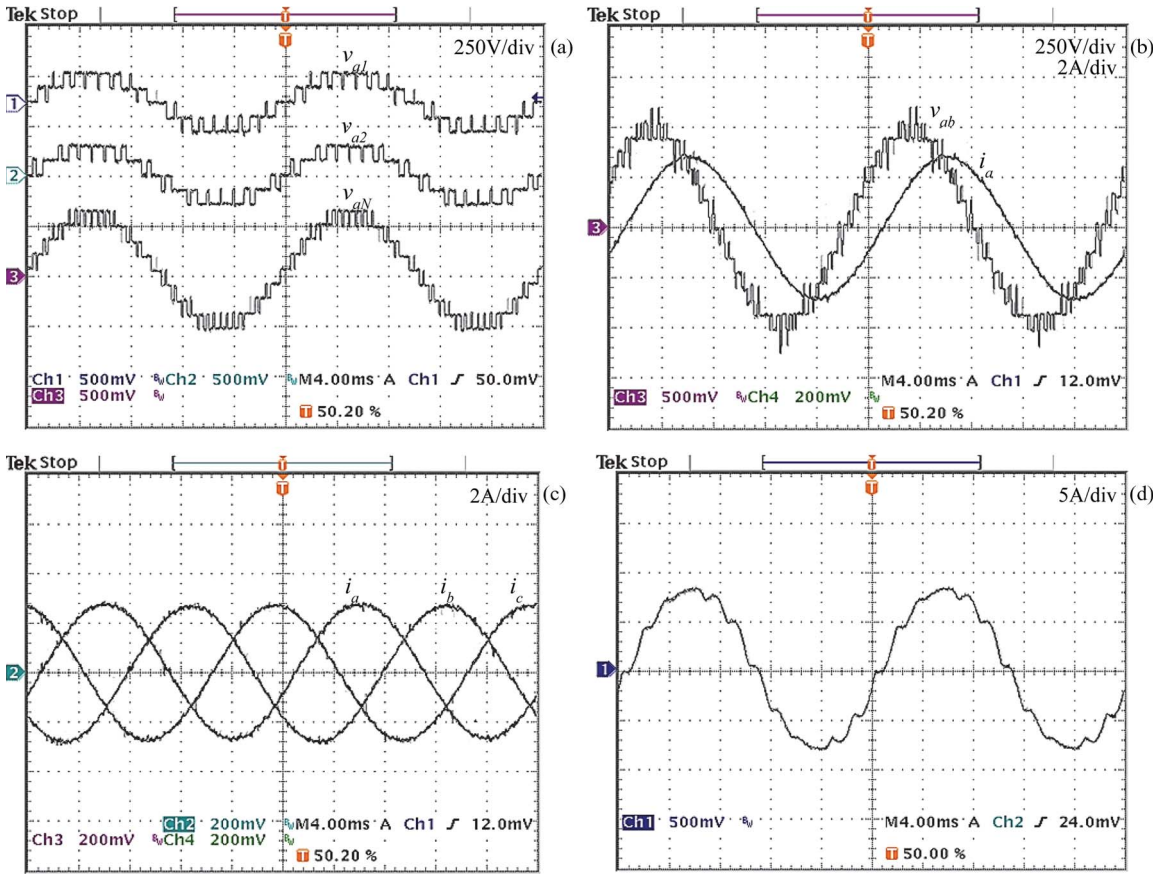

Fig. 18. Experimental results showing (a) each cell voltage and inverter phase voltage, (b) line voltage and current, (c) three-phase load current, and (d) main input current.

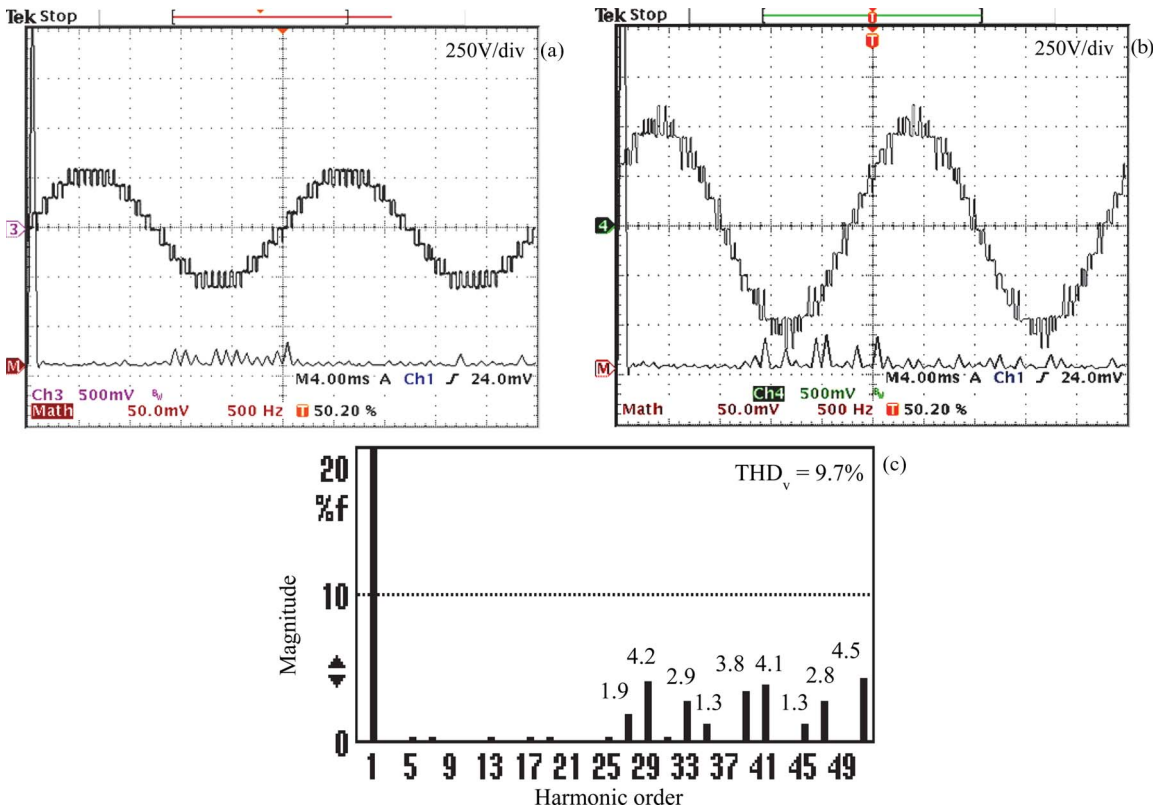

Fig. 19. Experimental results showing (a) phase voltage harmonics, (b) line voltage harmonics, and (c) detailed line voltage harmonics with its THD value.

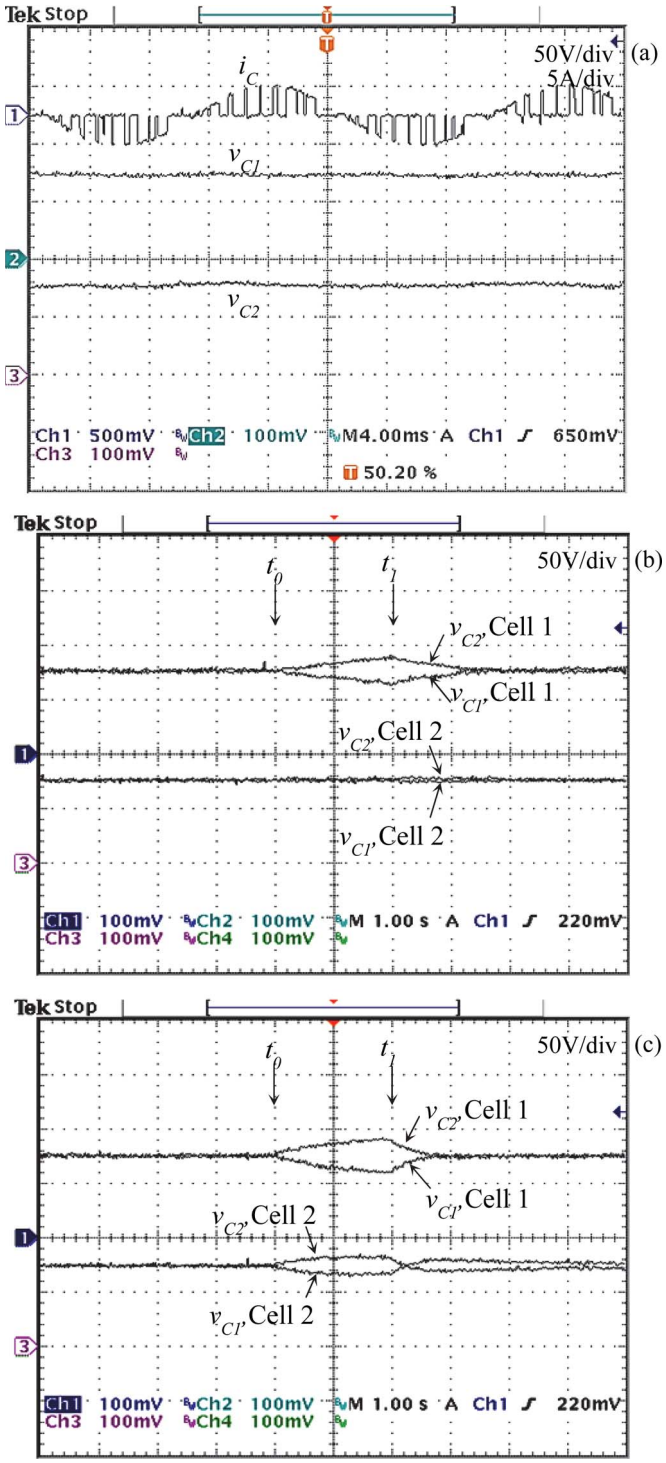

Fig. 20. Experimental results showing (a) midpoint capacitor current and voltages of Cell 1, (b) capacitor voltage balancing of Cell 2 enabled, and (c) capacitor voltage balancing of Cell 2 disabled.

VIII. Conclusion

In this paper, a cascaded multilevel inverter configuration based on a five-level TCHB power cell with multicarrier phase-shifted PWM modulation method, is presented. A new method to balance the midpoint capacitor voltage in each cell based on third harmonic offset injection was developed and tested. The output voltages of the proposed inverter were presented in a double Fourier integral form to determine their harmonics at various operating conditions. Detailed comparisons between the proposed inverter, cascaded NPC, 5L-CHB, and 9L-CHB in terms of power quality, power losses and inverter specifications were presented. From the findings, the proposed inverter is found potential not only for medium-voltage drive application but also other applications demanding higher output quality.

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