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A new three-level current-source PWM inverter and its application for grid connected power conditioner

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ABSTRACT

This paper presents a novel topology of a three-level current-source PWM inverter totally driven by using single gate-drive power supply used for a grid connected inverter. The great feature of the proposed inverter circuit is that all of the power switches are connected on common-source or common-emitter configuration. Using this common-source current-source inverter (CS–CSI) the number of gate-drive power supply can dramatically be reduced into only a single power source without using bootstrap technique or many isolated power supplies. Operation of the proposed new inverter was tested by using computer simulation and experimentally. The simulation and experimental results proved that the inverter works properly generate a three-level output current waveform and inject a sinusoidal current into power grid with unity power factor operation. During grid connected operation, almost all harmonic orders are suppressed by using an additional harmonic suppression technique.

1. Introduction

Recently, with the continuing increase of oil price and other fossil fuel, the distributed renewable power generation such as wind energy, fuel cell and photovoltaic are becoming more and more interesting from the environmental issue and energy conservation point of view [1,3,6,10]. The renewable energy sources such as photovoltaic (PV) solar energy becomes a very interesting alternative to supplement the generation of electricity, among green power sources because it can be utilized either at remote regions as stand alone apparatus or at urban application as grid interactive power source [13].

However, not many PV systems have so far been connected into the power grid due to the problems such as the relatively high cost of power converter and photovoltaic module, system complexity e.g. the need of transformer in connection system [5,8,9,15]. But, with the advanced technology in material technology of the solar cell, it leads to the solar panel becoming cheaper, thereby, a reduction of cost per inverter watt and system complexity are important matter to make PV generator system more attractive and become widely used.

1.1. Voltage-source and current-source inverter

Basically, there two major converter topologies used for energy converter are voltage-source inverter (VSI) and its dual, the current-source inverter (CSI) [4]. Voltage source inverter works converting the DC input voltage into AC output voltage waveform. The power source can be PV arrays, fuel cell, rectifier or battery. In a voltage source converter, the DC port is the capacitive port and voltage stiff (i.e. a large DC bus capacitor). The voltages in such a converter are well defined by this port and are generally considered independent of the converter operation. To protect the VSI circuit from short circuit caused by switching patterns of inverter switches, a dead time is needed in the circuit design of their gating signals.

In case of CSI, the converter converts the DC current-source into AC output current waveform. The DC port is inductive and current stiff. The current in this port is well defined and slow to change. The voltage (particularly at the AC port) is considered the variable directly controlled by the converter modulation [2,7]. Since the AC port usually has significant line or load inductance, line to line capacitors must be placed on the AC port. In contrast with VSI, for CSI, it is necessary to add an over-lap time in the gating signals.

A common problem in a CSI is related with its higher losses compared with VSI. The losses mainly come from the inductor used to generate current-source. But, with the advanced technology in material such as superconductor material, this problem will can be overcome in the near future.

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Currently interested topic is multilevel inverter topology (three-level and more) with output voltage or current [7,12,16]. The three-level converter both of CSI and VSI can offer substantial benefit for higher power applications compared to two-level inverter, including reduced harmonics contents of its output current/voltage. Fig. 1 presents a neutral point clamped (NPC) three-level VSI used as PV power conditioner for grid interface application. The PV arrays act as DC power source. The capacitors are used to synthesize three-level output voltage by controlling the switching state (ON and OFF) of the power switches Q1, Q2, Q3 and Q4 [20].

There are some limitations of using this circuit configuration such as dv/dt problem for high voltage and high switching frequency application [12]. It needs some isolated DC power supplies for its drive circuit or capacitors if bootstrap circuit is used. The capacitor size usually is very large in size, so it will need electrolytic capacitor whose life time is very limited.

1.2. Harmonics distortion in grid connected inverter

The quality of the inverter output current can be indicated by calculating its total harmonic distortion (THD) as follow

$$\mathrm{THD}(\%) = 100\sqrt{\left(\frac{i_2^2}{i_1^2}\right) + \left(\frac{i_3^2}{i_1^2}\right) + \cdots + \left(\frac{i_n^2}{i_1^2}\right)} \quad (1)$$

where $i_2, i_3, \ldots, i_n$ are the harmonic components of the output current and i_1 is the fundamental component of the output current.

Harmonic distortion in a grid connected inverter can be divided into low-order and high-order harmonic regions of the frequency spectrum [1,19]. High-order harmonic distortion is primarily associated with the inverter switching frequency harmonics. The widely used uni-polar pulse-width modulation (PWM), with its effective doubling of the switching frequency, pushes the lowest harmonics (in the idealized case) to sidebands grouped around twice the switching frequency. Provided the switching frequency is high enough, the attenuation of these high-order harmonics occurs naturally as a consequence of the filtering effect of the predominantly inductive power grid. For other high-order harmonics, passive output filters are a cost-effective means of suppressing inverter-generated distortion, whether arising from grid voltage distortion or from control loop deficiencies.

Low-order harmonics, on the other hand, are not attenuated by the natural filtering effect of the grid inductance and require bulky and costly output filters for their removal if a conventional passive filter is employed. It is thus common to rely on the inverter current control loop to reduce low-order harmonics to an acceptable level [1]. Low-order harmonic distortion of the actual current can occur as a result of both intrinsic and extrinsic effects.

Distortion generated intrinsically arises mainly from deficiencies in the inverter control loop, which result in an error between the sinusoidal reference and the actual inverter output. Some of the contributors to intrinsic low-order harmonic distortion are: (1) non-linear effects due device volt drops; (2) limited PWM resolution; (3) finite loop time; (4) finite loop gain; (5) lack of stiffness in the dc link resulting in excessive current ripple. Extrinsic sources of low-order harmonic distortion include the effects of connection to a weak and distorted grid. Here, the distorted grid voltage acts as an external disturbance, impeding the control task and resulting in a distorted output current [14].

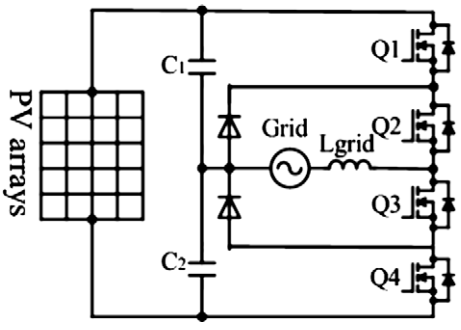


Fig. 1. Three-level VSI for grid-connected PV system.

To address some problems in three-level NPC inverter circuit and in application of grid connected inverter system, especially for further practical, longer lifetime requirement, a new and innovative power converter circuit is proposed in this research.

2. Proposed three-level current-source inverter

2.1. Duality of three-level power converter

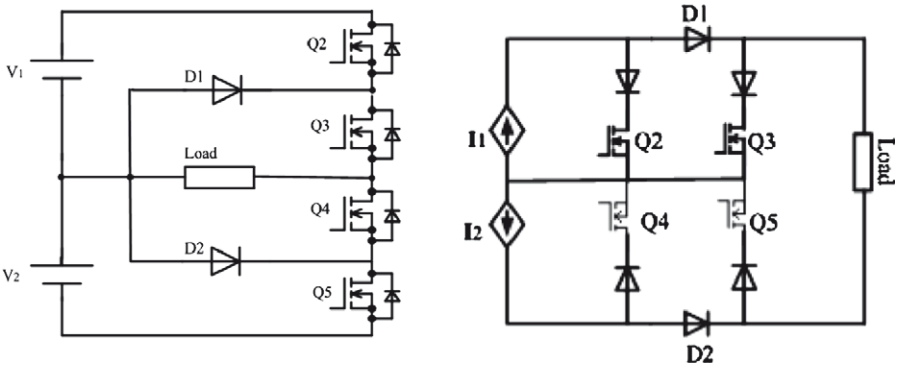
It is well known that an electrical network can be transformed to its dual equivalent [17,18]. Fig. 2a shows a NPC three-level VSI circuit. This power converter works generating a three-level output voltage waveform. Applying theory of circuit duality to this power converter, a current-source three-level power converter can be derived as shown in Fig. 2b. The DC voltage-sources, the parallel-connected diodes and transistors, and the inductive load are replaced with DC current-sources, series-connected diodes and transistors, and a capacitive load, respectively. In addition, operation modes of the current-source three-level power converter can easily be obtained by replacing 1: ON, 0: OFF and v with 0, 1 and i. The most significant feature of this new current-source three-level power converter is that all of the switching devices never require electrically isolated gate-drive power supply because their emitters (sources) are connected on an exactly identical potential level. In other words, this power converter is inherently and completely free from a violent potential change.

2.2. Three-level CSI with current generator circuit

The DC current-sources of inverter are derived by using buck chopper circuit as shown in Fig. 3. This current will be the input of the PWM inverter circuit. Blocking diodes are placed between the input inductors and the negative terminal of DC power source in order to prevent the current not flow back during positive and negative cycles. For analysis purpose of the buck chopper circuitry, we can consider this circuit comprises two buck choppers with common switch (Q1). The chopper behaves as current-source where during positive and negative cycle, a part of the input inductor current I_{Lin} will flow through blocking diode (I_d) during the switch Q1 ON and the remain current (I_L) will flow into the inverter during the switch Q1 OFF. The energy is stored as magnetic field in the input inductor during the switch Q1 ON, and when the chopper switch Q1 is OFF, during (1-DT), the stored energy in the input inductor is discharged to the load via the inverter as a pulse-width modulation (PWM) current, where D is the duty cycle of chopper. A low pass filter (Cf, Lf, Rf) is added to filter the PWM inverter output current to be a sinusoidal output current waveform. The operation modes of chopper circuit are shown in Fig. 4.

The input inductor current (I_{Lin}), gating signal (V_{gate}) of chopper's switch Q1 and current flowing into inverter (I_L) are shown in Fig. 5, with the assumption that the current rises and falls linearly. In fact, the current varies dependence on the time constant of circuit, but generally this time constant is much higher than the switching period [11].

A current control mode is applied to control the output current of chopper and inverter simultaneously. Making the input inductor current and the amplitude of output current Ipwm follows the



(a) Three-level NPC VSI (b) New three-level CSI

Fig. 2. Three-level NPC inverter (a), and its dual circuit (b).

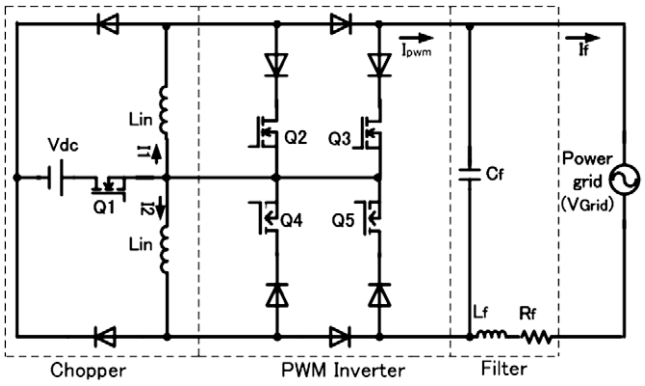


Fig. 3. Three-level CSI with current generator circuit.

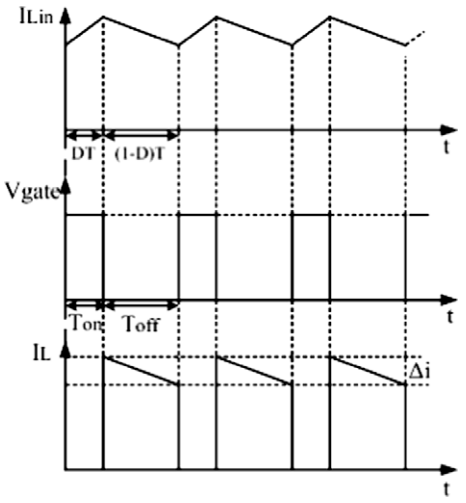


Fig. 5. Operation waveforms of chopper circuit.

reference current Iref is the objective of this current controller. The switching gate signals of switch Q1 (dc-to-dc switch) is generated by comparing the error signal of the average value of detected current flowing through both input inductors I1 and I2, and a triangular carrier wave after passing through a proportional integral regulator (PI). This signal is used to control the duty cycle of chopper to get balanced input inductors currents I1 and I2.

In order to avoid uncontrolled state of the output current by modulation signal during the ON-state of the switch Q1, the switching time between switch Q1 and the inverter switches (Q2, Q3, Q4, Q5) must be synchronized as shown in its current controller diagram in Fig. 6.

2.3. Inverter circuit and modulation strategy

The inverter circuit comprises of four switches (Q2, Q3, Q4, Q5) with all are connected on common-emitter and six diodes. I1 and I2 represent the steady state input inductor currents. The diodes connected in series with switching devices are used to protect them from transient voltage due to load current switching.

In this inverter circuit, the gating signals of the inverter switches are generated by using a sinusoidal reference wave modulated with two triangular carrier waves with the same frequency but with opposite offset value. This strategy is able to perform the sinusoidal PWM of the inverter as shown in Fig. 7. These signal patterns are used to control the inverter switches Q2, Q3, Q4 and Q5. The frequency of the reference signal determines the output current frequency of the inverter and its magnitude control the amplitude of the fundamental current component. In this circuit, a

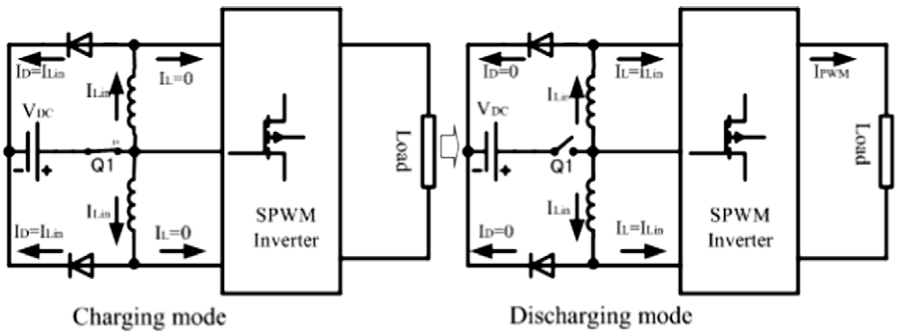


Fig. 4. Operation modes of chopper circuit.

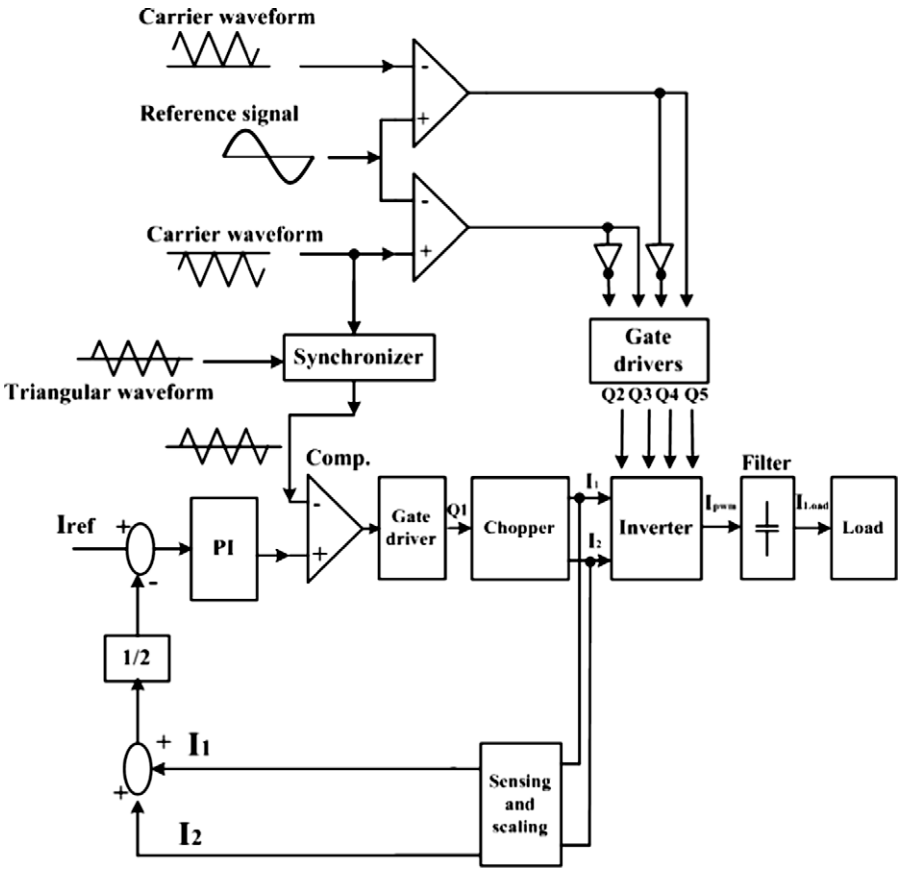


Fig. 6. Current controller block diagram of inverter.

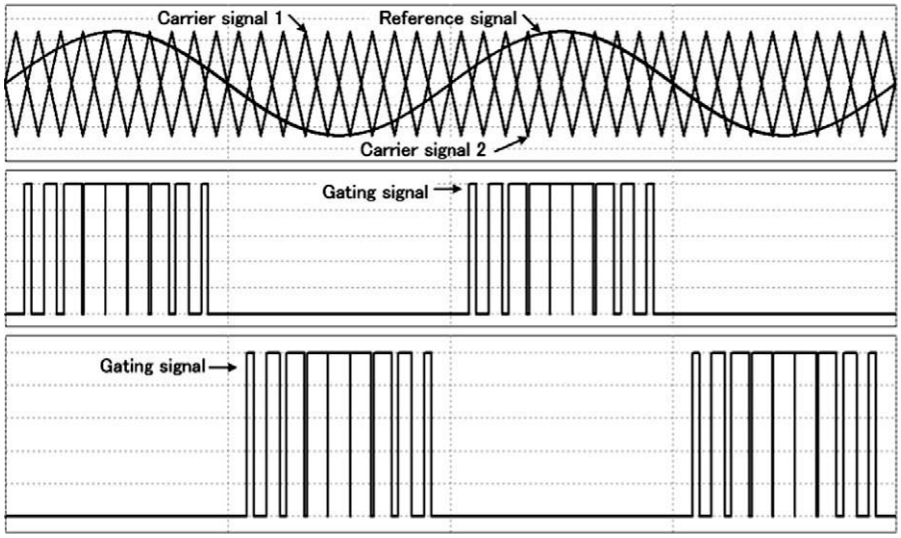


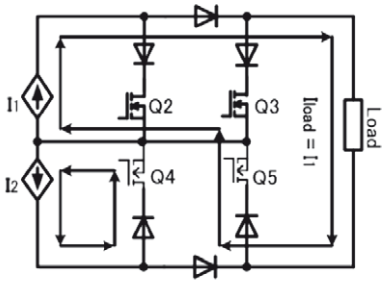
Fig. 7. Sinusoidal PWM for gating signals generation of three-level CSI.

reference signal frequency, 50 Hz, is used to meet Japanese electric frequency.

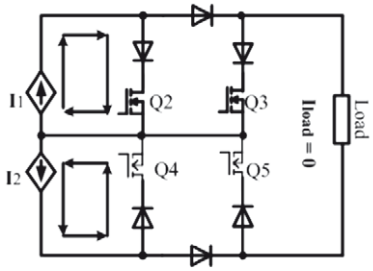
The current paths and switching combinations required to generate this three-level current are presented in Fig. 8a–c. The required three-level output current (positive, zero and negative levels) are generated as follows:

(1) Positive level current: Q5 is ON, connecting the input inductor current (I1) to the load. Q4 is ON, making the current path for input inductor current (I2). Switches Q2 and Q3 are OFF.
(2) Zero level current: Q2 and Q4 are ON, making the current path for current I1 and I2, respectively. Switches Q3 and Q5 are OFF.
(3) Negative level current: Q3 is ON, connecting the current I2 to the load. Q2 is ON, making the current path for input inductor current (I1). Switches Q4 and Q5 are OFF.

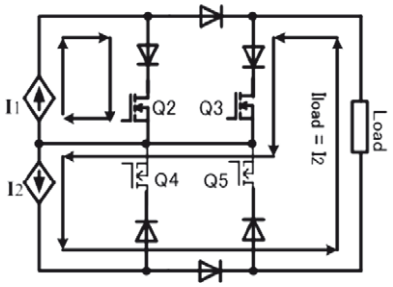
The switch states of the three-level current-source inverter are summarized in Table 1.



(a) Switching combination required to generate positive-level current



(b) Switching combination required to generate zero-level current



(c) Switching combination required to generate negative-level current

Fig. 8. Operation modes of proposed three-level CSI.

Table 1
Switch states of three-level CSI.

Output current	Switching state			
	Q2	Q3	Q4	Q5
Positive level (+)	0	0	1	1
Zero level (0)	1	0	1	0
Negative level (−)	1	1	0	0

Table 2
Circuit parameters.

Component	Type or value
Input voltage	DC 120 V
Input inductor	100 mH
Chopper switching frequency	10 kHz
Inverter switching frequency	30 kHz
Filter	Cf = 5 μF, Lf = 870 μH, Rf = 2 Ω
Load	R 5.5 Ω, L 3.4 mH
Modulation Index	0.9
Power grid	AC 70 V

3. Simulation results

This section describes the simulation results of the proposed three-level common-source CSI. The simulation parameters are shown in Table 2. In this simulation, the energy source was represented by a DC voltage source and the inverter was connected to AC power grid via a low pass filter (Cf, Lf, Rf). The input inductor values were chosen as 100 mH to get smooth enough input inductor current I1 and I2.

Fig. 9 shows the three-level and load current waveforms when the inverter is connected with an inductive load. Fig. 10 shows the

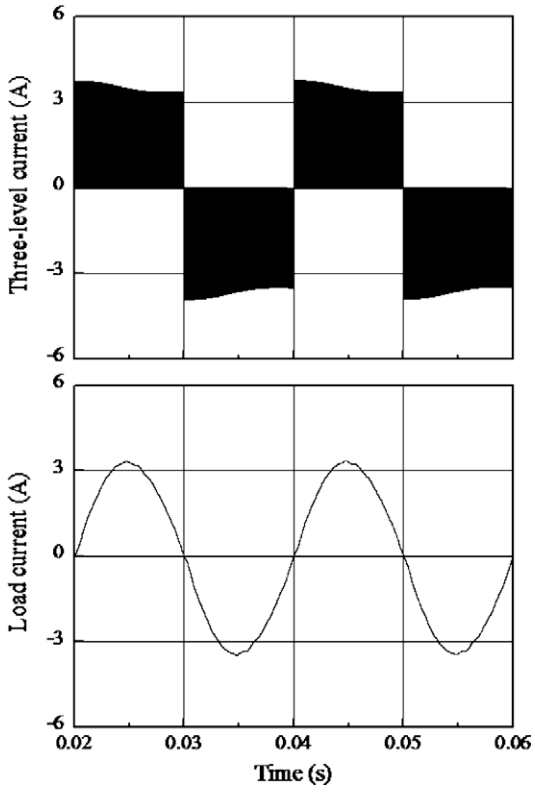


Fig. 9. Three-level and load current waveforms.

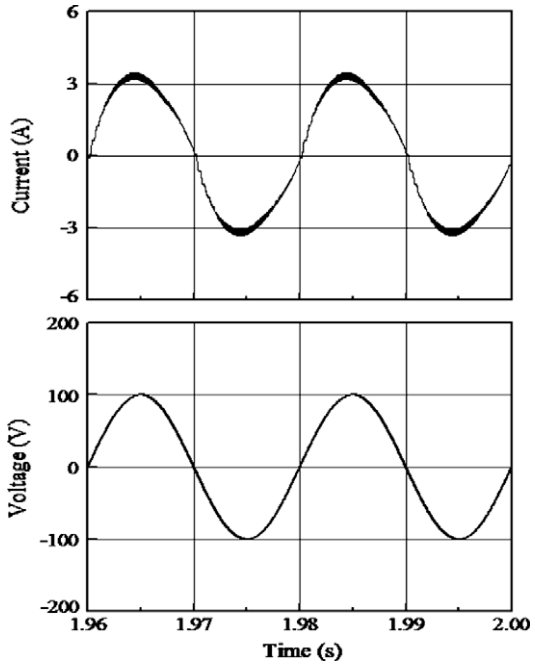


Fig. 10. Inverter output current and grid voltage waveforms.

inverter output current and the voltage of power grid during grid connected operation of the inverter. The inverter injects a sinusoidal output current into the power grid. From this figure, we can see the phase relationship between inverter output current and grid voltage. The inverter works properly injecting a sinusoidal output current with unity power factor operation. Fig. 11 shows the fast Fourier transforms (FFT) analysis presenting harmonic profile of the inverter output current during grid connected operation.

4. Experimental results and discussion

In order to verify the proposed configuration, a laboratory prototype was constructed with 300 V 30A FK30SM-6 MOSFETs and 1200 V 16A HFA16PB120 fast recovery diodes. The experimental circuit specifications are the same with the simulation parameter in Table 2. Figs. 12 and 13 show the three-level output current waveform and its waveform after filtering for inductive load test. The total harmonic distortion of this three-level output current is 5.475%. The filtered output current is almost perfect sinusoid.

Fig. 14 shows the inverter output current and grid voltage waveform during grid connected test. The inverter output current is an AC current with its harmonic profile is shown in Fig. 15. The inverter works injecting an AC current into the power grid with unity power factor operation. It agrees with the previous simulation results.

From the simulation and experimental results, it was proven that the proposed inverter circuit works generating a three-level output current and sinusoidal current waveform after filtering. During grid connected operation, the inverter injects the AC current into the power grid with high power factor. However, if we compare the inverter output current without and with grid connected operation, it can be seen that the inverter output current

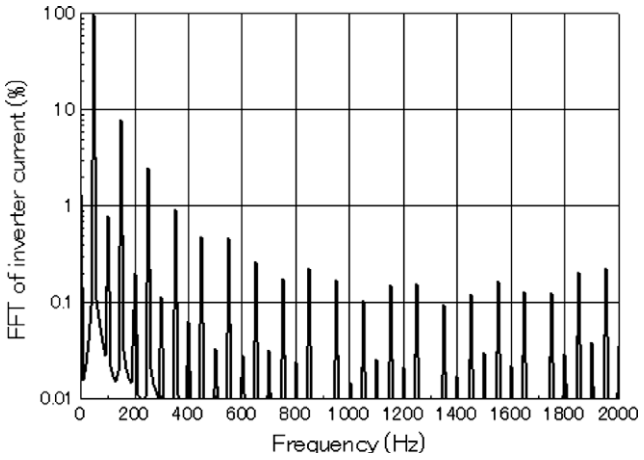


Fig. 11. FFT analysis of inverter output current.

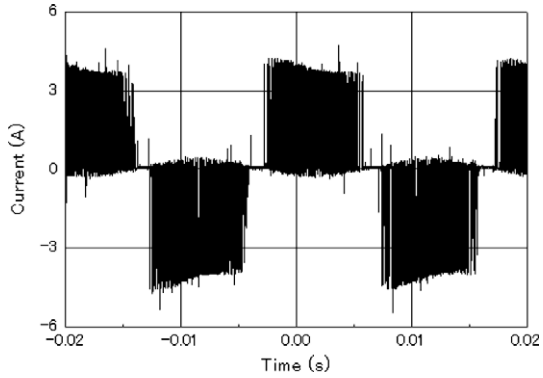


Fig. 12. Three level output current waveform.

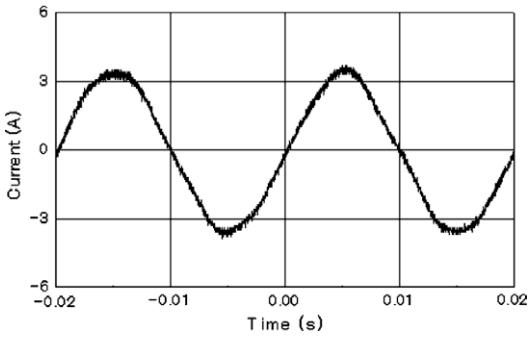


Fig. 13. Filtered output current waveform.

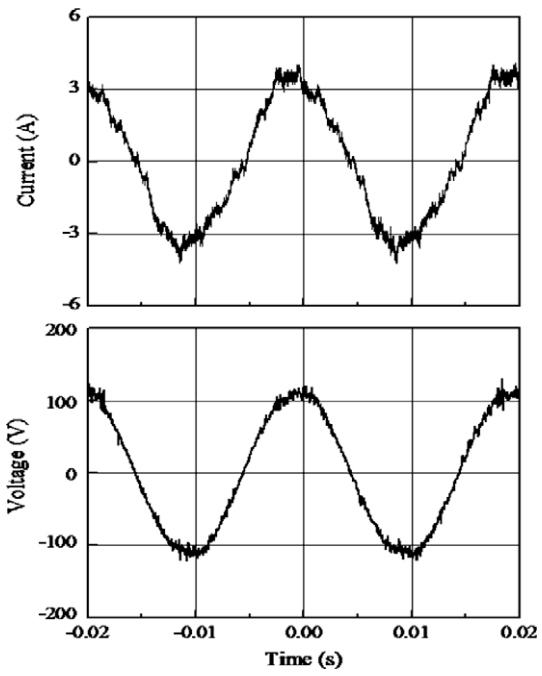


Fig. 14. Inverter output current and power grid voltage waveforms.

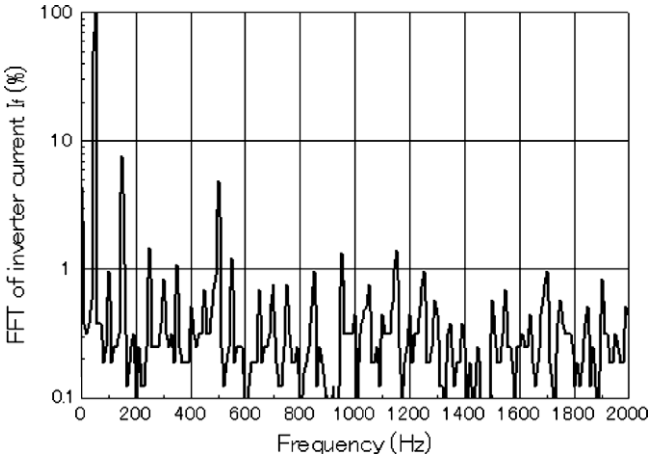


Fig. 15. FFT analysis of inverter output current i_f during grid connected operation; THD = 10.02%.

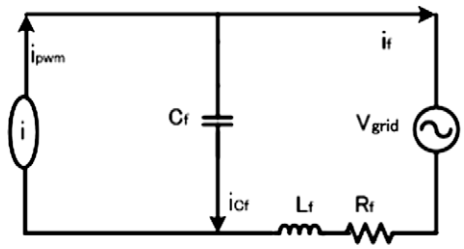


Fig. 16. Equivalent circuit of grid connected CSI.

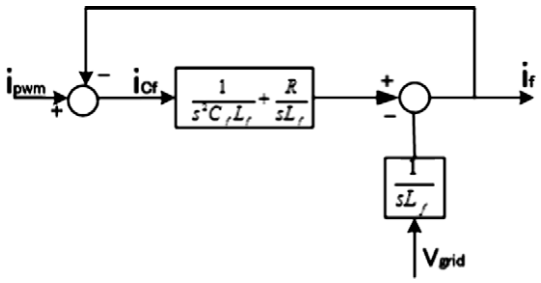


Fig. 17. Block diagram of grid connection system.

becomes more distorted when the inverter is connected with a distorted power grid. In this grid connected inverter system, this effect can be explained as follow.

Fig. 16 presents the equivalent circuit diagram of the inverter and power grid system. Current Ipwm is the inverter output current before filtering. It is a three-level PWM current waveform. Current i_f is the inverter output current after filtering by a low pass filter (Rf–Cf–Lf). It is a sinusoidal current with its harmonic contents. The power grid voltage and its harmonics contents are presented by a voltage source V_{grid}.

From this equivalent circuit, we have:

$$i_{pwm} = i_{Cf} + i_f \tag{2}$$

$$V_{Cf} + V_{Rf} = V_{grid} + V_{Lf} \tag{3}$$

$$i_{Cf} = Cf\frac{dV_{Cf}}{dt} \tag{4}$$

From Eqs. (3) and (4) we get,

$$V_{Cf} + V_{Rf} = V_{grid} + V_{Lf} \Rightarrow \frac{1}{Cf}\int i_{Cf}dt + i_{Cf}Rf = V_{grid} + Lf\frac{di_f}{dt}$$

$$\Rightarrow \frac{1}{sCf}i_{Cf} + i_{Cf}Rf = V_{grid} + sLfi_f \tag{5}$$

or

$$i_f = \left(\frac{1}{s^2LfCf} + \frac{Rf}{sLf}\right)i_{Cf} - \frac{V_{grid}}{sLf} \tag{6}$$

The system block diagram of the equivalent circuit can be derived based on Eqs. (2) and (6) as shown in Fig. 17. As it can be seen from this diagram, the grid voltage behaves as a disturbance for the inverter system when the inverter is connected to the power grid. As a result, it will distort the current injected into the power grid by the inverter (i_f). One of the methods to reduce this effect is by adding a current feedback loop control as an additional harmonic suppression circuit to suppress the harmonics during grid connected operation.

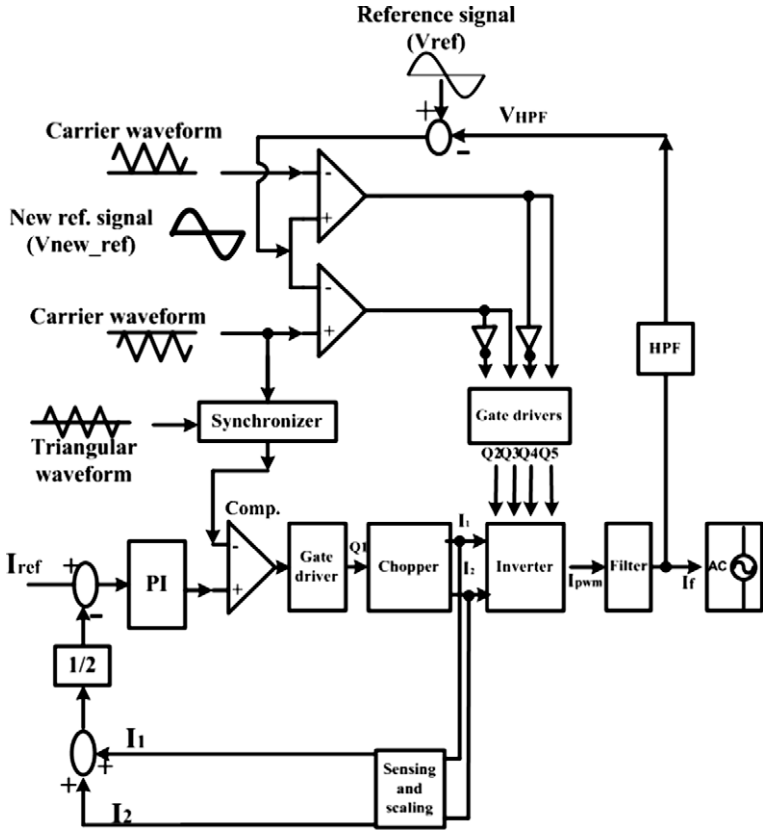


Fig. 18. Controller diagram with harmonic suppression.

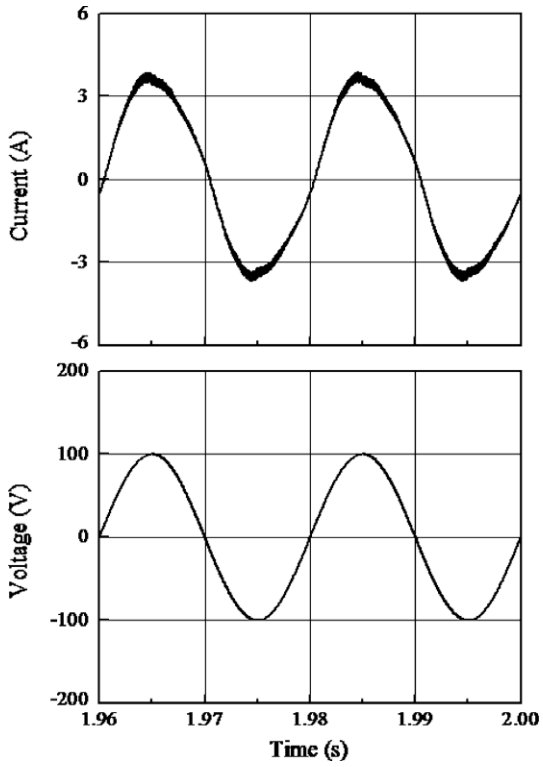


Fig. 19. Inverter output current and grid voltage with harmonic suppression.

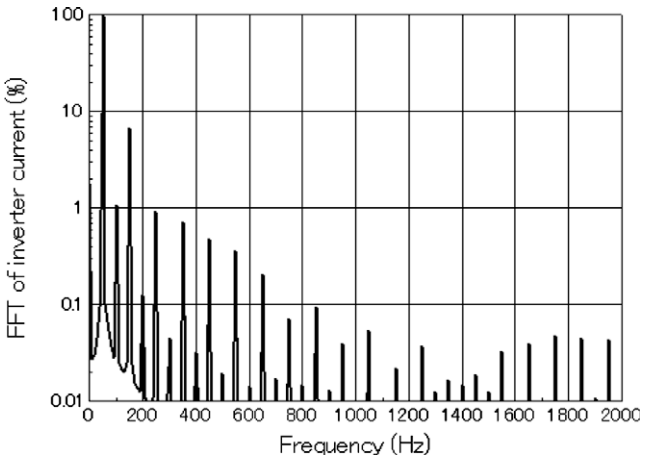


Fig. 20. FFT of inverter output current with harmonic suppression.

5. Proposed harmonics suppression method

In order to reduce the harmonic distortion problem of grid connected-inverter's output current, this section describes a proposed method to reduce the harmonic distortion during grid connected operation of the inverter. The current controller system block diagram of inverter circuit with harmonic suppression is presented in Fig. 18.

In this method, a high-pass-filter (HPF) is used to get high frequency component of inverter output current (f_H). This signal is fed to the original reference signal (f_R) of the sinusoidal pulse-width modulation technique. If the original reference signal is represented by f_R

$$f_R = A\cos\omega t \tag{7}$$

And the HPF signal, f_H

$$f_H = A_n \cos n\omega t + A_{n+1}\cos(n+1)\omega t + \cdots \tag{8}$$

n is the harmonic order.

Hence the new reference signal f_N is

$$f_N = f_R - f_H \tag{9}$$

This signal is the new reference signal of sinusoidal PWM. The frequency component of the HPF signal is determined by cut-off frequency of the high-pass-filter.

Fig. 19 shows the simulation result of the inverter output current and grid voltage during grid connected operation with proposed harmonic suppression method. Fig. 20 shows the FFT analysis of inverter output current. The simulation results show that almost all of harmonic orders are reduced compared with FFT result of previous system with no harmonic suppression, Fig. 11.

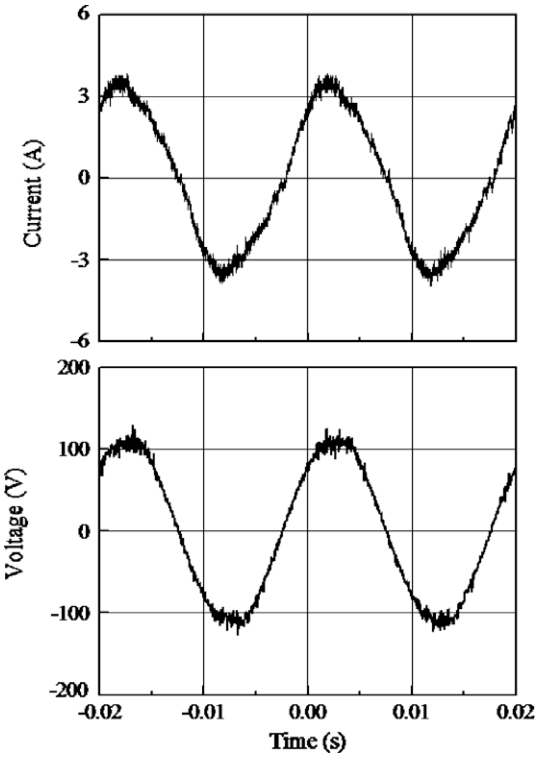


Fig. 21. Inverter output current and grid voltage with harmonic suppression circuit.

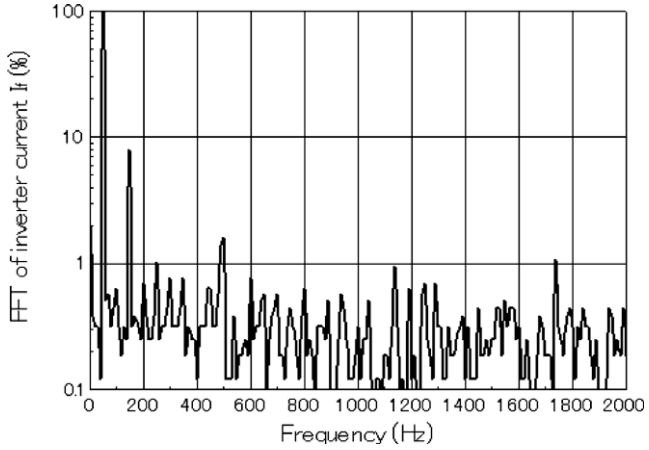


Fig. 22. FFT of inverter output current, i_f, with harmonic suppression circuit (THD = 8.08%).

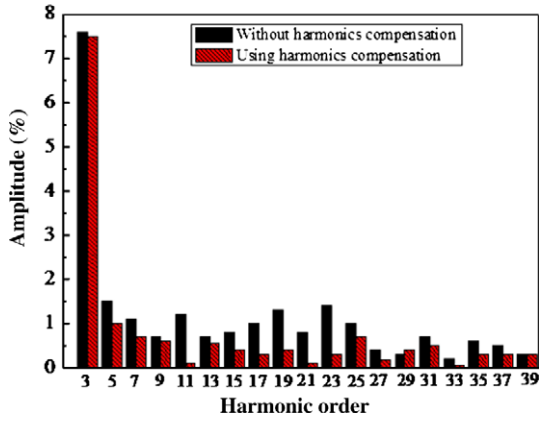


Fig. 23. Harmonics suppression result.

Fig. 21 shows the experimental result of inverter output current and grid voltage during grid connected operation test with harmonic suppression circuit. FFT analysis of the inverter output current is shown in Fig. 22. It can be seen that the method works well to suppress almost all of harmonic orders. The THD value of inverter current with harmonic suppression is 8.08% or 2% less than the previous system with no harmonic suppression. The inverter works properly injecting the AC current into power grid with high power factor operation. Fig. 23 shows the experimental results of harmonics suppression technique up to 39th harmonic order of the inverter output current.

6. Conclusions

A new three-level CSI PWM inverter with fully common-source topology at both chopper and inverter side has been proposed and verified using simulation and experimental prototype. The proposed inverter topology is proposed to be utilized for synthesizing sinusoidal output current from DC power source to be connected with power grid. Using this new three-level CSI topology the number of gate-drive power supply can dramatically be reduced into only a single power supply. The simulation and experimental results show that the proposed topology worked well to inject an AC output current into the power grid with unity power factor operation.

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