

Interlinking Converter to Improve Power Quality in Hybrid AC–DC Microgrids With Nonlinear Loads

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Abstract—To exploit the advancements of both ac and dc microgrids (MGs), hybrid ac–dc MGs (HMGs) have been considered. An interlinking converter (IC) is typically used to connect dc and ac MGs. In HMGs, the power quality is severely affected when nonlinear loads are connected to an ac bus. We developed an effective control scheme for the IC to maintain a sinusoidal point of common coupling (PCC) voltage under nonlinear load conditions in islanded HMGs. In the proposed control scheme, the IC controls the PCC voltage by providing harmonic currents caused by the nonlinear load as well as the active power sharing between dc distributed generation (DG) and ac DG. The system stability and controller design process were analyzed. Each power converter in the HMGs is controlled independently without a communication link, and the desired IC current is indirectly determined by considering the IC terminal voltage instead of the load current. Therefore, the control system can be implemented very easily with reduced cost. The performance of the proposed IC control scheme was verified by a simulation and experiment.

Index Terms—Hybrid ac–dc microgrids (HMGs), nonlinear loads, power quality, resonant controller.

NOMENCLATURE

$f_{ac}, f_{ac,norm}$	Instant and normalized ac bus frequency.
$f_{ac,max}, f_{ac,min}$	Maximum and minimum allowable ac bus frequency.
m_P, P_{ac}	Droop coefficient and active power of ac distributed generation (DG).
$R_{ac,L}$	Linear load in ac microgrid (MG).
$\sum_{h=5,7,\dots} i_{ac,h}$	Current source caused by nonlinear load in ac MG.
v_{ac}	AC bus voltage.
V_{ac}	Fundamental component of ac bus voltage.
$\tilde{v}_{ac}, \tilde{v}_{ac}^*$	Harmonic component of ac bus voltage and its reference.
$V_{dc}, V_{dc,norm}$	Instant and normalized dc bus voltage.
$V_{dc,max}, V_{dc,min}$	Maximum and minimum allowable dc bus voltage.

Manuscript received March 30, 2018; revised June 5, 2018 and August 9, 2018; accepted September 6, 2018. Date of publication September 17, 2018; date of current version July 31, 2019. This work was supported by the National Research Foundation of Korea through the Korean Government under Grant NRF-2015R1D1A1A09058166 and Grant NRF 018R1D1A1A09081779. Recommended for publication by Associate Editor Jun Wang. (Corresponding author: Hong-Hee Lee.)

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Digital Object Identifier 10.1109/JESTPE.2018.2870741

$m_{P_{dc}}, P_{dc}$	Droop coefficient and active power of dc DG.
$R_{dc,L}$	Linear load in dc MG.
i_{IC}, i_{IC}^*	Interlinking converter (IC) current and its reference.
I_{IC}, I_{IC}^*	Fundamental component of IC current and its reference.
$\tilde{i}_{IC}, \tilde{i}_{IC}^*$	Harmonic component of IC current and its reference.
e_{norm}	Error between $V_{dc,norm}$ and $f_{ac,norm}$.
P_{IC}, P_{IC}^*	Active power of IC and its reference.
Q_{IC}, Q_{IC}^*	Reactive power of IC and its reference.
$v_{IC,t}, v_{IC,t}^*$	IC terminal voltage and its reference.
Z_{IC}	Impedance of IC output filter.

Subscript d and q in the proposed IC control scheme are, respectively, the direct and quadrature components of the corresponding variable in fundamental rotating dq frame.

I. INTRODUCTION

CONVENTIONAL electric grids are gradually being changed, and the amount of distributed generation (DG) is steadily increasing [1], [2]. DG typically involves renewable energy sources (RESs), such as wind turbines or photovoltaics (PVs) [3]. The microgrid (MG) concept has been introduced to utilize these RESs [4], and ac MGs are commonly used for their high capability of operating with the ac grid and power system. Nevertheless, many RESs in an ac MG are naturally dc sources, such as PVs and batteries. Thus, dc/ac power converters have been used to integrate dc sources into ac MGs in spite of the high initial investment and power loss. Furthermore, most of the final loads are dc loads, such as LED lighting, computer systems, and electric vehicles [5].

Hybrid ac–dc MGs (HMGs) are considered as a promising solution to simultaneously exploit all the advancements offered by the ac and dc MGs [6]–[8]. HMGs consist of both ac and dc MGs. Generally, a dc/ac power converter called an interlinking converter (IC) is required to interface a dc MG with an ac MG [9], [10]. HMGs inherit the following benefits from both ac and dc MGs [11], [12]:

- 1) reduction of power conversion stages, system cost, and power loss;
- 2) improved system energy efficiency;
- 3) lower energy storage capacity;
- 4) higher reliability.

There are many studies of IC control strategies to transfer energy in HMGs [13], [14]. An IC can operate autonomously by using a normalization process to synthesize the droop characteristics of both ac and dc MGs [13]. However, only the fundamental power is exchanged through the IC. The linear relationship between the ac bus frequency and square of the dc bus voltage has been used to determine the fundamental active power exchanged in HMGs [14]. However, only ideal ac and dc bus voltages are considered with linear loads.

In practical applications, nonlinear ac loads are arbitrarily connected to an ac bus, and a large amount of harmonic current is drawn into the HMGs [15]. Harmonic current has many harmful impacts on power systems, such as highly distorted ac bus voltage, high-power loss, malfunction of electronic devices, and degradation of the power quality in HMGs [16]. In [17], the IC, which operates as a shunt active power filter (APF), only mitigates the harmonic components included in the utility grid current under an ideal ac bus voltage. Therefore, this IC controller cannot be used with highly distorted ac bus voltages. Tian *et al.* [18], [19] introduced new modulation strategies for the IC to compensate the harmonics in point of common coupling (PCC) voltage. Even though the power loss is reduced by using low-switching frequency to control the IC, the total harmonic distortion (THD) of PCC voltage is higher than 4%. Moreover, it also requires the load current measurement, communication links, and the central controller for operating IC, which is not simple because of the widely distributed loads in MGs. As a result, the total system cost is significantly increased and the IC is hard to operate autonomously in HMGs. In [20], the IC with an inductor, transformer, capacitor, and inductor topology is proposed for managing the power quality of ac MG in the HMGs. Even though IC can work in different operation modes, a transformer is needed. Consequently, it may affect the total system cost, size, and power loss. Furthermore, the experimental results are not provided to prove the feasibility in practice. In [21], a doubly fed induction generator is adopted to share the harmonic current with the IC. However, it may lead to some critical problem such as high circulating current and power loss in case of many parallel power circuits.

In this paper, we propose an effective control strategy for an IC in islanded HMGs to maintain a sinusoidal PCC voltage under nonlinear load conditions. The harmonic current due to the nonlinear load is compensated through the IC to keep the PCC voltage sinusoidal. The control scheme was developed using multiresonant (3R) and repetitive controller (RC) in order to deal with high-order harmonics. It can be implemented very easily because the desired IC harmonic current is determined by detecting the PCC voltage instead of the load current. Furthermore, the proposed scheme provides exact active power sharing between dc and ac MGs together with the harmonic current in an ac MG, and the IC can versatilely play as shunt APF besides its inherent role in HMGs. Moreover, it does not require communication links, central controller, transformer, or support from different power circuits. As a consequence, we can reduce the total system cost, size as well as power loss, and the IC can independently operate in HMGs. The performance of the proposed control

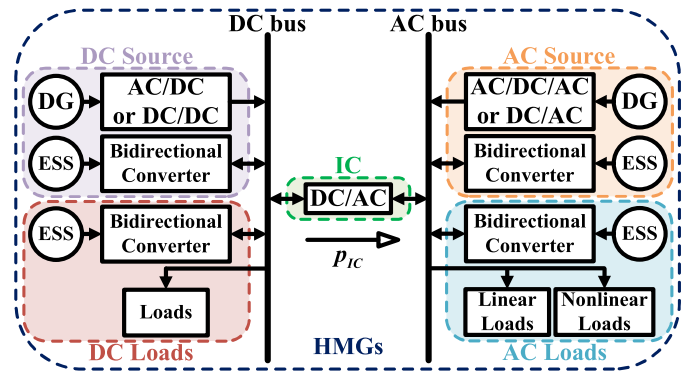


Fig. 1. HMGs structure.

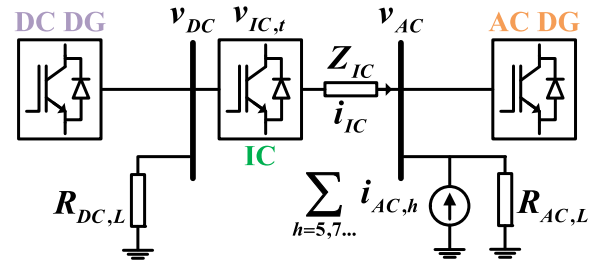


Fig. 2. Equivalent power circuit of HMGs with nonlinear load.

scheme was investigated and verified by a simulation and experiment. Design guidelines for an IC controller and a system stability analysis are also presented.

II. SYSTEM DESCRIPTION AND NORMALIZATION PROCESS

A. System Description

Fig. 1 shows the structure of HMGs which consist of both ac and dc MGs. Each MG has three main types of components: sources, energy storage systems, and local loads. When the power flows from the dc MG to the ac MG, the entire ac MG and IC act as a load from the point of view of the dc MG and vice versa. In the ac MG, there are two types of load: linear and nonlinear loads. Nonlinear loads are very common, such as adjustable speed drives, power supply units for computer systems, and welding machines. When a nonlinear load is connected to the ac bus, highly distorted current is injected into the power system, which can be modeled as a harmonic current source. Fig. 2 shows the equivalent power circuit of HMGs with nonlinear load.

B. Normalization Process

When ac and dc DG is controlled using a conventional droop control, the droop control equations are described as follows:

$$\begin{cases} f_{ac} = f_{ac,max} + m_P P_{ac} \\ f_{ac,min} \leq f_{ac} \leq f_{ac,max} \end{cases} \quad (1)$$

$$\begin{cases} V_{dc} = V_{dc,max} + m_{Pdc} P_{dc} \\ V_{dc,min} \leq V_{dc} \leq V_{dc,max} \end{cases} \quad (2)$$

where $f_{ac,max}$, $f_{ac,min}$, f_{ac} , m_P , and P_{ac} are the maximum and minimum allowable frequencies, instant frequency, droop coefficient, and active ac power, respectively. $V_{dc,max}$, $V_{dc,min}$,

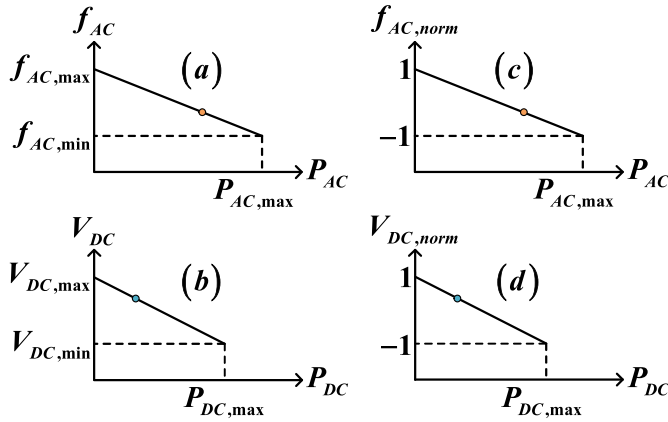


Fig. 3. (a) AC droop characteristics. (b) DC droop characteristics. (c) Normalized f_{ac} . (d) Normalized V_{dc} .

V_{dc} , m_{Pdc} , and P_{dc} are the maximum and minimum allowable voltages, instant voltage, droop coefficient, and active dc power, respectively. Fig. 3(a) and (b) shows the droop characteristics of (1) and (2). They are normalized in Fig. 3(c) and (d) by using the normalized equations in (3) and (4) to reflect the interaction between the ac MG and the dc MG from the point of view of the fundamental active power [13]

$$f_{ac,norm} = \frac{f_{ac} - 0.5(f_{ac,max} + f_{ac,min})}{0.5(f_{ac,max} - f_{ac,min})} \quad (3)$$

$$V_{dc,norm} = \frac{V_{dc} - 0.5(V_{dc,max} + V_{dc,min})}{0.5(V_{dc,max} - V_{dc,min})} \quad (4)$$

where $f_{ac,norm}$ and $V_{dc,norm}$ are the normalized ac frequency and dc voltage, respectively.

To combine the dc and ac droop characteristics, the error e_{norm} between the normalized dc voltage and ac frequency is defined

$$e_{norm} = V_{dc,norm} - f_{ac,norm}. \quad (5)$$

The fundamental active power of the IC is regulated to minimize the error e_{norm} as given in the following equation:

$$P_{IC}^* = K_n e_{norm} \quad (6)$$

where P_{IC}^* is the reference of the IC fundamental active power, and K_n is a constant gain. From (6), the IC fundamental current reference I_{IC}^* is obtained as follows:

$$I_{IC}^* = (v_{ac})^{-1} P_{IC}^*. \quad (7)$$

III. PROPOSED CONTROL SCHEME FOR IC

Fig. 4 shows the control block diagram of the proposed IC controller in the dq frame. It consists of four blocks: a fundamental current reference generator I_{IC}^* , a harmonic current reference generator \tilde{i}_{IC}^* , an inner current control loop for controlling i_{IC} , and a phase-locked loop. When the non-linear load is applied, the IC current reference i_{IC}^* is modified to (8) in order to eliminate the harmonic components in

the v_{ac} waveform:

$$i_{IC}^* = I_{IC}^* + \tilde{i}_{IC}^* \quad (8)$$

$$\tilde{i}_{IC}^* = - \sum_{h=5,7,\dots} i_{ac,h} \quad (9)$$

where $i_{IC,h}$ is the h th harmonic current generated by the non-linear load in Fig. 2. In practical applications, it is generally hard to extract the load current harmonic in (9) directly since the loads are widely distributed in the MG. To avoid this difficulty, the IC harmonic current reference \tilde{i}_{IC}^* is obtained indirectly by using the IC terminal voltage v_{ac} .

From Fig. 2, v_{ac} in the dq frame is expressed as

$$v_{ac} = V_{ac} + \tilde{v}_{ac} \quad (10)$$

where V_{ac} is the fundamental component of the ac bus voltage and \tilde{v}_{ac} is the harmonic component and it is extracted by using a first-order high-pass filter with cutoff frequency of 15 rad/s. To eliminate the harmonic voltage on the ac bus, \tilde{v}_{ac} in (10) should be regulated to zero by setting its reference \tilde{v}_{ac}^* to zero

$$\tilde{v}_{ac}^* = 0. \quad (11)$$

To maintain the oscillating voltage at zero, three dominant frequencies are handled by the 3R controller: the 6th, 12th, and 18th harmonics. From the terminal voltage regulation, the IC harmonic current reference \tilde{i}_{IC}^* in (8) is determined to eliminate the voltage harmonics

$$\tilde{i}_{IC}^*(s) = G_{3R}(s)[\tilde{v}_{ac}^* - \tilde{v}_{ac}(s)]. \quad (12)$$

In (12), $G_{3R}(s)$ is the transfer function of the 3R controller

$$G_{3R}(s) = \sum_{i=6,12,18} \frac{K_{Ri} \omega_c s}{s^2 + 2\omega_c s + (i2\pi f_{ac})^2} \quad (13)$$

where K_{Ri} is a resonant controller gain, and ω_c is the cutoff frequency. By substituting (7) and (12) into (8), the IC current reference is obtained, and its control block diagram in the dq frame is shown in Fig. 4. As shown in Fig. 4, the IC terminal voltage reference $v_{IC,t}^*$ to supply the desired current is generated by means of PI and RC by considering the $6n$ th ($n = 1, 2, \dots$) harmonics

$$v_{IC,t}^*(s) = G_{PI-RC}(s)[i_{IC}^*(s) - i_{IC}(s)] + v_{ac}(s) \quad (14)$$

where

$$G_{PI-RC}(s) = K_P + \frac{K_I}{s} + \frac{K_r Q(s) e^{-sT_d}}{1 - Q(s) e^{-sT_d}}. \quad (15)$$

In (15), K_P and K_I are the proportional and integral gains of PI controller, respectively, K_r is the RC gain, $Q(z)$ is a zero-phase low-pass filter, f_s is the sampling frequency, and $T_d = f_s/(6f_{ac})$ is an RC delay term.

IV. CONTROLLER DESIGN AND STABILITY ANALYSIS

The proposed control scheme was designed by investigating its stability from the inner current control loop, which includes the PI and RC blocks. After selecting PI and RC, the outer harmonic current reference generator is considered, and the 3R is determined.

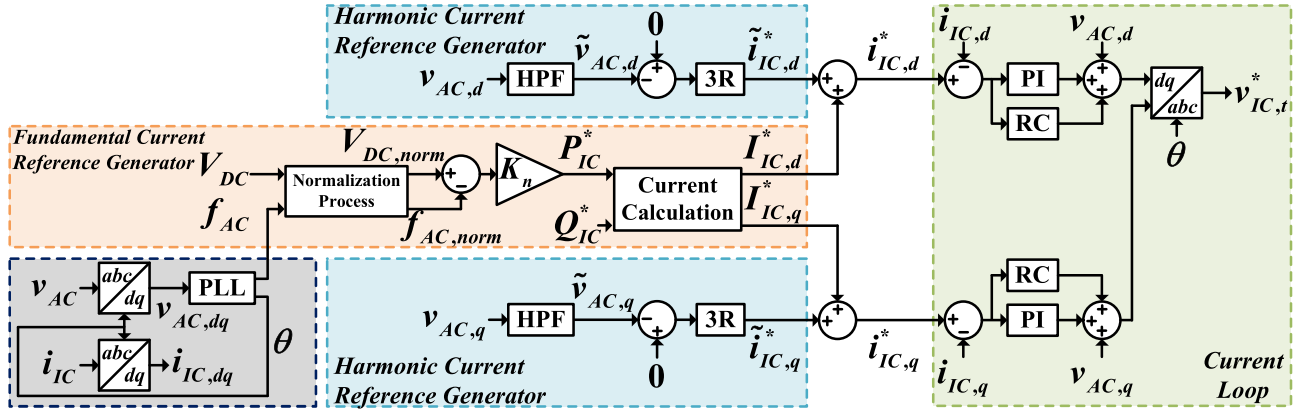


Fig. 4. Proposed IC control scheme in HMGs.

A. Inner Loop—PI Controller

As shown in Fig. 4, the fundamental component of the IC current is controlled to track I_{IC}^* by the PI controller in (15). Heuristically, K_I is first set as $100K_P$, and we adopt an open-loop transfer function $G_{o1}(z)$ and closed-loop transfer function $G_{c1}(z)$ of the inner current loop as follows:

$$G_{o1}(z) = G_{PI}(z)G_P(z) \quad (16)$$

$$G_{c1}(z) = \frac{G_{o1}(z)}{1 + G_{o1}(z)} \quad (17)$$

where $G_{PI}(z)$ is the z -domain transfer function of the PI controller in (15), and $G_P(z)$ is the z -domain transfer function of the IC output filter Z_{IC} in Fig. 2. $G_P(z)$ is derived from $G_P(s)$ by using a bilinear discretization method with sampling frequency f_s

$$G_P(z) = \frac{1}{Z_{IC}(s)} \Big|_{s=2f_s \left(\frac{1-z^{-1}}{1+z^{-1}} \right)}. \quad (18)$$

Since the PI controller deals with only I_{IC} , which is the dc component in the dq frame, the closed-loop transfer function $G_{c1}(z)$ should provide a very low-control bandwidth. Different values of K_P are placed in (16) to obtain $G_{c1}(z)$, and Bode diagrams of $G_{c1}(z)$ are plotted in Fig. 5. $G_{c1}(z)$ shows a cutoff frequency of 30 Hz with $K_P = 0.4$, which was selected for dc signal regulation.

K_I was then determined based on the unit step response of $G_{c1}(z)$ in Fig. 6. Considering the dynamic response and overshoot in the transient state, K_I is chosen to be around $40K_P$.

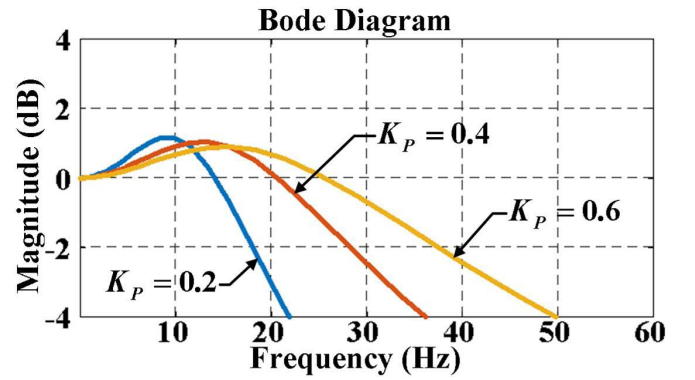
B. Inner Loop—RC

The IC current i_{IC} is regulated to periodically track the reference \tilde{i}_{IC}^* with the 6th, 12th, and 18th orders. The digitized RC transfer function $G_{RC}(z)$ is obtained from $G_{RC}(s)$ in (15) by using a bilinear discretization method

$$G_{RC}(z) = \frac{K_r Q(z) z^{-N+l}}{1 - Q(z) z^{-N}} \quad (19)$$

where N is the number of samples in a fundamental period

$$N = \frac{f_s}{6f_{ac}}. \quad (20)$$

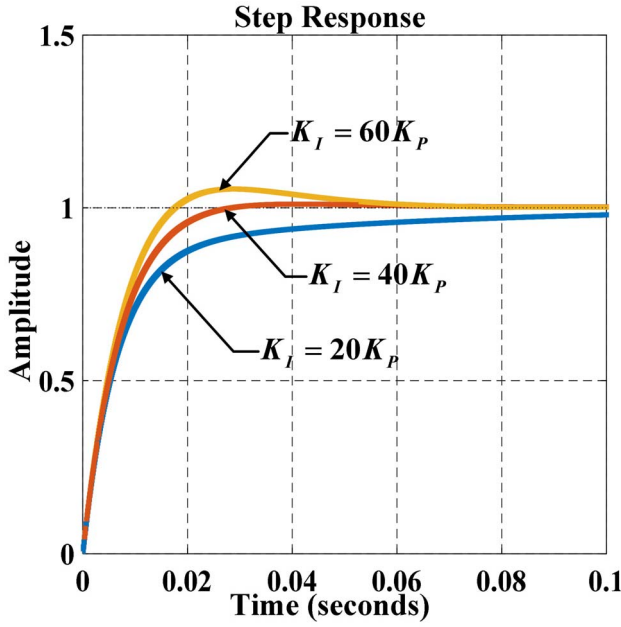
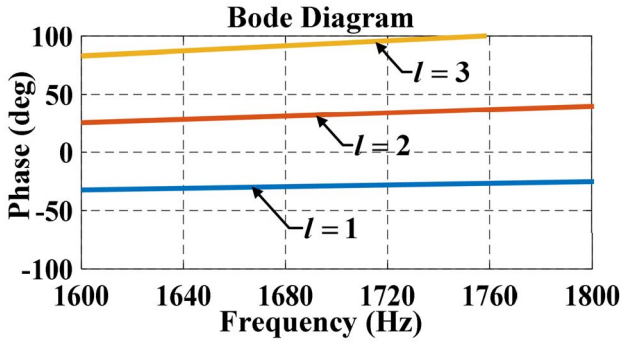
Fig. 5. Bode diagram of $G_{c1}(z)$ with different K_P .

To achieve effective compensation and adequate stability, we take into account three RC parameters in (19): the filter $Q(z)$, the phase lead term z^l , and the gain K_r . To implement $Q(z)$, the filter given in (21) is selected to provide a cutoff frequency about 2000 Hz [22], which can deal with very high-order harmonics

$$\begin{cases} Q(z) = \alpha_1 z + \alpha_0 + \alpha_1 z^{-1} \\ \alpha_1 = 0.2 \\ 2\alpha_1 + \alpha_0 = 1. \end{cases} \quad (21)$$

To compensate for the delay caused by the output filter Z_{IC} in Fig. 2, the phase lead term z^l is added to the RC transfer function, and l is chosen to minimize the phase lag of $z^l G_P(z)$ at high frequency [22]. Fig. 7 shows a Bode plot of $z^l G_P(z)$ with various values of l . It can be seen that $l = 2$ results in less phase lag of $z^l G_P(z)$, but $l = 3$ was chosen to consider the computation delay in practical applications.

The RC gain K_r is designed to simultaneously provide sufficient stability margin and good harmonic compensation. High K_r offers good selectivity and robust harmonic rejection. However, it may result in instability. Therefore, K_r is increased until it makes the system unstable, and this value of K_r is called the critical gain K_{r_cri} . We select K_r to be around $70\%K_{r_cri}$ for sufficient stability margin. To evaluate the stability of the inner current control loop with the RC, the


 Fig. 6. Unit step response of $G_{c1}(z)$ with different K_I .

 Fig. 7. Bode diagram of $z^l G_P(z)$ with different l .

open-loop transfer function $G_{o1}(z)$ and closed-loop transfer function $G_{c1}(z)$ in (16) and (17) are updated as follows:

$$G_{o1}(z) = G_{PI-RC}(z)G_P(z) \quad (22)$$

$$G_{c1}(z) = \frac{G_{o1}(z)}{1 + G_{o1}(z)}. \quad (23)$$

From (23), $G_{c1}(z)$ becomes unstable if and only if $1 + G_{o1}(z)$ introduces at least one zero outside of the stability region, which is inside of the unit circle in the z plane [23]. For various K_r , the pole-zero map of $1 + G_{o1}(z)$ is shown in Fig. 8. From Fig. 8, the RC critical gain K_{r_cri} becomes 1.2 because at least one zero of $1 + G_{o1}(z)$ is located on the unit circle. $K_r = 1.6$ leads to instability since two zeros of $1 + G_{o1}(z)$ are located outside of the unit circle. As a result, $K_r = 0.8$ is chosen.

C. Outer Loop—3R Controller

The 3R controller plays a vital role in the IC control scheme because it generates the IC reference current with the 6th, 12th, and 18th orders. From (13), the system's open-loop transfer

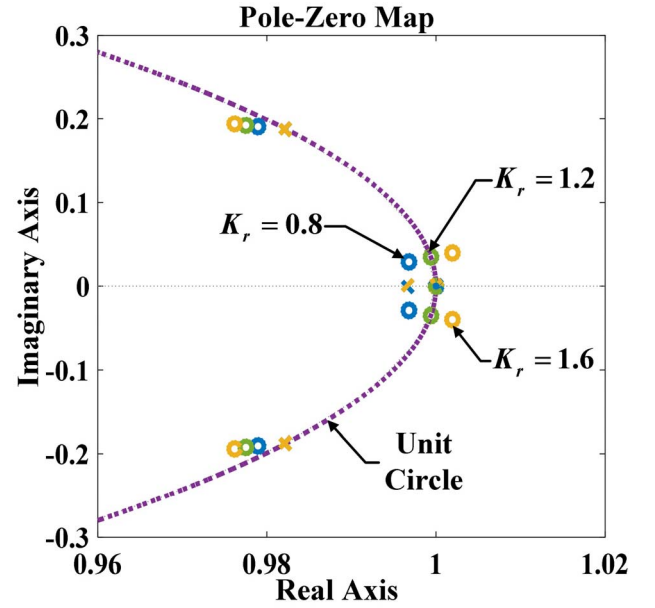

 Fig. 8. Pole-zero map of $1 + G_{o1}(z)$ with different K_r .

 TABLE I
SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
$f_{AC,max}$	50.5 Hz	$V_{DC,max}$	189 V
$f_{AC,min}$	49.5 Hz	$V_{DC,min}$	171 V
m_p	0.0104 Hz W ⁻¹	m_{pDC}	0.0300 V W ⁻¹
$R_{AC,L}$	60 Ω	$R_{DC,L}$	60 Ω
V_{AC}	60√2 V	$Z_{IC} = R_{IC} + jL_{IC}$	0.1 Ω + j2.9 mH

function $G_{o2}(z)$ is

$$G_{o2}(s) = G_{3R}(s)G_{c1}(s) = \left[\sum_{i=6,12,18} \frac{K_{Ri}\omega_c s}{s^2 + 2\omega_c s + (i2\pi f_{ac})^2} \right] G_{c1}(s) \quad (24)$$

$$G_{o2}(z) = G_{o2}(s)|_{s=2f_s \left(\frac{1-z^{-1}}{1+z^{-1}} \right)} \quad (25)$$

where K_{Ri} represents the controller gain for the i th order. To determine K_{R6} , the two other gains are disabled ($K_{R12} = 0$ and $K_{R18} = 0$) [24]. The IC controller is stable if and only if the Nyquist diagram of $G_{o2}(z)$ is fully inside the unit circle. Fig. 9 shows the Nyquist diagram of $G_{o2}(z)$ with different K_{R6} , and the critical gain K_{R6_cri} is almost 10. Generally, K_{R6} is set as 40% of K_{R6_cri} for adequate stability margin, and thus, $K_{R6} = 4$ was chosen. With a similar procedure, we selected the gains $K_{R12} = 1$ and $K_{R18} = 0.25$.

V. SIMULATION RESULTS

To verify the performance of the proposed IC controller, a simulation was carried out using PSIM software. The system parameters are listed in Table I.

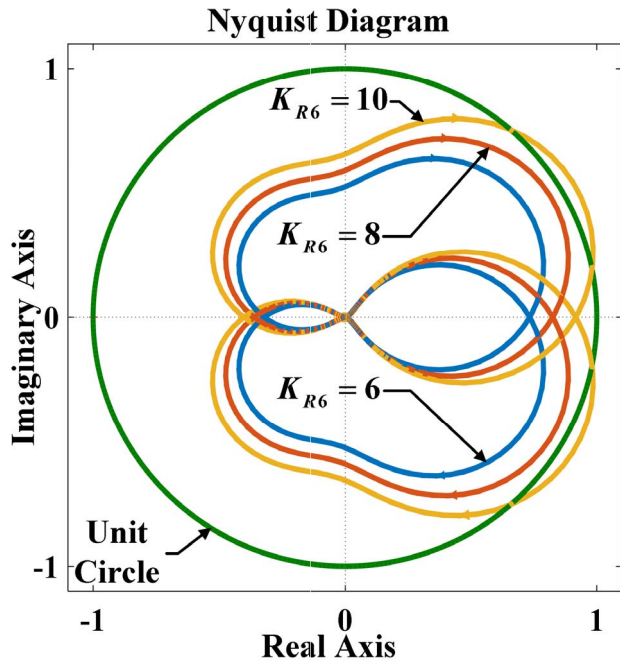


Fig. 9. Nyquist diagram of $G_{O2}(z)$ with different K_{R6} .

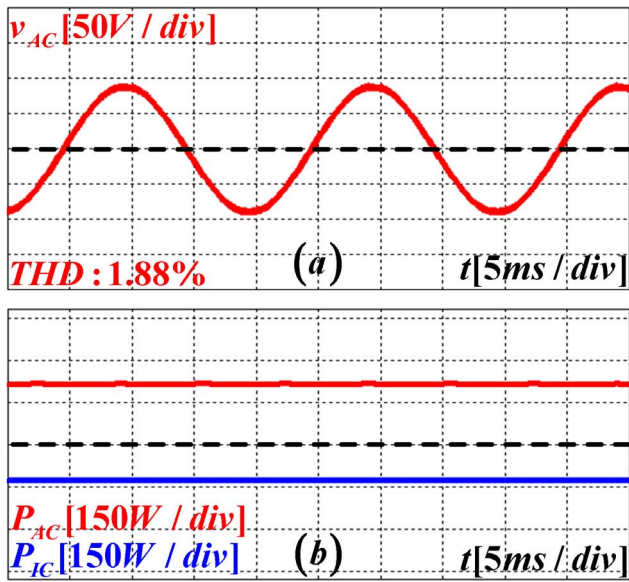


Fig. 10. Simulation results. Steady-state performance with linear load. (a) v_{ac} and its THD. (b) P_{ac} and P_{ic} .

A. Steady-State Performance

Fig. 10 shows the steady-state waveforms of the ac bus voltage and power flow when only linear load is applied in the HMGs. In Fig. 10(a), sinusoidal v_{ac} is well maintained, and its THD is about 1.88%. Fig. 10(b) shows the active power P_{ac} generated by the ac DG and the active power P_{ic} transferred by the IC. The load demand in the ac MG is quite low, so the surplus power of the ac DG is transferred to the dc MG via the IC to support the dc load, and the value of P_{ic} is negative.

When nonlinear load is connected along with the linear load used in Fig. 10, v_{ac} is seriously distorted, as shown

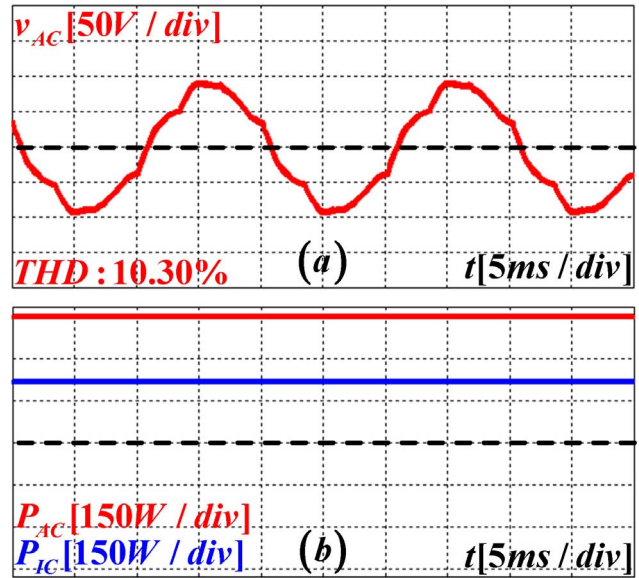


Fig. 11. Simulation results. Steady-state performance with nonlinear load and without harmonic current reference generator. (a) v_{ac} and its THD. (b) P_{ac} and P_{ic} .

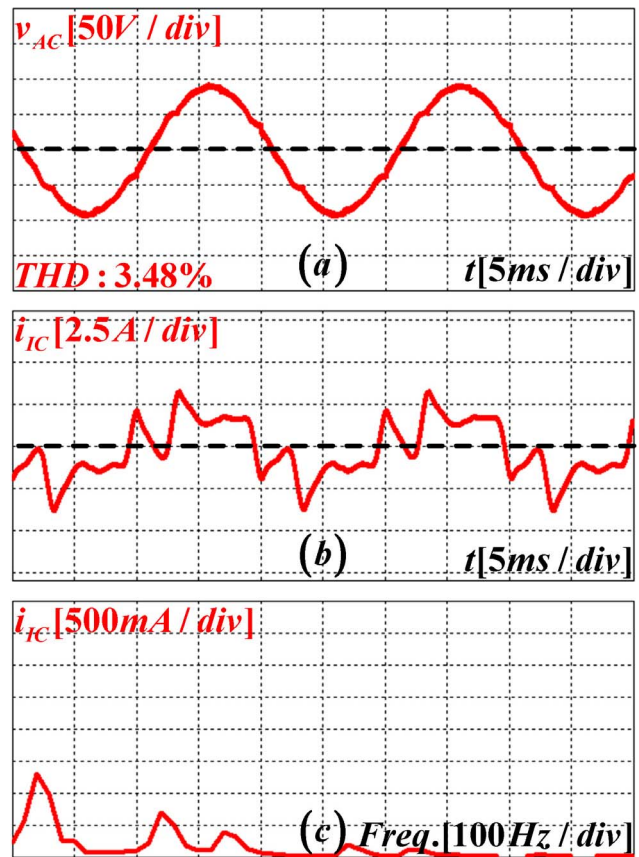


Fig. 12. Simulation results. Steady-state performance with nonlinear load and with the proposed IC control strategy. (a) v_{ac} and its THD. (b) i_{ic} . (c) FFT of i_{ic} .

in Fig. 11(a). This occurs because of the nonlinear load, which acts as a harmonic current source in HMGs. In Fig. 11(a), the THD of v_{ac} is about 10.30%, which is critical if a sensitive load is applied according to IEEE Std. 519-2014 [25]. In Fig. 11(b), P_{ic} becomes positive because both the dc MG and IC have to assist the ac MG due to the increased ac load

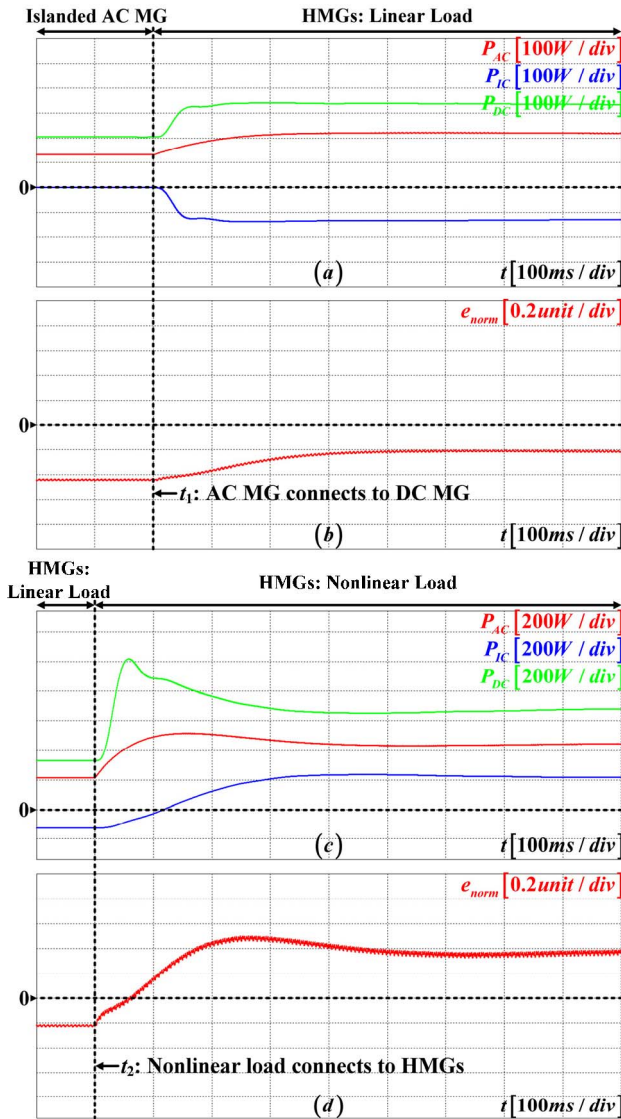


Fig. 13. Simulation results. Transient waveforms when (a) and (b) ac MG connects to dc MG via IC and (c) and (d) nonlinear load connects to HMGs. (a) P_{AC} , P_{IC} , and P_{DC} . (b) e_{norm} . (c) P_{AC} , P_{IC} , and P_{DC} . (d) e_{norm} .

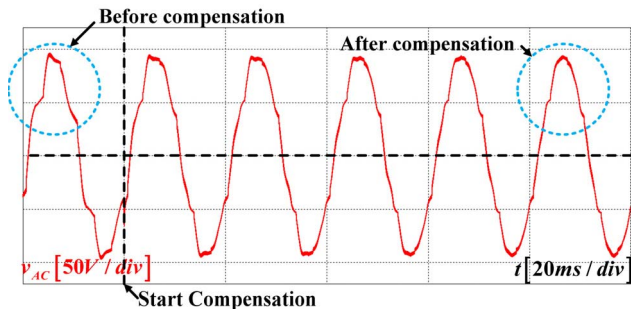


Fig. 14. Simulation results. Transient waveform of v_{ac} when the proposed IC controller is activated.

power compared with the power in Fig. 10. The fundamental active power is autonomously exchanged in HMGs according to the load condition. However, from the performance of the IC control scheme without harmonic current reference generator in Fig. 11, we can conclude that even though fundamental

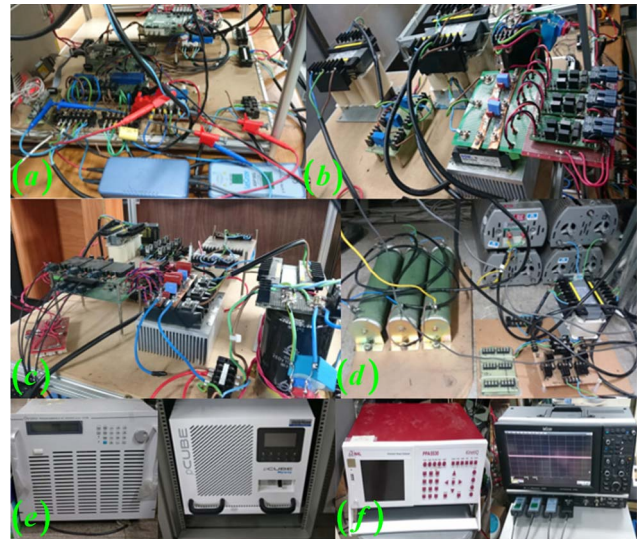


Fig. 15. Experimental setup. (a) DSP boards, sensing devices, and probes. (b) IC power circuit and its gate driver boards. (c) DGs power circuit and their gate driver boards. (d) Linear and nonlinear loads in HMGs. (e) Sources for powering DGs. (f) THD analyzer and oscilloscope.

TABLE II
SUMMARY OF THD VALUES OF SIMULATION RESULTS

v_{AC}	Linear load	Nonlinear load	
		Without harmonic compensation	With proposed scheme
THD(%)	1.88	10.30	3.48

active power sharing is accurately achieved, the power quality issue in the v_{ac} waveform is not solved.

Fig. 12 shows the performance of the proposed IC control strategy with nonlinear load. The ac bus voltage v_{ac} in Fig. 12(a) becomes almost a sinusoidal waveform compared with that in Fig. 11(a), and THD of v_{ac} is about 3.48%. The IC current waveform i_{IC} and its fast Fourier transform (FFT) are shown in Fig. 12(b) and (c). The IC current is highly distorted because it contains both the fundamental component I_{IC} and the harmonic component \hat{i}_{IC} . Fig. 12 shows that the proposed control strategy simultaneously achieves power quality improvement and fundamental power sharing under nonlinear load conditions. Table II summarizes the ac bus voltage THD for three cases shown in Figs. 10–12.

B. Transient-State Performance

Fig. 13 shows the dynamic performance of the proposed control scheme. In Fig. 13(a), ac MG and dc MG are interlinked by IC at t_1 when only linear load is applied in ac MG. Because e_{norm} is negative, as shown in Fig. 13(b), IC reference power P_{IC}^* is also negative from (6) in order to minimize the active power balancing error between ac and dc MGs, and IC power P_{IC} is transferred from ac MG to dc MG. In Fig. 13(a), the power P_{dc} also increases to restore dc bus voltage. When the nonlinear load is connected to ac MG at t_2 as in Fig. 13(c), the load demand in ac MG is increased, and $f_{ac, norm}$ becomes lower than $V_{dc, norm}$ because dc load power is not changed. As shown in Fig. 13(d), e_{norm} changes from negative to positive, and the IC reference power P_{IC}^*

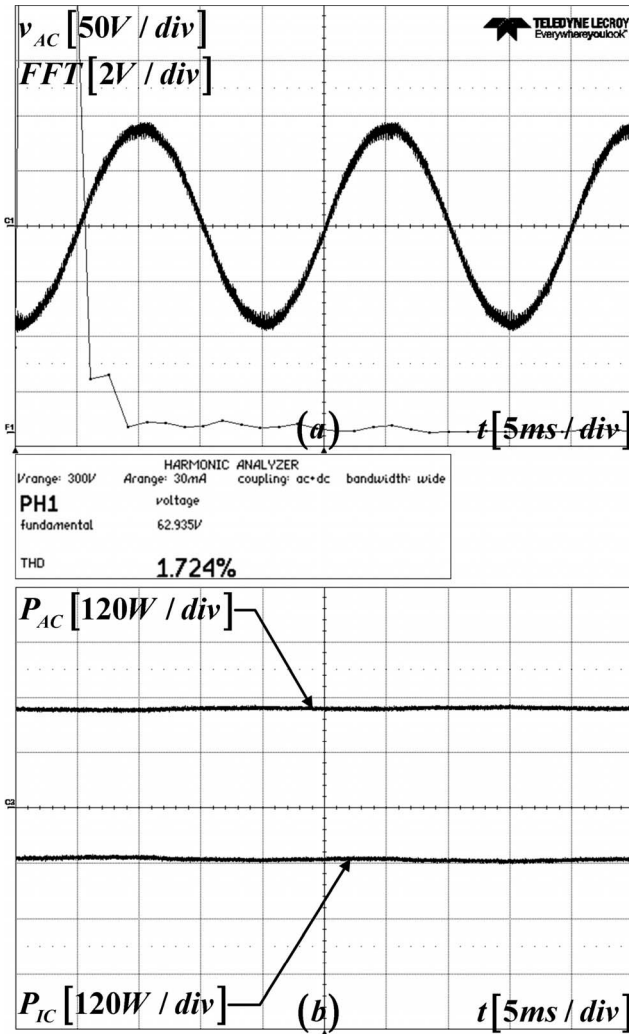


Fig. 16. Experimental results. Steady-state performance with linear load. (a) v_{ac} and its THD. (b) P_{ac} and P_{IC} .

becomes positive. Therefore, the IC power P_{IC} is transferred from dc MG to ac MG, and both power P_{dc} and power P_{ac} increase together to support the additional ac power demand; ac load power is simultaneously supplied by both ac DG and dc DG via IC. Even though dc load is maintained constant during ac load increment, the dc power in dc MG increases to minimize the error e_{norm} .

Regarding the power quality control performance, Fig. 14 describes the v_{ac} waveform when the proposed control strategy is activated. Before compensation, harmonic current with 22.27% THD is applied under 1.35-kW nonlinear load condition. Because the harmonic current reference generator blocks in Fig. 4 are disabled, IC cannot generate harmonic current to compensate ac bus voltage v_{ac} , and v_{ac} is highly distorted until harmonic compensation starts. When harmonic compensation starts, an additional harmonic current \tilde{i}_{IC}^* is added to the fundamental current i_{IC}^* , and the v_{ac} waveform becomes almost sinusoidal after five cycles, which is quite fast in terms of dynamic response. In Fig. 14, even though compensated ac bus voltage still contains harmonics, the THD of v_{ac} is significantly improved from 12.10% to 3.51%.

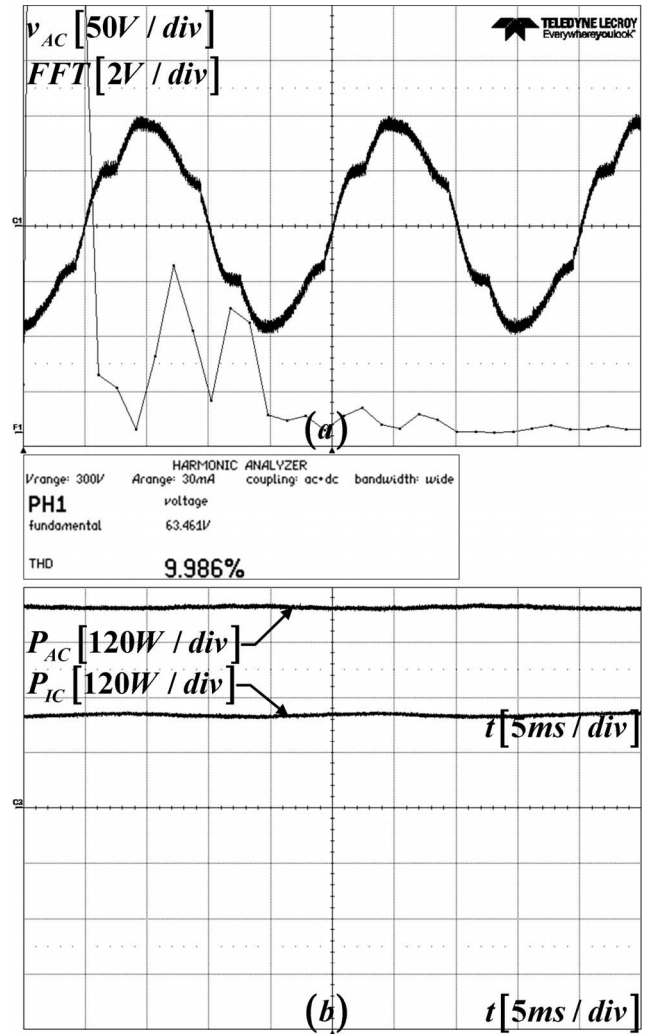


Fig. 17. Experimental results. Steady-state performance with nonlinear load and without harmonic current reference generator. (a) v_{ac} and its THD. (b) P_{ac} and P_{IC} .

VI. EXPERIMENTAL RESULTS

The system parameters for the experiment are the same as those used in the simulation and the experiment setup in laboratory is depicted in Fig. 15. The proposed IC controller was implemented with a 32-bit floating-point DSP (TMS320F28335; Texas Instruments). THD is measured by the power analyzer from Newtons4th Ltd.

A. Steady-State Performance

Fig. 16 shows the steady-state performance of the HMGs with linear load only. In Fig. 16(b), the power P_{ac} is higher than the demanded load in the ac MG, so the power P_{IC} transferred by the IC is negative to balance the power demand in the HMGs. The dc MG behaves like a load from the point of view of the ac MG.

Fig. 17(a) shows the distorted ac bus voltage and its THD due to the nonlinear load. The power quality in the HMGs is seriously degraded with nonlinear load conditions. P_{IC} changes from negative to a positive value in the fundamental power flow in Fig. 17(b). The total ac load power including linear and nonlinear loads is higher than the ac source power,

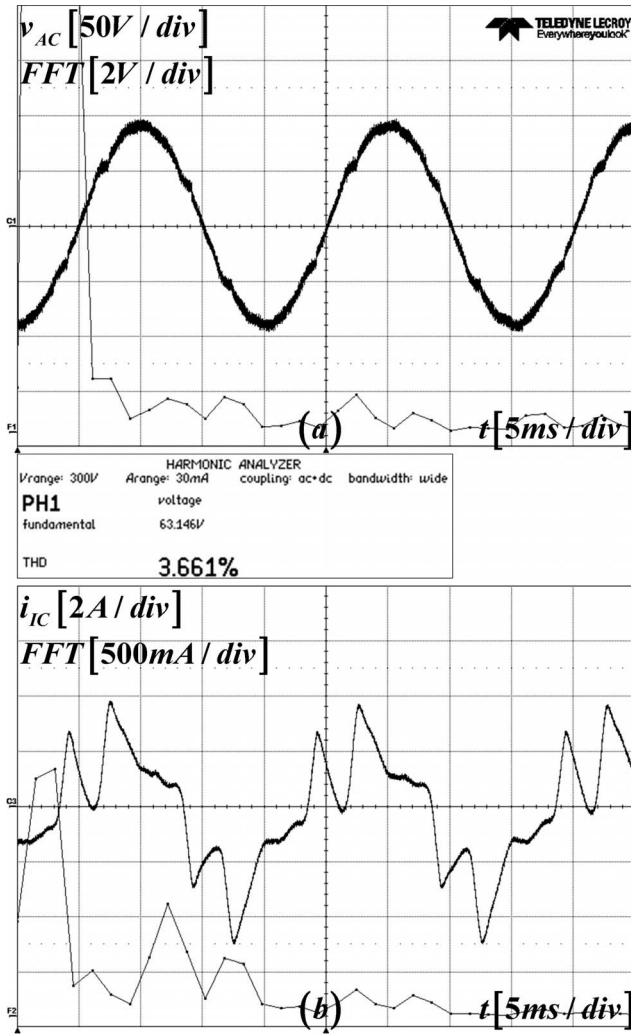


Fig. 18. Experimental results. Steady-state performance with nonlinear load and with the proposed IC control strategy. (a) v_{ac} and its THD. (b) i_{IC} and its FFT.

so the power flow direction changes from the dc MG to the ac MG, and P_{ac} is also increased to adapt to the increased load demand. In Fig. 17, however, there is still a power quality issue in v_{ac} even though the power sharing scheme is properly achieved.

Fig. 18(a) shows the performance of the proposed IC controller. It is clear that the ac bus voltage is significantly improved compared with that in Fig. 17(a), and v_{ac} almost becomes a sinusoidal waveform. Fig. 18(b) shows the waveform of i_{IC} , which verifies that the IC carries both the fundamental current and the harmonic current from the dc MG to the ac MG. The $(6n \pm 1)$ th ($n = 1, 2, \dots$) order harmonic currents exist in the spectrum of i_{IC} , and the entire dc MG and IC act as a shunt APF in the ac MG. As a result, the IC with the proposed control scheme can balance the power flow between the dc and ac MGs as well as mitigate the power quality degradation due to nonlinear load.

B. Transient-State Performance

The dynamic response of the system was also evaluated experimentally. In Fig. 19(a), an islanded ac MG is connected

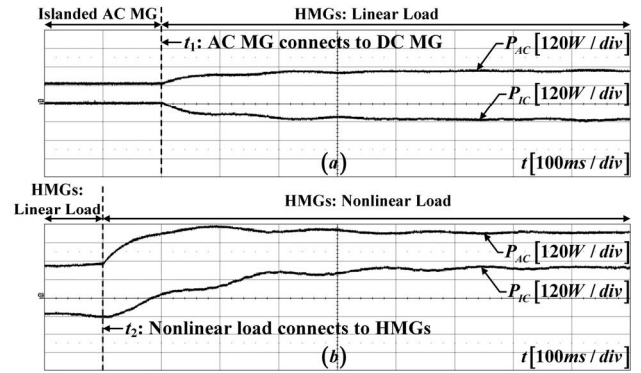


Fig. 19. Experimental results. Transient waveforms of P_{ac} and P_{IC} when (a) ac MG connects to dc MG via IC and (b) nonlinear load connects to HMGs.

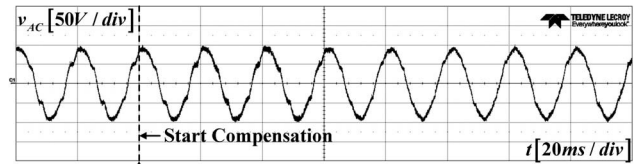


Fig. 20. Experimental results. Transient waveform of v_{ac} when the proposed IC controller is activated.

to a dc MG through the IC at t_1 , and the ac DG supports both the ac load and dc MG. P_{ac} and P_{IC} change quickly according to the power demand, as shown in Fig. 19(a). P_{ac} increases twice, P_{IC} varies from zero to a negative value, and the power flows from the ac to the dc MG by means of the IC.

In Fig. 19(b), a nonlinear load is added in HMGs at t_2 . Then, the powers P_{ac} and P_{IC} adaptively vary to satisfy the power demand in the ac MG. The transient condition continues around 500 ms. While P_{ac} increases to a surplus amount of power, P_{IC} changes its direction from negative to positive. The total load power in the ac MG is provided from two sources: the ac DG and the dc MG by means of the IC. Thus, the dynamic response of the power flow in HMGs with the proposed IC controller is quite fast.

Fig. 20 shows the v_{ac} waveform when the proposed IC control scheme is activated under nonlinear load conditions. v_{ac} is highly distorted before compensation due to the nonlinear load, but its waveform becomes almost sinusoidal within four fundamental cycles after the proposed control scheme is activated. The experimental results show that the proposed control scheme is effective for improving the power quality and keeping the power flow balanced in the HMGs.

VII. CONCLUSION

This paper proposed a robust and flexible control strategy for operating an IC in HMGs. The PCC voltage is stably kept sinusoidal in spite of nonlinear load by injecting harmonic currents through the IC. The proposed controllers were implemented with the aid of a resonant controller and RC, and the system stability and controller design process were analyzed.

With the proposed control scheme, we achieved bidirectional fundamental power sharing between the ac MG and dc MG with enhanced power quality under nonlinear load conditions. Moreover, there are no communication links between

the system configurations, and each power converter operates independently. Therefore, the proposed system can be implemented easily with reduced cost.

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