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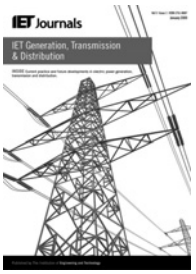

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Fast sag/swell detection method for fuzzy logic controlled dynamic voltage restorer

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Abstract: In this study, the design and analysis of a fuzzy logic (FL) controlled dynamic voltage restorer (DVR) are presented and extended to perform fast fault detection. A new control method for DVR is proposed by combining FL with a carrier modulated PWM inverter. The proposed control scheme is simple to design and has excellent voltage compensation capabilities. The proposed method for voltage sag/swell detection has the ability of detecting different kinds of power disturbances faster than conventional detection methods. Effectiveness of the proposed detection method is shown by comparison with the conventional methods in the literature. Simulation results under unbalanced supply voltage are presented to evaluate the performance of the designed DVR.

1 Introduction

Power quality is crucial to companies operating in a highly competitive business environment because it affects profitability, which definitely is a driving force in the industry. Control of most of the loads in the industry is mainly based on semiconductor devices, which causes such loads to be more sensitive against power system disturbances such as voltage sag, voltage swell, current harmonics, interruption and phase shift. Thus, the power quality problems have gained more interest recently [1, 2]. The dynamic voltage restorer (DVR) in a distribution network is a power quality device, which can protect these plants against the bulk of these disturbances that is distribution system voltage sags and swells related to remote system faults. DVR compensates for these voltage excursions provided that the supply grid does not get disconnected entirely through breaker trips [1]. The main considerations for the control system of a DVR include: sag/swell detection and voltage reference generation for transient/steady-state control of the injected voltage.

Voltage sag must be detected fast and corrected with a minimum of false operations. Monitoring of $\sqrt{V_d^2 + V_q^2}$ or V_d in a vector controller is the simplest type of sag detection, which will return the state of supply at any instant in time and hence, detect whether or not sag has occurred [3]. To separate the positive and negative sequence components, low pass filters (LPFs) are used after the $d-q$ transformation in the literature. For effective removal, the cut-off frequency of the LPF must be reduced, but has the side effect of reducing the controller response time [4]. Further information about conventional sag detection method is presented in [5].

In [4], a new control method for DVR system is proposed by detecting the negative and positive sequence components using differential controllers and digital filters. In this study, the control method in [4] is used for sag/swell detection. By using this proposed approach the detection time can be further improved with respect to conventional methods using LPF.

Recently, new fuzzy logic (FL) methods have been applied to custom power devices, especially for active power filters [6–11]. The operation of DVR is similar to that of active power filters in that both compensators must respond very fast on the request from abruptly changing reference signals. In the literature, FL control of DVR based on dq synchronous reference frame (SRF) is only examined in [12]. In [12], three-phase supply voltages are transformed into d and q coordinates. The reference values for V_d and V_q are compared with these transformed values and then voltage errors are obtained. FL controllers evaluating 81 linguistic rules process these errors in [12]. Resulting

outputs are re-transformed into three-phase domain and compared with a carrier signal to generate PWM inverter signals. The DVR in [12] has no sag detection function, which means that the device is always in operation and generates compensating voltage also for small voltage drops within 10% that causes high losses. In [12], the results only for balanced sags are presented.

The proposed voltage compensation method for DVR does not include any transformations. A FL controller utilising 49 linguistic rules directly processes three-phase supply voltages to improve the response time of DVR. The proposed DVR has the capability of both balanced and unbalanced voltage sag/swell compensation and can track changes in supply phase. Phase-locked loop (PLL) is applied to each supply phase independently. It can easily be implemented in real time and there are no current publications in this method as reported in [3].

The proposed mitigating device and control algorithm presented in this study differ from the previously discussed approaches in the following ways:

1. The proposed DVR is a multifunction device since it can mitigate the voltage sag, voltage swell and voltage unbalance.

2. A new rapid algorithm for sag/swell detection is presented. Passive filter with a low cut-off frequency is not used in sag/swell detection.

3. There is no transformation in voltage compensation control and each phase is controlled independently. With this method, minimum energy is injected and switching losses are reduced.

4. Extraction and tracking of disturbances are fast and accurate.

The paper is therefore organised as follows. After this introductory section, the general principles of the DVR operation and power circuit are described in Section 2. The innovative contributions of the study are presented in Section 3 where the proposed DVR control system is introduced. Section 3 includes explanations about conventional and proposed sag detection methods. The effectiveness of the proposed DVR control system is illustrated and case studies are presented in Section 4. Discussion of case results is presented in Section 5. Finally, the main points and significant results of the study are summarised in conclusions.

2 DVR power circuit

The system configuration of three-phase DVR is shown in Fig. 1. The power circuit of the DVR is composed of voltage source inverter, energy storage device, filter circuit and injection transformer.

DVR consists of three single-phase H-bridge pulse width modulation (PWM) inverters with insulated gate bipolar transistor (IGBT) switches. Use of single-phase H-bridge

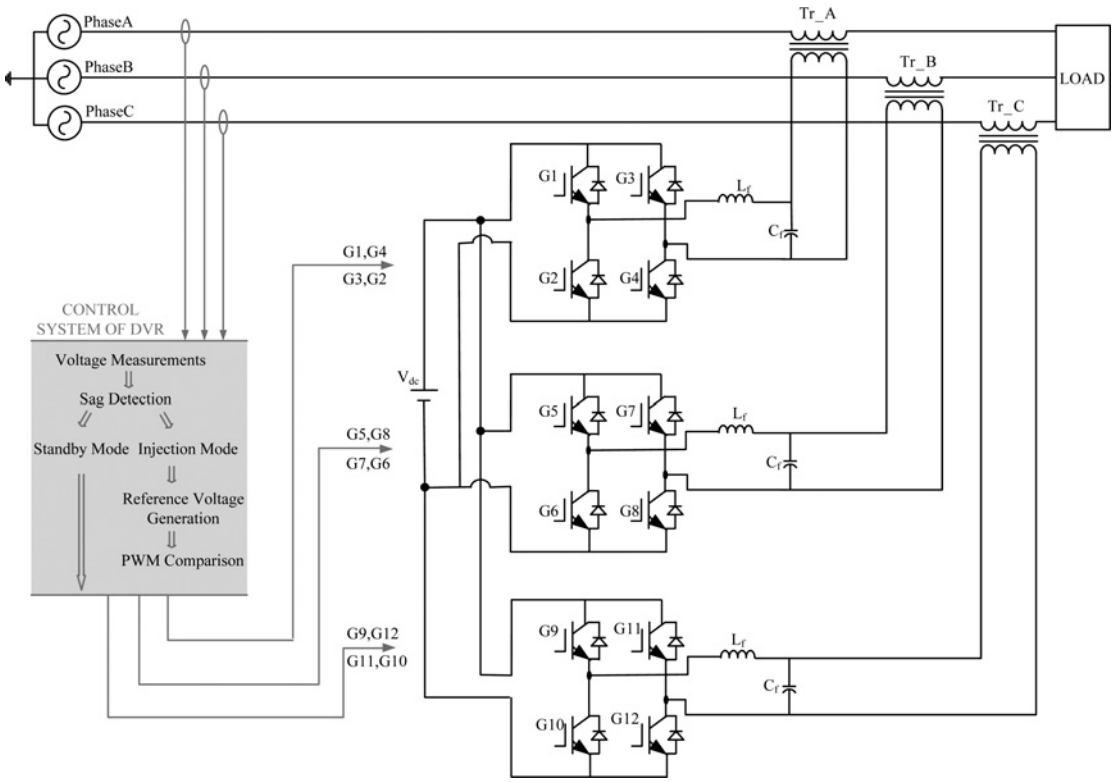

Figure 1 *System configuration of three-phase DVR*

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PWM inverters in DVR power circuit makes possible the injection of positive, negative and zero sequence voltages. Voltage source inverter (VSI) rating is relatively low in voltage and high in current because of the use of step-up injection transformers. The inverter side filtering is preferred in this study. Using this filtering scheme, the high-order harmonic currents are prevented from penetrating into the series transformer, thus reducing the voltage stress on the transformer. The DC link voltage is considered constant at 85 V.

3 Proposed DVR control

The control system of the proposed DVR in Fig. 1 is composed of sag/swell detection and voltage compensation parts as shown in Fig. 2.

Three-phase V_{abc} voltages are the input for the control system. The output of the control system is Pulse_*A*, Pulse_*B* and Pulse_*C*. The measured V_{abc} values are used to generate the compensation voltage and the transfer signal that activates the PWM pulse generator. Proposed DVR control system is clearly presented in Fig. 2.

3.1 Sag/swell detection method

In the proposed sag/swell detection method, the supply-side terminal voltages V_a, V_b and V_c are transformed into $d-q$ values of positive sequence SRF as shown in (1)–(3)

$$V_0 = 1/3(V_a + V_b + V_c) \tag{1}$$

$$\begin{pmatrix} V_d^{(p)} \\ V_q^{(p)} \end{pmatrix} = \frac{2}{3} R(\omega t) C \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \tag{2}$$

$$C = \begin{pmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix} \quad \text{and}$$

$$R(\omega t) = \begin{pmatrix} \cos \omega t & -\sin \omega t \\ \sin \omega t & \cos \omega t \end{pmatrix} \tag{3}$$

$R(\omega t)$ is a matrix that rotates by phase angle ωt. The superscript (p) represents that this is the value in positive sequence SRF. The subscripts d and q represent d-axis and q-axis values in SRF, respectively. The subscripts p and n show that this is the value of positive and negative sequence components at $t = 0$. Thus this vector is a constant value. The positive sequence rotates counter-clockwise and the

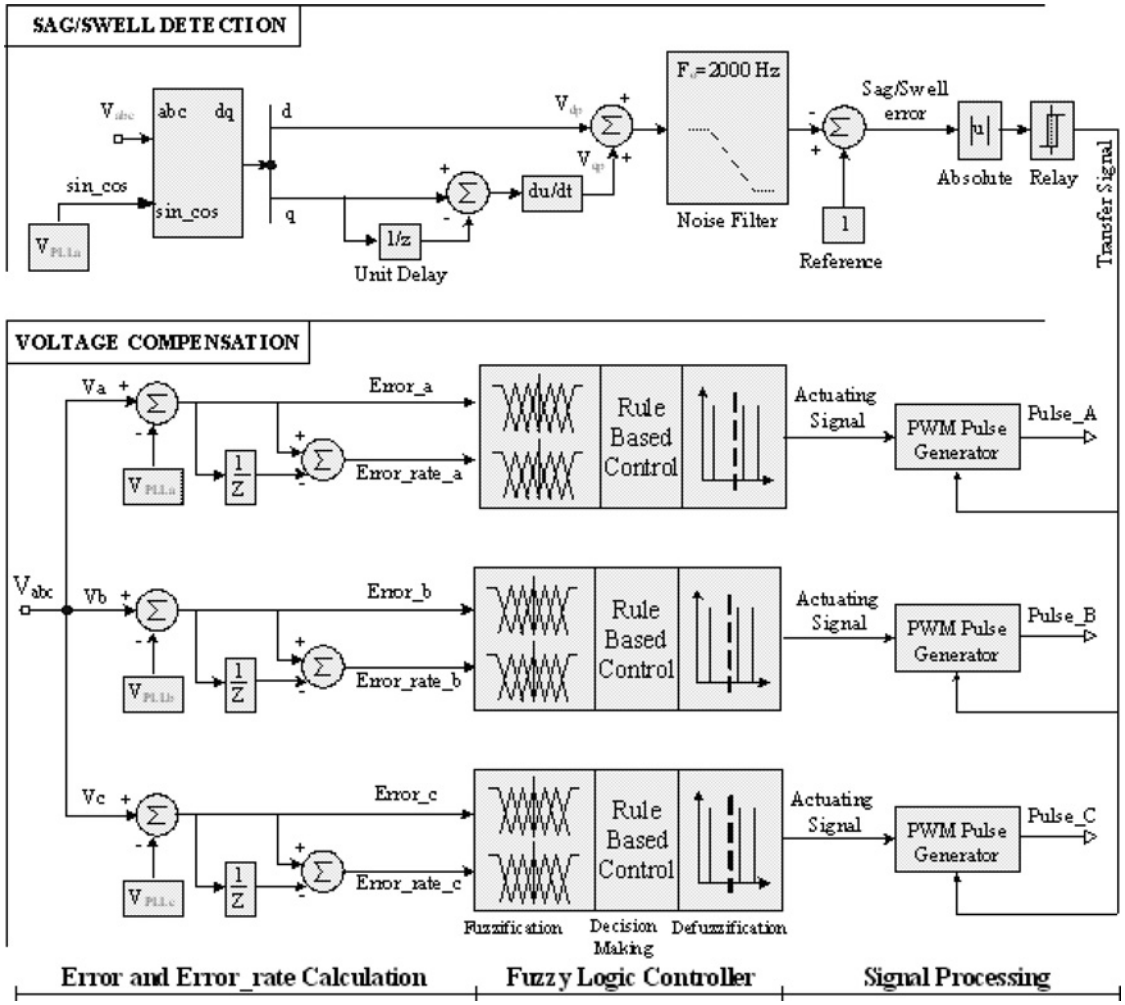

Figure 2 *Control system of proposed DVR*

negative sequence rotates clockwise direction in the stationary reference frame. When they are shown in positive sequence SRF the positive sequence becomes a DC component and the negative sequence a 100 Hz component as expressed in (4). For the symmetrical balanced faults, there is no need to extract the positive and negative sequence SRF. Using only d component is sufficient for control of DVR. The d component is a DC value for symmetrical balanced faults. Unbalanced voltage sag causes negative sequence components to appear in the supply voltage. For effective control without phase shift in steady state, the positive and negative sequence components that have DC values should be separated. In order to achieve this, the differential controller method is used. Fig. 2 shows the structure of sag/swell detection unit.

Equation (2) is composed of both of positive and negative sequence components. This is expressed by (4). Equation (5) shows the differentiated form of (4) in time domain

$$\begin{pmatrix} V_d^{(\mathrm{p})} \\ V_q^{(\mathrm{p})} \end{pmatrix} = \begin{pmatrix} V_{d\mathrm{p}} \\ V_{q\mathrm{p}} \end{pmatrix} + R(-2wt)\begin{pmatrix} V_{d\mathrm{n}} \\ V_{q\mathrm{n}} \end{pmatrix} \tag{4}$$

$$\begin{pmatrix} \dot{V}_d^{(\mathrm{p})} \\ \dot{V}_q^{(\mathrm{p})} \end{pmatrix} = -2wR\left(\frac{\pi}{2}\right)R(-2wt)\begin{pmatrix} V_{d\mathrm{n}} \\ V_{q\mathrm{n}} \end{pmatrix} \tag{5}$$

The differential of $R(-2\omega t)$ becomes $-2\omega R(\pi/2)R(-2\omega t)$ and the differential of the positive sequence is zero since it is constant. Equation (5) is rotated by 90° and divided by -2ω as follows

$$-\frac{1}{2w}R\left(\frac{\pi}{2}\right)\begin{pmatrix} \dot{V}_d^{(\mathrm{p})} \\ \dot{V}_q^{(\mathrm{p})} \end{pmatrix} = R(\pi)R(-2wt)\begin{pmatrix} V_{d\mathrm{n}} \\ V_{q\mathrm{n}} \end{pmatrix} \tag{6}$$

Since the sum of a vector and the same vector phase shifted by 180° becomes zero, the sum of (4) and (6) leaves an only positive sequence component that is a DC component and all negative sequence components are removed

$$\begin{pmatrix} V_d^{(\mathrm{p})} \\ V_q^{(\mathrm{p})} \end{pmatrix} - \frac{1}{2w}R\left(\frac{\pi}{2}\right)\begin{pmatrix} \dot{V}_d^{(\mathrm{p})} \\ \dot{V}_q^{(\mathrm{p})} \end{pmatrix} = \begin{pmatrix} V_{d\mathrm{p}} \\ V_{q\mathrm{p}} \end{pmatrix} \tag{7}$$

Equation (7) shows that positive sequence components can be detected without using LPFs, so the stability and accuracy of control can be obtained. With the same method, the DC negative sequence components can be calculated with the following equation

$$\begin{pmatrix} V_d^{(\mathrm{n})} \\ V_q^{(\mathrm{n})} \end{pmatrix} - \frac{1}{2w}R\left(\frac{\pi}{2}\right)\begin{pmatrix} \dot{V}_d^{(\mathrm{n})} \\ \dot{V}_q^{(\mathrm{n})} \end{pmatrix} = \begin{pmatrix} V_{d\mathrm{n}} \\ V_{q\mathrm{n}} \end{pmatrix} \tag{8}$$

High-quality voltages only include positive sequence d component. For efficient sag compensation, $V_{d\mathrm{pref}} = 1$ and $V_{q\mathrm{pref}} = 0$ are chosen. The resulting $V_{d\mathrm{p}}$ and $V_{q\mathrm{p}}$ are added and passed through a noise filter. This noise filter barely has any influence on the control system since the noise filter has a large cut-off frequency of 2000 Hz. The output of noise filter is compared with the addition of $V_{d\mathrm{pref}} = 1$ and $V_{q\mathrm{pref}} = 0$ and which equals unity that represents an ideal signal to generate the sag detection signal.

3.2 Voltage compensation

In the proposed method, PLL for each phase tracks the phase of network voltage phasor and generates a reference signal with magnitude of unity locked to supply frequency for each phase. The supply voltage for each phase is converted to pu and error is obtained from the difference of reference PLL generated signal and actual supply voltage converted to pu. Error and error rate are the inputs for the FL controller. Output of the FL controller is fed to the PWM generator to produce switching pulses for VSI.

The desired response from DVR-PLL system is quite different from other applications. This is because the phase of the supply voltage prior to the sag is generally preferred and if the PLL reacts quickly to changes in the phase during sag, the post-sag phase may be used. Therefore the DVR would not be able to compensate for the phase jump. Conventionally, once sag is detected, the target phase of the voltage reference is fixed to the pre-sag phase to ensure that if the reference is faithfully tracked, then the load voltage phase will remain unaffected [13]. Through a suitable choice of the time constant of the PLL, the DVR restores the instantaneous voltage waveform in the sensitive load side to the same phase and magnitude as the initial pre-sag voltage. The proposed DVR can compensate positive, negative and zero sequence components and this is verified with different case studies. To maximise dynamic performance, direct feed-forward-type control is applied in the control concept of DVR. With this concept a fast response time (approximately 1 ms) can be achieved to compensate distribution system voltage sags [1].

The FL controller for the proposed DVR has two real-time inputs measured at every sampling time, named error and error rate and one output named actuating signal for each of the phases.

For phase A, the error and error rate are defined as

$$e_{\mathrm{A}} = V_{\mathrm{PLL_A}} - V_{\mathrm{S_A}} \tag{9}$$

$$\Delta e_{\mathrm{A}} = \mathrm{err}_{\mathrm{A}}(n) - \mathrm{err}_{\mathrm{A}}(n-1) \tag{10}$$

The input signals are fuzzified and represented in fuzzy set notations by membership functions. The defined 'if ... then ...' rules produce the linguistic variables and these variables are defuzzified into control signals for comparison with a carrier signal to generate PWM inverter gating pulses. The theory of FL controllers is extensively described

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in [14–16]. The solution of defuzzification process results from (11)

$$U = \frac{\sum_i y_i \mu(y_i)}{\sum_i \mu(y_i)} \tag{11}$$

where U denotes the crisp value of the output, y_i represents the normalised controller output for the ith interval and $\mu(y_i)$ is the associated membership grade.

The development of the rules requires a thorough understanding of the process to be controlled. Proposed FL controller can be characterised as follows:

- seven fuzzy sets for each input and output,
- triangular and trapezoidal membership functions for each input,
- constant membership function for the output,
- fuzzification using continuous universe of discourse,
- implication using the 'min' operator,
- Sugeno inference mechanism based on fuzzy implication and
- defuzzification using the 'wtaver' method.

The systematic approach presented in [17] is used for the analysis and design of proposed FLC. Membership functions are preliminarily selected as symmetrical and the approach proposed by Arslan and Lee [17] can be successfully applied to symmetrical membership functions. The error and error rate memberships are divided into five triangular and two trapezoidal fuzzy sets in width and this allows the operation to change gradually from one state to the next. With this scheme, the input state of variable no longer jumps abruptly from one state to the next. A certain amount of overlap is desirable otherwise the controller may run into poorly defined states, where it does not return a well-defined output.

Membership functions and rules are obtained from an understanding of DVR behaviour and application of systematic procedure presented in [17] and are modified and tuned by simulation performance. Rules table and the stability of the fine tuned controller with simulation performance are justified using the approach in [17].

The fuzzy control rules are generally set up by assigning an output fuzzy set to each of the fuzzy area in heuristic manner. According to [17], membership functions of I/O fuzzy sets and assignment of the control rules in the error phase plane are obtained as given in Fig. 3*a*. Fig. 3*b* shows the input and output membership functions of FL controller in Fig. 2:

1. Draw parallel lines $|\Delta\text{err} + \eta\text{err}| = 2\eta C_{\text{SP}}$ in the error phase plane.

2. Assign an output fuzzy set Z to the dotted points on $\Delta\text{err} + \eta\text{err} = 0$.

Assign an output fuzzy set NS to the dotted points in the inner region of $0 < \Delta\text{err} + \eta\text{err} \leq 2\eta C_{\text{SP}}$ and assign PS to the inner region of $2\eta C_{\text{SN}} \leq \Delta\text{err} + \eta\text{err} < 0$.

Assign an output fuzzy set NB to the dotted points above $\Delta\text{err} + \eta\text{err} = 2\eta C_{\text{SP}}$ and assign PB to the below of $\Delta\text{err} + \eta\text{err} = 2\eta C_{\text{SN}}$, where e is the error, Δe is the error rate, η is positive real number and C is the mean values of the corresponding fuzzy sets.

By following systematic assignment procedure, a stable and optimised rule table is obtained as presented in Table 1.

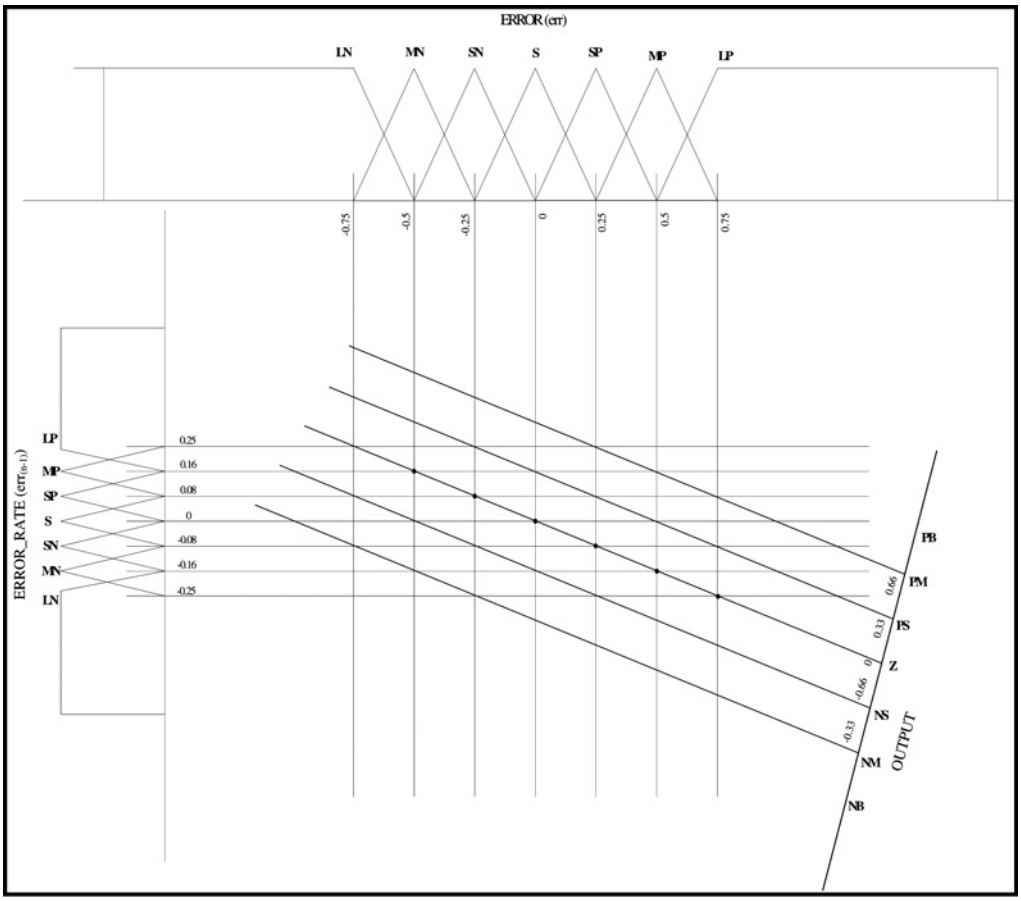
Fig. 3*a* shows that the rules table is optimised improving the fuzzy controller performance. The simulation results show the effectiveness and the robustness of the proposed method.

There are 49 rules to carry out optimum control action and each rule expresses an operating condition in the system. Forty-nine rules can guarantee acceptable and optimum control as in [18–21]. Extensive simulation results presented in Section 4 and supporting references [18–21] show that acceptable and robust controls for the designed systems are greatly achieved.

The output of FL controller is the reference variable for the PWM signal generator. The output of FL controller with changing amplitude and frequency passes through a comparator and is compared with a carrier signal at 5 kHz. When the FL output's magnitude exceeds carrier signal's magnitude, the PWM circuit produces high output. Conversely, when the FL output's magnitude is less than the carrier signal magnitude, PWM circuits produce low output. The magnitude of FL controller output is adjusted to take values -1 and 1 at 0.5 per unit voltage sag. The carrier signal is a saw tooth waveform at 5 kHz taking values between -0.7 and 0.7. The generation of switching signals for phase A is shown in Fig. 4. PWM pulse generation is enabled by the transfer signal from sag/swell detection block.

The upper relay element is set to give a logical value of 1 at the output when the input of itself is greater than 0. The output of lower relay is the complement of upper one.

During standby operation of DVR, two lower IGBTs of each phase H-bridge inverter remain turned on whereas the two upper IGBTs remain turned off, forming a short circuit across the secondary (inverter side) windings of the series transformer through L_{f} [22]. Thus, there is no need to use of bypass switches across the transformers.



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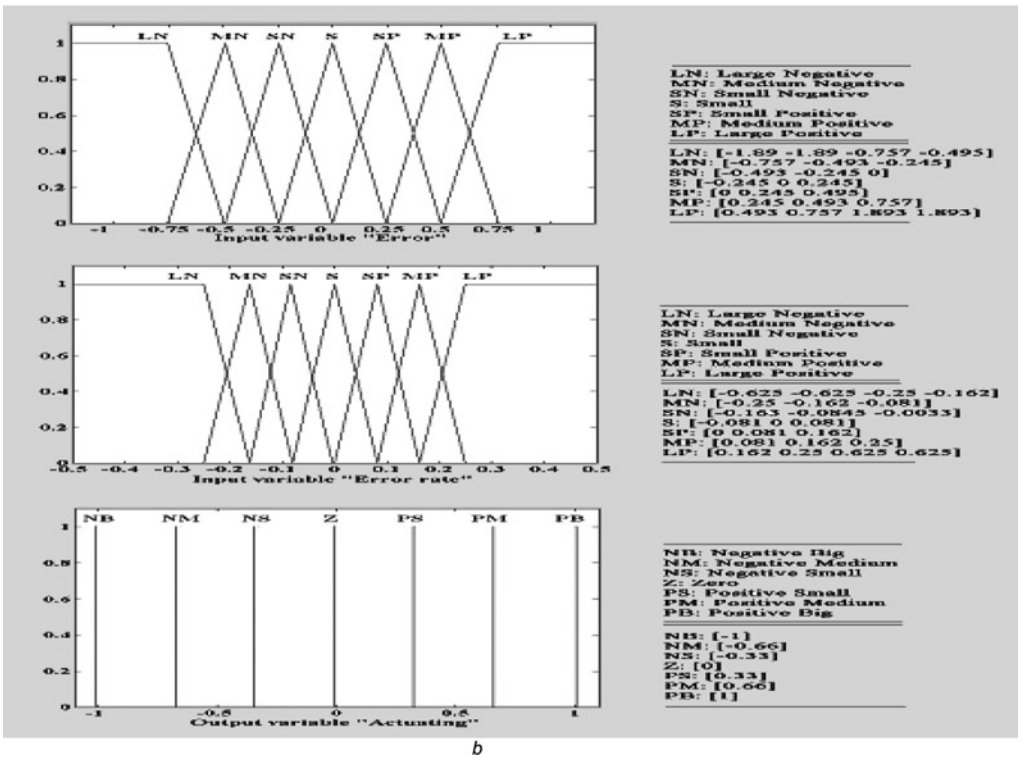

b

Figure 3 *Membership figures for input and output*

a Membership shapes of I/O fuzzy sets and assignment of the control rules in the error phase plane
b Membership functions for inputs and output

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Table 1 Fuzzy decision table

$e/\Delta e$	LP	MP	SP	S	SN	MN	LN
LP	PB	PB	PB	PM	PM	PS	Z
MP	PB	PB	PM	PM	PS	Z	NS
SP	PB	PM	PM	PS	Z	NS	NM
S	PM	PM	PS	Z	NS	NM	NM
SN	PM	PS	Z	NS	NM	NM	NB
MN	PS	Z	NS	NM	NM	NB	NB
LN	Z	NS	NM	NM	NB	NB	NB

Table 2 Simulation parameters

Parameter	Value
power supply	380 V_{rms} (line to line), 50 Hz
	supply resistance $R = 0.06\ \Omega$
sensitive load	380 V_{rms} (line to line), 3 kVA
single-phase injection transformer	55/110 V_{rms}, 1 kVA
	leakage inductance = 0.01 pu
DC link	85 V_{dc}
carrier frequency	5 kHz
inverter filter	inductance, $L_f = 7$ mH
	capacitance, $C_f = 28.4\ \mu$F

4 Simulation results

The performance of the designed DVR is evaluated using MATLAB/Simulink. Maximum single-phase injection capability of the DVR is 50% of nominal value. The total period of simulation for each case is 0.2 s and sample time is 20 μs. The design parameters are given in Table 2.

There are four possible types of faults that can occur in a typical power distribution system. The probabilities of prevalence of the various types of faults are as follows [23]:

1. single line-to-ground faults (SLGFs): 70%,
2. line-to-line faults: 15%,
3. double line-to-ground faults: 10% and
4. three-phase faults: 5%.

The case studies are performed taking the findings of [23] into consideration. Case studies evaluate the performance of proposed DVR from the point of view of sag/swell detection speed and compensation voltage quality. The fault circuit consisting of three-phase adjacent parallel loads creates balanced or unbalanced faults at desired time and magnitude.

4.1 Single line-to-ground fault

Most of the faults are SLGFs. In this case, the SLGF occurs on phase A of supply voltage resulting in 50% decrease from nominal value between the period 0.06 and 0.14 s. Fig. 5 shows the supply voltage, injected voltage (high-voltage side of the transformer) and load voltage.

Initially, there is no voltage injection and power flow from DVR to the system because no voltage sag is sensed. As soon as the sag starts, DVR produces the missing voltage so that the voltage sag does not affect the sensitive load. Table 3 summarises the total harmonic distortion (THD) and pu amplitude values of supply, injected and load voltages during fault.

The load voltage is nearly perfect sinusoid with low THD of 1.19%. The DVR can insert some harmonics to the sensitive load voltage because of oscillations between the filter inductance and filter capacitance.

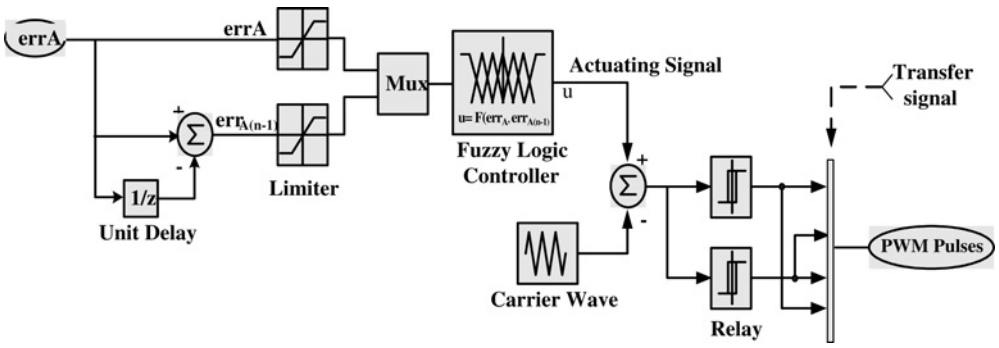

Figure 4 *Generation of PWM switching signals*

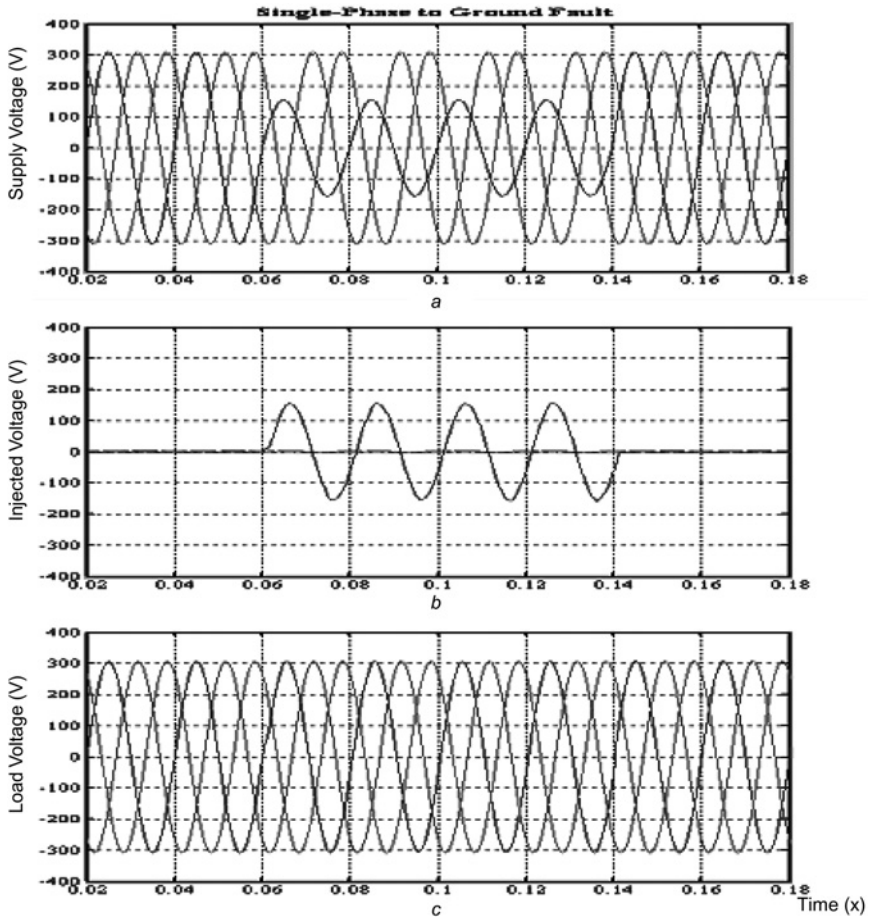

Figure 5 *Case 1: waveforms of the supply, injected and load voltages*

In this case study, the fault of 80 ms duration initiates at time $t_s = 0.06$ s and is cleared at time $t_c = 0.14$ s. The conventional detection method detects the starting time of the fault at 0.0633 s and ending time of the fault at 0.1475 s. With the proposed detection method, the starting and ending times of the fault are detected at 0.0605 and 0.1402 s, respectively. Voltage sag error and transfer signals for both methods are shown in Fig. 6.

Table 3 THD and pu values of measured voltages

Voltage	Supply	Injected	Load
Phase A			
THD, %	0.02	2.36	1.19
amplitude, pu	0.498	0.494	0.976
Phase B			
THD, %	0.01	0.01	0.01
amplitude, pu	0.997	0.012	0.986
Phase C			
THD, %	0.01	0.01	0.01
amplitude, pu	0.997	0.012	0.986

4.2 Line-to-line fault (voltage sag associated with phase angle jump)

In Case 2, the amplitudes of phase A and phase B supply voltages are both decreased to 40% from the nominal values with phase shift of 36° in both phases between the periods 0.06 and 0.14 s. Fig. 7 shows the supply voltage with 36° phase angle jump, the injected voltage and the load voltage.

It is apparent that the injected voltage is not in phase with the sagged voltage. The phase angle jump has been reduced to 4° as shown in Fig. 7*c*. Table 4 summarises the THD and pu amplitude values of supply, injected and load voltages during fault.

In this case study, the conventional detection method detects the starting time of the fault at 0.0615 s and ending time of the fault at 0.1469 s. With the proposed detection method, the starting and ending times of the fault are detected at 0.0601 and 0.1401 s, respectively. Voltage sag error and transfer signals for both methods are shown in Fig. 8.

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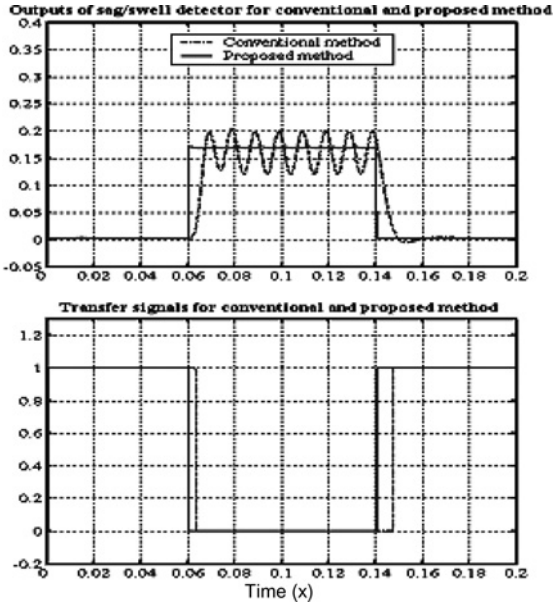

Figure 6 *Voltage sag error and transfer signals for conventional method and proposed method*

4.3 Voltage swell caused by SLGF

In Case 3, B phase and C phase supply voltages increase to 25% above their nominal values during the period 0.06–0.14 s. Fig. 9 shows the supply voltages, injected voltages and load voltages at double line swell.

Table 4 THD and pu values of measured voltages

Voltage	Supply	Injected	Load
Phase A			
THD, %	0.05	7.23	3.44
amplitude, pu	0.576	0.447	0.944
Phase B			
THD, %	0.04	5.76	3.84
amplitude, pu	0.576	0.626	0.938
Phase C			
THD, %	0.01	0.01	0.01
amplitude, pu	0.997	0.01	0.987

Table 5 summarises the THD and pu amplitude values of supply, injected and load voltages during fault. The results indicate the capability of DVR to deal with voltage swells.

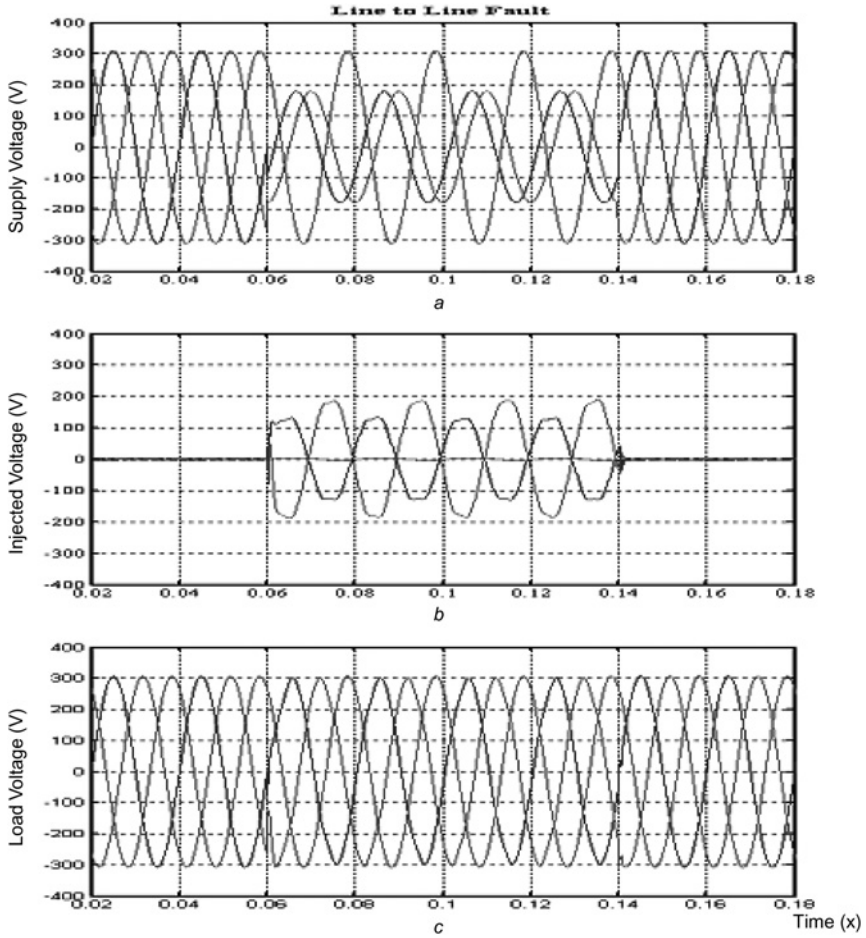

Figure 7 *Case 2: waveforms of the supply injected and load voltages*

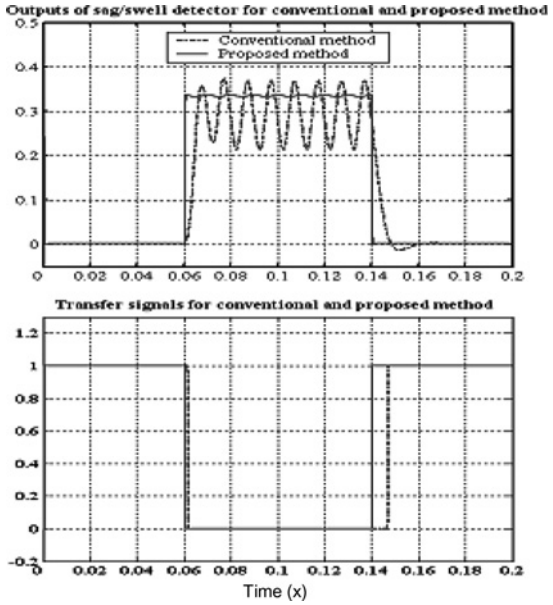

Figure 8 *Voltage sag error and transfer signals for conventional method and proposed method*

In Case 3, the conventional detection method detects the starting time of the fault at 0.0614 s and ending time of the fault at 0.1487 s. With the proposed detection method, the starting and ending times of the fault are detected at 0.0601 and 0.1402 s, respectively. Voltage swell error and transfer signals for both methods are shown in Fig. 10.

5 Discussion of case results

The proposed DVR was tested for three cases and it is shown that the accurate and quick compensation are provided with FL controlled DVR. According to EN 50160, the admissible maximum voltage variation should be within 10% of nominal value and voltage THD should be smaller than 8%. The load voltage magnitude between 0.916 and 0.987 pu and THD lower than 3.86% were obtained by using proper control strategy and applying a tuned LC filter in the circuit. Thus the results meet the recommended standard limits.

Throughout the simulation cases, rapidly damped oscillations can be observed in the load voltages at the starting and ending times of faults. This is caused by an instantaneous reduction of the voltage reference calculated by the feed forward part and/or the voltage angle when the fault occurs.

Another important point for reliable operation of DVR is fast fault detection in the system. The detection times for

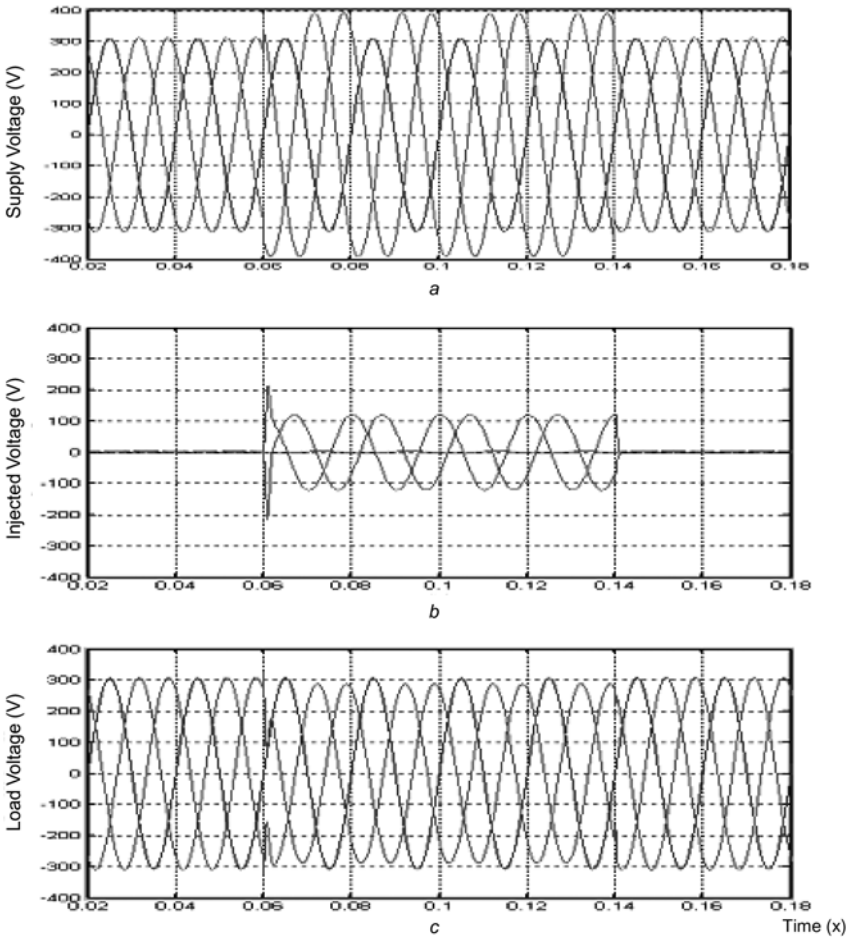

Figure 9 *Case 3: waveforms of the supply, injected and load voltages*

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Table 5 THD and pu values of measured voltages

Voltage	Supply	Injected	Load
Phase A			
THD, %	0.01	0.01	0.01
amplitude, pu	0.997	0.012	0.986
Phase B			
THD, %	0.02	5.16	2.19
amplitude, pu	1.25	0.392	0.921
Phase C			
THD, %	0.02	8.38	3.57
amplitude, pu	1.25	0.391	0.916

various fault types for both methods are summarised in Table 6.

The proposed method demonstrates better dynamic response and gives more accurate signal for tracking the disturbances than conventional method because a fast technique to detect the positive and the negative sequences is used. The method detects the fault start time about seven times more sensitive and the fault end time at least 14 times more sensitive than conventional detection method, respectively. The proposed method is superior to the conventional method with respect to suppressing the ripples on the error signal. Thus, the disoperation of switching elements during fault can be prevented and reliable control of non-linear and dynamic systems can be effectively satisfied.

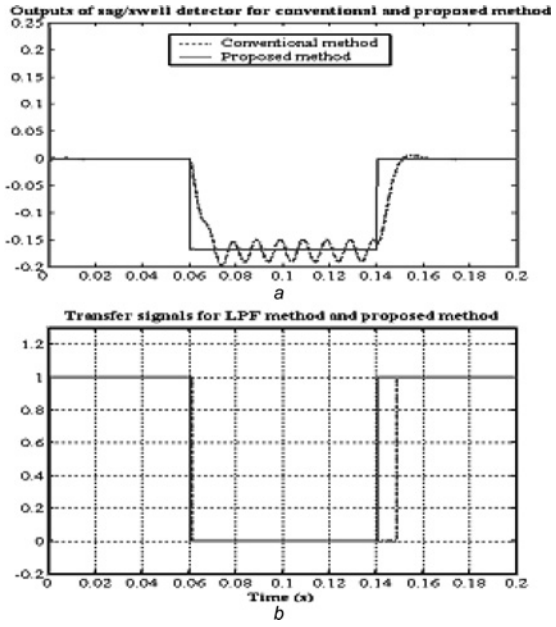

Figure 10 *Voltage swell error and transfer signals for conventional method and proposed method*

Table 6 Fault detection times in milliseconds for both methods

Sag/swell detection	Case 1		Case 2		Case 3	
	Start	End	Start	End	Start	End
conventional method	3.3	7.5	1.5	6.9	1.4	8.7
proposed method	0.5	0.2	0.1	0.1	0.1	0.2
improvement in milliseconds	2.8	7.3	1.5	6.8	1.3	8.5

6 Conclusions

This study aims to help the improvement of DVR technology by adopting new control approaches to the system. The integration of FL to the controller system of DVR eliminates the main drawbacks of conventional compensation methods such as slow transient response, necessity of complex mathematical modelling of the system and requirement of the transformation process. By applying successfully new sag/swell detection method to DVR, the DVR can quickly be switched online or offline and the compensation process can be simultaneously initiated.

The response and performance of the designed DVR are evaluated using MATLAB/Simulink by applying different test cases. THD and per unit values of the load voltage are always kept below the standard limits by using proper control strategy. This indicates that the designed system has superior performance to mitigate the balanced and unbalanced voltage sags and swells. The sag/swell start and end times were quickly detected with no oscillations. This ability of fast switching can also be used in static transfer switch to increase reliability in power systems.

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