Control of Reduced-Rating Dynamic Voltage Restorer With a Battery Energy Storage System

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***Abstract*—In this paper, different voltage injection schemes for dynamic voltage restorers (DVRs) are analyzed with particular focus on a new method used to minimize the rating of the voltage source converter (VSC) used in DVR. A new control technique is proposed to control the capacitor-supported DVR. The control of a DVR is demonstrated with a reduced-rating VSC. The reference load voltage is estimated using the unit vectors. The synchronous reference frame theory is used for the conversion of voltages from rotating vectors to the stationary frame. The compensation of the voltage sag, swell, and harmonics is demonstrated using a reduced-rating DVR.**

***Index Terms*—Dynamic voltage restorer (DVR), power quality, unit vector, voltage harmonics, voltage sag, voltage swell.**

I. Introduction

POWER QUALITY problems in the present-day distribution systems are addressed in the literature [1]–[6] due to the increased use of sensitive and critical equipment pieces such as communication network, process industries, and precise manufacturing processes. Power quality problems such as transients, sags, swells, and other distortions to the sinusoidal waveform of the supply voltage affect the performance of these equipment pieces. Technologies such as custom power devices are emerged to provide protection against power quality problems [2]. Custom power devices are mainly of three categories such as series-connected compensators known as dynamic voltage restorers (DVRs), shunt-connected compensators such as distribution static compensators, and a combination of series- and shunt-connected compensators known as unified power quality conditioner [2]–[6]. The DVR can regulate the load voltage from the problems such as sag, swell, and harmonics in the supply voltages. Hence, it can protect the critical consumer loads from tripping and consequent losses [2]. The custom power devices are developed and installed at consumer point to meet the power quality standards such as IEEE-519 [7].

Voltage sags in an electrical grid are not always possible to avoid because of the finite clearing time of the faults that cause the voltage sags and the propagation of sags from the transmission and distribution systems to the low-voltage loads. Voltage sags are the common reasons for interruption in production plants and for end-user equipment malfunctions in general. In particular, tripping of equipment in a production line can cause production interruption and significant costs due to loss of production. One solution to this problem is to make the equipment itself more tolerant to sags, either by intelligent control or by storing "ride-through" energy in the equipment. An alternative solution, instead of modifying each component in a plant to be tolerant against voltage sags, is to install a plantwide uninterruptible power supply system for longer power interruptions or a DVR on the incoming supply to mitigate voltage sags for shorter periods [8]–[23]. DVRs can eliminate most of the sags and minimize the risk of load tripping for very deep sags, but their main drawbacks are their standby losses, the equipment cost, and also the protection scheme required for downstream short circuits.

Many solutions and their problems using DVRs are reported, such as the voltages in a three-phase system are balanced [8] and an energy-optimized control of DVR is discussed in [10]. Industrial examples of DVRs are given in [11], and different control methods are analyzed for different types of voltage sags in [12]–[18]. A comparison of different topologies and control methods is presented for a DVR in [19]. The design of a capacitor-supported DVR that protects sag, swell, distortion, or unbalance in the supply voltages is discussed in [17]. The performance of a DVR with the high-frequency-link transformer is discussed in [24]. In this paper, the control and performance of a DVR are demonstrated with a reduced-rating voltage source converter (VSC). The synchronous reference frame (SRF) theory is used for the control of the DVR.

II. Operation of DVR

The schematic of a DVR-connected system is shown in Fig. 1(a). The voltage $V_{\rm inj}$ is inserted such that the load voltage $V_{\rm load}$ is constant in magnitude and is undistorted, although the supply voltage V_s is not constant in magnitude or is distorted. Fig. 1(b) shows the phasor diagram of different voltage

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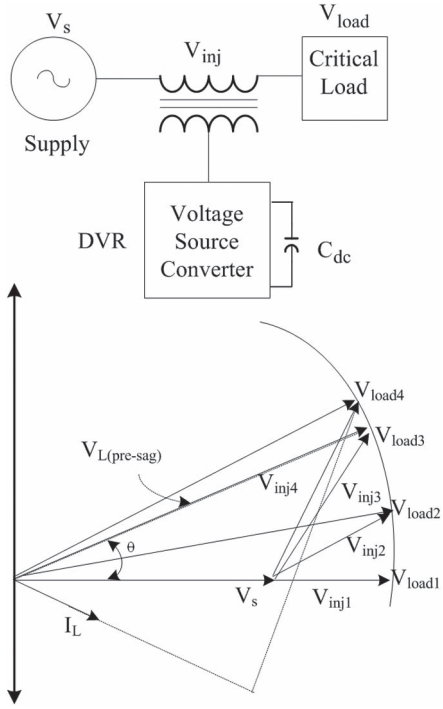

Fig. 1. (a) Basic circuit of DVR. (b) Phasor diagram of the DVR voltage injection schemes.

injection schemes of the DVR. $V_{L(\mathrm{pre-sag})}$ is a voltage across the critical load prior to the voltage sag condition. During the voltage sag, the voltage is reduced to V_s with a phase lag angle of θ. Now, the DVR injects a voltage such that the load voltage magnitude is maintained at the pre-sag condition. According to the phase angle of the load voltage, the injection of voltages can be realized in four ways [19]. V_{inj1} represents the voltage-injected in-phase with the supply voltage. With the injection of V_{inj2}, the load voltage magnitude remains same but it leads V_s by a small angle. In V_{inj3}, the load voltage retains the same phase as that of the pre-sag condition, which may be an optimum angle considering the energy source [10]. V_{inj4} is the condition where the injected voltage is in quadrature with the current, and this case is suitable for a capacitor-supported DVR as this injection involves no active power [17]. However, a minimum possible rating of the converter is achieved by V_{inj1}. The DVR is operated in this scheme with a battery energy storage system (BESS).

Fig. 2 shows a schematic of a three-phase DVR connected to restore the voltage of a three-phase critical load. A three-phase supply is connected to a critical and sensitive load through a three-phase series injection transformer. The equivalent voltage of the supply of phase A v_{Ma} is connected to the point of common coupling (PCC) v_{Sa} through short-circuit impedance Z_{sa}. The voltage injected by the DVR in phase A v_{Ca} is such that the load voltage v_{La} is of rated magnitude and undistorted. A three-phase DVR is connected to the line to inject a voltage in series using three single-phase transformers T_r. L_r and C_r represent the filter components used to filter the ripples in the injected voltage. A three-leg VSC with insulated-gate bipolar transistors (IGBTs) is used as a DVR, and a BESS is connected to its dc bus.

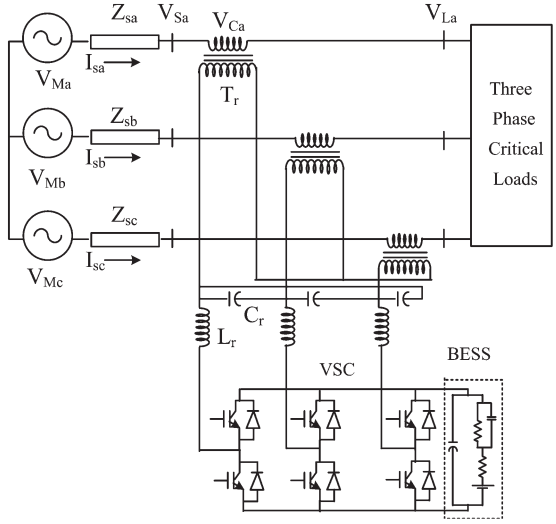

Fig. 2. Schematic of the DVR-connected system.

III. Control of DVR

The compensation for voltage sags using a DVR can be performed by injecting or absorbing the reactive power or the real power [17]. When the injected voltage is in quadrature with the current at the fundamental frequency, the compensation is made by injecting reactive power and the DVR is with a self-supported dc bus. However, if the injected voltage is in-phase with the current, DVR injects real power, and hence, a battery is required at the dc bus of the VSC. The control technique adopted should consider the limitations such as the voltage injection capability (converter and transformer rating) and optimization of the size of energy storage.

A. Control of DVR With BESS for Voltage Sag, Swell, and Harmonics Compensation

Fig. 3 shows a control block of the DVR in which the SRF theory is used for reference signal estimation. The voltages at the PCC v_S and at the load terminal v_L are sensed for deriving the IGBTs' gate signals. The reference load voltage V_L^* is extracted using the derived unit vector [23]. Load voltages (V_{La}, V_{Lb}, V_{Lc}) are converted to the rotating reference frame using $abc{-}dqo$ conversion using Park's transformation with unit vectors $(\sin, \theta, \cos, \theta)$ derived using a phase-locked loop as

$$\begin{bmatrix} v_{Lq} \\ v_{Ld} \\ v_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{La\mathrm{ref}} \\ v_{Lb\mathrm{ref}} \\ v_{Lc\mathrm{ref}} \end{bmatrix}. \quad (1)$$

Similarly, reference load voltages $(V_{La}^*, V_{Lb}^*, V_{Lc}^*)$ and voltages at the PCC v_S are also converted to the rotating reference frame. Then, the DVR voltages are obtained in the rotating reference frame as

$$v_{Dd} = v_{Sd} - v_{Ld} \quad (2)$$

$$v_{Dq} = v_{Sq} - v_{Lq}. \quad (3)$$

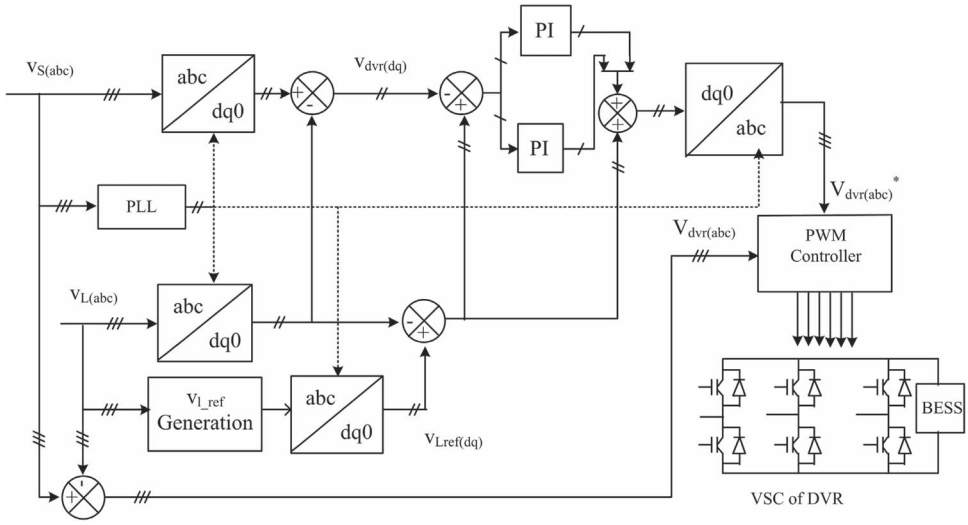

Fig. 3. Control block of the DVR that uses the SRF method of control.

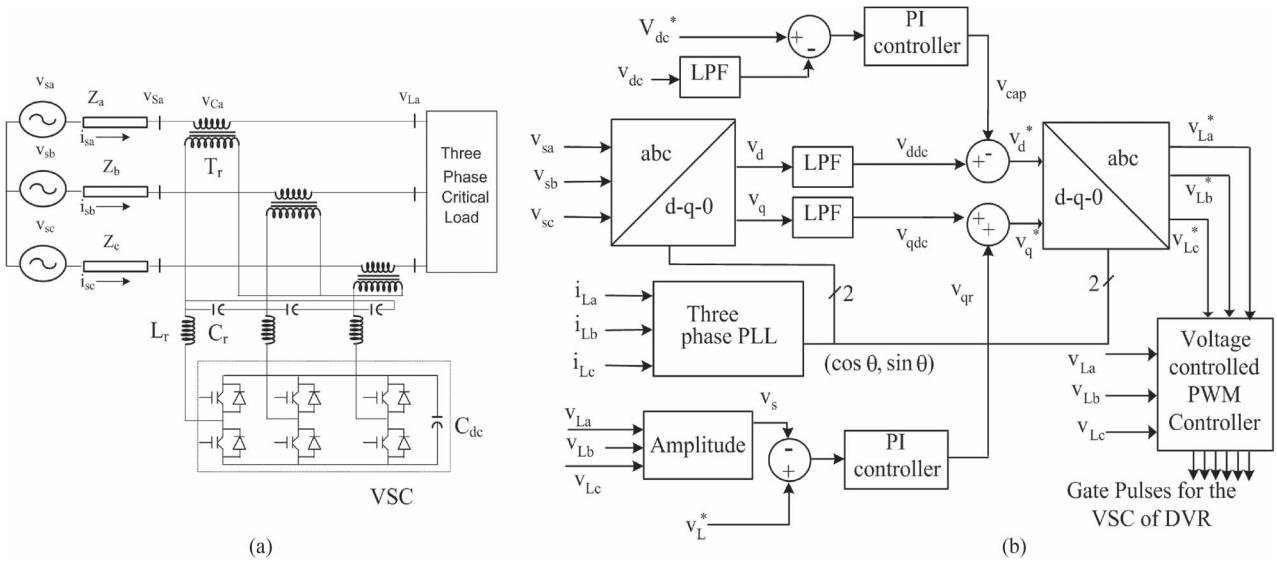

Fig. 4. (a) Schematic of the self-supported DVR. (b) Control block of the DVR that uses the SRF method of control.

The reference DVR voltages are obtained in the rotating reference frame as

$$v^*_{Dd} = v^*_{Sd} - v_{Ld} \tag{4}$$
$$v^*_{Dq} = v^*_{Sq} - v_{Lq}. \tag{5}$$

The error between the reference and actual DVR voltages in the rotating reference frame is regulated using two proportional–integral (PI) controllers.

Reference DVR voltages in the abc frame are obtained from a reverse Park's transformation taking V^*_{Dd} from (4), V^*_{Dq} from (5), V^*_{D0} as zero as

$$\begin{bmatrix} v^*_{\mathrm{dvr}a} \\ v^*_{\mathrm{dvr}b} \\ v^*_{\mathrm{dvr}c} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} v^*_{Dq} \\ v^*_{Dd} \\ v^*_{D0} \end{bmatrix}. \tag{6}$$

Reference DVR voltages $(v^*_{\mathrm{dvr}a}, v^*_{\mathrm{dvr}b}, v^*_{\mathrm{dvr}c})$ and actual DVR voltages $(v_{\mathrm{dvr}a}, v_{\mathrm{dvr}b}, v_{\mathrm{dvr}c})$ are used in a pulsewidth-modulated (PWM) controller to generate gating pulses to a VSC of the DVR. The PWM controller is operated with a switching frequency of 10 kHz.

B. Control of Self-Supported DVR for Voltage Sag, Swell, and Harmonics Compensation

Fig. 4(a) shows a schematic of a capacitor-supported DVR connected to three-phase critical loads, and Fig. 4(b) shows a control block of the DVR in which the SRF theory is used for the control of self-supported DVR. Voltages at the PCC v_S are converted to the rotating reference frame using $abc{-}dqo$ conversion using Park's transformation. The harmonics and the oscillatory components of the voltage are eliminated using low-pass filters (LPFs). The components of voltages in the d- and q-axes are

$$v_d = v_{d\mathrm{dc}} + v_{d\mathrm{ac}} \tag{7}$$
$$v_q = v_{q\mathrm{dc}} + v_{q\mathrm{ac}}. \tag{8}$$

The compensating strategy for compensation of voltage quality problems considers that the load terminal voltage should be of rated magnitude and undistorted.

In order to maintain the dc bus voltage of the self-supported capacitor, a PI controller is used at the dc bus voltage of the

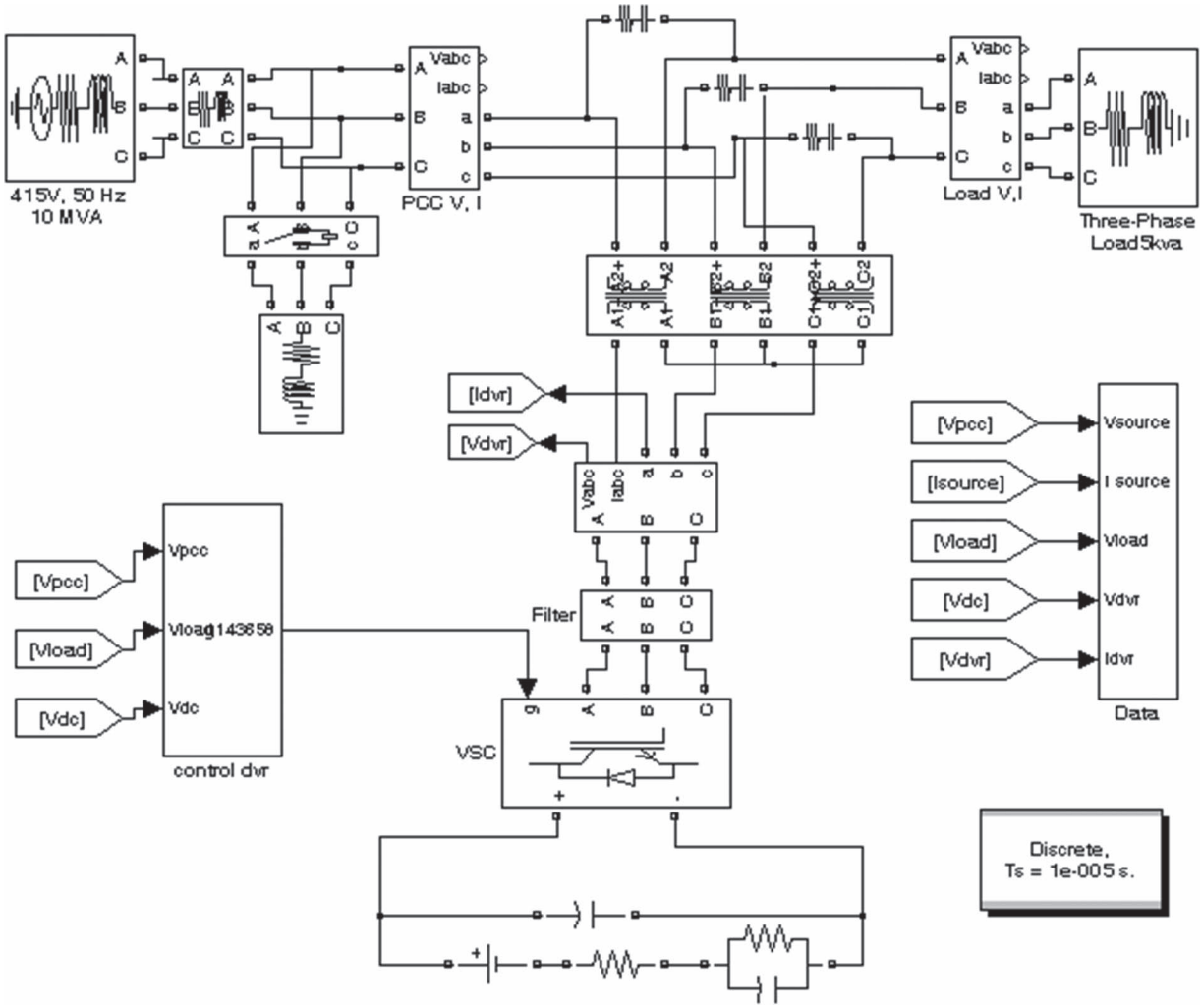

Fig. 5. MATLAB-based model of the BESS-supported DVR-connected system.

DVR and the output is considered as a voltage $v_{\rm cap}$ for meeting its losses

$$v_{{\rm cap}(n)} = v_{{\rm cap}(n-1)} + K_{p1}\left(v_{de(n)} - v_{de(n-1)}\right) + K_{i1} v_{de(n)} \quad (9)$$

where $v_{de(n)} = v^*_{\rm dc} - v_{{\rm dc}(n)}$ is the error between the reference $v^*_{\rm dc}$ and sensed dc voltages $v_{\rm dc}$ at the nth sampling instant. K_{p1} and K_{i1} are the proportional and the integral gains of the dc bus voltage PI controller.

The reference d-axis load voltage is therefore expressed as follows:

$$v^*_d = v_{d{\rm dc}} - v_{\rm cap}. \quad (10)$$

The amplitude of load terminal voltage V_L is controlled to its reference voltage V^*_L using another PI controller. The output of the PI controller is considered as the reactive component of voltage v_{qr} for voltage regulation of the load terminal voltage. The amplitude of load voltage V_L at the PCC is calculated from the ac voltages (v_{La}, v_{Lb}, v_{Lc}) as

$$V_L = (2/3)^{1/2}\left(v^2_{La} + v^2_{Lb} + v^2_{Lc}\right)^{1/2}. \quad (11)$$

Then, a PI controller is used to regulate this to a reference value as

$$v_{qr(n)} = v_{qr(n-1)} + K_{p2}\left(v_{te(n)} - v_{te(n-1)}\right) + K_{i2} v_{te(n)} \quad (12)$$

where $v_{te(n)} = V^*_L - V_{L(n)}$ denotes the error between the reference V^*_L and actual $V_{L(n)}$ load terminal voltage amplitudes at the nth sampling instant. K_{p2} and K_{i2} are the proportional and the integral gains of the dc bus voltage PI controller.

The reference load quadrature axis voltage is expressed as follows:

$$v^*_q = v_{q{\rm dc}} + v_{qr}. \quad (13)$$

Reference load voltages $(v^*_{La}, v^*_{Lb}, v^*_{Lc})$ in the abc frame are obtained from a reverse Park's transformation as in (6). The error between sensed load voltages (v_{La}, v_{Lb}, v_{Lc}) and reference load voltages is used over a controller to generate gating pulses to the VSC of the DVR.

IV. Modeling and Simulation

The DVR-connected system consisting of a three-phase supply, three-phase critical loads, and the series injection transformers shown in Fig. 2 is modeled in MATLAB/Simulink environment along with a sim power system toolbox and is shown in Fig. 5. An equivalent load considered is a 10-kVA 0.8-pf lag linear load. The parameters of the considered system for the simulation study are given in the Appendix.

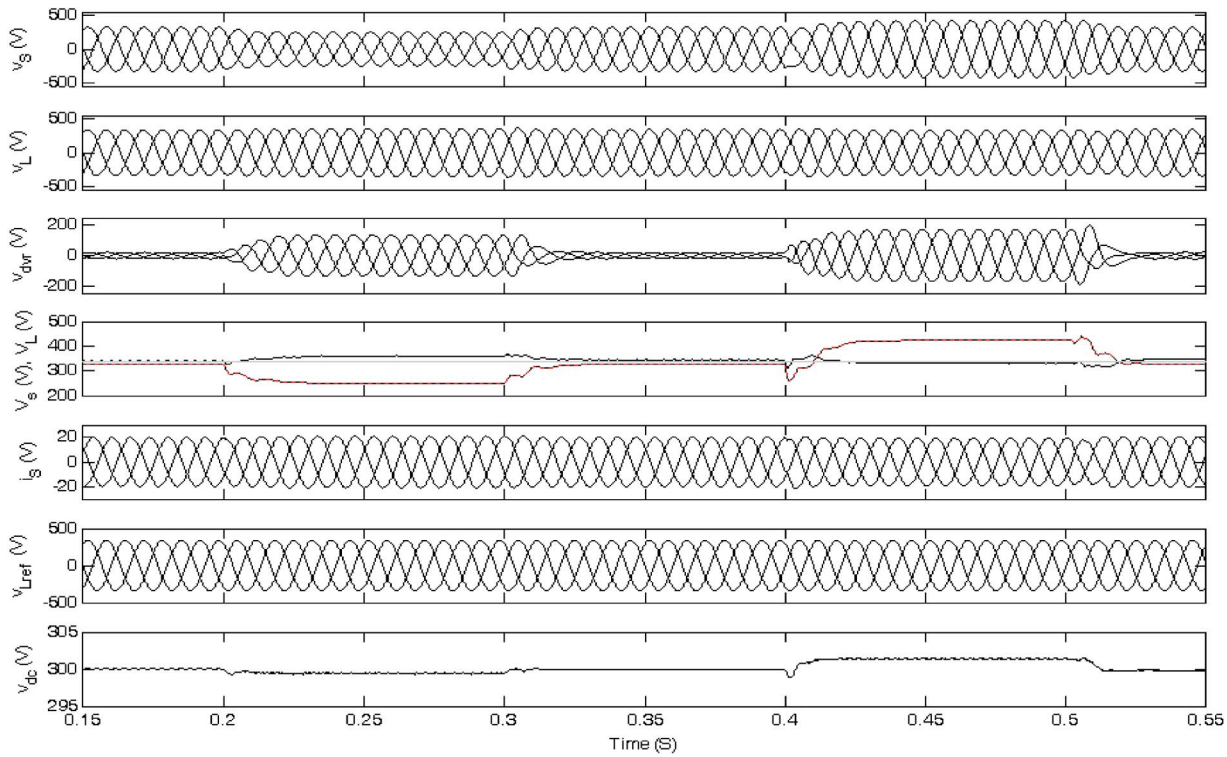

Fig. 6. Dynamic performance of DVR with in-phase injection during voltage sag and swell applied to critical load.

The control algorithm for the DVR shown in Fig. 3 is also modeled in MATLAB. The reference DVR voltages are derived from sensed PCC voltages $(v_{\rm sa}, v_{\rm sb}, v_{\rm sc})$ and load voltages (v_{La}, v_{Lb}, v_{Lc}). A PWM controller is used over the reference and sensed DVR voltages to generate the gating signals for the IGBTs of the VSC of the DVR.

The capacitor-supported DVR shown in Fig. 4 is also modeled and simulated in MATLAB, and the performances of the systems are compared in three conditions of the DVR.

V. Performance of the DVR System

The performance of the DVR is demonstrated for different supply voltage disturbances such as voltage sag and swell. Fig. 6 shows the transient performance of the system under voltage sag and voltage swell conditions. At 0.2 s, a sag in supply voltage is created for five cycles, and at 0.4 s, a swell in the supply voltages is created for five cycles. It is observed that the load voltage is regulated to constant amplitude under both sag and swell conditions. PCC voltages v_S, load voltages v_L, DVR voltages v_C, amplitude of load voltage V_L and PCC voltage V_s, source currents i_S, reference load voltages $v_{L\rm ref}$, and dc bus voltage $v_{\rm dc}$ are also depicted in Fig. 6. The load and PCC voltages of phase A are shown in Fig. 7, which shows the in-phase injection of voltage by the DVR. The compensation of harmonics in the supply voltages is demonstrated in Fig. 8. At 0.2 s, the supply voltage is distorted and continued for five cycles. The load voltage is maintained sinusoidal by injecting proper compensation voltage by the DVR. The total harmonics distortions (THDs) of the voltage at the PCC, supply current, and load voltage are shown in Figs. 9–11, respectively. It is observed that the load voltage THD is reduced to a level of 0.66% from the PCC voltage of 6.34%.

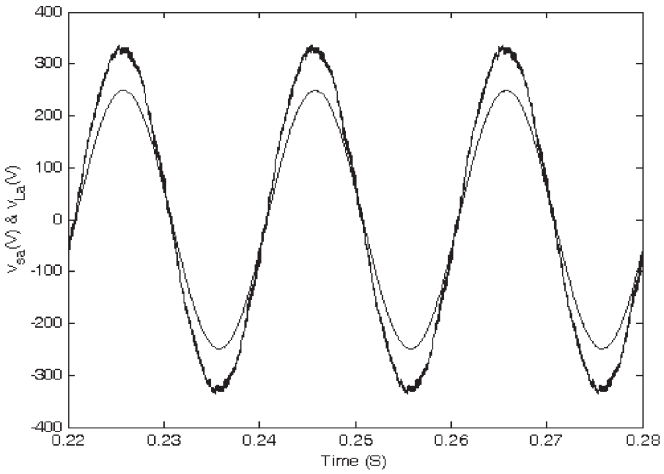

Fig. 7. Voltages at the PCC and load terminals.

The magnitudes of the voltage injected by the DVR for mitigating the same kinds of sag in the supply with different angles of injection are observed. The injected voltage, series current, and kilovoltampere ratings of the DVR for the four injection schemes are given in Table I. In Scheme-1 in Table I, the in-phase injected voltage is $V_{\rm inj1}$ in the phasor diagram in Fig. 1. In Scheme-2, a DVR voltage is injection at a small angle of 30°, and in Scheme-3, the DVR voltage is injected at an angle of 45°. The injection of voltage in quadrature with the line

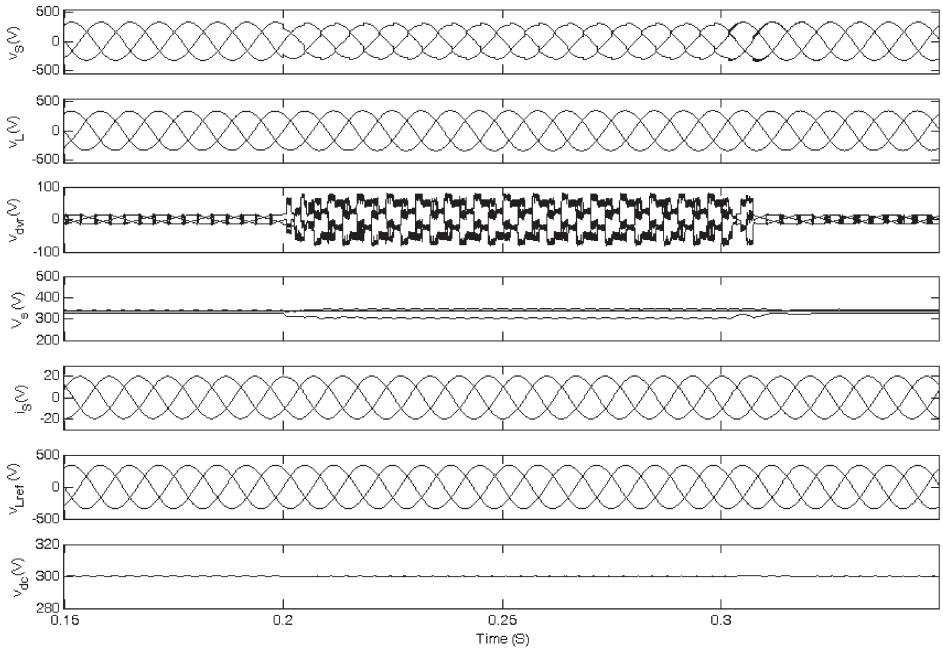

Fig. 8. Dynamic performance of DVR during harmonics in supply voltage applied to critical load.

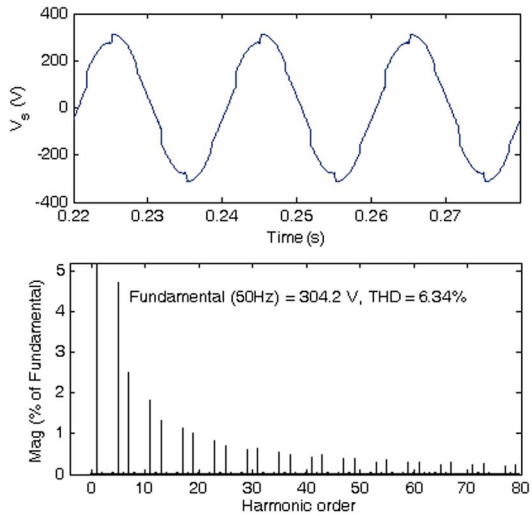

Fig. 9. PCC voltage and harmonic spectrum during the disturbance.

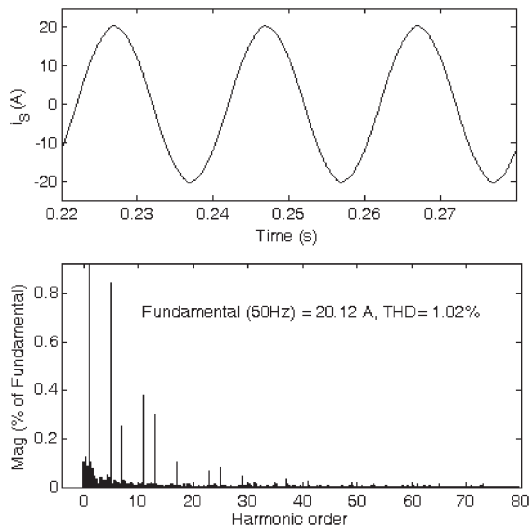

Fig. 10. Supply current and harmonic spectrum during the disturbance.

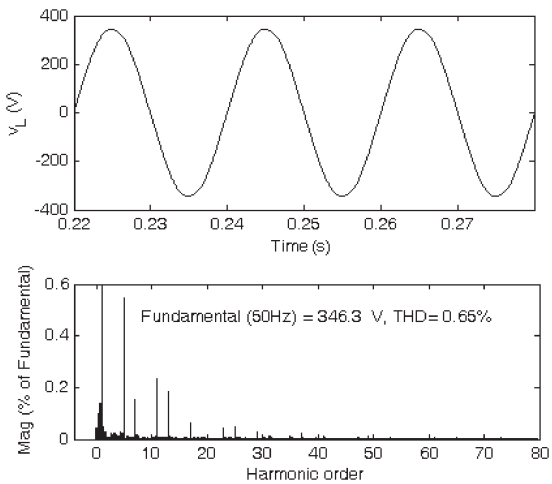

Fig. 11. Load voltage and harmonic spectrum during the disturbance.

TABLE I
COMPARISON OF DVR RATING FOR SAG MITIGATION

	Scheme-1	Scheme-2	Scheme-3	Scheme-4
Phase Voltage (V)	90	100	121	135
Phase Current (A)	13	13	13	13
VA per phase	1170	1300	1573	1755
KVA (% of Load)	37.5%	41.67%	50.42%	56.25%

current is in Scheme-4. The required rating of compensation of the same using Scheme-1 is much less than that of Scheme-4. The performance of the self-supported DVR (Scheme-4) for compensation of voltage sag is shown in Fig. 12(a) and that of a voltage swell is shown in Fig. 12(b). It is observed that the injected voltage is in quadrature with the supply current, and hence, a capacitor can support the dc bus of the DVR. However, the injected voltage is higher compared with an in-phase injected voltage (Scheme-1).

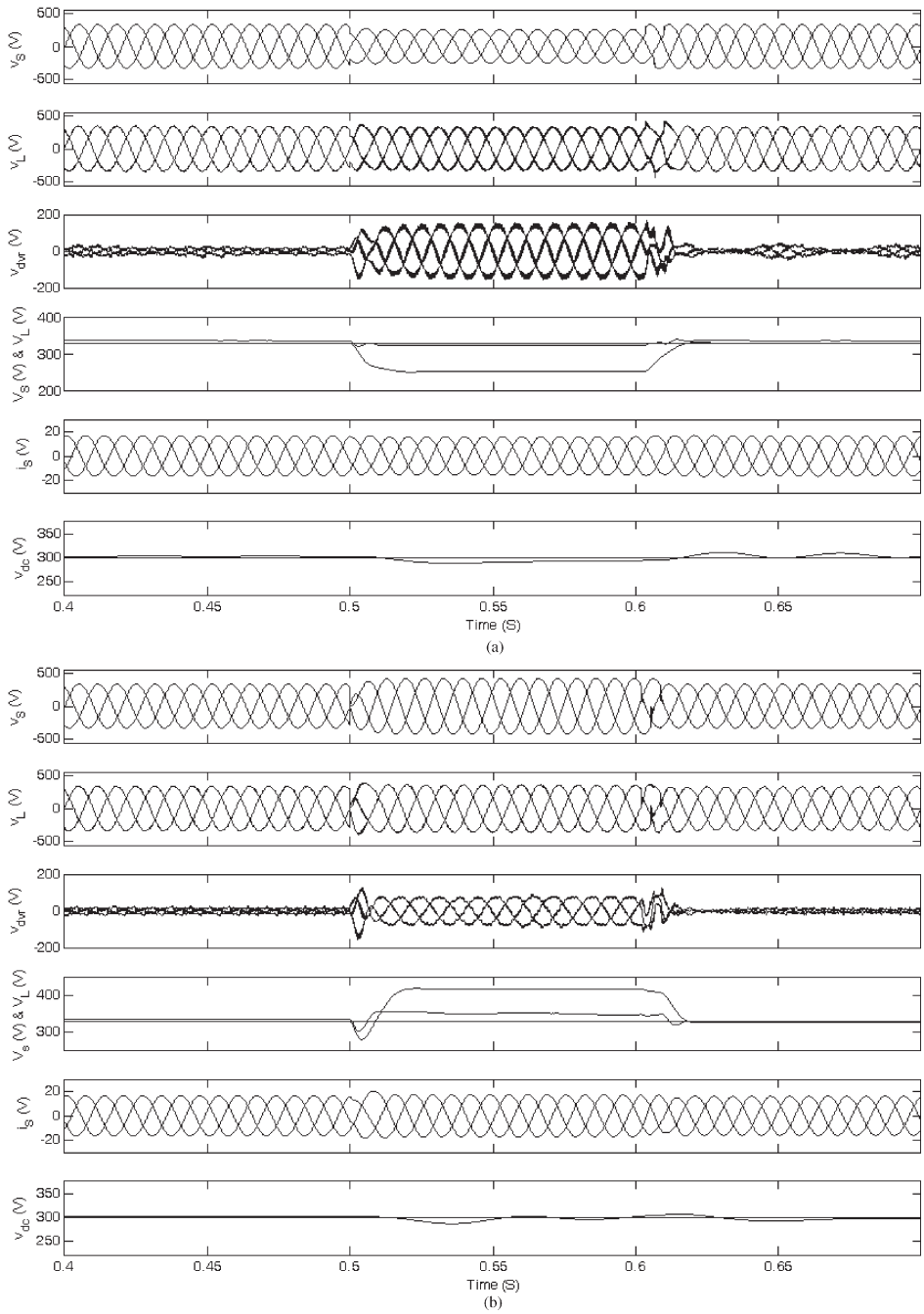

Fig. 12. Dynamic performance of the capacitor-supported DVR during (a) voltage sag and (b) voltage swell applied to critical load.

VI. Conclusion

The operation of a DVR has been demonstrated with a new control technique using various voltage injection schemes. A comparison of the performance of the DVR with different schemes has been performed with a reduced-rating VSC, including a capacitor-supported DVR. The reference load voltage has been estimated using the method of unit vectors, and the control of DVR has been achieved, which minimizes the error of voltage injection. The SRF theory has been used for estimating the reference DVR voltages. It is concluded that the voltage injection in-phase with the PCC voltage results in minimum rating of DVR but at the cost of an energy source at its dc bus.

Appendix

AC line voltage:	415 V, 50 Hz
Line impedance:	$L_s = 3.0$ mH, $R_s = 0.01\ \Omega$
Linear loads:	10-kVA 0.80-pf lag
Ripple filter:	$C_f = 10\ \mu$F, $R_f = 4.8\ \Omega$
DVR with BESS	
DC voltage of DVR:	300 V
AC inductor:	2.0 mH
Gains of the d-axis PI controller:	$K_{p1} = 0.5$, $K_{i1} = 0.35$
Gains of the q-axis PI controller:	$K_{p2} = 0.5$, $K_{i2} = 0.35$
PWM switching frequency:	10 kHz
DVR with dc bus capacitor supported	
DC voltage of DVR:	300 V

AC inductor:	2.0 mH
DC bus voltage PI controller:	$K_{p1} = 0.5$, $K_{i1} = 0.35$
AC load voltage PI controller:	$K_{p2} = 0.1$, $K_{i2} = 0.5$
PWM switching frequency:	10 kHz
Series transformer:	three-phase transformer of rating 10 kVA, 200 V/300 V.

REFERENCES

[1] M. H. J. Bollen, *Understanding Power Quality Problems—Voltage Sags and Interruptions*. New York, NY, USA: IEEE Press, 2000.

[2] A. Ghosh and G. Ledwich, *Power Quality Enhancement Using Custom Power Devices*. London, U.K.: Kluwer, 2002.

[3] M. H. J. Bollen and I. Gu, *Signal Processing of Power Quality Disturbances*. Hoboken, NJ, USA: Wiley-IEEE Press, 2006.

[4] R. C. Dugan, M. F. McGranaghan, and H. W. Beaty, *Electric Power Systems Quality*, 2nd ed. New York, NY, USA: McGraw-Hill, 2006.

[5] A. Moreno-Munoz, *Power Quality: Mitigation Technologies in a Distributed Environment*. London, U.K.: Springer-Verlag, 2007.

[6] K. R. Padiyar, *FACTS Controllers in Transmission and Distribution*. New Delhi, India: New Age Int., 2007.

[7] *IEEE Recommended Practices and Recommendations for Harmonics Control in Electric Power Systems*, IEEE Std. 519, 1992.

[8] V. B. Bhavraju and P. N. Enjeti, "An active line conditioner to balance voltages in a three phase system," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 287–292, Mar./Apr. 1996.

[9] S. Middlekauff and E. Collins, "System and customer impact," *IEEE Trans. Power Del.*, vol. 13, no. 1, pp. 278–282, Jan. 1998.

[10] M. Vilathgamuwa, R. Perera, S. Choi, and K. Tseng, "Control of energy optimized dynamic voltage restorer," in *Proc. IEEE IECON*, 1999, vol. 2, pp. 873–878.

[11] J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," in *Proc. IEEE APEC*, 2001, vol. 2, pp. 1267–1273.

[12] A. Ghosh and G. Ledwich, "Compensation of distribution system voltage using DVR," *IEEE Trans. Power Del.*, vol. 17, no. 4, pp. 1030–1036, Oct. 2002.

[13] A. Ghosh and A. Joshi, "A new algorithm for the generation of reference voltages of a DVR using the method of instantaneous symmetrical components," *IEEE Power Eng. Rev.*, vol. 22, no. 1, pp. 63–65, Jan. 2002.

[14] I.-Y. Chung, D.-J. Won, S.-Y. Park, S.-I. Moon, and J.-K. Park, "The DC link energy control method in dynamic voltage restorer system," *Int. J. Elect. Power Energy Syst.*, vol. 25, no. 7, pp. 525–531, Sep. 2003.

[15] E. C. Aeloíza, P. N. Enjeti, L. A. Morán, O. C. Montero-Hernandez, and S. Kim, "Analysis and design of a new voltage sag compensator for critical loads in electrical power distribution systems," *IEEE Trans. Ind. Appl.*, vol. 39, no. 4, pp. 1143–1150, Jul./Aug. 2003.

[16] J. W. Liu, S. S. Choi, and S. Chen, "Design of step dynamic voltage regulator for power quality enhancement," *IEEE Trans. Power Del.*, vol. 18, no. 4, pp. 1403–1409, Oct. 2003.

[17] A. Ghosh, A. K. Jindal, and A. Joshi, "Design of a capacitor supported dynamic voltage restorer for unbalanced and distorted loads," *IEEE Trans. Power Del.*, vol. 19, no. 1, pp. 405–413, Jan. 2004.

[18] A. Ghosh, "Performance study of two different compensating devices in a custom power park," *Proc. Inst. Elect. Eng.—Gener., Transm. Distrib.*, vol. 152, no. 4, pp. 521–528, Jul. 2005.

[19] J. G. Nielsen and F. Blaabjerg, "A detailed comparison of system topologies for dynamic voltage restorers," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1272–1280, Sep./Oct. 2005.

[20] M. R. Banaei, S. H. Hosseini, S. Khanmohamadi, and G. B. Gharehpetian, "Verification of a new energy control strategy for dynamic voltage restorer by simulation," *Simul. Model. Pract. Theory*, vol. 14, no. 2, pp. 112–125, Feb. 2006.

[21] A. K. Jindal, A. Ghosh, and A. Joshi, "Critical load bus voltage control using DVR under system frequency variation," *Elect. Power Syst. Res.*, vol. 78, no. 2, pp. 255–263, Feb. 2008.

[22] D. M. Vilathgamuwa, H. M. Wijekoon, and S. S. Choi, "A novel technique to compensate voltage sags in multiline distribution system—The interline dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1603–1611, Oct. 2006.

[23] A. Chandra, B. Singh, B. N. Singh, and K. Al-Haddad, "An improved control algorithm of shunt active filter for voltage regulation, harmonic elimination, power-factor correction, and balancing of nonlinear loads," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 495–507, May 2000.

[24] A. Y. Goharrizi, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Three-phase HFL-DVR with independently controlled phases," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1706–1718, Apr. 2012.

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