Instantaneous-Power-Based Busbar Numerical Differential Protection

Francis A. Moreno Vásquez and Kleber M. Silva, *Member, IEEE*

***Abstract*—This paper presents a new method for busbar differential protection based on the instantaneous power concept. In order to do so, the instantaneous power per phase of each network element connected to the busbar is computed by using the instantaneous current values and a voltage memory action strategy. The performance of the proposed technique is compared to one of the traditional instantaneous-current-based differential protection algorithms, which is widely used by manufacturers of commercial relays. Both internal and external faults, as well as evolving external-to-internal faults, were simulated in a power substation with double-bus single-breaker configuration using the software ATPDraw. The obtained results reveal that the proposed algorithm is twice or more faster than the traditional instantaneous-current-based algorithm for most of the internal and evolving external-to-internal faults, while ensuring secure operation for external ones even when severe current transformer (CT) saturation takes place, through a new harmonic power restraint strategy. Also, since the proposed method provides faster fault detection time, the requirements for CT time to saturate may be alleviated, guaranteeing correct operation even in the case of early CT saturation.**

***Index Terms*—Busbars protection, differential protection, instantaneous power differential protection.**

I. Introduction

In THE last years, the capacity of generation and transmission systems has risen to supply the growing demand for affordable energy. Consequently, the busbars have become a critical component of power system insofar as rated voltage is higher, and more bays are connected to them. Therefore, modern busbar protection schemes must be used to improve speed, security and selectivity in fault clearance, reducing the disturbance footprint [1], [2].

Traditionally, the busbar differential protection is based on either high or low impedance schemes [3], [4]. The high impedance one is very robust for CT saturation, but it neither properly handles multiple CT ratios nor allows to share CTs. Moreover, since all the CTs within the protection zone must have their secondary circuitry physically connected, the high impedance differential element is applied only for simple busbar configurations. On the other hand, nowadays, modern low impedance differential relays have been widely used for both simple and complex busbar arrangements, since it can easily deal with dynamic zone reconfiguration and multiple CT ratios. Also, since measured currents are handled via software, this scheme can be used in both centralized and distributed bus protection architecture straightforwardly.

An advanced busbar relaying system is reported in [5], based on instantaneous values and phasor quantities of currents as well. Another works have proposed to estimate the power system source impedance, either directly obtained from currents and voltages measurements [6] or by calculating their positive- and negative-sequence values [7], thereby internal and external faults in busbar can be properly discriminated. On the other hand, the polarity of superimposed currents of transmission lines connected to busbars was used in [8] to distinguish external and internal faults. Also, some techniques have been reported to avoid false trip command issuing during external faults with CT saturation by means of either blocking the trip command [9] or using a CT secondary current waveform compensation algorithm [10].

Alternatively, some authors have evaluated the amplitude and polarity of traveling waves of currents to single out bus-connected faulted lines [11], [12]. Moreover, in [13]–[17], different wavelet-based schemes were used to analyze high frequencies transient components generated by faults. Despite these methods provides ultra-high-fast operating times for internal faults and security for external ones, their performance are jeopardized whenever transients are over-damped. That is the why manufactures have not been used transient-based methods in standalone protection schemes yet [18].

Another promising schemes that have been still little explored in power system protection are based upon directional and differential power-based concept. In fact, even though some protective algorithms of motors [19], generators [20] and transformers [21], [22] have been formulated based on that, its use for busbar protection has not been reported yet.

In this context, this paper presents a new differential busbar protection scheme based on the instantaneous power concept. The proposed tripping logics are inspired in the well-known 1-out-of-1 and 2-out-of-2 logics commonly used in commercial busbar protection relays. As a byproduct, a new harmonic power restraint strategy is also proposed to be used during external faults. Through a comparison with the performance of the traditional instantaneous-current-based algorithm, the obtained

Manuscript received May 4, 2018; revised September 1, 2018 and November 19, 2018; accepted January 22, 2019. Date of publication January 29, 2019; date of current version March 22, 2019. This work was supported in part by the Brazilian Coordination for Improvement of Higher Education Personnel (Capes) and in part by the Brazilian Federal District Research Foundation (FAPDF). Paper no. TPWRD-00497-2018. *(Corresponding author: Francis A. Moreno Vasquez.)*

The authors are with the Department of Electrical Engineering, University of Brasilia, Brasília 70910-900, Brazil (e-mail: francisarody@gmail.com; klebermelo@unb.br).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPWRD.2019.2896035

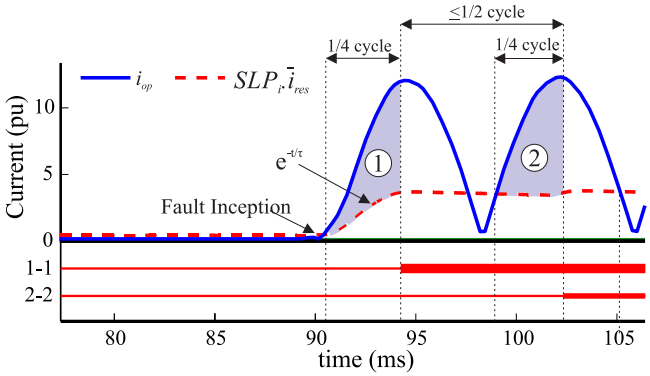

Fig. 1. Plotting i_{op} and $\bar{i}_{res}$ for an internal fault.

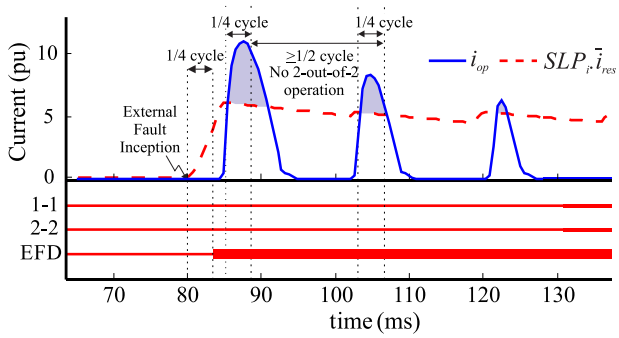

Fig. 2. Plotting i_{op} and $\bar{i}_{res}$ for an external fault with CT saturation.

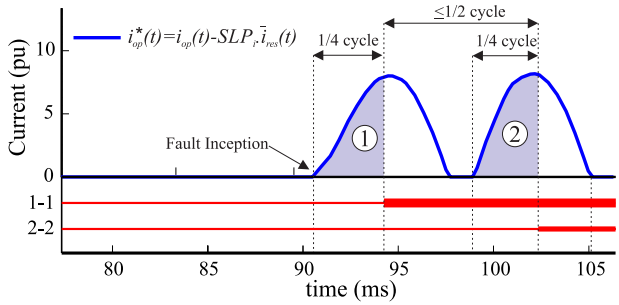

Fig. 3. Instantaneous-current-based operation lobes for the internal fault depicted in Fig. 1.

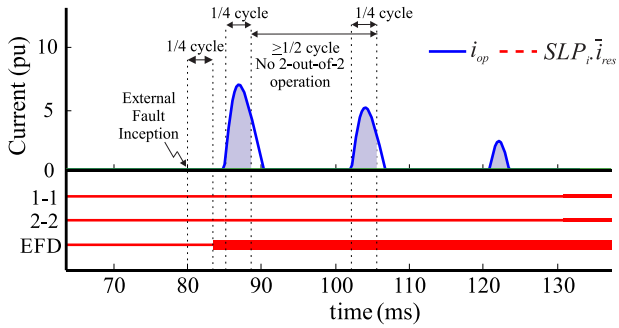

Fig. 4. Instantaneous-current-based operation lobes for the external fault depicted in Fig. 2.

results reveal that the proposed method has a faster response for internal and evolving external-to-internal faults, besides providing security for external faults, even when early and severe CT saturation takes place. Therefore, it has proven to be quite suitable for real-world numerical busbar differential protection applications.

II. Traditional Instantaneous-Current-Based Differential Busbar Protection

The traditional busbar differential protection function (ANSI code 87B) computes the operating current, i_{op}, and the restraint current, i_{res}, as follows:

$$i_{op} = \left| \sum_{r=1}^{R} i_r \right| \quad \text{and} \quad i_{res} = \sum_{r=1}^{R} |i_r| \,, \tag{1}$$

where i_r represents the current in the r-th element and R the total number of network elements connected to the busbar. Initially, the trip command is sent if i_{op} is higher than a minimum pickup value, and greater than a percentage value of i_{res}. These two parameters are set considering the CTs ratios mismatch and saturation. However, i_{res} could be affected by severe external faults which can eventually saturate the CT, causing instabilities on algorithm and leading to relay misoperation. Therefore, its smoothed version, $\bar{i}_{res}$, is obtained by means of a filtering process, as described by [23], [24].

The traditional 87B function detects an internal fault if the aforementioned tripping conditions are satisfied during 1/4 cycle after the fault inception (i.e., one count after fault inception), as illustrated in Fig. 1. Indeed, this is the minimum time before CT saturation takes place [24]. In this case, the trip command is sent by the fast operation logic 1-out-of-1.

Conversely, when an external fault takes place, usually $\bar{i}_{res}$ promptly raises its value and i_{op} kept almost unchanged. Nonetheless, if the CT saturates, i_{op} increases during the saturation periods (Fig. 2) and may become larger than $SLP \cdot \bar{i}_{res}$, what may cause relay false trip [24]. Therefore, an external fault can be identified if i_{op} does not increase before the CT time to saturate (1/4 cycle). In this case, 87B function activates the secure operation mode during 150 ms, in which the fast logic is blocked. However, the protective scheme must provide an additional strategy to detect evolving external-to-internal faults. In this regard, the backup logic 2-out-of-2 verifies if the tripping conditions are met for two consecutive lobes spaced by a time less than and equal to 1/2 cycle (Fig. 1).

Aiming to better illustrate the operating conditions, hereafter the current $i^*_{op}(t) = i_{op}(t) - SLP_i \cdot \bar{i}_{res}(t)$ is analyzed instead of i_{op} and $\bar{i}_{res}$ individually. For instance, in Fig. 3, it is shown $i^*_{op}(t)$ computed for the case of the internal fault of the Fig. 1, whereas in Fig. 4 it is shown $i^*_{op}(t)$ correspondent to the case of external fault with CT saturation shown in Fig. 2.

III. Proposed Instantaneous-Power-Based Busbar Protection Algorithm

A. Overview

Considering a sinusoidal ideal voltage source with phase angle equal to zero, $v(t) = \sqrt{2}V sin(\omega t)$, connected to a predominantly inductive load, the current can be defined by

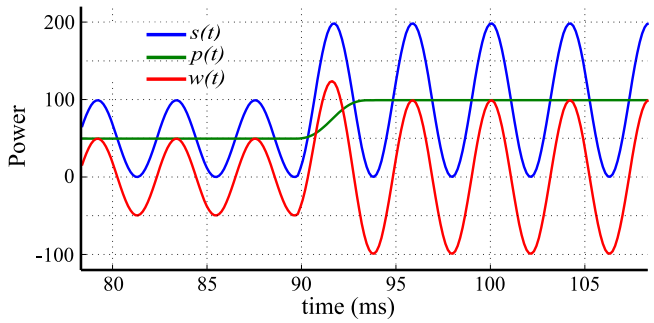

Fig. 5. Instantaneous power composition.

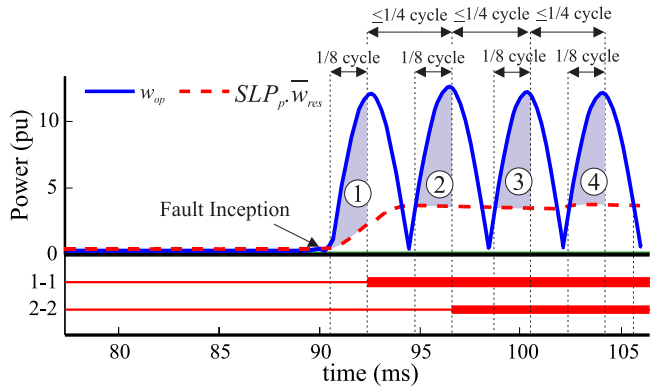

Fig. 6. Plotting w_{op} and $\overline{w}_{res}$ for an internal fault.

$i(t) = \sqrt{2}Isin(\omega t - \theta_{vi})$, where θ_{vi} is the power angle. Therefore, the instantaneous power $s(t)$ can be expressed as:

$$s(t) = v(t) \cdot i(t) = VIcos\theta_{vi} - VIcos(2\omega t - \theta_{vi}). \quad (2)$$

As one can see from (2), $s(t)$ has an alternate component that oscillates at twice the fundamental frequency of the system, added to an average value, which represents the active power $p(t) = VIcos\theta_{vi}$.

The waveform of $s(t)$ during a fault is illustrated in Fig. 5, assuming that the decaying dc component in the current signal is perfectly removed. Besides, the suitable application of the instantaneous power concept into differential protection depends on having a zero-average-value signal, aiming to calculate the operating and restraint quantities. That is achieved by removing $p(t)$ from $s(t)$, i.e. $w(t) = s(t) - p(t)$, as shown in Fig. 5. Therefore, the operating power (w_{op}), the restraint power (w_{res}) and its smoothed version ($\overline{w}_{res}$) can be calculated similarly to the instantaneous-current-based algorithm described in (1) using $w(t)$ rather than $i(t)$. Even so, one ought to bear in mind that the active power removing procedure requires 1/2 cycle data window, so that during the transient period that comprises 1/2 cycle after the fault inception, the active power may not be perfectly removed.

Taking advantage of having a signal that oscillates at twice the fundamental frequency of the system, the well-known tripping logics 1-out-of-1 and 2-out-of-2 can be adapted to use power signals instead of current signals, in order to issue a trip command for internal faults in an eighth cycle (two times faster ideally), as shown in Fig. 6. By the way, the operating lobes with this strategy are better addressed by plotting

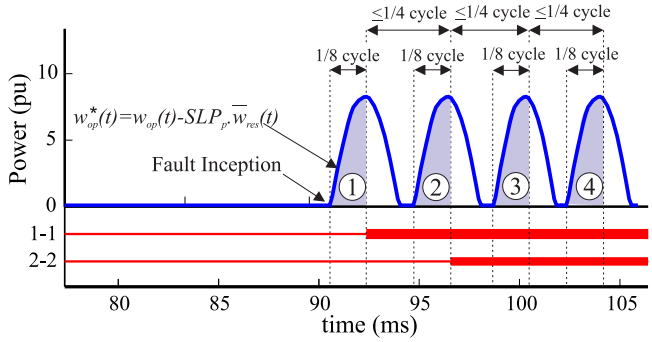

Fig. 7. Instantaneous-power-based operating lobes for the internal fault depicted in Fig. 6.

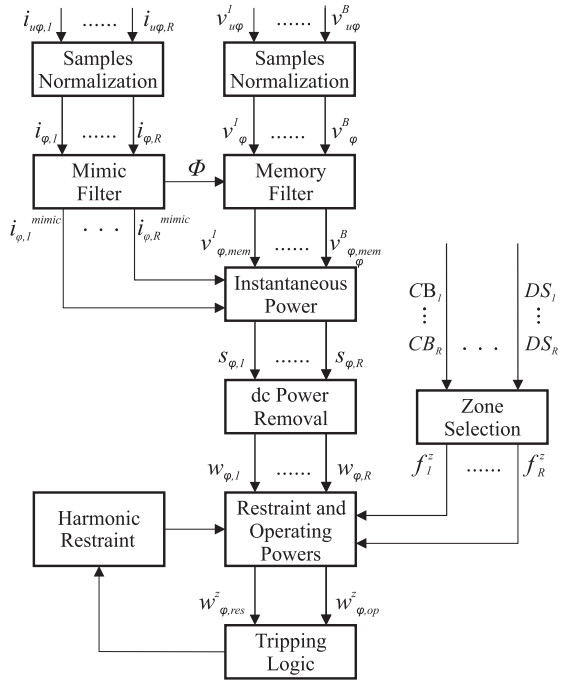

Fig. 8. Flowchart of the proposed 87BP protection scheme.

$w^*_{op}(t) = w_{op}(t) - SLP_p \cdot \overline{w}_{res}(t)$, as shown in Fig. 7. Likewise, the elimination of an evolving external-to-internal fault by using the adapted logic 2-out-of-2 is possible through the verification of the presence of two consecutive operating lobes, within 1/4 cycle. As a result, an instantaneous-power-based differential protection system provides counting double lobes if compared with traditional instantaneous-current-based algorithm in a same interval, ideally reducing the tripping times by a half, irrespectively to the fault type. It is noteworthy to point out that the proposed scheme is based on the differential principle, in such way that the phase angles θ_{vi} of the instantaneous-power signals, shown in (2), are not required.

B. Overall Description of the Proposed Scheme

The block diagram shown in Fig. 8 summarizes the overall process of the proposed scheme. The subscript φ represents the phase quantities, since low-impedance differential busbar protection is phase-segregated. Basically, the original currents signals $i_{u\varphi,r}$ of the r-th network element are firstly normalized

to compensate CT ratio mismatch. Then, the digital mimic filter is used to eliminate the decaying dc component from current signals. The voltage signals $v^b_{u\varphi}$ at the bus b, in turn, pass through a memory filter, in order to overcome voltage drop that may arise when faults take place. After that, the per phase-instantaneous powers, $s_{\varphi,r}$, are calculated considering the zone selection logic, evaluating the status of circuit breakers (CBs) and disconnect switches (DSs). Then, the average dc power is extracted, aiming to correctly calculate the operating power w_{op} and the restraint power w_{res}, which are used as inputs of the proposed tripping logics. Moreover, an innovative harmonic restraint scheme is used to improve protection security during external faults with CT saturation.

C. Samples Normalization

The low impedance protection scheme allows the use of CTs with different ratios because the individual secondary currents can be normalized in the same base through internal calculations in modern relays [25].

In that sense, to compensate CT ratio mismatches, the current signals $i_{u\varphi,r}$ are divided by $TAP_{i,r}$, resulting the normalized current signals $i_{\varphi,r}$ in per unit:

$$TAP_{i,r} = \frac{CTR_{MAX} I_{NOM}}{CTR_r}, \tag{3}$$

where CTR_{MAX} and I_{NOM} are the large ratio among the installed CTs and its nominal secondary current, respectively, and CTR_r is the CT ratio of the corresponding terminal.

Analogously, the normalized voltages signals v^b_φ are obtained dividing the voltage signals $v^b_{u\varphi}$ by TAP^b_v defined as:

$$TAP^b_v = \frac{V_{NOM}}{VTR_b}, \tag{4}$$

where V_{NOM} is the nominal voltage rate of system and VTR_b is the ratio of either voltage transformer (VT) or coupling capacitor voltage transformer (CCVT) installed at bus b.

D. Digital Mimic Filter

From (2), one can see that in the case of voltages and currents are pure sinusoidal signals with the same frequency, the instantaneous power is computed as a double-frequency sinusoidal signal plus an average value. However, when a fault takes place, a decaying dc component arises in current signal, in such way that a non-periodic component is added to the instantaneous power, resulting in a complete distorted signal. Therefore, to properly use the instantaneous power concept in differential protection applications, this decaying dc component must be gotten rid off. Aiming to do so, the traditional digital mimic filter is applied to $i_{\varphi,r}$ [26], resulting in the filtered current $i^{mimic}_{\varphi,r}$. Nevertheless, it introduces a phase shift angle ϕ, which can be calculated as:

$$\phi = \arctan\left[\frac{\tau_d \sin\delta}{(1+\tau_d) - \tau_d \cos\delta}\right], \tag{5}$$

where τ_d is decaying time constant of the filter and $\delta = 2\pi/N$ is the digital angular frequency, being N the number of samples per cycle at the fundamental frequency.

E. Memory Filter

Whenever a fault takes place in a busbar, its voltage may collapse, leading to instantaneous power equal to zero. In order to overcome this drawback, a voltage memory action is performed in the proposed scheme. Firstly, the voltage phasor $\widehat{V}^b_\varphi$ at phase φ of the bus b is estimated. Here, it is done by using the modified cosine filter [27]. Then, the memorized voltage $\widehat{V}^b_{\varphi,mem} = V^b_{\varphi,mem}\angle\theta^b_{\varphi,mem}$ is computed by using the following memory filter [28]:

$$\widehat{V}^b_{\varphi,mem}[k] = \alpha\widehat{V}^b_\varphi[k] + (1-\alpha)\widehat{V}^b_{\varphi,mem}[k-1], \tag{6}$$

with the vanishing factor α obtained by

$$\alpha = \frac{1}{MN+1}, \tag{7}$$

where M is the decaying time constant of the memory filter in number of cycles. Also, since in the proposed scheme the digital mimic filter is applied only to current signals, its phase shift angle must be added to $\bar{V}^b_{\varphi,mem}$, avoiding that a false power factor arises. Therefore, the instantaneous memorized voltage signal $v^b_{\varphi,mem}$ at phase φ of the bus b is obtained as:

$$v^b_{\varphi,mem}[k] = V^b_{\varphi,mem}\cos(k\delta + \theta^b_{\varphi,mem} + \phi). \tag{8}$$

F. Instantaneous Power Calculation

The instantaneous power $s^b_{\varphi,r}$ of the phase φ at the network element r connected to the bus b can be computed as:

$$s^b_{\varphi,r}[k] = v^b_{\varphi,mem}[k] \cdot i^{mimic}_{\varphi,r}[k], \tag{9}$$

which still includes a dc power level that must be removed.

G. DC Power Removal

As described in Section III-A, in order to correctly calculate the operating and restraint powers, the dc power must be removed from $s^b_{\varphi,r}$ as follows:

$$w^b_{\varphi,r}[k] = s^b_{\varphi,r}[k] - \frac{2}{N}\sum_{n=1}^{N/2} s^b_{\varphi,r}[k - N/2 + n], \tag{10}$$

where the second term represents the average value of $s^b_{\varphi,r}$ within a moving data window whose length is equal to $N/2$.

H. Zone Selection

The zone selection is performed by means of enabling flags f^z_r which are obtained from the status of circuit breakers and disconnecting switches for a network element r connected to the busbar, thereby measured currents are removed or included in a bus zone z. Aiming to aid the reader, a thorough example of zone selection logics for a double bus single breaker arrangement proposed by the IEEE Power System Relaying Committee is readily available in [1]. Also, it is noteworthy to point out that zone selection logics are segregated per phase, requiring the status of each circuit breaker pole and the contacts of disconnecting switches in each phase [29].

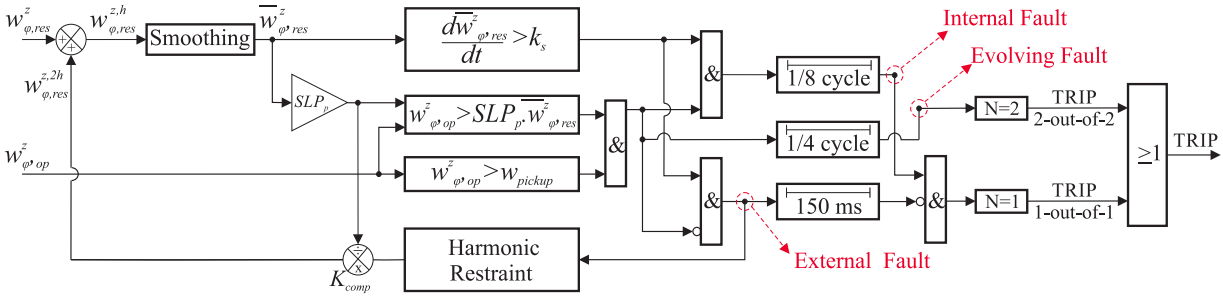

Fig. 9. Tripping logic of the proposed 87BP protection scheme.

I. Operating and Restraint Powers

The operating power, $w^z_{\varphi,op}$, and the restraint power, $w^z_{\varphi,res}$, are calculated as follows:

$$w^z_{\varphi,op}[k] = \left| \sum_{r=1}^{R} f^z_r w^b_{\varphi,r}[k] \right| \tag{11}$$

$$w^z_{\varphi,res}[k] = \sum_{r=1}^{R} \left| f^z_r w^b_{\varphi,r}[k] \right|. \tag{12}$$

Similarly to current-based algorithm, a smoothed restraint power $\bar{w}^z_{\phi,res}$ is used, whose time constant being the half of the value considered in traditional function 87B.

J. Harmonic Restraint

During CT saturation, harmonic components arise in current signals [24]. Not to mention that, once the proposed scheme uses the digital mimic filter (which is a high-pass filter [26]), this harmonic content becomes larger. When this phenomena takes place, the distortion of the secondary current causes the appearance of an operation current lobe in each saturation period, as explained in Sec. II. A similar behavior can be seen in instantaneous-power signals. In this case, $s(t)$ is distorted and the extraction of DC power, $p(t)$, leads to obtain a distorted $w(t)$ also. From this signal, the result of $w^z_{\varphi,op} - SLP.w^z_{\varphi,res}$ is the emergence of two operation lobes during each CT saturation period, as seen in Fig. 10. That represents a risk for the relay security because the time interval between these lobes could be lesser than the minimum time to declare an internal fault through the logic 2-out-of-2, i.e., 1/4 of cycle. Therefore, for the sake of security, the restraint power is further reinforce through a sort of second harmonic restraint power, as discussed next.

Basically, the 2nd harmonic component $\widehat{I}_{2h} = I_{2h}\angle\theta_{2h}$ is estimated for each phase φ at the network element r connected to the bus b. Thereby, a virtual current signal i_{2h} with frequency equal to the fundamental frequency of the system is reconstructed:

$$i_{2h}[k] = I_{2h}[k]\cos\left(k\delta + \theta_{2h}[k]\right). \tag{13}$$

The virtual 2nd harmonic power is computed by the product of i_{2h} and the memorized voltage signals $v^b_{\varphi,mem}$. Then, its average value is removed and the harmonic restraint power, $w^{z,2h}_{\varphi,res}$, is calculated. This value is used to reinforce $w^z_{\varphi,res}$ only when an external fault occurs, so that restraint signal to be

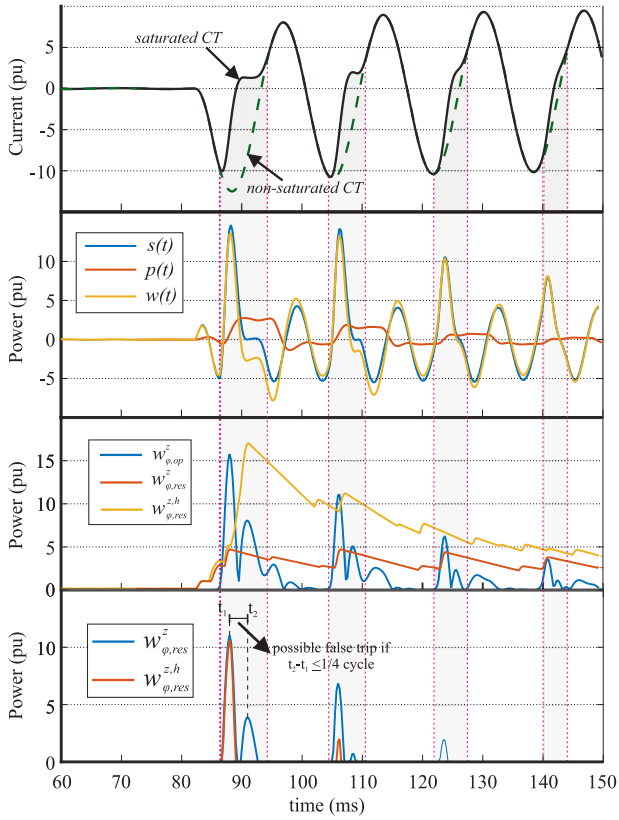

Fig. 10. Comparison between w^*_{op} with and without 2nd harmonic restraint strategy during an external fault with CT saturation.

smoothed can be now expressed by

$$w^{z,h}_{\varphi,res}[k] = w^z_{\varphi,res}[k] + \frac{K_{comp}}{SLP_p} w^{z,2h}_{\varphi,res}[k], \tag{14}$$

where K_{comp} is a percentage of the 2nd harmonic power. As a result, lobes, w^*_{op}, that arises when CT saturation takes place during external faults are reduced, as illustrated in Fig. 10, avoiding false trip command issuing. It is important to highlight that in this figure the lobes of w^*_{op} do not take place during the whole saturation periods, because they exist only when $w_{op} > SLP_p \cdot \overline{w}_{res}$ (See Sec. III-B).

K. Tripping Logic

The proposed tripping logic is illustrated in Fig. 9. It uses the operating power $w^z_{\varphi,op}$ and smoothed restraint power $\bar{w}^z_{\varphi,res}$ in

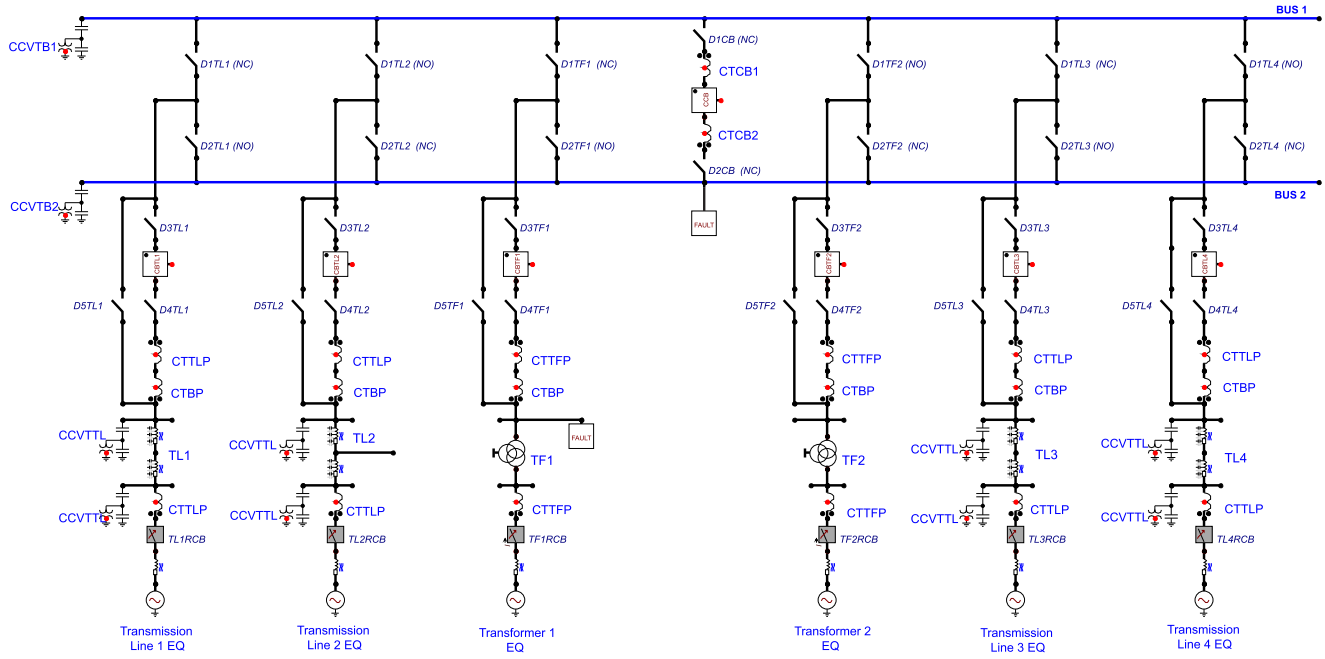

Fig. 11. Single-line diagram of the evaluated double busbar single breaker arrangement.

a similar way to instantaneous-current-values in traditional 87B protection function, but the particularities of power signals are taking into account, as discussed next.

1) Disturbance detector (DD): The first step is to implement a disturbance detector by identifying severe variations of $\bar{w}^z_{\varphi,res}$ through,

$$d\bar{w}^z_{\varphi,res}[k] = \left| \frac{\bar{w}^z_{\varphi,res}[k] - \bar{w}^z_{\varphi,res}[k-1]}{dt} \right|. \quad (15)$$

The signals, $\bar{w}^z_{\varphi,res}$, are used for transient detection because they appear in both internal and external faults. Its value must be greater than a minimum value, k_s, given in pu/s.

2) External fault detector (EFD): If disturbance detector is activated, the proposed scheme verify if the operational conditions are met:

$$w^z_{\varphi,op} > w_{min} \text{ and } w^z_{\varphi,op} > SLP_p.\bar{w}^z_{\varphi,res}, \quad (16)$$

where w_{min} is a minimum value of $w^z_{\varphi,op}$. If this condition does not occur at first eighth cycle, the external fault flag, EFD, is activated and the proposed scheme starts the secure operation mode, thereby the trip 1-out-of-1 is blocked during 150 ms. Also, during this time, the harmonic restraint strategy is activated.

3) Logic 1-out-of-1: If $w^z_{\varphi,op}$ immediately increases after disturbance detection, the hypothesis of an external fault is discarded and faster trip logic, 1-out-of-1, will be ready to operate. For that to happen, it must be verified that operational conditions (16) are met during an eighth cycle (Fig. 7).

4) Logic 2-out-of-2: Whenever an external fault is detected and the secure operation mode is activated, the trip command is only issued by the 2-out-of-2 logic. For that, the following operational conditions must be met for two consecutive operation lobes, with a maximum interval of 1/4 cycle (Fig. 7):

$$w^z_{\varphi,op} > w_{min} \text{ and } w^z_{\varphi,op} > SLP_p.\bar{w}^{z,h}_{\varphi,res}. \quad (17)$$

As one can see, the difference between the operational conditions (16) and (17) lies in the fact that in the last the reinforced restraint power $\bar{w}^{z,h}_{\varphi,res}$ defined in (14) is used rather than $\bar{w}^z_{\varphi,res}$, since an external fault has been detected.

IV. Power System Description

The proposed scheme, here properly named as 87BP protection function, was compared with the traditional instantaneous current-based 87B function using fault signals simulated in in the 230 kV/60 Hz power system model shown in Fig. 11. For the sake of simplicity, the proposed scheme takes into account the adaptive logics of bus zone selection for a double bus single breaker arrangement reported by the IEEE Power System Relaying Committee in [1]. During the normal operation condition, it is considered that the transmission lines $TL1$ and $TL3$, as well as the power transformer $TF1$, are connected to Bus 1, whereas the transmission lines $TL2$ and $TL4$, and the transformer $TF2$ are connected to Bus 2. Moreover, each downstream power system is connected to the remote terminal of each branch, and they are represented by Thevenin equivalent circuits. The models for CTs and CCVTs are those reported in [30]. Some of the obtained results are presented next. Firstly, the results for three case studies are presented: internal fault, external fault with CT saturation and evolving external-to-internal fault. Then, a massive data analysis was carried out, considering both internal and evolving faults.

TABLE I
OPERATION TIMES FOR AN INTERNAL THREE PHASE FAULT

Logic	Phase A	Phase B	Phase C
87BP 1-1	2.08	3.64	2.08
87B 1-1	4.68	4.42	4.42
87BP 2-2	6.25	7.81	5.46
87B 2-2	24.73	22.39	9.11

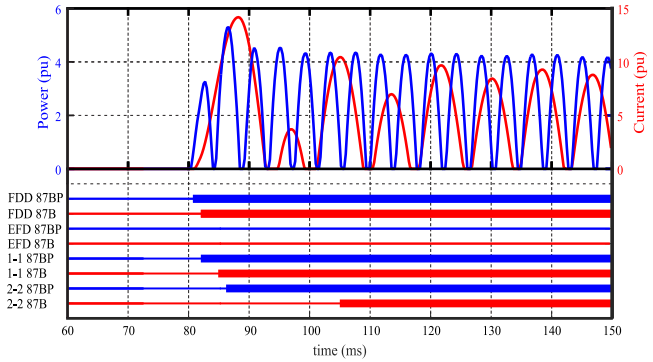

Fig. 12. ω_{op}^{*} and i_{op}^{*} in phase A for an internal three phase fault.

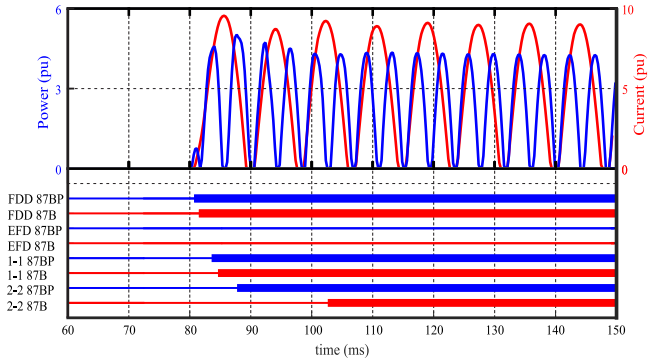

Fig. 13. ω_{op}^{*} and i_{op}^{*} in phase B for an internal three phase fault.

V. PERFORMANCE ANALYSIS

A. Internal Fault

In this case, a three phase fault is simulated at 80 ms at Bus 1. The operating times are summarized in Table I, revealing that the proposed 87BP function is really faster than the traditional 87B function. The performance of 87BP and 87B functions are shown in Fig. 12, 13 and 14 for each phase element. As one can see, the proposed scheme is approximately two times faster than 87B, because the time spent for having one lobe in current signals encompasses two lobes in power signals (see Fig. 14). Also, since the decaying dc component removal is not performed in the traditional 87B function, the lobes of current signals alternate between high and low levels, what may delay the trip command issued by logic 2-out-of-2 (Figs. 12 and 13).

B. External Fault With CT Saturation

In order to show the effect of CT saturation, a close-in external AG fault in the TL1 was simulated at 80 ms. The external

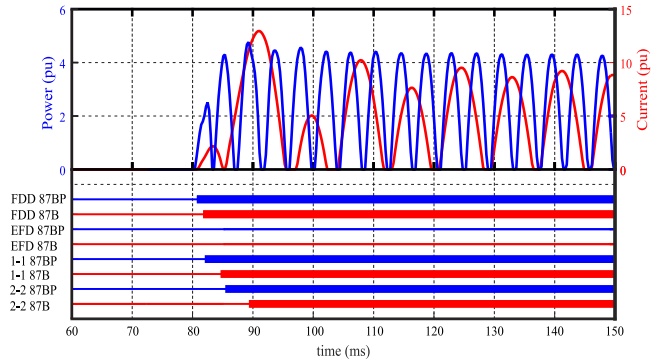

Fig. 14. ω_{op}^{*} and i_{op}^{*} in phase C for an internal three phase fault.

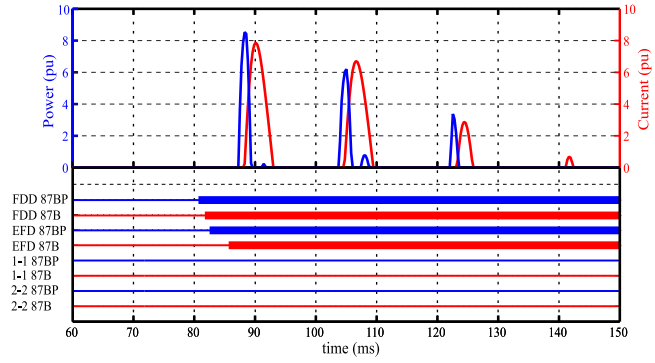

Fig. 15. ω_{op}^{*} and i_{op}^{*} in phase A for an external AG fault with CT saturation.

fault is detected by 87PB and 87B functions at 82.29 ms and 85.41 ms, respectively, before the CT saturation (see Fig. 15). Then, the secure operation mode is activated in both functions. As one can see, even though operating lobes arise due to CT saturation, the 2-out-of-2 logic is not met and no false trip command is issued. It is noteworthy to point out that the proposed harmonic restraint strategy guarantees a more safer operation of the proposed scheme.

It is important to mention that a CT correctly dimensioned must satisfy the requirement of the minimum CT time to saturate to ensure the proper operation of the relay. Ideally, this time must be at least 4 ms [24]. Nevertheless, nowadays some relays available in the market already requires that this time is not lesser than 2 ms [25], [31]. That means the proposed method is technically suitable for implementation in real world application. In turn, late saturation cases do not represent an important concern for proposed method because the operation power does not increase in first 1/8 cycle, so the logic 1-out-of-1 is blocked. Additionally, the relay would not operate with 2-out-of-2 logic because the restraint signal would be reinforced by the harmonic component.

C. Evolving Fault

In this case, it was simulated the same AG external fault described in Sec. V-B, but here it evolves to an internal ABG fault at 102 ms. Since the secure operation mode was enabled in

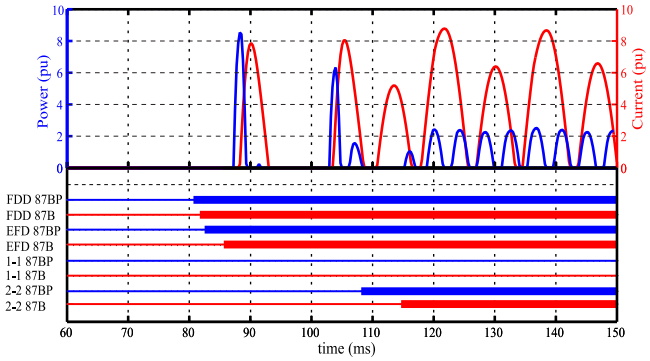

Fig. 16. ω^*_{op} and i^*_{op} in phase A for an external AG fault with CT saturation, that evolves to an ABG internal fault.

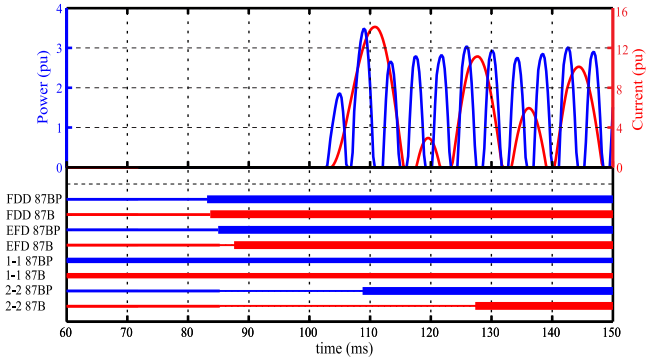

Fig. 17. ω^*_{op} and i^*_{op} in phase B for an external AG fault with CT saturation, that evolves to an ABG internal fault.

both 87BP and 87B functions, the trip command is only issued by the 2-out-of-2 logic. Fig. 16 shows the performance of the phase A elements. As can be seen, the proposed 2-out-of-2 logic detects the internal fault in phase A at 107.8 ms, where as the function 87B detects the same fault only at 114.32 ms. Indeed, due to the decaying dc component effect, the lobes of current signals alternate between high and low levels, delaying the trip command issuing very much. Fig. 17, in turn, shows the performance of the phase B elements. These elements also detect external fault, in such way that both 87BP and 87B functions activated the secure operation mode. As a result, when the external fault evolves to the internal one, the trip command is issued by the 2-out-of-2 logic of 87BP and 87B functions at 108.6 and 127.1 ms, respectively.

D. Massive Data Analysis

A massive data analysis was performed with the intention to fully test the proposed scheme, and to observe its advantages when compared to the traditional 87B function. In addition, the noise effect in protection schemes are assessed by adding to the simulated signals a white random noise with signal-to-noise ratio (SNR) per sample of 50 dB. In this regard, internal and evolving external-to-internal faults were simulated in the power system of Fig. 11, by varying the fault resistance of ground faults (R_G), the resistance between phases of ungrounded faults (R_F), the fault inception angle (θ) and the fault type, as described in Tab. II. Also, it was considered that all evolving faults start from an external AG fault with $R_G = 150\,\Omega$.

TABLE II
FAULT PARAMETERS USED IN THE MASSIVE DATA ANALYSIS

Parameter	Value
R_G	0, 25, 50, 75 and 100 Ω
R_F	0, 5, 10, 15 and 20 Ω
θ	0°, 30°, 60°, . . . , 150° and 180°
Fault Type	AG, BG, CG, AB, BC, CA, ABG, BCG, CAG and ABC

TABLE III
STATISTICS OF THE OPERATING TIMES IN MILLISECONDS

Measure	Internal Faults		Evolving Faults	
	Without Noise	With Noise	Without Noise	With Noise
μ_{prop}	2.4804	2.7845	3.1652	3.5967
σ_{prop}	0.6878	0.4522	2.9112	3.0285
μ_{87B}	5.1855	5.8246	6.9581	7.5507
σ_{87B}	1.1721	1.3155	5.9953	5.8165

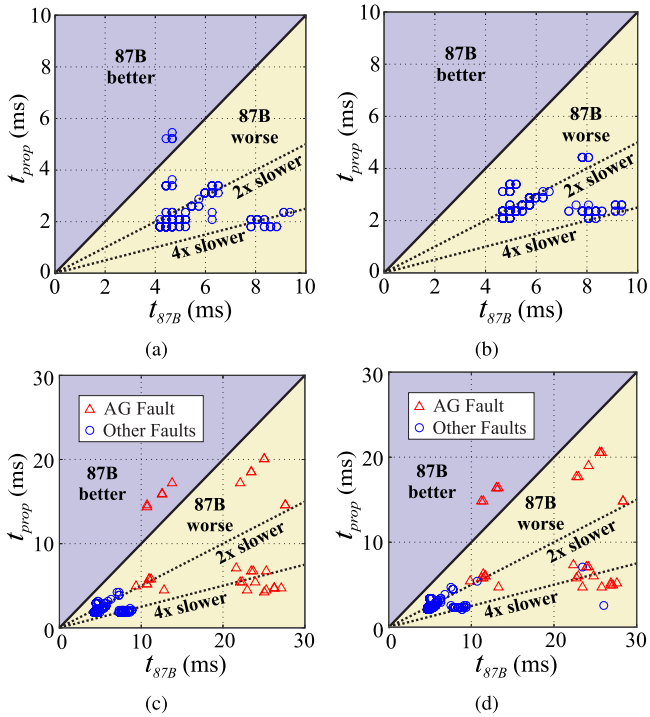

Fig. 18. Dispersion graphics of the operating times of the proposed algorithm (t_{prop}) and the current-based 87B function (t_{87B}): (a) internal faults without noise; (b) internal faults with noise; (c) evolving external-to-internal faults without noise; (d) evolving external-to-internal faults with noise.

The operating time mean (μ) and standard deviation (σ) of the proposed scheme and the 87B function are summarized in Tab. III. The Figs. 18(a) shows that internal faults can be detected twice, or even fourth, times faster with the proposed scheme. Besides, although the mean operating time is a little bigger when noise is introduced, this tendency is maintained, as shown in Fig. 18(b). The same trend is present in evolving fault cases, as shown in Fig. 18(c) and 18(d). Specifically, considering a total of 700 cases, for 87,85% of internal faults and for 97,00% of

evolving faults, the proposed method is about two times or even faster than the traditional 87B function. Likewise, for 1,3% of internal faults and 1,43% of external faults, the proposed method is faster less than two times faster than traditional 87B function. In other words, in the overwhelming majority of the cases, the proposed algorithm gives better response times than traditional protection method.

Nevertheless, it was identified that the instantaneous-power based algorithm is worse than current-based algorithm in six internal faults with noise, (0,85% of internal faults). It occurs because the digital mimic filter greatly reduced the first operating power lobe, leading to an undesired delaying in the 1-out-of-1 logic operation. Conversely, since the 87B function does not use the digital mimic filter, the decaying dc component creates a large first operation lobe, leading to a quite faster trip command issuing. On the other hand, in eleven evolving faults (1,57% of evolving faults) the proposed method is a little bit slower than 87B function. It occurs in some cases in which the AG external fault evolves to an AG internal fault. Indeed, in these cases, since in the proposed scheme the harmonic restraint is enabled (see Sec. III-J), the first operating power lobes are reduced, delaying the trip command issuing by the 2-out-of-2 logic. Also, it is noteworthy to point out, when the AG external fault evolves to other types of faults, the differential elements of the other phases may not detect the external fault, in such way that, in these cases the operating time when the internal fault takes place is governed by the 1-out-of-1 logic.

Finally, it must be mentioned that the time specified in all results are related to the time spent after the fault inception until operating conditions are met. Nevertheless, this time already includes the one sample delay caused by the mimic filter, which is applied on current samples directly. In turn, the phasor estimation process applied to voltage signals and during the harmonic restraint strategy do not impact on the tripping time. Moreover, in practical applications, the time necessary to send the trip command can be typically about 0.5 ms greater due to actual communication delay [32].

VI. Discussion

By the overall analysis of the proposed algorithm and obtained results, the following aspects must be highlighted:

1) Among the different strategies to deal with fundamental frequency deviation, the variable sampling measurement environment that is widely used in numerical relays has been considered [29]. By doing so, DFT-based phasor estimation algorithms can be used in off-nominal fundamental frequency scenarios straightforwardly, guarantying the dependability of the proposed algorithm.
2) Even though harmonic restraint has been used to improve the dependability of current-based differential protection applications since 1940s [33], a harmonic restraint strategy for instantaneous-power-based differential schemes using a virtual 2nd harmonic power as proposed here has not been reported yet.
3) As the same as the traditional 87B, the sensibility of the proposed algorithm is governed by the value of SLP, since $w^*_{op}(t) = w_{op}(t) - SLP_p \cdot \overline{w}_{res}(t)$, as described in Sec. III-B. For example, in Figs. 19(a) and 19(b), it is illustrated the first operating lobe for different values of fault resistance (0-300 Ω) considering $SLP = 0.30$ and $SLP = 0.15$, respectively. As one can see, a higher SLP leads to smaller operating lobes, so that the trip command may be delayed or even not issued. On the other hand, for a lower SLP, the operating lobes are larger, increasing the sensibility of the proposed scheme. Nevertheless, one ought to bear in mind that a smaller SLP may jeopardize the security of the protection scheme as a whole. That is the why it has been used $SLP = 0.3$ in this work.

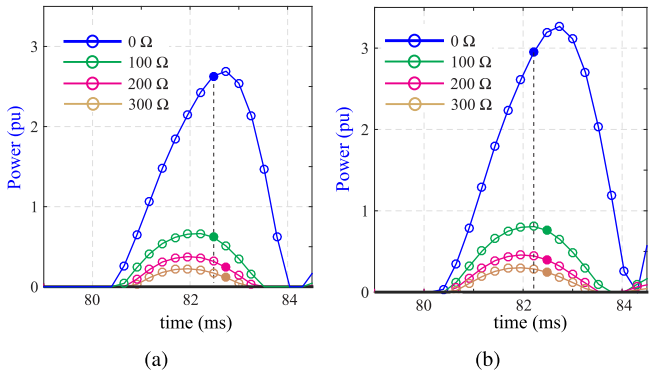

Fig. 19. First operation lobes in case of an internal fault with several fault resistances with: (a) $SLP = 0.3$; (b) $SLP = 0.15$.

4) Even though there are several quite efficient algorithms reported in the literature on the subject to remove the decaying DC component effect on phasor estimation process, these algorithms are not suitable for applying to current signals directly as required in the proposed algorithm. In fact, there are few papers proposing schemes that can be applied directly to current signals, such as the one reported in [34]. However, the digital mimic filter is still the more suitable to be used in the proposed algorithm, since it requires only one sample to filter out the decaying DC component [26], whereas other methods require either half or full cycle data windows.
5) In real world applications, an adaptive voltage memory action can be used, as discussed in [28]. For example, in normal operation, a short memory must be used, in such a way that the memorized positive sequence voltage $\hat{V}_{1m}$ quickly becomes equal actual positive sequence voltage $\hat{V}_1$. If a fault takes place and the voltage collapse, a large voltage memory action is required to provide a steady voltage reference, ensuring the protection dependability. This kind of adaptive voltage memory strategy has been also used by relay manufactures [29].
6) An additional survey reveals that the only methods faster than proposed are those based on wavelet transform [17], and others which combine an overcurrent differential element and a CT saturation detector [9], [10]. The principal benefits and drawbacks of first method are explained in Section I. In turn, the other ones are faster because it was assumed that the trip command can be issued if the

operating conditions are met for only one sample. However, this condition is not suitable for the sake of security, as discussed in Sec. II. Instead, the trip command must be issued only if the operating conditions are met during 1/4, in case of current-based method. In the case of the proposed algorithm, it is required that the operating conditions are met for 1/8 cycle of consecutive samples. Therefore, among the references included in the literature review and considering the practical point of view, one can realize that the proposed scheme is slower than transient-based methods only.

VII. Conclusion

This paper presents a novel busbar differential protection based on the instantaneous power concept. The proposed algorithm is based on a mature protection philosophy (i.e., the tripping logics 1-out-of-1 and 2-out-of-2) adapted to evaluate instantaneous power signals, whereby it provides tripping times two or more times faster than the traditional 87B protection function for most of cases, besides ensuring the same protection dependability. A new harmonic restraint strategy is also presented to improve the security of the proposed scheme for external faults with CT saturation. The proposed algorithm is not blocked during external faults, thereby it is able to properly detect evolving faults. Conversely, the major of the algorithms reported in the literature are blocked whenever an external fault takes place, in such way that they fail to detect evolving faults. In respect to CT saturation, in real world protection applications, manufactures specify the requirement of the minimum CT time to saturate to ensure the proper operation of their busbar relays. Theoretically, this time is 1/4 of cycle as described in [24] but modern relays can require only 1/8 of cycle [25]. By using the proposed method, one can realize that this time can be twice lesser than theoretical value, i.e., it can be the order of 1/8 of cycle (about 2 ms for a 60 Hz power system), what alleviates the CT dimensioning requirements, guarantees the correct operation even in the case of early CT saturation (which takes place 1/8 cycle after the fault inception) and makes possible its implementation in commercial relays.

References

[1] *Guide for Protective Relay Applications to Power System Buses*, IEEE Std C37.234-2009, IEEE Power & Energy Society, Power System Relaying Committee, Piscataway, NJ, USA, 2009.

[2] *Modern Techniques for Protecting Busbars in HV Networks*, Cigré TB 431, Cigré Working Group B5.16, 2010.

[3] K. Behrendt, D. Costello, and S. E. Zocholl, "Considerations for using high-impedance or low-impedance relays for bus differential protection," in *Proc. IEEE 63rd Annu. Conf. Protective Relay Eng.*, Mar. 2010, pp. 1–15.

[4] C. Martin, S. Chase, T. X. Nguyen, D. J. Hawaz, J. Pope, and C. Labuschagne, "Bus protection considerations for various bus types," presented at the 40th Annu. Western Protective Relay Conf., Spokane, WA, USA, Oct. 2013.

[5] A. Guzmán, B. L. Qin, and C. Labuschagne, "Reliable busbar protection with advanced zone selection," *IEEE Trans. Power Del.*, vol. 20, no. 2, pp. 625–629, Apr. 2005.

[6] C. Fernandez, "An impedance-based CT saturation detection algorithm for bus-bar differential protection," *IEEE Trans. Power Del.*, vol. 16, no. 4, pp. 468–472, Oct. 2001.

[7] M. S. Sachdev, T. S. Sidhu, and H. S. Gill, "A busbar protection technique and its performance during CT saturation and CT ratio-mismatch," *IEEE Trans. Power Del.*, vol. 15, no. 3, pp. 895–901, Jul. 2000.

[8] S. Song and G. Zou, "A novel busbar protection method based on polarity comparison of superimposed current," *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 1914–1922, Aug. 2015.

[9] Y. C. Kang, U. J. Lim, S. H. Kang, and P. A. Crossley, "A busbar differential protection relay suitable for use with measurement type current transformers," *IEEE Trans. Power Del.*, vol. 20, no. 2, pp. 1291–1298, Apr. 2005.

[10] Y. C. Kang, J. S. Yun, B. E. Lee, S. H. Kang, S. I. Jang, and Y. G. Kim, "Busbar differential protection in conjunction with a current transformer compensating algorithm," *IET Gen., Transmiss. Distrib.*, vol. 2, no. 1, pp. 100–109, Jan. 2008.

[11] G. Zou and H. Gao, "A traveling-wave-based amplitude integral busbar protection technique," *IEEE Trans. Power Del.*, vol. 27, no. 2, pp. 602–609, Apr. 2012.

[12] Z. Guo, J. Yao, and Z. Tan, "Hilbert– Huang transform-based transient busbar protection algorithm," *IET Gener., Transmiss. Distrib.*, vol. 9, no. 14, pp. 2032–2039, Jun. 2015.

[13] M. M. Eissa, "A novel wavelet approach to busbar protection during ct saturation and ratio mismatch," *Elect. Power Syst. Res.*, vol. 72, pp. 41–48, Jun. 2004.

[14] M. E. Mohammed, "High-speed differential busbar protection using wavelet-packet transform," *IEE Proc. - Gener., Transmiss. Distrib.*, vol. 152, no. 6, pp. 927–933, Nov. 2005, doi: 10.1049/ip-gtd:20045162.

[15] S. A. Gafoor and P. V. R. Rao, "A transient current based busbar protection scheme using wavelet transforms," *Int. J. Elect. Power Energy Syst.*, vol. 33, pp. 1049–1053, 2011.

[16] M. M. Eissa, "New differential busbar characteristic based on high frequencies extracted from faulted signal during current transformer saturation," *IET Gener., Transmiss. Distrib.*, vol. 8, pp. 619–628, 2014.

[17] K. M. Silva, A. M. P. Escudero, F. V. Lopes, and F. B. Costa, "A wavelet-based busbar differential protection," *IEEE Trans. Power Del.*, vol. 33, no. 3, pp. 1194–1203, Jun. 2018.

[18] *SEL-T400L Time-Domain Line Protection*, Schweitzer Eng. Lab., Inc., Pullman, WA, USA, 2016.

[19] G. Didier, H. Razik, O. Caspary, and E. Ternisien, "Rotor cage fault detection in induction motor using global modulation index on the instantaneous power spectrum," in *Proc. 4th IEEE Int. Symp. Diagnostics Elect. Mach., Power Electron. Drives*, Aug. 2003, pp. 104–109.

[20] H. Ma, Z. Zhang, P. Ju, W. Shi, and C. Wang, "Stator fault detection of doubly-fed induction generators using rotor instantaneous power spectrum," in *Proc. IEEE 10th Int. Symp. Diagnostics Elect. Mach., Power Electron. Drives*, Sep. 2015, pp. 165–170.

[21] T. Zheng, W. S. Liu, X. Y. Zhang, S. H. Jiao, and T. S. Bi, "A new approach based on the instantaneous power for transformer differential protection," in *Proc. 8th IEE Int. Conf. Develop. Power Syst. Protection*, Apr. 2011, pp. 331–334.

[22] D. P. Balachandran, R. S. Kumar, and B. Jayanand, "Instantaneous power based detection of inrush currents in single phase transformers," in *Proc. IEEE Energytech*, May 2012, pp. 1–5.

[23] A. Kumar and P. Hansen, "Digital bus-zone protection," *IEEE Comput. Appl. Power*, vol. 6, no. 4, pp. 29–34, Oct. 1993.

[24] G. Ziegler, *Numerical Differential Protection, Principles and Applications*, vol. 2. Weinheim, Germany: Wiley-VCH, 2012.

[25] *SEL-487B Bus Differential and Breaker Failure Relay, Instruction Manual*, Schweitzer Eng. Lab., Inc., Pullman, WA, USA, 2018.

[26] G. Benmouyal, "Removal of dc-offset in current waveforms using digital mimic filtering," *IEEE Trans. Power Del.*, vol. 10, no. 2, pp. 621–630, Apr. 1995.

[27] D. G. Hart, D. Nosovel, and R. A. Smith, "Modified Cosine Filters," U.S. Patent 6 154 687, Nov. 28, 2000.

[28] K. M. Silva and M. L. S. Almeida, "Positive sequence voltage memory filter for numerical digital relaying applications," *Electron. Lett.*, vol. 51, no. 21, pp. 1697–1699, Oct. 2015.

[29] H. J. Altuve and E. O. Schweitzer, *Modern Solutions for Protection, Control and Monitoring of Electric Power Systems*. Pullman, WA, USA: Schweitzer Eng. Lab., Inc., 2010.

[30] *EMTP Reference Models for Transmission Line Relay Testing*, IEEE Power System Relaying Committee, IEEE Power Eng. Soc., Piscataway, NJ, USA, 2004.

[31] *Busbar Protection REB670 2.0 ANSI, Application Manual*, ABB, Västerås, Sweden, 2014.

[32] S. Jena and B. R. Bhalja, "Numerical busbar differential protection using generalised alpha plane," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 1, pp. 227–234, 2018.
[33] C. D. Hayward, "Harmonic-current-restrained relays for transformer differential protection," *Elect. Eng.*, vol. 60, no. 6, pp. 377–382, Jun. 1941.
[34] J. M. Argelles, M. Z. Arrieta, J. L. Domnguez, B. L. Jaurrieta, and M. S. Benito, "A new method for decaying dc offset removal for digital protective relays," *Elect. Power Syst. Res.*, vol. 76, pp. 194–199, 2006.

Francis A. Moreno Vásquez received the B.Sc. degree in electromechanical engineering from National University "Pedro Ruiz Gallo," Perú, in 2011, and the M.Sc. degree in mechanical sciences from the University of Brasília, Braslia, Brazil, in 2014. He is currently working toward the Ph.D. degree in electrical engineering at the University of Brasília. His research interests include power system protection, electromagnetic transients, and electrical generation.

Kleber M. Silva (M'05) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Campina Grande, Campina Grande, Brazil, in 2004, 2005, and 2009, respectively. Since 2009, he has been a Professor with the University of Brasília, Brasília, Brazil, and the Head of the Power System Protection Group. He is an Associate Editor for the IEEE TRANSACTIONS ON POWER DELIVERY and Member of SC B5—Protection and Automation Committee of Cigré Brazil. His research interests focus on power system protection, fault location, and electromagnetic transients.