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Design and implementation of a three-level active power filter for harmonic and reactive power compensation

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ABSTRACT

This paper presents a unified design and implementation of active power filters (APF) for medium-voltage high-power applications. A fast and accurate harmonic extraction technique based on the time transformation algorithm (TTA) is developed. A novel approach is used to derive the mathematical model describing the relation between the output current and the control signal of the NPC inverter for active power filter. Accordingly, the current controller and voltage controller are designed using the derived model. The neutral-point voltage is maintained near zero using a feed-forward controller. The designed three-level APF is feasible to implement, comparatively cheaper and reduces the filter size. From both the simulation and experimental results, it is found that the developed system provides excellent performance in regulating voltage and reducing harmonics significantly, from 26.3% to 4.0%.

1. Introduction

Industrial loads are predominantly composed of nonlinear loads in the form of frequency changers, motor drives and power converters. These are the main sources of harmonic pollution in grids, resulting in poor efficiency, a degraded power factor and can damage a equipment connected to the grid. The active power filter (APF) gives the most promising solution to compensate for the adverse effects of harmonics and reactive power simultaneously by using suitable control algorithms [1–5]. Different configurations of APF are available on the market for commercial use, and among them a shunt APF is widely used. The shunt APF (SAPF) is connected in parallel with the source and the load, injecting harmonics of opposite polarity to those present in the load current at the point of common coupling (PCC).

In the low-voltage field, there are already lots of well-rounded APF products below 690 V. However, in the high-voltage and high-power fields, the traditional two-level APF cannot fulfil their requirements because of the shortcomings of power switches as high-voltage semiconductor switches are still being remedied. A multilevel converter can be used as an alternative high-voltage switching device for high-power medium-voltage applications [6]. In addition, a multilevel converter has the advantages of low loss, low electromagnetic interference and low waveform distortion, and has become the new direction of development for active power filters [7–10].

The use of an APF at medium and high voltages is limited due to semiconductor's reverse-voltage rating constraint, high losses caused by switching high voltage and high current and high *dv/dt* generating electro-magnetic interference (EMI) as well as insulation degradation in electronic and electrical systems. An APF can be used in high-voltage applications, but comes with issues like losses, unreliability, complex control structure, high cost and a surge over-voltage problem. Another alternative is a cascaded connection of two PWM (pulse-width modulation) VSIs (voltage source inverters) with different power rating and switching frequency. This reduces the switching stress and commutation loss but the overall cost and size of the equipment goes up.

Multilevel inverters with different topologies have been developed for medium voltages and high-rated power applications to cover up the deficiencies of the above alternatives [11]. Neutral point clamped [12], flying capacitor [13], and cascade half-bridge [14] are the three most common topologies in multilevel inverters. The authors in [15] presented a comprehensive comparison of these three topologies. In an active power filter for commercial application, the cost, size and reliability of the system are of prime importance. The cost and size of capacitors are greater than diodes and the failure rate is higher in capacitors than diodes. In real power conversion cascaded H-bridge (CHB) requires an isolated dc source, but not in APF, however there are many voltage variables that need to be controlled in the case of APF which makes its control more complex. Therefore, NPC is selected owing to

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the application requirements and the ease of design and implementation as proposed in [16].

Current harmonic extraction technique plays a crucial role, especially in feedforward harmonic detection control structure determining speed and accuracy of APF [17,18]. Reference current extraction is carried out in two domains, frequency (fast Fourier transform (FFT), discrete Fourier transform (DFT)) and time (p-q, synchronous d-q, etc.). Time-domain techniques are preferred over frequency-domain techniques owing to their faster response and simplicity in real-time implementation [19,20].

As the APF needs to generate non sinusoidal currents, the design and implementation of the current controller is very demanding. Various control techniques like proportional-integral (PI), hysteresis, proportional-resonant (PR), and advanced and intelligent control have been proposed and used [21–23]. PI is still preferred due to its simpler implementation, and its performance conforms to the grid requirements [24]. The topological structure (NPC inverter) brings an unbalance of neutral-point voltage which is addressed using a feed-forward controller [25].

There has been a considerable interest in the use of a three-level inverter for APF but very few studies are available interlinking the various stages of implementation. This paper aims to bridge that gap by focusing on different stages of implementation. A unified complete control structure, consisting of harmonic current detection method, current control, DC-voltage control and neutral-point voltage control, for the APF with a three-level NPC converter is developed and implemented. A novel and simple approach for deriving mathematical model of three level NPC inverter is proposed in the paper. Compared to the previous approaches, the proposed modelling utilizes state space averaging method. The derived model simplifies the controller parameter design procedure and are used to design optimal control parameters for inner current and outer voltage control loop. The accuracy and performance of the derived model is verified through simulation and experimental results. Parameters of the power circuit are determined mathematically which ensures the optimum performance of the designed APF. The designed system accurately detects the harmonic and reduces to acceptable level. Finally, the simulation results are verified by experimental results to validate the efficacy of the proposed methods.

The paper is organized into four sections. Section 2 provides a brief review of APF principles and power-circuit parameter design. The control subsystem, consisting of a harmonic detection mechanism and voltage and current controller design, is discussed in Sections 3 and 4. The simulation and experimental results are presented in Sections 5 and 6. Section 7 presents a summary of this paper.

2. Power-circuit parameter design

There are three main power-circuit parameters to be calculated: (i) reference value of DC-side voltage; (ii) output filter inductor; and (iii) DC-side capacitance. The DC-link voltage should be at least greater than the peak of the line-to-neutral voltage to realize the compensation characteristics. The voltage rating of the switching devices is given by:

$$V_{\text{device-rating}} \times (m-1) \geq 2V_{\text{ll}}, \quad V_{\text{device-rating}} \geq V_{\text{ll}} \tag{1}$$

where $m = 3$. The performance of an APF depends upon the selection of capacitor's value; the DC-side voltage should be constant for good compensation. Unlike in a two-level inverter, the voltage rating of the capacitors is reduced in a three-level inverter and is half of the DC-side reference voltage. During compensation the voltage of the capacitor fluctuates, and the fluctuation is a function of the capacitance and the reference DC-side voltage. Higher fluctuations will degrade the compensation performance while lower fluctuations require a higher capacitance, which increases the size and cost. Hence it should be limited to within a pre-specified value by selecting a suitable capacitance which can be determined as [26]:

$$C \geq \frac{3E_m I_m}{2\varepsilon\omega V_{\text{dc}}^2} \tag{2}$$

where E_m is the grid peak voltage, I_m is the output nominal current, ε is the DC voltage fluctuation component which is taken 10%, ω is grid angular frequency and V_{dc} is the dc side voltage. The output inductor provides an interface of the APF with the electrical system as well as filtering out the high-frequency switching ripples of the inverter output AC current. In general, the larger the value of the inductor the betters the suppression of switching ripple, but with poor current tracking and larger size, cost will be higher. In comparison to a two-level inverter, the output voltage of a 3-level inverter is more like a sine wave, hence the filtering requirement is reduced. The inductor's value is determined based on the maximum ripple allowed in the output current [27] and given as:

$$L_a \geq \frac{(\text{Vdc}/2)(1-|D|)|D|\ T_s}{2\Delta I_{L\,\max}} \tag{3}$$

where $\Delta I_{L\max}$ is the maximum ripple current in one switching cycle, D is the duty cycle and T_s is the switching time period. From the above equation it is clear that L_a has maximum value when $(1 - |D|) = |D|$.

3. Current reference estimation

The generalized structure of a three-phase shunt APF with a three-level NPC inverter is shown in Fig. 1. The power stage consists of a three-level NPC VSI behaving as a current source, connected in parallel at the point of common coupling (PCC). The load current is sensed and the harmonic content present in it is extracted, serving as a reference compensation current for the inner current control loop. The current control loop ensures that the APF generates a reference current to achieve the desired compensation. A voltage control loop is essential to maintain the DC-side capacitor voltage to a reference value against the losses in the VSI.

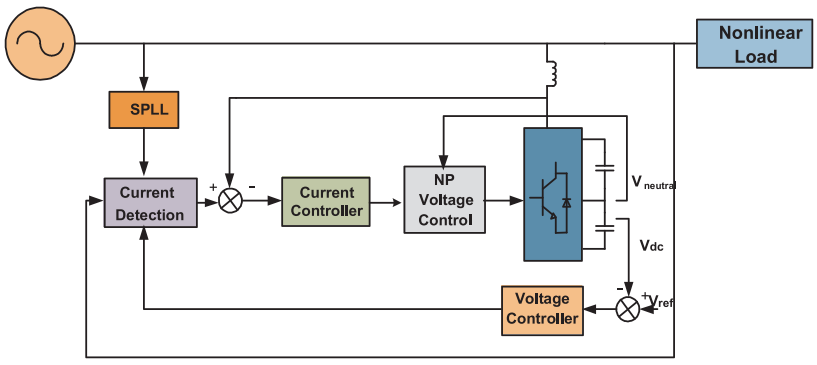


Fig. 1. General control structure of APF with 3-level NPC inverter.

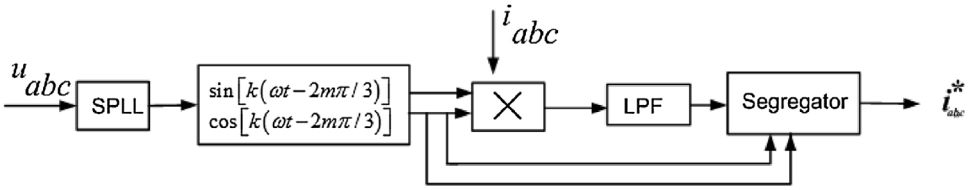


Fig. 2. Harmonic current detection algorithm based on orthogonal theorem.

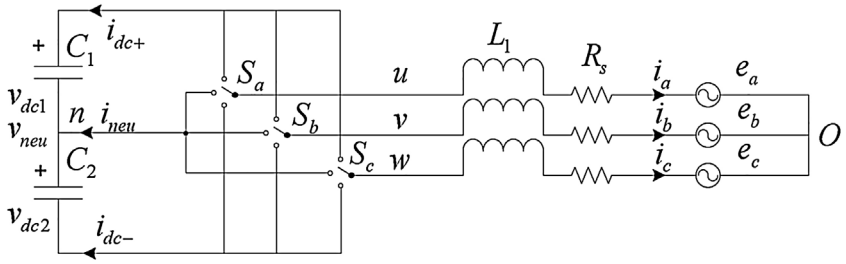


Fig. 3. Simplified circuit of three-level inverter.

The instantaneous reactive power theory (IRPT) (p-q theory) proposed by Akagi promoted the use of APF. However, the transformation between a, b, c coordinates and p-q coordinates makes the designing of the controller more complex. Besides, current harmonic detection based on algorithms using IRPT cannot be used for selected order harmonic extraction. Current harmonic extraction based on a Fourier transform either fast Fourier transform (FFT) or discrete Fourier transform (DFT), gives good precision and can be used for selected order harmonics but it introduces a time delay in the system which makes it impractical for real-time application with dynamically varying loads. Various harmonic detection methods are evaluated in different studies [19]. However, they are not suitable for some abnormal operating conditions. Based on DFT and IRPT, a time-domain transformation algorithm (TTA) is proposed for current harmonic detection [28]. This method utilizes the advantages of both the frequency and time domain approach. Fig. 2 shows a block diagram of current harmonic detection based on TTA. This method can detect positive/negative sequences of fundamental current, active and reactive components of fundamental current and selected order harmonics. Moreover, the delay introduced by this method is half that of DFT and the same as IRPT but it does not require any coordinate transformation. A synchronizing signal, in phase with the grid voltage, is necessary for current harmonic extraction. The synchronizing signal is obtained using software phase lock loop (SPLL) based on a d-q transformation. SPLL is the realization of a PLL using digital devices like digital signal processor (DSP) and field-programmable gate array (FPGA). The PLL based on a d-q transformation provides fast and accurate response and better performance in abnormal grid conditions [29].

4. Modeling and control of three-level NPC inverter

Compared to a two-level inverter, the control of a three-level inverter is more complex owing to the large number of switching states and the complexity of the circuit. An accurate mathematical model describing the characteristics of the inverter is necessary because the design of accurate controller parameters strictly depends on it. This in turn ensures closed loop operation of the APF will generate the desired and specified compensation performance. The establishment of switch model though closest to the real system, is discontinuous which do not facilitate the theoretical analysis and derivation of its mathematical model. Several modelling approaches for multilevel inverter have been reported in [30,31]. These approaches are either too complicated or insufficient for aiding in controller design. Furthermore, a simplified model that can capture the important dynamics of the system and a simpler implementation of controller design seems to be lacking. The state-space averaging method as compared to switch method is very good solution to model a system when the difference between switching frequency and control frequency is large. The average model of the switching state is used to replace the switch. The state averaging method is a very powerful tool for modelling the power converter.

4.1. State space model of three-level NPC inverter

In order to derive a simple mathematical model of the three-level NPC inverter for APF, the following assumptions are made:

1. The switching loss is ignored and the line resistance is represented by R_s. The output inductor is purely inductive (L_1) and its saturation effect is not considered.
2. The balanced grid voltage is considered.
3. The midpoint voltage drift is ignored because a separate feed-forward control is used to balance neutral-point voltage fluctuations.

Fig. 3 shows the switching function of the diode-clamp three-level inverter topology in which each phase's IGBT bridge arm is equivalent to a single-pole three-throw switch, e_a, e_b, e_c are three-phase grid voltages, i_a, i_b, i_c are the filter output currents, v_{dc2} and v_{dc1} are equal capacitor voltages. The switching state function S_k is defined by:

$$S_k = \begin{cases} 1 \\ 0 \\ -1 \end{cases} \quad k = a, b, c \tag{4}$$

Thus, the combination of the switching function S relative to terminal a, b, c and terminal u, v, w can be written as:

$$\begin{cases} V_{un} = \frac{S_a}{2} V_{dc} \left(S_a = -1, 0, 1 V_{un} = -\frac{V_{dc}}{2}, 0, \frac{V_{dc}}{2} \right) \\ V_{vn} = \frac{S_b}{2} V_{dc} \left(S_b = -1, 0, 1 V_{vn} = -\frac{V_{dc}}{2}, 0, \frac{V_{dc}}{2} \right) \\ V_{wn} = \frac{S_c}{2} V_{dc} \left(S_c = -1, 0, 1 V_{wn} = -\frac{V_{dc}}{2}, 0, \frac{V_{dc}}{2} \right) \end{cases} \tag{5}$$

In order to facilitate a further derivation of three-level mathematical model of APF, the switching function S_k, S_{1k}, S_{2k}, S_{3k} are introduced: when $S_k = 2$, define $S_{1k} = 1$, $S_{2k} = 0$, $S_{3k} = 0$; when $S_k = 1$, define $S_{1k} = 0$, $S_{2k} = 0$, $S_{3k} = 1$; when $S_k = 0$, $S_{1k} = 0$, $S_{2k} = 1$, $S_{3k} = 0$; and the decomposition satisfies the following constraint relations:

$$\begin{cases} S1k + S2k + S3k = 1 \quad k \subset [a, b, c] \\ \text{Sik} \subset [0, 1] \quad i \subset [1, 2, 3] \quad k \subset [a, b, c] \end{cases} \tag{6}$$

thus it can be written as:

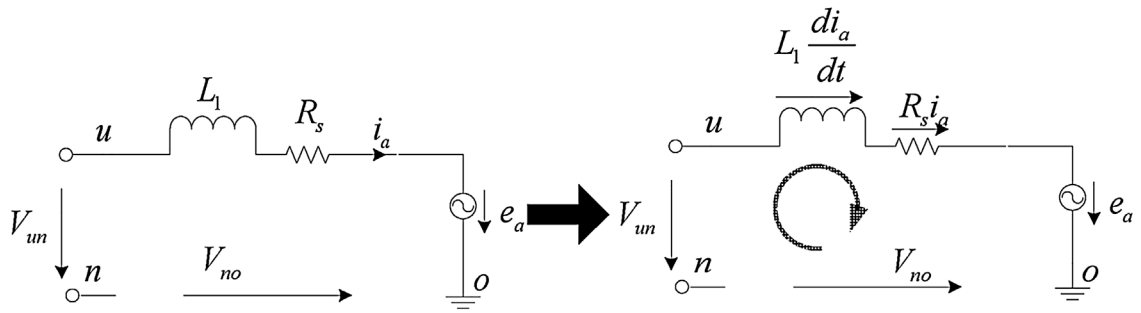


Fig. 4. Buck equivalent three-level NPC inverter circuit.

$$\begin{aligned} V_{\mathrm{un}} &= S_{1a}V_{\mathrm{dc1}} - S_{2a}V_{\mathrm{dc2}} \\ V_{\mathrm{vn}} &= S_{1b}V_{\mathrm{dc1}} - S_{2b}V_{\mathrm{dc2}} \\ V_{\mathrm{wn}} &= S_{1c}V_{\mathrm{dc1}} - S_{2c}V_{\mathrm{dc2}} \end{aligned} \tag{7}$$

The single leg of the three-level active power filter in Fig. 3 is simplified into the equivalent buck circuit as shown in Fig. 4. For a balanced load scenario, we can consider a single phase for analysis and its related equations and expressions are applicable for other two phases, the Kirchhoff voltage equation for phase A:

$$L_1\frac{di_a}{\mathrm{dt}} = -R_s i_a - e_a + V_{\mathrm{uo}} \tag{8}$$

In the three-phase three-wire system:

$$\begin{aligned} &i_a + i_b + i_c = 0 \\ &e_a + e_b + e_c = 0 \end{aligned} \tag{9}$$

$$\text{As} \quad V_{\mathrm{no}} = -\frac{1}{3}(V_{\mathrm{un}} + V_{\mathrm{vn}} + V_{\mathrm{wn}}) \tag{10}$$

Substituting (5) into (8) we get:

$$V_{\mathrm{no}} = -\frac{1}{3}(S_{1a} + S_{1b} + S_{1c})V_{\mathrm{dc1}} + \frac{1}{3}(S_{2a} + S_{2b} + S_{2c})V_{\mathrm{dc2}} \tag{11}$$

In addition, the DC side current is i_{dc+}, i_{dc-}:

$$\begin{aligned} i_{\mathrm{dc+}} &= C_1\tfrac{dV_{\mathrm{dc1}}}{\mathrm{dt}} = -S_{1a}i_a - S_{1b}i_b - S_{1c}i_c \\ i_{\mathrm{dc-}} &= C_2\tfrac{dV_{\mathrm{dc2}}}{\mathrm{dt}} = S_{2a}i_a + S_{2b}i_b + S_{2c}i_c \end{aligned} \tag{12}$$

Merge (8)–(12), when the mathematical model of the diode clamped three-level active power filter is given by:

$$\begin{aligned} L_1\frac{di_a}{\mathrm{dt}} = -R_s i_a &+ \left(S_{1a} - \frac{S_{1a} + S_{1b} + S_{1c}}{3}\right)V_{\mathrm{dc1}} \\ &+ \left(-S_{2a} + \frac{S_{2a} + S_{2b} + S_{2c}}{3}\right)V_{\mathrm{dc2}} - e_a \end{aligned} \tag{13}$$

$$\begin{aligned} C_1\tfrac{dV_{\mathrm{dc1}}}{\mathrm{dt}} &= -S_{1a}i_a - S_{1b}i_b - S_{1c}i_c \\ C_2\tfrac{dV_{\mathrm{dc2}}}{\mathrm{dt}} &= S_{2a}i_a + S_{2b}i_b + S_{2c}i_c \end{aligned} \tag{14}$$

According to state space,

$$Z\dot{X} = \mathrm{AX} + \mathrm{Be}$$

where

$$Z = [L_1 \quad L_1 \quad L_1 \quad C_1 \quad C_2]$$

$$X = [i_a \quad i_b \quad i_c \quad V_{\mathrm{dc1}} \quad V_{\mathrm{dc2}}]^T$$

$$\begin{bmatrix} R_s & 0 & 0 & S_{1a} - \frac{S_{1a}+S_{1b}+S_{1c}}{3} & -S_{2a} + \frac{S_{2a}+S_{2b}+S_{2c}}{3} \\ 0 & -R_s & 0 & S_{1b} - \frac{S_{1a}+S_{1b}+S_{1c}}{3} & -S_{2b} + \frac{S_{2a}+S_{2b}+S_{2c}}{3} \\ 0 & 0 & -R_s & S_{1c} - \frac{S_{1a}+S_{1b}+S_{1c}}{3} & -S_{2c} + \frac{S_{2a}+S_{2b}+S_{2c}}{3} \\ -S_{1a} & -S_{1b} & -S_{1c} & 0 & 0 \\ S_{2a} & S_{2b} & S_{2c} & 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$e = [e_a \quad e_b \quad e_c \quad 0 \quad 0]^T$$

This is the mathematical model of three level NPC inverter, the next step is to get the average model from this model and then small signal model is determined from the average model.

4.2. Three-level NPC inverter average model

Consider $C = 2C_1 = 2C_2$, $V_{dc} = V_{dc1} = V_{dc2}$, $V_{dc1} = V_{dc2}$ and, after simplification of (13) and (14) we get:

$$\begin{aligned} L_1\frac{di_a}{\mathrm{dt}} = -R_s i_a &+ \left(S_{1a} - \frac{S_{1a} + S_{1b} + S_{1c}}{3}\right)V_{\mathrm{dc1}} \\ &+ \left(-S_{2a} + \frac{S_{2a} + S_{2b} + S_{2c}}{3}\right)V_{\mathrm{dc1}} - e_a \end{aligned} \tag{15}$$

$$C\frac{dV_{\mathrm{dc}}}{\mathrm{dt}} = (S_{2a} - S_{1a})i_a + (S_{2b} - S_{1b})i_b + (S_{2c} - S_{1c})i_c \tag{16}$$

Applying the switching-cycle average algorithm on (8) and (9):

$$\begin{aligned} L_1\frac{d\overline{i_a}}{\mathrm{dt}} = -R_s \overline{i_a} &+ \left(\overline{S_{1a}} - \frac{\overline{S_{1a}} + \overline{S_{1b}} + \overline{S_{1c}}}{3}\right)V_{\mathrm{dc1}} \\ &+ \left(-\overline{S_{2a}} + \frac{\overline{S_{2a}} + \overline{S_{2b}} + \overline{S_{2c}}}{3}\right)V_{\mathrm{dc1}} - \overline{e_a} \end{aligned} \tag{17}$$

$$C\frac{d\overline{V_{\mathrm{dc}}}}{\mathrm{dt}} = (\overline{S_{2a}} - \overline{S_{1a}})\overline{i_a} + (\overline{S_{2b}} - \overline{S_{1b}})\overline{i_b} + (\overline{S_{2c}} - \overline{S_{1c}})\overline{i_c} \tag{18}$$

4.3. Small signal model of three-level NPC inverter

As can be seen from (17) and (18), by ignoring DC voltage fluctuations and considering the grid voltage to be balanced, there are only six variables $\overline{S_{1a}}$, $\overline{S_{1b}}$, $\overline{S_{1c}}$, $\overline{S_{2a}}$, $\overline{S_{2b}}$, $\overline{S_{2c}}$ to control the phase current for each phase, making the model much simpler than if these variables into the model are considered. As midpoint voltage fluctuation within one switching cycle, i.e. V_{neu} is constant in one switching cycle; $\frac{\overline{S_{2a}}+\overline{S_{2b}}+\overline{S_{2c}}}{3} - \frac{\overline{S_{1a}}+\overline{S_{1b}}+\overline{S_{1c}}}{3}$ is also constant and, in the small-signal model, a small perturbation added to a constant is zero. Finally, the small-signal model is given by:

$$\begin{cases} L_1\frac{d\widehat{i_a}}{\mathrm{dt}} = -R_s\widehat{i_a} + \frac{\widehat{S_a}}{2}V_{\mathrm{dc}} \\ C\frac{d\widehat{V_{\mathrm{dc}}}}{\mathrm{dt}} = -\widehat{S_a}\,\overline{i_a} - \widehat{S_b}\,\overline{i_b} - \widehat{S_c}\,\overline{i_c} - \overline{S_a}\,\widehat{i_a} - \overline{S_b}\,\widehat{i_b} - \overline{S_c}\,\widehat{i_c} \end{cases} \tag{19}$$

The transfer function of the three-phase current switching state S_k can be obtained from (19):

$$\begin{cases} G_{i_a s_a}(s) = \frac{(V_{\rm dc}/2)}{L_1 S + R_s} \\ G_{i_b s_b}(s) = \frac{(V_{\rm dc}/2)}{L_1 S + R_s} \\ G_{i_c s_c}(s) = \frac{(V_{\rm dc}/2)}{L_1 S + R_s} \end{cases} \quad (20)$$

It can be seen that the transfer function for all the three-phase current is the same, so transfer function for three level APF current can be generally written as:

$$G_{\rm is}(s) = \frac{(V_{\rm dc}/2)}{L_1 S + R_s} \quad (21)$$

The sampling and computational delay in digital implementation is approximated as:

$$G_{\rm pwm}(S) = \frac{1}{1 + T_d s} \quad (22)$$

Substituting $L_1 = 0.2$ mH, $R_s = 0.1\ \Omega$, $V_{dc} = 750$ V in Eq. (21), the system transfer function is given by:

$$G_i = G_{\rm pwm}(s) G_{\rm is}(s) \quad (23)$$

4.4. Control structure

The equivalent control block diagram for a three-level inverter for APF application is shown in Fig. 5.

4.4.1. Inner current control loop

The current control loop in the APF is quite demanding due to a non-sinusoidal reference current wave shape. The current control is designed to minimize tracking error adhering to grid total harmonic distortion (THD) requirement and fast dynamic response in the event of load and source variations. In this paper, a PI controller is used to control the current output. The current control loop ensures that the output current of the APF tracks the reference harmonic current. For better compensation, the loop gain is required to have high gain and bandwidth. The equivalent loop gain for the current control loop is given by:

$$G_i = G_{\rm PI}(s) G_{\rm pwm}(s) G_{\rm is}(s)$$

The Bode plots of the loop gain of the uncompensated and PI compensated system are given in Fig. 6. The Bode diagram with compensator shows that the crossover frequency is 3 kHz, which is 25 times the fundamental frequency and provide fast response. The loop gain at the harmonic frequencies is high enough for the controller to generate them with minimum error. In addition, the phase margin of 30° results in a stable system.

4.4.2. Voltage control loop

The voltage control loop maintains the DC-capacitor to a specified reference voltage against the loss in energy in the switching device and parasitic components [32]. This is realized by drawing an in-phase current from the utility voltage to counter the drop of DC-voltage. The effect of capacitor voltage variations due to changes in the APF output current is determined based on the average power transfer in one fundamental cycle.

As in the three-level NPC inverter, there are two capacitors on the DC-side, the voltage on each needs to be controlled. The capacitor

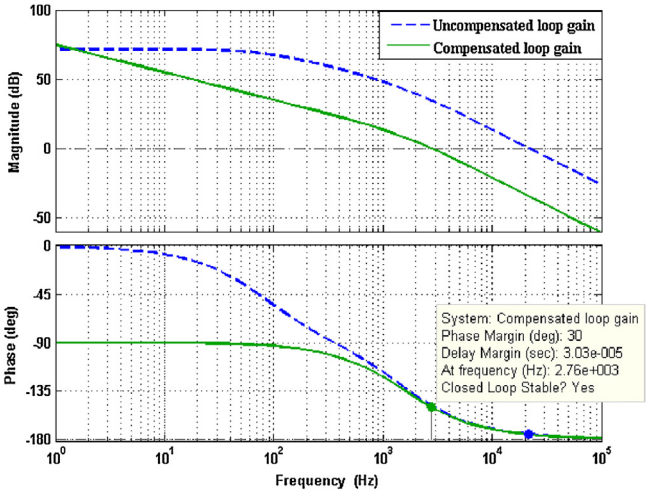


Fig. 6. Loop gain of current control loop.

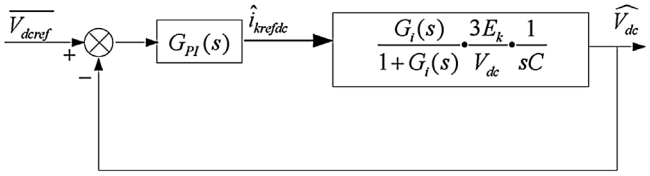


Fig. 7. Simplified block diagram for voltage control loop.

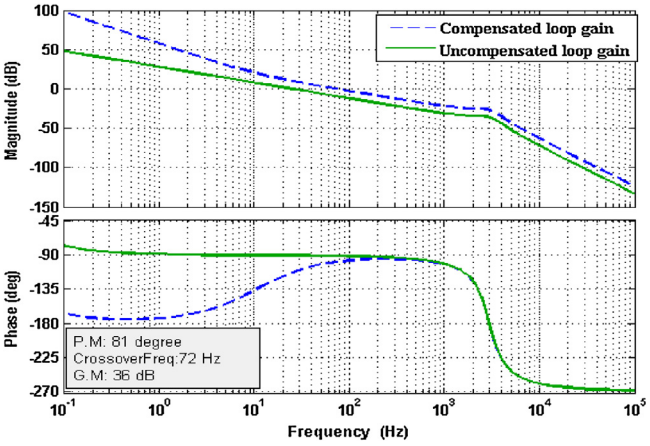


Fig. 8. Loop gain of voltage control loop.

Table 1
System parameters used in simulation.

System parameter	Value
Line voltage	220 V, 50 Hz
APF output inductor	0.2 mH
DC side capacitors	5000 μF each
DC side voltage	750 V
Switching frequency	10 kHz
Power converter	IGBTs

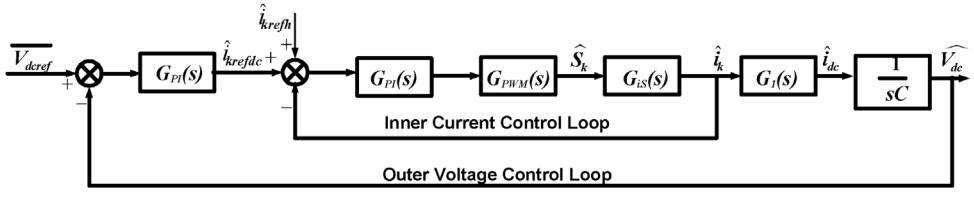


Fig. 5. Control block diagram of APF using three-level inverter.

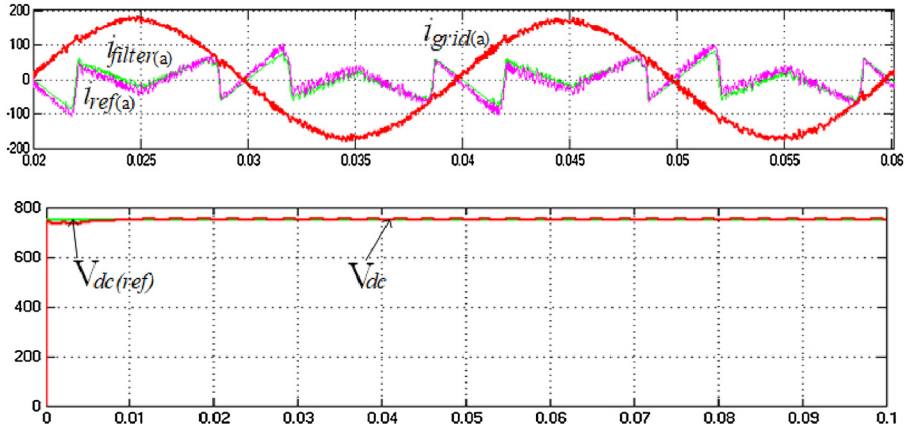


Fig. 9. Current tracking and voltage tracking performance.

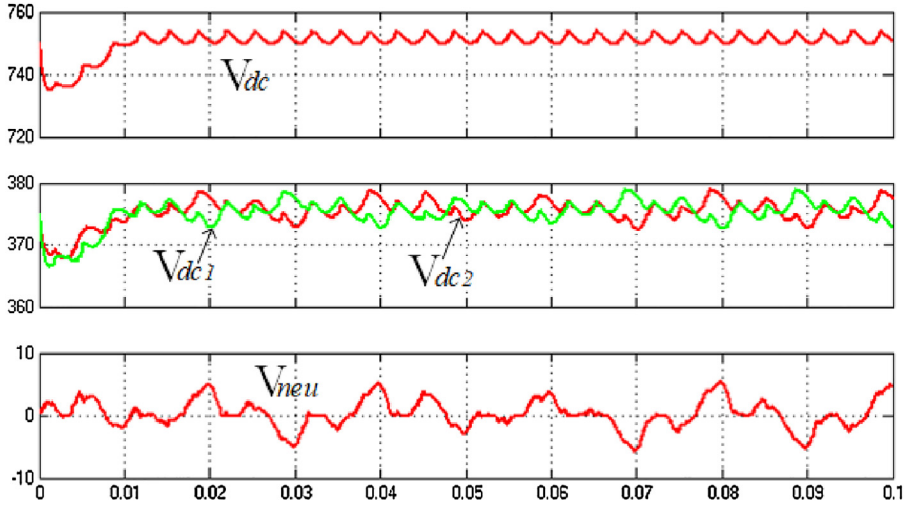


Fig. 10. Midpoint voltage control waveform with same capacitors value.

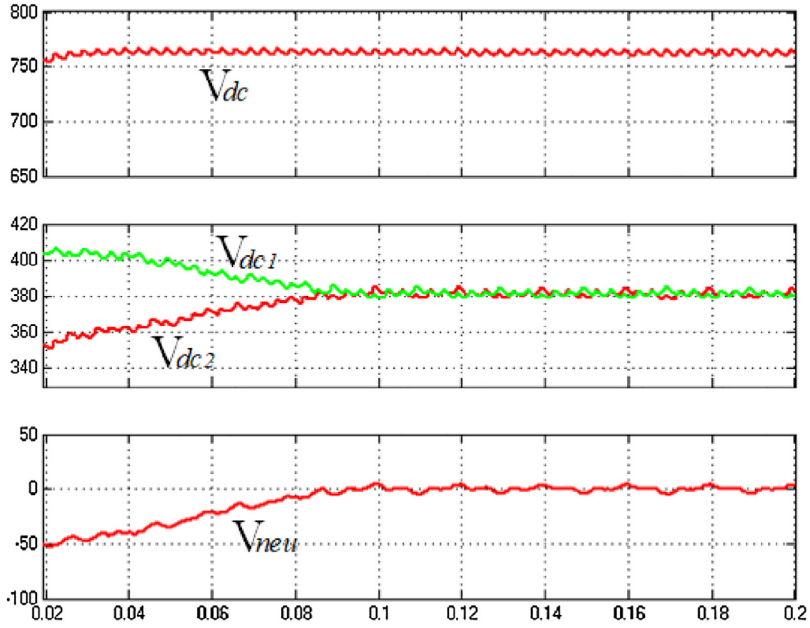


Fig. 11. Midpoint voltage control waveform with different capacitors value.

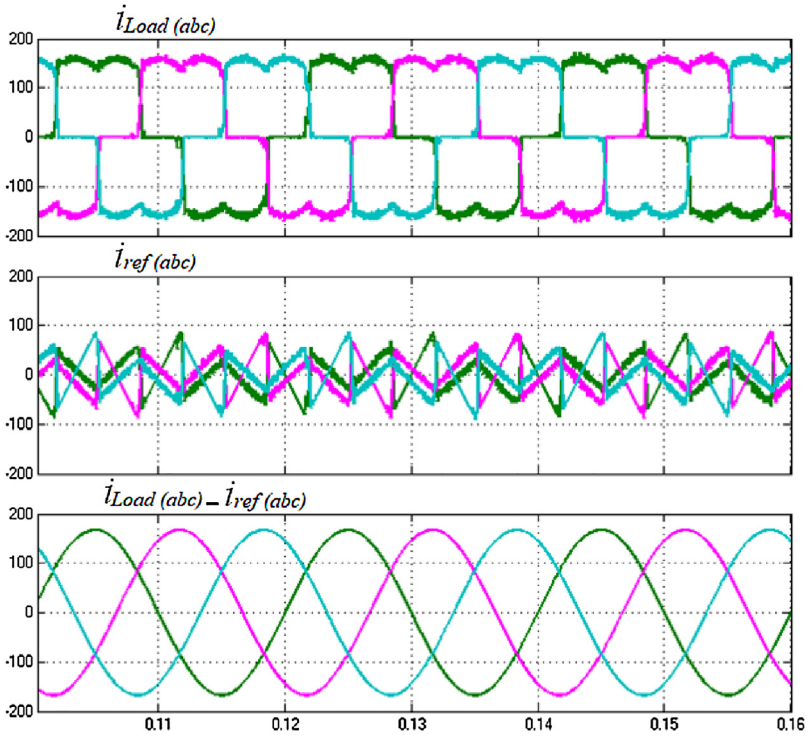


Fig. 12. Current harmonic detection waveform.

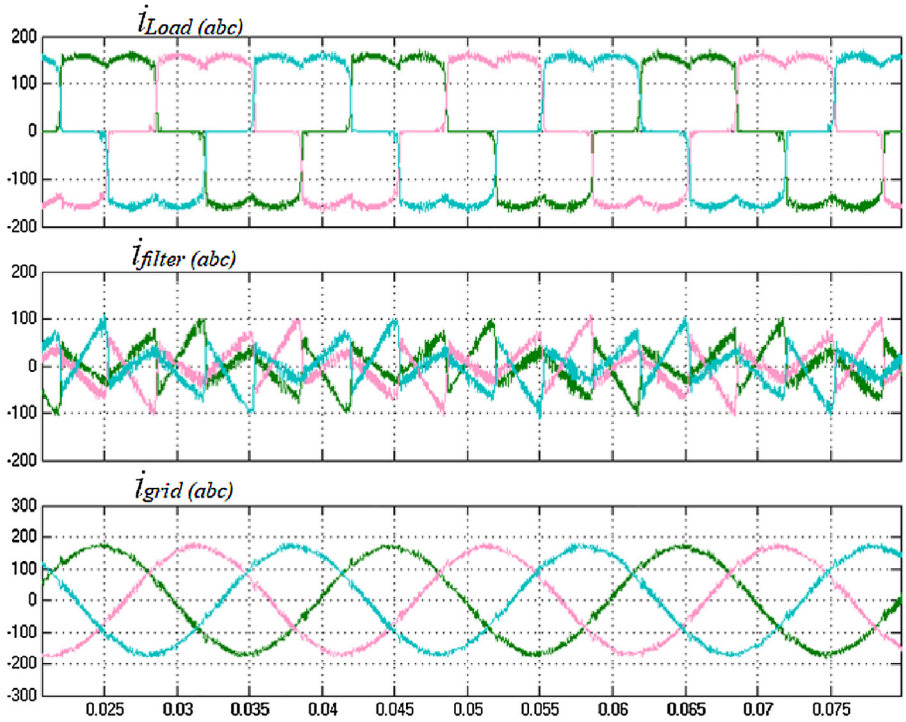


Fig. 13. Compensation effect of three-level APF.

voltage control is for power balance and hence to derive a simplified model, a lossless system is assumed and both the capacitors are considered as a single unit. Equating input and output power, the transfer function, $G_1(S)$ relating the APF output current to DC-side current is given as:

$$3i_k E_k = V_{\mathrm{dc}} i_{\mathrm{dc}}$$

where V_{dc} is DC-side voltage and E_k is the three-phase line-to-line RMS voltage and

$$G_1(s) = \frac{3E_k}{V_{\mathrm{dc}}}$$

The simplified block diagram of the voltage control loop is shown in Fig. 7. For the outer voltage control loop the influence of the inner current control loop can be neglected. The inner current control loop has a high gain in the frequency range until 3 kHz, hence a gain of "1"

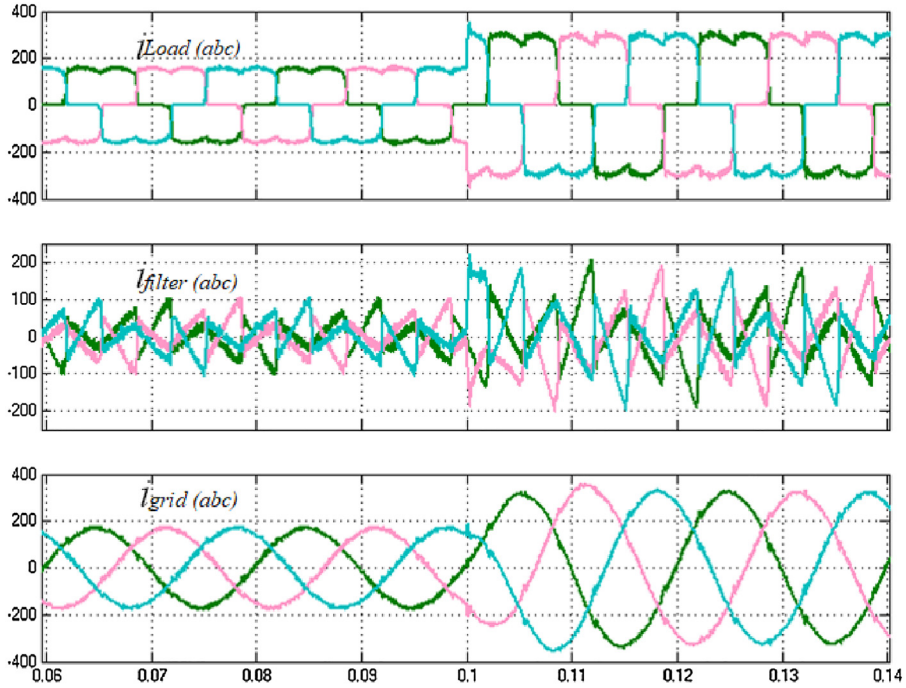


Fig. 14. Compensation effect of three-level APF during load change.

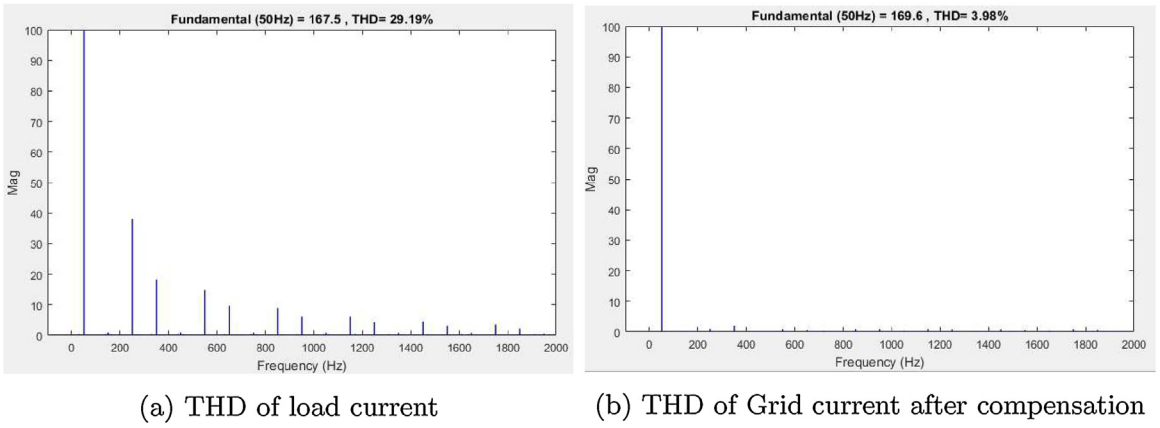


Fig. 15. THD of the grid current before and after compensation.

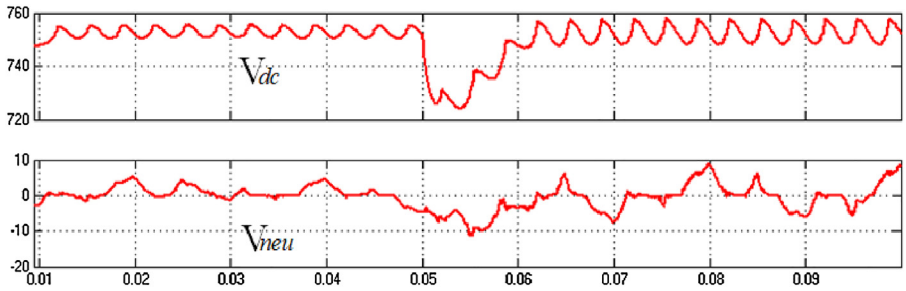


Fig. 16. DC side voltage and neutral point voltage during load change.

can be taken for its equivalent closed-loop transfer function. The outer control loop is designed with a low-crossover frequency, generally 100 Hz to prevent output current distortion. The effect of the inner current control loop is seen at higher frequency in the form of a resonance peak. However, these are not considered for design of the voltage control loop as they are beyond the frequency of interest. The loop gains of uncompensated and PI compensated voltage control loop are shown in Fig. 8.

4.5. Neutral-point voltage control

Neutral-point voltage imbalance is an important issue in NPC inverter topology [25]. An unbalanced neutral-point voltage will cause damage to switching devices, and a low-frequency ripple appears at the

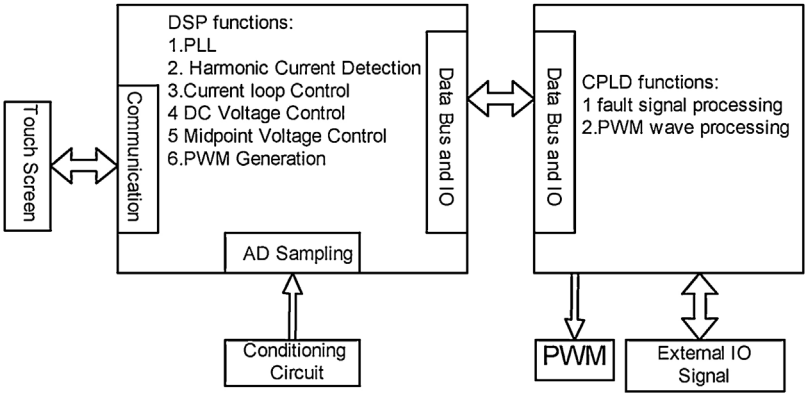
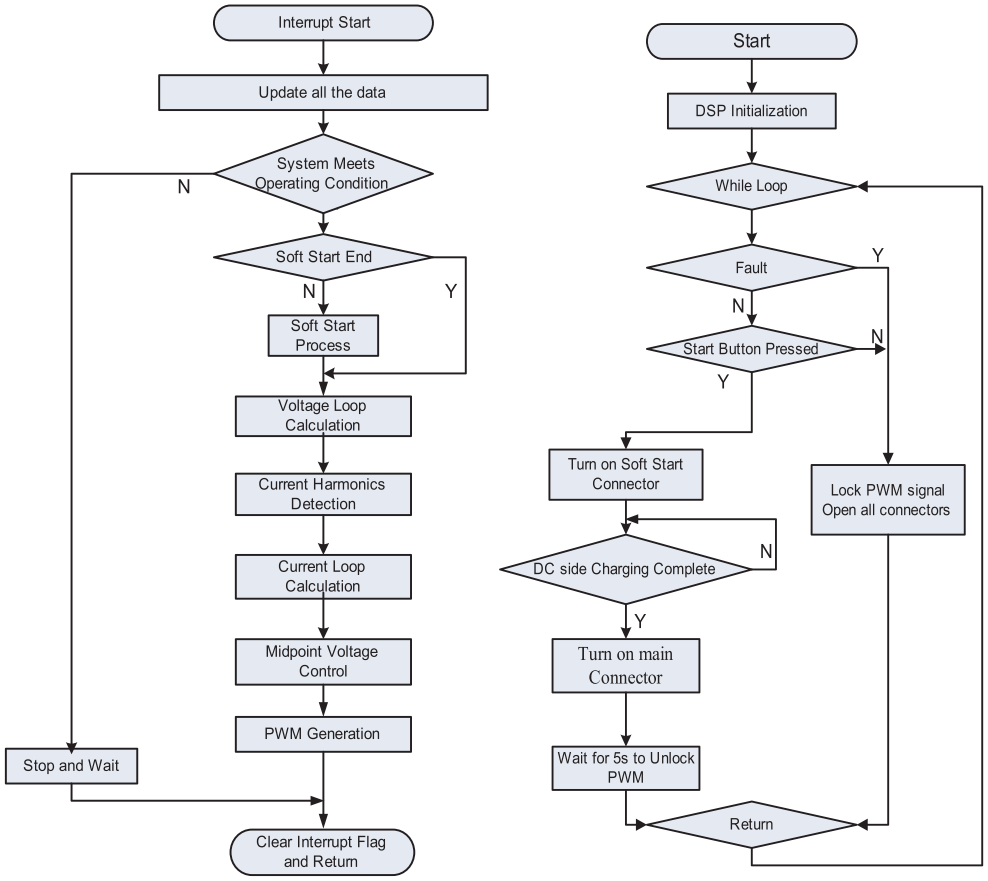


Fig. 17. Overall block diagram of experimental setup for controller and monitoring.



(a) Interrupt subroutine flow diagram (b) Program flow diagram

Fig. 18. Overall program structure for digital controller implementation in DSP.

neutral point resulting in low-frequency harmonics in the output voltage, which increases the THD of the output current [33]. As it is complicated to solve this issue directly, various algorithms have been introduced to balance the neutral-point voltage for carrier based modulation as well as for space-vector modulation.

Based on a multicarrier modulation strategy, a zero-sequence injection method is used to control the neutral-point voltage in this paper [34]. In this paper, using the neutral current direction and the voltage difference between the two DC-side capacitors, the appropriate zero-sequence component is calculated and is superimposed on the reference voltages. Neutral-point voltage control based on space vector modulation (SVM) can also be used [35,36].

5. Simulation results

The shunt three-level active power filter connected to a non-linear load is simulated using the MATLAB/SIMULINK environment. The system parameters considered for the study of the APF for simulation are mentioned in Table 1.

The simulation is carried out using the controller parameters from the derived model and shown in Fig. 9. This validates the derived model and truly represents the characteristics of the three-level inverter. Fig. 9 shows the current tracking and voltage tracking performance. It can be seen that the tracking error in the inner current control loop is very small, and the average model used for the voltage control loop also results in very good tracking of the reference DC-side voltage.

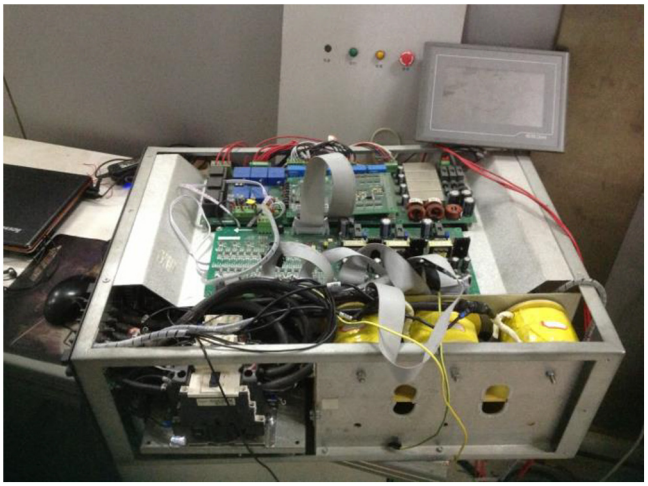


Fig. 19. Three-level APF overall laboratory experimental setup.

Table 2
System parameters used in experiment.

System parameter	Value
Line voltage	50 V
APF output inductor	0.4 mH 100 A
DC side capacitors	19,800 μF
DC side voltage	100 V
Switching frequency	10 kHz
Power converter	IGBTs

Fig. 10 shows the response of the midpoint voltage control. The method to control midpoint voltage is based on the injection of a zero-sequence voltage with the SPWM modulation strategy used in the simulation. It can be seen from the simulation that the maximum fluctuation in the midpoint voltage is 4 V, which is quite reasonable. In the actual system, the DC-side capacitors value cannot be exactly the same, as discussed earlier. In order to test the effectiveness of the midpoint voltage control in extreme cases, the two capacitance values are set to 4000 μF and 6000 μF, and the initial voltage of the two capacitors is set to 412 V and 338 V while the other parameters remain unchanged. The simulation under these circumstances is shown in Fig. 11. The simulation based on harmonic detection is shown in Fig. 12. As can be seen from the waveforms below, the harmonic detection algorithm based on TTA can accurately detect the harmonic content of the load.

The compensation characteristic of the three-level APF is shown in Fig. 13. The nonlinear load is an uncontrolled rectifier with an inductor on the DC-side of value 0.08 mH and a resistance of 3.2 Ω. The amount of rectifier load current is 160 A with 28.45% total harmonic distortion. The three-level APF compensation result is shown in Fig. 13 where the uppermost plot is the load current, the middle one is filter output current and the lower one is the grid current after compensation. It can be clearly seen that about 90% harmonic reduction occurs after compensation.

The compensation effect of the three-level APF due to sudden load change is shown in Fig. 14. It can be seen that when the load changes abruptly the output has some reaction immediately, but reaches the steady state within half of a fundamental cycle. The APF response to track harmonics is also fast and settles down within half a fundamental cycle. Fig. 15a shows the FFT analysis of the load current and Fig. 15b shows the FFT analysis of the grid current with THD reduced to 3.42% from 28.45%.

As can be seen from Fig. 16, when the load suddenly increases, the DC-side voltage and the midpoint-voltage fluctuations also increase because the APF output current suddenly increases, resulting in a sudden increase of the neutral current, but still the DC side voltage and the midpoint voltage fluctuations are small (RMS less than 5 V).

6. Experimental verification

The prototype model of the shunt APF was developed in the laboratory to validate the APF functionality using the three-level NPC inverter. DC side of the inverter is connected with a 35-kW Chroma DC power supply which is used as dc source voltage for inverter during the experiment of three-level NPC inverter setup. The three-phase variable AC supply is used as grid source which connected to three-level APF and nonlinear load. An uncontrolled bridge rectifier is used as a nonlinear load.

6.1. Hardware setup for control

The control system hardware circuit mainly consists of three circuit boards, a control board, a logic control panel and an IGBT driver board. The Control board mainly includes the digital signal processor (DSP), complex programmable logic device (CPLD), analog to digital convertor (AD), analog signal conditioning circuitry and digital IO signal isolation circuit. For a DSP TI's TMS320F2812 chip is selected, while Altera Corporation's MAXII series EPM1270T144I5 chip is selected as CPLD. The division of tasks between CPLD and DSP is shown in Fig. 17. It can be seen that DSP plays a leading role in the digital control of the entire device, Soft PLL, harmonic current detection algorithms, the digital control of the current loop, DC voltage and the midpoint voltage balance digital control, generation of PWM signal to drive the IGBT. CPLD plays an auxiliary role in the overall digital control; due to its rapid response, fast processing and hardware features, it is used to detect error signals and respond quickly, for example to a fault signal or a

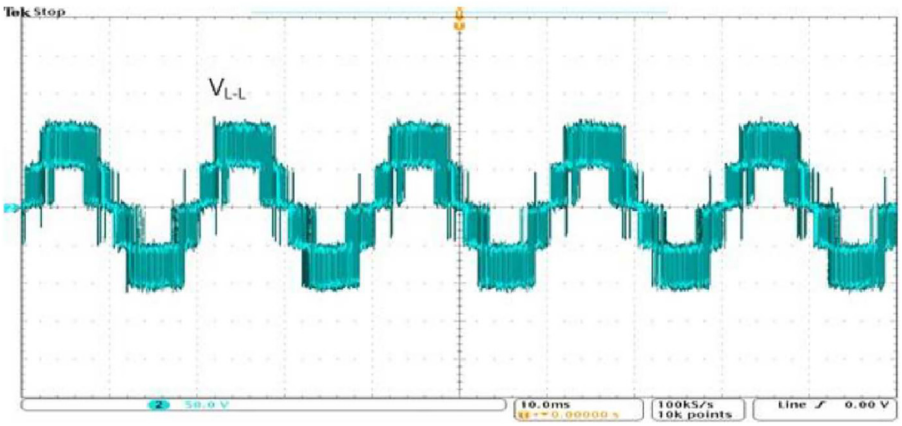


Fig. 20. Three-level inverter output voltage.

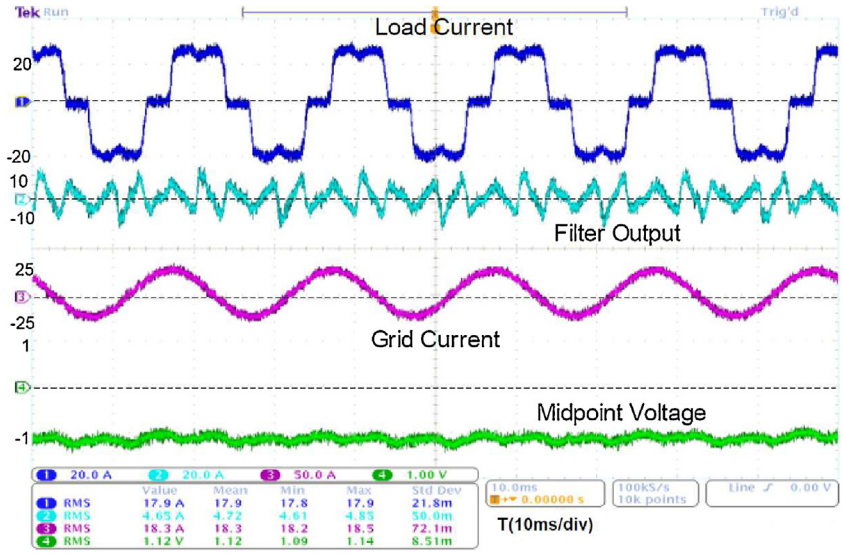


Fig. 21. Experimental waveform of APF after compensation.

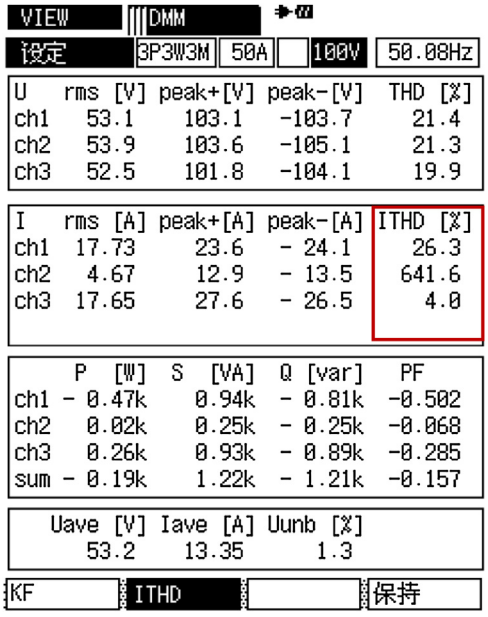


Fig. 22. THD of load and source.

PWM signal.

The computing panel of the digital control board also has three AD chip, the model is AD7658. Any analog signals from external sensors to digital control panel are passed through the AD for analog-to-digital conversion, but before AD sampling the signal is passed through an analog filter which filters out unwanted high-frequency interference. In a three-level APF, the signals that need to be conditioned through analog filter are three-phase grid voltage, two DC bus voltages, three-phase filter output current, and the three-phase load current. So the design of the cut-off frequency of the low pass filter for this analog signal conditioning needs special attention.

The program is written in the C language and can be divided into three blocks: the while loop in the main program, the timer interrupt and the communications interrupt. For safe operation of the device, a main loop is devised which checks the fault signal at start of every cycle. If fault status is normal, the corresponding data processing and control algorithms are carried out else, it will stop all the PWM outputs, causing the device operation to stop. The program flow diagram is shown in Fig. 18a.

Since the switching frequency is 10 kHz so the interrupt cycle is of 100 μs. For every time interrupt occur, the control program of the three ADs start sampling the external analog signal; once the signal is sampled the conditioning of the sample is the next step. The program reads the DC-bus voltage, AC voltage signal, load current, neutral-point voltage and APF output current. First of all, the AC voltage is taken and used for generating a reference sine wave, after which harmonic and reactive current extraction from the load current is carried out. After calculating the reference current through the DC-voltage control, the current control algorithm is carried out. Finally, the midpoint voltage-control program runs and the zero sequence component is added to the modulating voltage and then ultimately PWM signal is generated. The program flow diagram is shown in Fig. 18b.

6.2. Experimental results

Fig. 19 shows the three-level active power filter prototype developed in the laboratory. The system parameters used in the experimental platform are shown in Table 2.

The experiment on the three-level APF is carried out step by step. In the first step, the APF is checked as a rectifier, so the APF is working as a controlled rectifier to maintain the DC-voltage constant without producing harmonics at the output. Fig. 20 shows that the APF output line-to-line voltage has five levels and approximates a sine wave, resulting in low loss, low electromagnetic interference and low waveform distortion as compared to a conventional inverter. Fig. 21 shows the load current, grid current and APF output current and midpoint voltage in the steady state. It can be seen that the grid current waveform after compensation compared to the load current waveform has more obvious improvement. Besides, the midpoint voltage fluctuation meets the design requirements. The THD of the source current is much reduced, from 26.3% to 4% as shown in Fig. 22.

Figs. 23 and 24 show the compensation effect of the three-level APF when there is a sudden change in load. Fig. 23 shows the condition of sudden change from no load to load while Fig. 24 shows the opposite. It can be seen from the waveforms when load is changed suddenly, the output has some reaction immediately but reaches the steady state within one fundamental frequency cycle. The midpoint voltage at a sudden load experienced fluctuations, obviously this is because the output current of the APF suddenly increases, resulting in a sudden increase in line current, but still the midpoint voltage fluctuations remain small (less than 2 V).

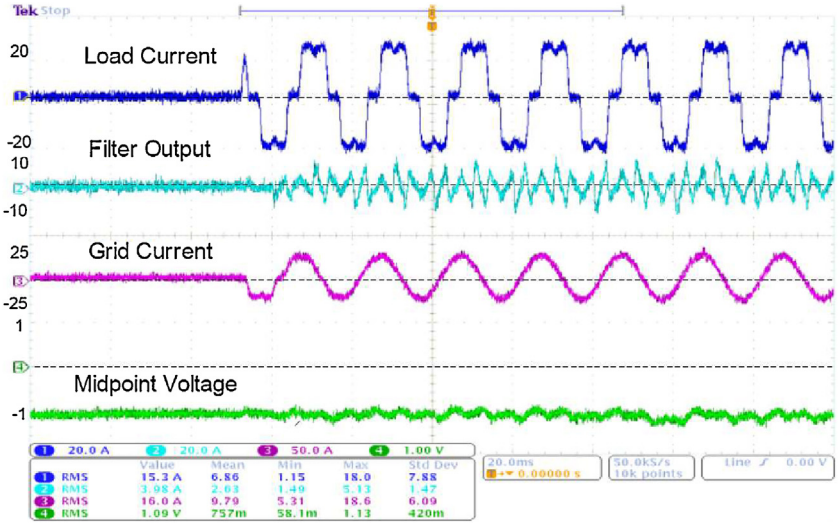


Fig. 23. Compensation waveform in case of sudden load change from no load to load.

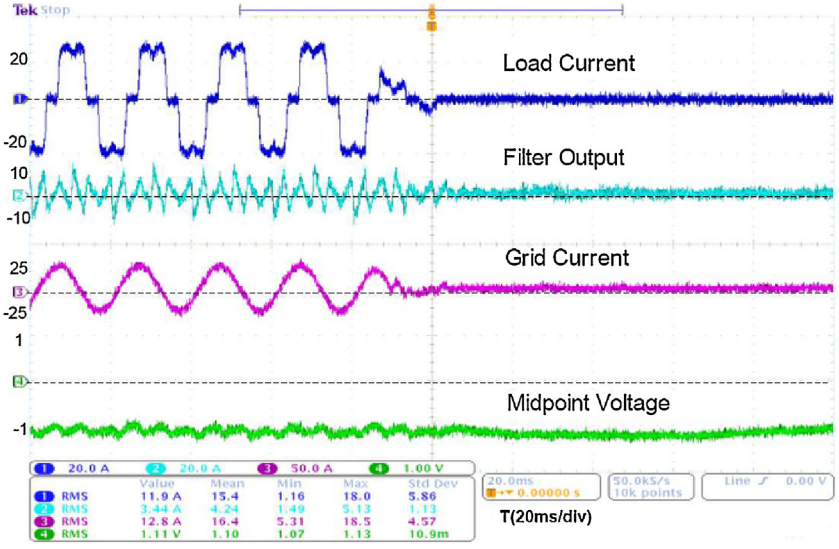


Fig. 24. Compensation waveform in case of sudden load change from load to no load.

7. Conclusion

This paper presents the suitability of using three-level NPC inverter topology for a high-power medium voltage APF application. A three-level NPC inverter topology can address the deficits of the two-level inverter topology, and the neutral-point voltage unbalance (considered to be one drawback) does not limit the effectiveness of the topology. The paper mainly focuses on the modelling and controller design of three phase three level NPC inverter. A simplified novel approach was used to derive a model for three-phase three-level NPC inverter using state-space analysis. The derived model accurately represents the system characteristics and helped in controller design, resulting in a good tracking response of the current controller. The DC-side voltage is also maintained at reference voltage with good precision. The paper also utilizes a harmonic extraction technique based on the time transformation algorithm in the proposed topology. This harmonic extraction method provides fast and accurate reference current generation. The overall compensation performance was evaluated in simulation and on experimental platform, showing excellent compensation performance in the steady and dynamic states.

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