Compensation of CVT Increased Error and Its Impacts on Distance Relays

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***Abstract*—Increased ratio error of capacitor voltage transformers (CVTs) has been recently encountered in several substations in Iran. The results of the performed diagnostic tests indicate that short-circuited capacitor elements, especially in the low-voltage capacitor, have increased the CVT error. In this paper, some simple and effective techniques are suggested to solve this problem. One of the proposed methods to compensate the increased error is utilization of an auxiliary voltage transformer (AVT), which does not require disassembling the CVT. The practical aspects of this method, its effects on the CVT transient response, and the influence of the AVT improper design on the performance of distance relay are scrutinized in this paper. Furthermore, the design requirements of the AVT to avoid distance relay malfunctions due to the AVT ferroresonance are discussed.**

***Index Terms*—Auxiliary voltage transformer (AVT), capacitor voltage transformer (CVT), distance relay, ferroresonance, transient response.**

I. Introduction

VARIOUS problems have recently arisen in some of the high-voltage (HV) substations in Iran. These problems include distance relay blocking due to the fuse failure unit operation [1], failure to synchronize the transmission line with the grid, and unequal measured voltage magnitudes of the feeders connected to the same bus. Initial investigations indicated that the increased error of the capacitive voltage transformer (CVT) is the main reason for these problems.

A CVT is comprised of a capacitive voltage divider (CVD), a compensating reactor (CR), an intermediate voltage transformer (IVT), and a ferroresonance suppression circuit (FSC) (Fig. 1). The CVD consists of an HV capacitor C_1 and a low-voltage (LV) capacitor C_2, both consisting of some capacitor elements connected in series [2].

In recent years, some investigations have been reported on the CVT temporary error due to the transient voltage appearing at the CVT output terminal as a result of a nearby fault [3], [4]. However, few reports regarding the increased CVT steady-state error or the causes of CVT failure have been published. An increase in CVT error due to a change of the CR reactance and more important, change of the CVD capacitance is reported by a CVT manufacturer [5]. Old capacitors were insulated by mineral oil-impregnated kraft paper. It is concluded in [5] that the increased ratio error was caused by the insulation material, which is prevented in modern CVTs by using polypropylene film. Although this insulation material is a proper substitute for kraft paper, investigations on ten impaired CVTs demonstrated that the polypropylene film was the major insulation for these CVT capacitor elements [6]. Consequently, the CVT increased error is not completely prevented even by using better insulation materials.

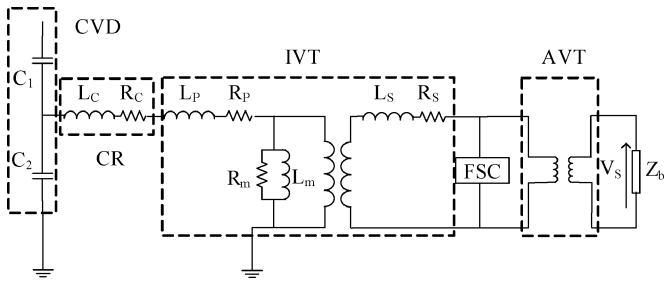

Fig. 1. Circuit diagram of a typical CVT.

A statistical assessment of CVT failures is accomplished for the Brazil grid and the steady-state increase of CVT ratio error is introduced as a serious problem of operating CVTs [7]. Furthermore, comprehensive *in-situ* diagnostic tests are presented in [6]. In this study, ten CVTs with the rated primary voltages of 230 or 400 kV, which have voltage ratio errors higher than 5%, are chosen for diagnostic studies of the increased ratio errors. Experimental analyses reveal that the excessive ratio error is mainly caused by the short-circuited capacitor elements of CVTs. In other words, the measured capacitances of C_1, C_2, or both, for nine of the investigated CVTs are considerably different from their rated values, taking into account their permissible tolerances. Moreover, an auxiliary voltage transformer (AVT) is widely utilized to adjust the input voltage of synchronizing and directional earth fault (DEF) relays. The occurrence of ferroresonance due to saturation of the AVT connected to the CVT secondary side is introduced as a main reason for short circuits of capacitor elements. This phenomenon may only take place if an improper AVT is employed [6].

In this paper, several practical methods for compensating the CVT error are discussed. Besides replacing the entire CVD or just the defected capacitor elements, which require a considerable amount of time and expense, two other methods are suggested. The first method is the utilization of a series capacitor at the end of the C_2 terminal. As the second method, an AVT is recommended to be connected to the CVT secondary side. To investigate this method, the transient response of a CVT, which

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TABLE I
RATED PARAMETERS OF THE SIMULATED 400-kV CVT

Parameter	Value
C_1 [nF]	7.8
C_2 [nF]	125
No. of series elements for C_1	293
No. of series elements for C_2	18
$L_{eq}=L_C+L_P+L'_S$ [H]	75.8
$R_{eq}=R_C+R_P$ [Ω]	2794
R_S [Ω]	0.12
Turn ratio of IVT	233

has some short-circuited capacitor elements, is studied and compared with the IEC standard requirements [8]. The results of the performed studies show that if the conditions indicated in this paper are satisfied, the proposed methods can be implemented *in-situ* with negligible cost and without the need to disassemble the impaired CVT.

Ferroresonance between the AVT magnetizing inductance and the CVD capacitors, which is briefly called "AVT ferroresonance", may occur if an AVT with an improper voltage factor is utilized at the secondary side of a CVT [6]. In this paper, the AVT ferroresonance phenomenon is investigated using an accurate hysteresis model. In addition, as the worst possible case, the AVT ferroresonance caused by the transmission line reclosing and its influence on the performance of line distance relay during in-zone and out-of-zone faults is studied. It is shown that the relay maloperation can be prevented using an appropriate AVT design. Finally, the AVT tapping arrangement and an appropriate tap-setting method are suggested for practical implementation of this proposed method.

II. COMPENSATION OF THE INCREASED CVT ERRORS

A. CVT Increased Error

Short-circuited capacitor elements of a CVT increase capacitive amounts of C_1 or C_2. Under such conditions, not only does the CVT ratio error increase, but also resonance of the IVT series impedance with the CVD capacitors, which minimizes the CVT output voltage phase displacement (PD), is not met. Briefly, this event has the following consequences:

- The short circuit of C_1 elements increases the CVT output voltage. For example, for a typical CVT shown in Fig. 1 and with the parameters given in Table I, a short circuit of 29 elements (i.e., about 10% of the capacitor elements), results in a 10.3% increased ratio error and 0.5 min additional PD, for a resistive burden of 100 VA.
- The short circuit of C_2 elements decreases the CVT output voltage. For example, for the studied CVT, about 11% short-circuited elements give rise to a 10.5% increased ratio error and 11-min additional PD.

Due to the unfavorable impacts of the increased errors on the measurement, control, and protection equipment, some techniques to compensate these errors are proposed in this paper.

According to some of the manufacturers, the life expectancy of CVTs is about 25–30 years [9]. Thus, if the operation lifetime of a CVT is longer, it can be assumed that the increased CVT error is caused by the insulation aging. In such a condition, occurrence of subsequent damages to the CVD is highly probable, especially when the measured dissipation factor is high.

All electrical insulations in power apparatus have a measurable quantity of dielectric loss for an applied ac voltage, known as the dissipation factor, tgδ [10]. The typical value of this parameter is about 0.1% for CVDs which use the polypropylene film insulator and about 0.2% for those which use a combination of polypropylene film and paper [8]. A significant increase from these typical values indicates that the quality of the CVD insulator has been degraded.

If the CVT lifetime is more than 30 years or the measured tgδ is higher than 0.2%, it is advisable to replace the entire CVD, in order to prevent the subsequent damages. Otherwise, some reasons other than the general aging may have resulted in failure of the CVD capacitors. In such conditions when the *in-situ* tests are passed by the IVT [6], it may be possible to continue utilizing the CVT, without replacement or disassembly of the CVD. This is possible after compensating the increased CVT error using appropriate techniques. Two proposed techniques to compensate the increased CVT error are described in the following subsections.

Although capacitor replacement is a reliable method to solve the problem of increased CVT error, this technique is very expensive and time consuming. In addition, due to some operational restraints, technical issues, and economical considerations, replacement of the impaired CVT, the entire CVD, or even blown capacitor elements may not be easily possible and practical, whereas both of the proposed techniques can be implemented as simple and economical alternative methods in a short time.

B. Compensation of the Increased C_2 Capacitance

The capacitor C_2 includes just a limited number of capacitive elements. Therefore, only one or two short-circuited elements usually results in an increased ratio error of more than 5%. However, overvoltages across the healthy capacitor elements are still tolerable. The terminal at the end of C_2 (i.e., the one which must be connected to the ground or the communication equipment) is normally accessible inside the CVT terminal box. Thus, in the first proposed method, to compensate the short-circuited capacitor elements of C_2, an appropriate amount of capacitance can be connected in series with C_2. Since this capacitor is connected to the end of C_2, disassembling the CVD is not required.

In this method, not only should a capacitor with the rated voltage of a few kilovolts be used, but it should also be insulated from the grounded metallic CVT terminal box. Moreover, the bushing through which the end of the C_2 terminal is accessible must be able to tolerate this voltage. Therefore, to implement this method, the capacitor-rated voltage and its dimensions must be chosen appropriately. Meanwhile, it should be considered that the additional PD can also be compensated by this method.

C. CVT Error Compensation Using an AVT

The utilization of an appropriately designed AVT is the other proposed method to compensate the increased CVT error caused by a few short-circuited capacitor elements of C_1 or C_2. An

TABLE II
CONSTANT PARAMETERS VALUES

n	a_n	b_n	c_n	d_n	e_n
1	-0.49493	-0.08711	-0.593e-7	0.00040	0.00481
2	-0.55892	-0.08555	0.514e-7	0.00034	0.00481

AVT is a small low-power and LV transformer which can be connected to the secondary side of the CVT in order to correct the ratio error.

If the increased CVT ratio error is caused by the short circuit of C_1 elements, which results in output overvoltage, using an AVT is usually sufficient to compensate the ratio error, whereas the additional PD should also be compensated if a few capacitor elements of C_2 are short-circuited, which results in output undervoltage. This could be important when the CVT is connected to a distance relay or particularly a tariff meter where an additional error in the measurement of active power is caused by the increased PD.

Utilization of the AVT connected to the CVT secondary side has already been experienced in many substations to adjust the input voltage of synchronizing relays and DEF units. Meanwhile, to compensate the CVT increased errors using this method, it must be investigated: 1) whether the impaired CVT with blown capacitor elements can fulfill the IEC 60044-5 requirements, especially subsidence voltage and damping of ferroresonance oscillations, considering a nonsaturable AVT to compensate the increased CVT ratio error, and 2) whether AVT saturation may result in additional transients.

III. TRANSIENT RESPONSE OF AN IMPAIRED CVT

The impacts of the blown CVD capacitor elements on the subsidence transients and ferroresonance oscillations of the CVT are studied in this section. Obviously, such a study requires an accurate CVT model.

A. CVT Modeling

The technical parameters of a 400-kV CVT, the circuit diagram of which is shown in Fig. 1, are given in Table I. The CVT is equipped with a passive FSC (PFSC) which is a 2.8-Ω damping resistor in series with a saturable inductor. The hysteresis curves of this reactor and the IVT magnetic core are measured at the frequency of 1 Hz to reduce the effect of winding internal capacitances [11]–[13]. The hysteresis characteristic of the IVT, the PFSC inductor, and the AVT are modeled using the Preisach theory. The hysteresis characteristic of the AVT is assumed to be similar to the characteristic of the PFSC inductor [6]. The ascending part of the IVT major loop after being shifted to the origin of coordinates is precisely represented by fitting the function B(H) to the measured data, using an LES curve-fitting method

$$B(H) = \begin{cases} a_1 \mathrm{tg}^{-1}(b_1 H) + c_1 H^2 + d_1 H + e_1 & H \geq 0 \\ a_2 \mathrm{tg}^{-1}(b_2 H) + c_2 H^2 + d_2 H + e_2 & H < 0 \end{cases} \quad (1)$$

where the constants a_n, b_n, c_n, d_n, and e_n for the IVT magnetizing branch are given in Table II.

The magnetizing branches of the IVT, AVT, and PFSC inductor are modeled using variable current sources which resemble the excitation current i_e defined by

$$i_e = i_h + i_{\mathrm{eddy}} \quad (2)$$

where i_h is the hysteresis current and is determined based on the Preisach hysteresis model, and i_{eddy} is the eddy current

$$i_{\mathrm{eddy}} = \sigma_e \times v_e \quad (3)$$

where $\sigma_e = 8 \times 10^{-4}\ \Omega^{-1}$ is the eddy current factor of the laminations [14], and v_e is the excitation voltage.

The total core flux density B consists of two parts

$$B(H) = B_{\mathrm{hys}}(H) + B_{\mathrm{sat}}(H) \quad (4)$$

where H is the core magnetic-field intensity. $B_{\mathrm{hys}}(H)$ is the flux density corresponding to the hysteresis component of the magnetization characteristic, defined by the Preisach theory [15]. Meanwhile, $B_{\mathrm{sat}}(H)$ is a linear single-valued function which describes the flux density in the saturation region as

$$B_{\mathrm{sat}}(H) = \frac{l_c}{N^2 A} L_{\mathrm{sat}} H \quad (5)$$

where L_{sat}, N, l_c, and A denote the air-core inductance, the number of winding turns, the core mean flux path length, and the effective core cross-section area, respectively [16].

Using the method introduced in [16] and [17], the measured hysteresis loops data are used to identify the Everett function [18], which defines the hysteresis loops for the Preisach model. Numerical implementation of the Preisach model (i.e., determination of the magnetic flux density B as a function of the field intensity H) is illustrated in [19]. The value of i_h in each sampling period is determined by an iterative method adopted to solve the system equations.

This hysteresis model can generate the symmetric and asymmetric minor loops and the remanent flux, which is essential to study the CVT transients after fast autoreclosure of the transmission line [16].

B. Subsidence Voltage

When a close-in short-circuit fault occurs on a transmission line, the CVT primary voltage drops to near zero, similar to a step function. Under such a condition, the CVT secondary voltage includes some oscillatory components known as subsidence transient voltage [20], [21]. The subsidence voltage caused by the short circuit at the voltage zero point may result in the malfunction of high-speed digital relays such as distance relays [22]. This voltage consists of oscillatory low frequency and decaying dc components.

In order to reduce the adverse effects of the CVT subsidence voltage on protective relays, the magnitude and duration of the subsidence transients should be limited to the prespecified values determined by the IEC standard [8]. Thus, the CVT transient response test must be performed on the protection class CVTs, as a type test.

In order to compare the subsidence voltage of a healthy CVT with that of the impaired one, several cases are investigated. For

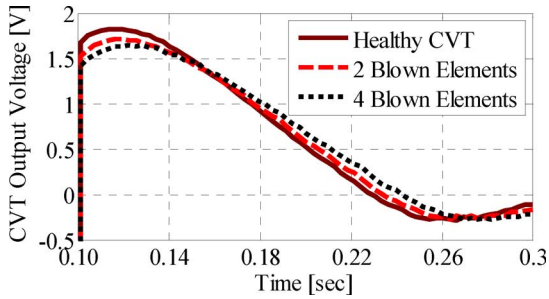

Fig. 2. CVT subsidence voltage for a fault at the voltage zero.

instance, in Fig. 2, the transient response of a healthy CVT is compared with the responses of two impaired CVTs during a short circuit at the voltage zero instant (i.e., the worst case from the viewpoint of relay maloperation [20]). In this case, the impaired CVTs have two and four short-circuited C_2 capacitor elements. This figure shows that the magnitude of the CVT subsidence voltage has negligible variations when C_2 capacitors are short-circuited. The same result is observed when C_1 capacitor elements are short-circuited. Consequently, blown capacitor elements do not have a major effect on the subsidence voltage oscillations.

C. CVT Ferroresonance Oscillations

CVTs are prone to ferroresonance due to the series connection of the IVT magnetic inductance with the CVD equivalent capacitance which is the sum of the C_1 and C_2 capacitances. CVT ferroresonance can take place particularly when a short circuit occurs on the circuit connected to the CVT secondary side, and it is cleared by the fuse which protects the secondary circuit.

When some of the capacitor elements are blown, the equivalent capacitance of the CVD increases which results in an increment of the stored energy in the CVD. In this condition, the FSC damping resistor may not be able to mitigate the ferroresonance of the impaired CVT, especially when some of the C_1 capacitor elements are blown which increases the IVT primary voltage.

In order to investigate the effects of the blown C_2 capacitor elements on the CVT ferroresonance, a short circuit is applied on the CVT secondary side, which is cleared after 50 ms. As illustrated in Fig. 3, the oscillatory ferroresonance voltage does not change considerably for short-circuited C_2 capacitor elements.

The C_1 capacitor is comprised of numerous elements. The short circuit of some of the C_1 elements increases the stored energy in the remaining CVD capacitor elements. Moreover, it increases the primary voltage of the IVT. As illustrated in Fig. 4, 10% short-circuited C_1 elements (29 elements) result in magnification of ferroresonance oscillations. It should be noted that if the number of the blown capacitor elements is more than 13% of the total number of C_1 elements (38 elements), the FSC will not be able to damp the ferroresonance oscillations, as depicted in Fig. 4. Therefore, in order to prevent more damage to the CVD capacitors and to ensure an acceptable transient response, using the CVT error compensation method is recommended only if less than 10% of the C_1 capacitor elements are short-circuited.

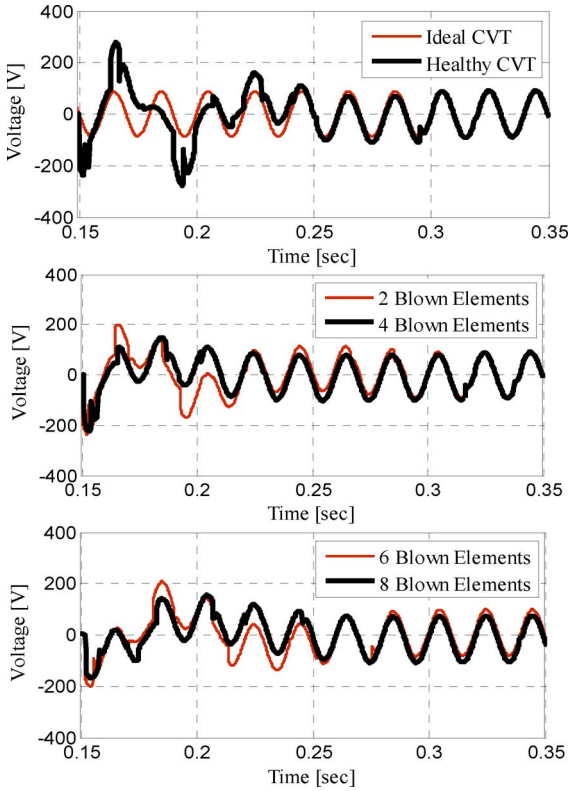

Fig. 3. Comparison of the CVT output voltages during ferroresonance for different numbers of short-circuited C_2 elements.

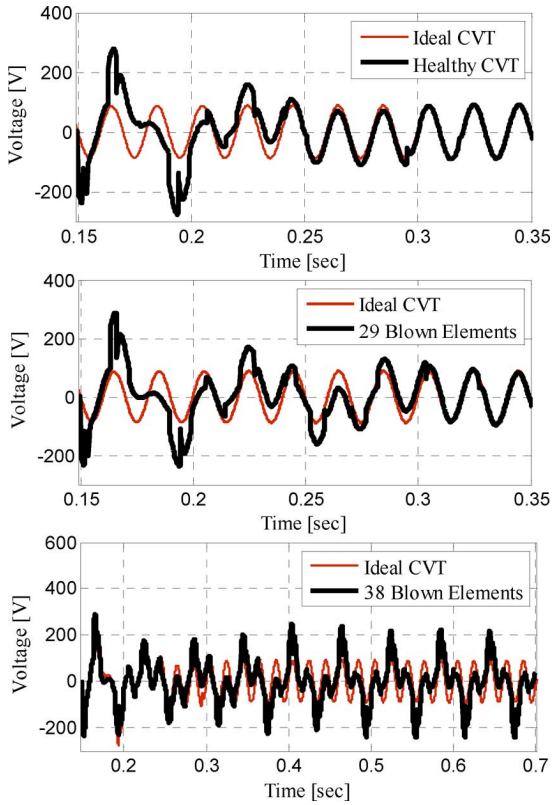

Fig. 4. Comparison of the CVT output voltages during ferroresonance for different numbers of short-circuited C_1 elements.

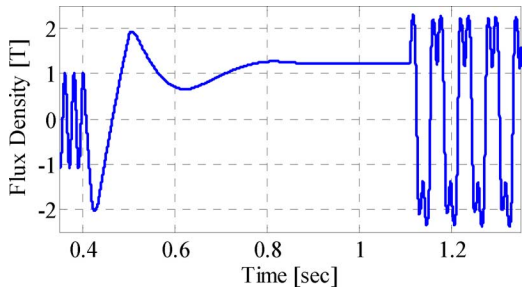

Fig. 5. AVT core flux density during line reclosure.

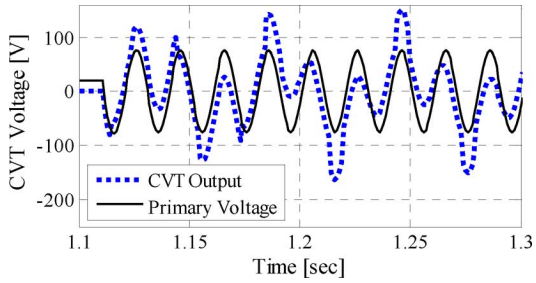

Fig. 6. CVT output voltage compared to the scaled primary voltage.

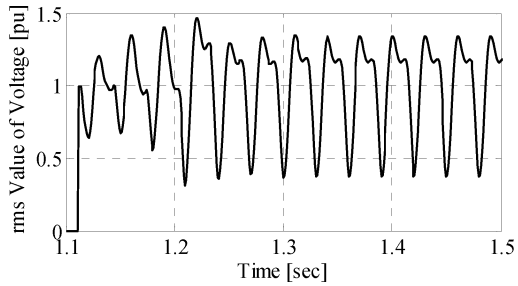

Fig. 7. Per-unit rms value of the CVT voltage after reclosing the faulted line.

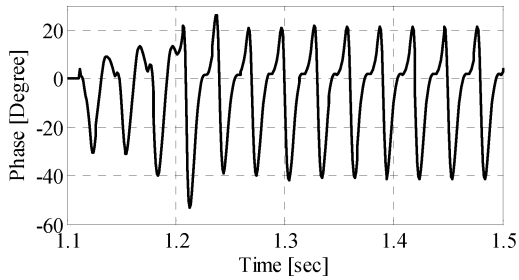

Fig. 8. Phase of the CVT output voltage.

IV. Compensation of Increased CVT Error by AVT

Compensation of the increased error using AVT is preferred to the other methods, because it involves less labor and expenses, and it can be implemented simply in the substation. Moreover, it does not lead to any subsequent damage to the CVT, such as penetration of moisture and pollutants into the insulation oil, caused by disassembling the CVT or CVD. However, a saturable AVT may affect the performance of the transmission-line distance relay which requires investigation.

In this method, an AVT is connected to the secondary side of the CVT. Therefore, during a phase-to-ground fault on a three-phase network, the voltage across the IVT and AVT is increased depending on how the system neutral is grounded. Based on the IEC standard, an IVT with an earth fault factor (EFF) of 1.5 should be used in systems with a solidly grounded neutral [8]. In order to prevent voltage oscillations and relay maloperation, the AVT voltage factor $(\mathrm{V_f})$ should be considered equal to or greater than EFF of the IVT. Initially, the $\mathrm{V_f}$ is considered equal to 1.5. Then, the application of higher $\mathrm{V_f}$ amounts is investigated.

To compare the transient response of the impaired CVT with that of the healthy one, the CVT is simulated based on the developed model of Subsection III-A in the PSCAD software environment.

A. AVT Ferroresonance After Line Reclosure

These days, controlled closing and reclosing are utilized for transmission-line circuit breakers (CBs) to mitigate the switching overvoltages by making the current when the voltage is close to zero [23], [24]. However, energizing a magnetic core at the voltage zero instant leads to a flux twice its rated value. Therefore, deep saturation of the AVT is expected whenever the CVT is re-energized by energizing its associated transmission line. This is the most severe AVT ferroresonance condition which is selected for study in this paper [6].

As illustrated in Fig. 5, subsequent to the outage of a transmission line due to a phase-to-ground fault at 70% of the line length at 0.4 s, a flux of about 1.21 T remains in the AVT core. Afterwards, when the CVT is reenergized at the voltage zero, depending on the polarity of the remanent flux, the AVT may be deeply saturated. This results in the occurrence of ferroresonance between the AVT magnetizing inductance and the CVD capacitors. Not only does the AVT ferroresonance influence the insulation of the CVT capacitor elements, but it also may adversely impact the performance of the distance relay, which is discussed in the following subsection.

B. Influence of AVT Ferroresonance on Distance Relay

In order to study the effect of the AVT ferroresonance on the transmission-line distance relay, a phase-to-ground fault at 70% of the line length (i.e., an in-zone fault) is investigated. Fig. 6 compares the CVT secondary voltage and the scaled primary voltage during the AVT ferroresonance caused by the transmission-line reclosure at the voltage zero point. To investigate the influence of the voltage oscillations caused by the AVT ferroresonance, a typical distance relay is modeled where the conventional full-cycle Fourier filter is utilized [25]. The estimated magnitude and phase of the CVT output voltage are oscillatory as shown in Figs. 7 and 8, respectively.

As shown in Fig. 9, if the voltage of an ideal voltage transformer is used to calculate the fault-loop impedance, the measured impedance will correctly converge to the positive impedance of the faulted section. This figure demonstrates that the measured impedance may have an uninfluential change

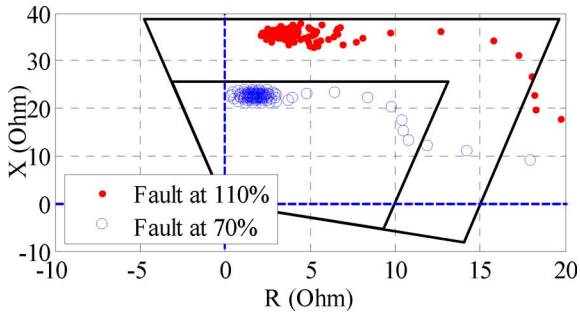

Fig. 9. Measured impedance trajectory using an ideal voltage transformer for faults at 70% and 110%.

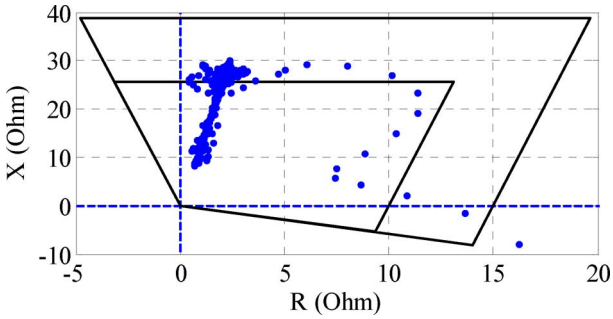

Fig. 10. Oscillations of the measured impedance trajectory caused by AVT ferroresonance after line reclosure for the fault at 70%.

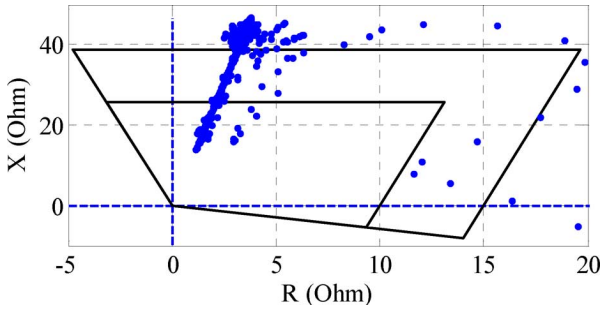

Fig. 11. Oscillations of the measured impedance trajectory caused by AVT ferroresonance after line reclosure for the fault at 110%.

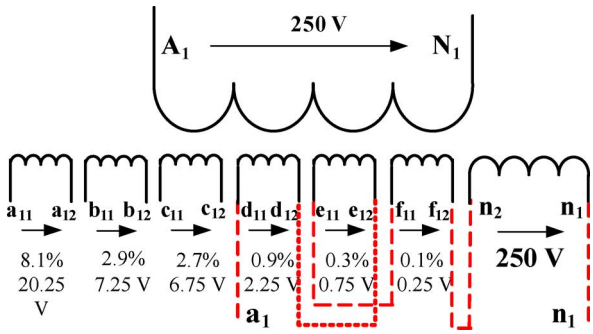

Fig. 12. Tapping arrangement of the proposed AVT.

due to the fault current decaying dc component, but the relay operates correctly.

Fig. 10 shows the impact of the oscillations caused by the AVT ferroresonance on the measured impedance trajectory. It is assumed that the estimated impedance should remain inside zone-1 for more than five samples to activate the relay. As illustrated, the impedance trajectory enters zone-1 of the distance relay for a few samples and then exits from it for a while. This may result in delayed operation of the relay for the faults inside zone-1.

The influence of the AVT ferroresonance is also investigated for a phase-to-ground fault at 110% of the transmission-line length (i.e., a zone-2 fault). The trajectories of the measured impedances are, respectively, depicted in Figs. 9 and 11, for the ideal voltage transformer and the nonideal CVT which is affected by the AVT ferroresonance oscillations. It is illustrated that as a result of the AVT ferroresonance caused by line autoreclosure for a zone-2 fault, the impedance trajectory enters the relay zone-1 which may lead to distance relay overreach.

It is demonstrated that the AVT ferroresonance may lead to underreach or overreach of the distance relay. Consequently, prevention of the AVT ferroresonance or fast damping of the corresponding oscillations is crucial due to its influence on distance relay performance. This will be explained in the next section.

V. Practical Aspects of Error Compensation by AVT

The practical aspects of the CVT increased error compensation using an AVT and the related suggestions are described in this section.

A. Appropriate Voltage Factor for the AVT

As discussed in the previous section, due to utilization of an AVT with a voltage factor of 1.5, the AVT core saturates before saturation of the PFSC inductor and the IVT core. Not only is this not considered in the design of CVT and its ferroresonance damping device, but also its effects are not compensated by the protective relay algorithms. Thus, the oscillatory overvoltages caused by AVT ferroresonance may result in CVT failure and relay maloperation. An influential technique to resolve these problems is the prevention of AVT ferroresonance by utilizing an AVT with a voltage factor higher than that of the IVT. For the studied CVT, the measured IVT voltage factor is 3.5; hence, the AVT with a voltage factor about 4 should be utilized. This is a simple and low-cost practical technique which provides very good performance. The results of complementary studies indicated that the CVT secondary voltage would be free of any oscillations or overvoltages after reclosing the transmission line, in the case of utilizing the aforementioned AVT.

B. Nominal Voltage and Taps of the AVT

The CVT-rated secondary voltage is conventionally $100/\sqrt{3}$ or $110/\sqrt{3}$ V. Thus, the appropriate AVT should have a rated voltage of about 250 V. In other words, the AVT knee-point voltage should be calculated based on the voltage factor equal to 4. Moreover, to achieve acceptable precision, it is recommended to utilize an AVT with a minimum tapping step of 0.1%. Therefore, the proposed tapping arrangement of the AVT is illustrated in Fig. 12.

As shown in Fig. 12, the tapping windings are designed to adjust the taps in the range of $\pm 15\%$ for which the increase or decrease of the output voltage depends on the utilized polarity for

the tapping windings. For instance, the applied tapping windings and their polarities for the AVT depicted in Fig. 12 result in the turn ratio of 1:1.07 between the AVT primary side, A1-N1, and the utilized secondary side a1-n1.

C. Conditions for Utilizing the AVT

Although application of an AVT to compensate the CVT increased error has many advantages, its constraints should also be considered. This method is recommended if the insulations of the IVT and the CVD are in good condition. In order to evaluate the insulation condition of the IVT and C_2 without disassembling the impaired CVT, an induced voltage test using about twice the rated voltage (i.e., 120 V) is recommended. The test is successful if no voltage collapse or insulation breakdown occurs during the test time of about 1 min. Moreover, to evaluate the insulation condition of the CVD, especially C_1 elements, the capacitance and tgδ of the CVD-rated capacitor C_R (series connection of C_1 and C_2) must be measured after disconnecting C_2 from the ground.

If one of the following conditions is satisfied, utilization of an AVT to compensate the CVT errors might not be quite successful. In these conditions, it is better to change the entire CVD elements.

- The CVT ratio error is more than about -50%, which is caused by at least nine short-circuited C_2 capacitor elements.
- The CVT error is more than $+10\%$, which is caused by at least 29 short-circuited C_1 capacitor elements.
- The measured dissipation factor is higher than 0.2%.
- The measured C_R capacitance is higher than 1.1 times the rated capacitance. This condition indicates a short circuit of a considerable number of C_1 and C_2 elements, which may accelerate the aging of capacitor elements due to the large applied voltage across other healthy elements and oil contamination.

D. AVT Tap Setting Neglecting Phase Displacement

Additional CVT output PD can be neglected when few capacitor elements of C_1 or less than three elements of C_2 are short-circuited, as shown in Fig. 13. If a healthy CVT from a different transmission line is available, it can be utilized as the reference CVT to set the taps of the AVT. As illustrated in Fig. 14, the 1n terminals of both CVTs are connected to the substation ground. The AVT tap connections must be set in order to minimize the voltage difference between the 1a terminal of the healthy CVT and the appropriate AVT tap as much as possible. This method should be applied when all burdens are connected to the reference and impaired CVTs.

E. AVT Tap Setting Considering Phase Displacement

As shown in Fig. 13, phase displacement of the studied CVT at the rated burden is more than the acceptable threshold if short-circuited C_2 elements are more than three. In such a condition, it may also be required to compensate the PD, especially when a tariff meter is connected to the CVT. The PD is heavily dependent on the burden of the impaired CVT.

Therefore, at first, all burdens of the impaired CVT should be disconnected. Subsequently, the ratio error compensation

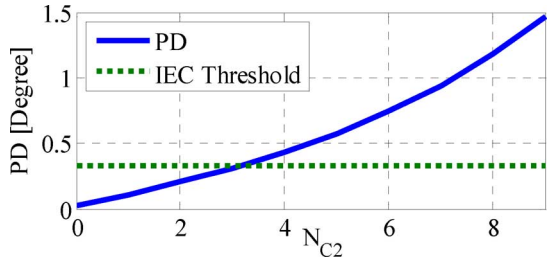

Fig. 13. Phase displacement versus the number of blown C_2 elements.

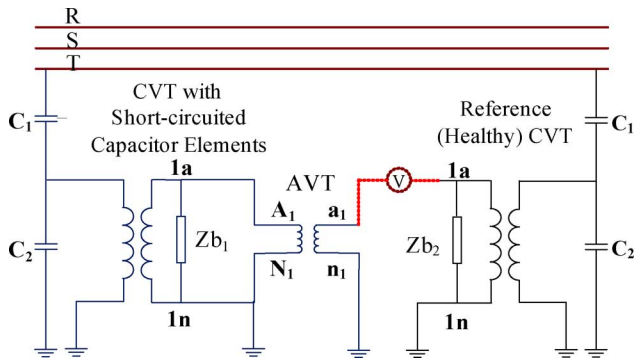

Fig. 14. AVT tap setting using a healthy CVT connected to the same phase.

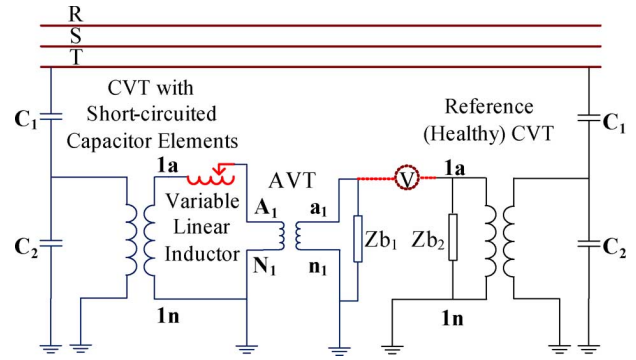

Fig. 15. Inductor tap setting using a reference CVT connected to the same phase after the AVT tap setting.

method introduced in the previous subsection should be performed to adjust the AVT tap.

To compensate the ratio error and especially PD for the operating condition when all burdens are connected to the CVT, a linear inductor with an air-gapped core and multiple taps should be utilized. This inductor is connected in series with the primary side of the AVT as shown in Fig. 15. In this condition, all burdens should be connected to the secondary side of the AVT. Afterwards, the tap of the linear inductor is set so that the voltage measured by the voltmeter is minimized.

VI. Conclusion

In this paper, two low expense and practical methods for compensating the CVT increased errors (i.e., connection of a capacitor in series with the C_2 capacitor and utilization of an AVT at the secondary side of the CVT) are suggested. Although the first method can be practically implemented *in-situ*, the dimensions of the additional capacitor and insulation considerations may limit their applications. Meanwhile, the application of an

AVT, which can be implemented temporarily or even for a long time, does not require disassembling the CVT and can be applied easily *in-situ*. It is shown that in the case of error compensation using an AVT, the transient response of the studied CVT would comply with the requirements of the IEC60044-5 standard if the number of blown capacitor elements is less than 13% of the total elements of C_1.

The simulation results demonstrated that AVT ferroresonance may occur due to utilization of an AVT with the voltage factor of 1.5. This leads to an underreach or overreach of the transmission-line distance relay and results in delayed operation or maloperation of the relay. Accordingly, an AVT with a voltage factor of about 4 should be utilized to prevent AVT ferroresonance and relay maloperation.

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