A Transformerless Active Voltage Quality Regulator With the Parasitic Boost Circuit

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Abstract—Voltage sags have always been a huge threat to sensitive industrial and commercial electrical consumers, and deep sags with long duration time are usually more intolerable. In this paper, a new topology of series-connected compensator is presented to mitigate long duration deep sags, and the compensation ability is highly improved with a unique shunt converter structure acting as a parasitic boost circuit that has been theoretically analyzed. Additionally, the proposed active voltage quality regulator is a costeffective solution for long duration sags that are lower than 50% of the nominal voltage as it is transformerless compared with the traditional dynamic voltage restorer. High operation efficiency is ensured by applying the dc-link voltage adaptive control method. Analysis, along with simulation and experimental results, is presented to verify the feasibility and effectiveness of the proposed topology.

Index Terms—Dynamic voltage restorer (DVR), dynamic sag correction, long duration deep sag, parasitic boost circuit, series-connect compensator.

I. INTRODUCTION

DOWER quality (PQ) problems have obtained increasing attentions as they can affect lots of sensitive end-users including industrial and commercial electrical consumers. Studies indicate that voltage sags, transients, and momentary interruptions constitute 92% of all the PQ problems occurring in the distribution power system [1]. In fact, voltage sags have always been a huge threat to the industry, and even 0.25 s voltage sag is long enough to interrupt a manufacture process resulting in enormous financial losses [2], [3]. Voltage sags are generally classified according to its depth and duration time. Typical sag can be a drop to between 10% and 90% of the rated RMS voltage and has the duration time of 0.5 cycles to 1 min [4]. According to the data presented in [5], majority of the sags recorded are of depth no less than 50%, but deeper sags with long duration time obviously cannot be ignored as they are more intolerable than shallow and short-duration sags to the sensitive electrical

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Source L_1 C_2 VIH L_f Sensitive load

Fig. 1. Single-phase DySC configuration.

consumers. More characteristics about voltage sags are described in [6].

Many customer power devices have been proposed to mitigate such voltage sags for sensitive loads [7]. The most studied voltage regulator topologies can generally categorized into two groups: the inverter-based regulator and direct ac-ac converters. In [8]-[11], several ac-ac converter-based regulators are introduced. Series-connected devices (SD) are voltage-sourceinverter-based regulators and an SD compensate for voltage sags by injecting a missing voltage in series with the grid [12]. There are lots of SD topologies, and key features related to the evaluation of a certain SD topology are the cost, complexity, and compensation ability. Dynamic voltage restorer (DVR) is a commonly used SD and has been widely studied. Different types of DVRs are discussed in [13]. In [14], four typical DVR system topologies are investigated and experimentally compared. The overall evaluation has shown that DVR with no storage and load-side-connected shunt converter ranks the highest as it can compensate for long-duration deep sags at a relatively low complexity and cost. Applications based on this topology are given in [15]-[20].

However, the aforementioned DVR topology is still not a costeffective solution for long duration deep sags as it regularly contains a series transformer that is heavy, bulky, and costly operating at the line frequency [16]. This drawback is obviously nonignorable especially in low-power applications. In [21] and [22], a type of transformerless SD topology known as dynamic sag corrector (DySC) is proposed, and it is a low cost, small size, light weight, and highly effective system for sag mitigation as the series transformer is no longer needed. There are several circuit structures of the DySC including two given in [21] and [22], and Fig. 1 illustrates another possible configuration. When the grid voltage differs from its desired waveform, a missing voltage



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will be injected and filtered by the DySC through its half-bridge series converter (V1, V2) and output filter (L_f, C_f) to maintain the load voltage at its rated value. During this period of time, the energy needed for the compensation is provided by the residual supply via a passive shunt converter (D1, D2, L_1) and stored in the dc-link capacitors (C_1, C_2) . So, the dc-link voltage should always be lower than the peak value of the supply voltage, and it means that the DySC can only compensate for voltage sags no deeper than 50% since the largest injection voltage of the DySC is solely determined by its dc-link voltage. As mentioned in [21] and [22], the ride-through time of the DySC in deeper voltage sags is limited by the dc-link energy storage, and it is inadequate to provide reliable protection for sensitive loads.

So, although the DySC is an excellent solution for sags in many cases, it is invalid for long-duration deep sags as its compensation ability is limited by the passive rectifier. In [23] and [24], either PWM rectifier or backup grid is adopted to increase the energy provided during voltage sags. But the compensation ability is greatly enhanced at the expense of significantly increasing the complexity and cost. In this paper, position of the shunt converter and series converter in the DySC is changed according to the structure differences between the DVR with the load-side-connected shunt converter and the DVR with the supply-side-connected shunt converter. As a result, the shunt converter together with the series converter formed a boost charging circuit and the dc-link voltage will be charged to exceed the peak value of the supply voltage. This obtained novel topology is called the transformerless active voltage quality regulator with the parasitic boost circuit (PB-AVQR), and it is capable of mitigating long duration deep voltage sags without increasing the cost, volume, and complexity compared with the traditional DySC topology. The dc-link voltage adaptive control method proposed in [25] is also applied in the PB-AVQR to improve its operation efficiency.

This paper starts with introducing the operating mode and working principles of the proposed configuration. Then, the parasitic boost circuit model is provided followed by the theoretical analysis to calculate its dc-link voltage. At last, the simulation results using MATLAB and experimental results on a 220 V-2 kW prototype are given to verify the feasibility and effectiveness of the PB-AVQR topology.

II. TOPOLOGY AND PRINCIPLE

As shown in Fig. 2, the PB-AVQR topology is mainly consists of five parts, including a static bypass switch (VT1, VT2), a half-bridge inverter (V1, V2), a shunt converter (VT3, VT4), a storage module (C_1, C_2) , and a low-pass filter (L_f, C_f) . The operating mode and applied control strategies are similar to what have been described in [25]. Under normal operating conditions, the static bypass switch is controlled to switch on and the normal grid voltage is delivered directly to the load side via this bypass switch. When an abnormal condition is detected, the static bypass switch will be switched OFF and the inverter will be controlled to inject a desired missing voltage in series with the supply voltage to ensure the power supply of sensitive loads. There are totally two different kinds of control strategies



Fig. 2. Proposed PB-AVQR topology.



Fig. 3. SPB-AVQR topology.

in the proposed PB-AVQR system. When the grid voltage is lower than the rated voltage, an in-phase control strategy will be adopted and a phase-shift control strategy will be applied when the supply voltage is higher than the nominal voltage.

Working principle of the PB-AVQR is different compared with that of the DySC due to its unique shunt converter structure. When the proposed configuration is analyzed, both the operating states of the switches (V1, V2) and the trigger angles of the thyristors (VT1, VT2) should be taken into consideration. So, a simplified PB-AVQR (SPB-AVQR) circuit shown in Fig. 3, where two thyristors (VT3, VT4) in the proposed PB-AVQR are replaced by two diodes (D1, D2), is firstly introduced to better explain its working principles. The following analysis will be based on the SPB-AVQR which can be regarded as a special type of PB-AVQR. The only difference between these two configurations is that the shunt converter of the PB-AVQR is controllable while the shunt converter of the SPB-AVQR is uncontrollable. That is to say, the dc-link voltage of the SPB-AVQR represents the upper limit of the dc-link voltage in the PB-AVQR structure. So, theoretical conclusions drawn with the SPB-AVQR are basically applicable to the PB-AVQR.

As shown in Fig. 3, switches V1 and V2 are now also parts of the parallel circuit, which means that the dc-link voltage will be affected by the on/off status of the switches. So, the turn



Fig. 4. Operating conditions during positive half-cycle. (a) V2 switched on. (b) V2 switched off.

on and turn off conditions of the compensation process should be considered to understand the working principles about the parasitic boost circuit of the SPB-AVQR. Figs. 4 and 5 illustrate four different operating conditions of the SPB-AVQR within one switching cycle during the positive and negative half-cycle of the sinusoidal supply voltage separately. Both the compensation process and charging process can be explained based on these operating conditions. In Figs. 4 and 5, the solid line means that there is current flowing through and arrows depict directions.

Operating conditions during the positive half-cycle are illustrated in Fig. 4. When V2 is switched on, as shown in Fig. 4(a), the grid charges the inductor L_1 via the diode D2 and the capacitor C_2 discharges to maintain the load voltage. When V2 is switched off, as shown in Fig. 4(b), the energy stored in the inductor during previous period is released to dc-link capacitors C_1 and C_2 through VD1 which is the antiparallel diode of V1. Operating conditions during the negative half-cycle are given in Fig. 5. When V1 is switched on, as shown in Fig. 5(a), the inductor L_1 is charged via the diode D1, and the load is compensated by the capacitor C_1 . When V1 is switched off, as shown in Fig. 5(b), the energy stored in L_1 is released through VD2, which is the antiparallel diode of V2, to capacitors C_1 and C_2 . So, in each half-cycle of the grid, one capacitor of the dc-link discharges to provide the energy needed for the compensation, and this energy is actually obtained from the supply source via the charging process described earlier.



Fig. 5. Operating conditions during negative half-cycle. (a) V1 switched on. (b) V1 switched off.

Apparently, the charging circuit of the proposed configuration works exactly like a boost circuit and the dc-link voltage in this situation is controlled by the duty ratio of the two switches. So, the compensation ability of the SPB-AVQR is theoretically unlimited as long as the grid is strong enough to provide the needed power. However, as the boost circuit is parasitic on the series inverter, and the two switches are actually controlled according to the missing voltage, there still exist some restrictions. The relationships between the dc-link voltage and other system parameters will be discussed in the next section.

In Figs. 4 and 5, two endpoints of the inverter are marked as a and b. Parts of the waveforms obtained at the inverter side and load side under four operating conditions are schematically shown in Fig. 6, where U_{aN} represents the voltage between aand N. As shown in Fig. 6, when V1/V2 is switched on/off, the dc-link voltage will be added/subtracted to the supply voltage to get a switching pulse voltage U_{aN} and the switching harmonics of U_{aN} will be filtered by L_f and C_f to get a smooth load voltage. So, the load voltage will be maintained at its rated value if the inverter is properly controlled according to the required missing voltage during sags.

III. MODELING AND THEORETICAL ANALYSIS

DC-link voltage is a key parameter to evaluate the compensation ability about a series compensation device since it decides



Fig. 6. Waveforms of supply voltage, load voltage, and U_{aN} . (a) V2 on/off. (b) V1 on/off.

the maximum value of the injected compensation voltage. In this section, in order to evaluate the compensation ability of the proposed topology and verify its feasibility in mitigating longduration deep sags, relationships between the dc-link voltage and other system parameters will be derived based on the circuit model of the aforementioned operating conditions. As can be seen from Figs. 4 and 5, working principles during the positive and negative half-cycle of the supply voltage are the same, so the following analysis will be focused on the situation in the positive half-cycle. The control strategy applied for voltage sags is in-phase compensation, so the energy needed to maintain the load voltage in one half-cycle can be expressed as follows [26]:

$$E_0 = \frac{T_0 \Delta V}{2V_{\rm ref}} P_0 \tag{1}$$

where T_0 is the grid voltage period time, V_{ref} is the rated rms value of the load voltage, P_0 is the rated load power, and ΔV is the rms value of the missing voltage. In steady-state compensation, the energy needed for the compensation should completely be provided by the residential grid which is also the charging energy through the parasitic boost circuit in this case. So the charging energy provided during $T_0/2$ referred to as E_1 equals to E_0 . E_0 can be easily obtained according to (1), but the calculation of E_1 involves with the operating conditions shown in Fig. 4. The simplified circuit model of Fig. 4 is illustrated in Fig. 7, where compensation loop including the filter and the load is ignored and only the charging circuit is considered.



Fig. 7. Simplified circuit model. (a) V2 turned on. (b) V2 turned off.

In Fig. 7, V_S is the rms value of the supply voltage. Two state equations can be obtained based on Fig. 7 and written as follows:

$$\begin{cases} L_1 \frac{dI_{\rm on}}{dt} = \sqrt{2}V_S \sin(\omega t) \\ L_1 \frac{dI_{\rm off}}{dt} = \sqrt{2}V_S \sin(\omega t) - V_{\rm dc1} - V_{\rm dc2}. \end{cases}$$
(2)

According to [27] and [28], the analysis will be significantly simplified if some realistic approximations are carried out. Then (2) can be discretized into (3) based on two following assumptions: C_1 and C_2 are well designed so that V_{dc1} and V_{dc2} can be regarded equal without considering their ripple voltages; the switching frequency is much higher than the line frequency that the supply voltage in the *n*th switching cycle can be treated as a constant value

$$\begin{cases} L_1 \Delta I_{\text{on}n} = \sqrt{2} V_S \sin(\omega n T_s) t_{\text{on}n} \\ L_1 \Delta I_{\text{off}n} = [\sqrt{2} V_S \sin(\omega n T_s) - 2 V_{\text{dc}}] t_{\text{off}n} \end{cases}$$
(3)

where $t_{\text{on}n}$ and $t_{\text{off}n}$ are, respectively, the turn-on and turn-off time of V2 in the *n*th switching cycle, T_s is the switching period, V_{dc} is the steady-state dc-link voltage, and $\Delta I_{\text{on}n}$ or $\Delta I_{\text{off}n}$ represents the variation amount in charging current during $t_{\text{on}n}$ or $t_{\text{off}n}$. As the analysis is within the positive half-cycle of the grid, there exists a constraint: $n \leq T_0/2T_s$. Apparently, $t_{\text{on}n}$ and $t_{\text{off}n}$ here are actually the inverter's duty cycle and they can be expressed as (4) when two-level symmetric regular-sampled PWM method is adopted [29]

$$\begin{cases} t_{\text{on}n} = \frac{T_s}{2} \left[1 + \frac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{\text{dc}}} \right] \\ t_{\text{off}n} = \frac{T_s}{2} \left[1 - \frac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{\text{dc}}} \right]. \end{cases}$$
(4)

The recursion formula of the charging current at the end of the *n*th switching cycle can be obtained by combining (3) and (4)

$$I_{\text{off}\,n} = I_{\text{off}\,(n-1)} + \frac{T_s}{L_1} [\sqrt{2} V_{\text{ref}} \sin(\omega n T_s) - V_{\text{dc}}] \quad (5)$$

where $I_{\text{off}n}$ represents the charging current instantaneous value at the end of the *n*th switching cycle and $\Delta I_{\text{on}n}$ can be derived at the same time

$$\Delta I_{\text{on}n} = \frac{\sqrt{2}T_s V_S \sin(\omega n T_s)}{2L_1} \left[1 + \frac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{\text{dc}}} \right].$$
(6)

The energy stored in an inductor is related to the current that flows through it, so the charging energy provided by the grid via the parasitic boost circuit in the nth switching cycle can be expressed and then rearranged as follows:

$$E_{\text{in}n} = \frac{1}{2} L_1 \Delta I_{\text{on}n}^2 + L_1 I_{\text{off}(n-1)} \Delta I_{\text{on}n}.$$
 (7)

 $I_{\text{off}(n-1)}$ in (7) can be superimposed according to the recursion formula shown in (5). Before the expression is given, there are some features about the charging current should be clarified: 1) the value of the charging current cannot be lower than zero as the current flowing through a diode is unidirectional; 2) the value of the charging current can either be zero or nonzero and its value always decreases after increasing in one half-cycle of the sinusoidal grid voltage. Then, the nonzero terms of the charging current can be derived as follows:

$$I_{\text{off}(n-1)} = \sum_{k=n_0}^{n-1} \frac{T_s}{L_1} \left[\sqrt{2} V_{\text{ref}} \sin(\omega k T_s) - V_{\text{dc}} \right]$$
(8)

where n_0 is the initial superposition instant and $I_{\text{off}n}$ is always equal to zero when n is smaller than n_0 . So, n_0 can be calculated according to (5) and expressed as follows:

$$n_0 = \operatorname{ceil}\left(\frac{T_0 \operatorname{arcsin} \frac{V_{dc}}{V_{ref}}}{2\pi T_s}\right) \tag{9}$$

where ceil(•) represents the rounded up function and the arcsine function here ranges from 0 to $\pi/2$. Furthermore, when the charging current calculated by (8) decreases to the value no more than zero, n will reach its upper limit denoted by n_e . Substituting (6), (8), and (9) into (7), the energy provided by the supply in the *n*th switching cycle can be written as follows:

$$E_{\text{in}n} = \frac{T_s^2 V_s^2 A^2}{4L_1} (1 + \sqrt{2}BA)^2 + \frac{\sqrt{2}T_s^2 V_s A}{2L_1 V_{\text{dc}}} \times (V_{\text{dc}} + \sqrt{2}\Delta VA) \sum_{k=n_0}^{n-1} (\sqrt{2}V_{\text{ref}}C - V_{\text{dc}})$$
(10)

where

$$A = \sin \omega nT$$
$$B = \frac{\Delta V}{V_{\rm dc}}$$
$$C = \sin \omega kT$$

 E_1 now can be obtained if (10) is added with *n* ranging from 1 to $T_0/2T_s$. So, the overall energy balance equation can be written as follows:

$$E_{1} = \frac{T_{s}^{2}V_{S}^{2}}{4L_{1}} \left(\sum_{n=1}^{\frac{T_{0}}{2T_{s}}} A^{2} + 2\sqrt{2}B \sum_{n=1}^{\frac{T_{0}}{2T_{s}}} A^{3} + 2B^{2} \sum_{n=1}^{\frac{T_{0}}{2T_{s}}} A^{4} \right) + \frac{T_{s}^{2}\sqrt{2}V_{S}}{2L_{1}} \sum_{n=n_{0}}^{n_{e}} \left[(A + \sqrt{2}BA^{2}) \sum_{k=n_{0}}^{n-1} (\sqrt{2}V_{\text{ref}}C - V_{\text{dc}}) \right] = \frac{T_{0}\Delta V}{2V_{\text{ref}}} P_{0} = E_{0}.$$
(11)

The charging current peak value I_{max} is considered to arise at the switching cycle after the value of (8) reaches its upper limit. So I_{max} is expressed as follows:

$$I_{\max} = \frac{\sqrt{2T_s V_S \sin(\omega n_{\max} T_s)}}{2L_1} [1 + \sqrt{2}B \sin(\omega n_{\max} T_s)] + \sum_{n=n_0}^{n_{\max}} \frac{T_s}{L_1} (\sqrt{2}V_{\text{ref}}C - V_{\text{dc}})$$
(12)

where n_{\max} is the switching cycle when $I_{\text{off}n}$ reaches its maximum value and n_{\max} can be written as follows:

$$n_{\max} = \operatorname{ceil}\left[\frac{T_0(\pi - \arcsin\frac{V_{\mathrm{dc}}}{V_{\mathrm{ref}}})}{2\pi T_s}\right].$$
 (13)

So far, the main features of the SPB-AVQR topology can be described by (11) and (12). As shown in (11), the dc-link voltage is not only related to the supply voltage, but also associated with the charging inductance, load active power, and switching frequency. However, the dc-link voltage cannot be obtained directly from (11) as n_0 and n_e cannot be computed with unknown dc-link voltage. So, an iterative algorithm is applied to estimate the dc-link voltage, where $T_s, V_S, T_0, V_{\text{ref}}, L_1$, and P_0 are all treated as constants. A flow chart of the adopted calculating method is illustrated in Fig. 8, where V_{dc0} is the initial value for V_{dc} and ΔV_{dc} is the iterative step. The algorithm is terminated if the error between E_0 and E_1 is smaller than the error tolerance ε . Moreover, the charging current can be calculated by (12) and (13) as long as V_{dc} is obtained.

Fig. 9 shows the relationships between the steady-state dclink voltage and the supply voltage with different inductance values obtained according to (11). Other system parameters are listed as follows: $P_0 = 2 \text{ kW}$, $T_s = (1/15000)\text{s}$, $T_0 = 0.02 \text{ s}$, $V_{\text{ref}} = 220 \text{ V}$. The black solid line in Fig. 9 is the $V_{\text{dc}} - V_S$ curve of the DySC topology. As can be seen in Fig. 9, the steady-state dclink voltage of the SPB-AVQR under different supply voltage is much higher than that of the DySC topology and it decreases slightly with the falling of the supply. Additionally, when the supply voltage is lower than 50% of its rated value, the dc-link voltage of the SPB-AVQR is still maintained high enough for the compensation while that of the DySC is too low to mitigating the deep sag. Fig. 9 also indicates that the dc-link voltage of the SPB-AVQR becomes higher with a lower inductance under the same circumstance. Fig. 10 gives the $I_{\text{max}} - V_S$ curve under the



Fig. 8. Flow chart for calculating V_{dc} .



Fig. 9. $V_{dc} - V_S$ curve of the SPB-AVQR with different inductances.



Fig. 10. $I_{max} - V_S$ curve of the SPB-AVQR with different inductances.



Fig. 11. $V_{dc} - V_S$ curve of the PB-AVQR with different trigger angles.

same condition. It presents that the steady-state charging current peak value increases with the decreasing of the supply voltage and it can be suppressed by increasing the charging inductance.

Although conclusions drawn from the theoretical analysis for the SPB-AVQR can also be applied to the proposed PB-AVQR topology, there still exist some differences in their dc-link voltages. When the proposed PB-AVQR is discussed, the trigger pulse angle α for VT3 and VT4 should also be taken into consideration. In the PB-AVQR circuit, the charging process begins after the VT3 or VT4 is triggered, so the initial superposition instant n_0 in (11) is now determined by α denoted by n_1 and the energy balance equation is written as follows:

$$\frac{T_s^2 V_S^2}{4L_1} \left(\sum_{n=n_1}^{n_e} A^2 + 2\sqrt{2}B \sum_{n=n_1}^{n_e} A^3 + 2B^2 \sum_{n=n_1}^{n_e} A^4 \right) \\
+ \frac{T_s^2 \sqrt{2}V_S}{2L_1} \sum_{n=n_1}^{n_e} \left[(A + \sqrt{2}BA^2) \sum_{k=n_1}^{n-1} \left(\sqrt{2}V_{\text{ref}}C - V_{\text{dc}} \right) \right] \\
= \frac{T_0 \Delta V}{2V_{\text{ref}}} P_0.$$
(14)

Here, n_e is still determined by (8) as aforementioned and n_1 can be derived as follows:

$$n_1 = \operatorname{ceil}\left(\frac{\alpha T_0}{2\pi T_s}\right). \tag{15}$$

Furthermore, the thyristors are triggered only once in each half-cycle and the current through them should be higher than the holding current to maintain the triggered state. So, α is required to meet the constraint expressed as follows:

$$\sqrt{2V_{\rm ref}}\sin\alpha > V_{\rm dc}.$$
 (16)

The charging current peak value of the PB-AVQR can still be described by (12) as long as n_0 is substituted with n_1 .

As can be seen from (14) and (15), the trigger pulse of the PB-AVQR will certainly affect its dc-link voltage and charging current. Fig. 11 shows the $V_{dc}-V_S$ curve under the influence of α according to (14). The charging inductor in Fig. 11 is set to 2 mH and other parameters remain the same as those in Fig. 9. Fig. 11 demonstrates that the steady-state dc-link voltage gets higher with a smaller trigger angle as the charging time



Fig. 12. $I_{max} - V_S$ curve of the PB-AVQR with different trigger angles.

becomes longer. It also indicates that the PB-AVQR is capable of mitigating deep sags with a proper trigger pulse. Fig. 12 presents how α affects the $I_{\rm max} - V_S$ curve under the same condition. As shown in Fig. 12, the charging current peak value can be reduced by decreasing α with the same supply voltage.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to show the validity of the proposed PB-AVQR, simulation and experimental results are presented in this section. The simulation results are based on the MATLAB software and the experimental results are based on a 2 kW single-phase prototype. The control method applied for the inverter is proposed in [30] and the control method for the thyristors is demonstrated in [25].

A. System Parameters

There are mainly four parameters need to be designed, namely the dc-link capacitor C_1/C_2 , the filter inductor L_f , the filter capacitor C_f , and the charging inductor L_1 .

During the steady-state compensation, one capacitor discharges at the switched-on position and two capacitors are both charged at the switched-off position in each switching cycle. Furthermore, C_1 and C_2 discharge, respectively, in the negative and positive half-cycle of the supply. So, if the two capacitors are treated equally during the charging process, the energy-balance equation that required for the capacitors can be written as

$$\frac{T_0 \Delta V}{4V_{\rm ref}} P_0 = \frac{1}{2} C_{1(2)} V_{\rm dc}^2 - \frac{1}{2} C_{1(2)} (V_{\rm dc} - v_{\rm dc})^2 \qquad (17)$$

where v_{dc} is the fluctuation voltage of V_{dc} . In the theoretical analysis, the dc-link voltage is assumed to be a constant, so v_{dc}/V_{dc} here is limited within 5% at the voltage drop of 50% to minimize the overall dc-link voltage ripple. In this way, the estimated minimum value of C_1/C_2 can be calculated according to (17) with V_{dc} substituted by the dc-link set value V_{dc-set} . How to set the dc-link value is introduced in [25] and in this paper it is given as

$$V_{\rm dc-set} = \begin{cases} 1.2 \times \sqrt{2}(V_{\rm ref} - V_S) + 40 & V_S < V_{\rm ref} \\ 1.5 \times \sqrt{2}(V_S^2 - V_{\rm ref}^2) + 40 & V_S > V_{\rm ref}. \end{cases}$$
(18)

TABLE I System Parameters

Description	Parameters	Real value
Nominal voltage	V_{ref}	220V
Line frequency	f_0	50Hz
Switching frequency	f_s	15kHz
DC-link capacitor	C_{1}/C_{2}	$4700 \mu F$
Filter inductor	L_{f}	1.5mH
Filter capacitor	C_{f}	$20\mu F$
Charging inductor	L_1	2mH



Fig. 13. Simulation result of the DySC.

As shown in Figs. 9–12, a higher dc-link voltage will be obtained with a smaller L_1 , but the peak value of the charging current will get larger at the same time. So, charging inductance L_1 is designed as a result of the compromise between the compensation ability and the charging current peak value.

The main function of the output LC filter in the proposed structure is to eliminate the harmonic components of the injected compensation voltage. The value of L_f and C_f are designed according to its natural frequency and several other criterions which are given as follows [31]:

$$\begin{cases} \frac{1}{2\pi\sqrt{L_f C_f}} = \chi f_s \\ L_f < \frac{v_L}{\omega_0 I_{L \max}} \\ C_f < \frac{I_{\text{ripple}}(\chi^2 + 1)}{8V_{\text{dc}} f_s} \end{cases}$$
(19)

where f_s is the switching frequency, v_L is the voltage drop across the inductor L_f at $I_{L \max}$, $I_{L \max}$ is the maximum value of the load current, I_{ripple} is the maximum ripple current of the filter and χ is the coefficient between the switching frequency and the filter's natural frequency. Generally, χ ranges from 0.05 to 0.2.

The PB-AVQR system's key parameters are listed in Table I according to the design principles mentioned earlier.

B. Simulation Results

Fig. 13 shows the simulation results of the DySC topology with different supply voltages. In the simulation, the supply



Fig. 14. Simulation result of the PB-AVQR.

voltage drops to 180 V at 0.1 s and then falls to 100 V at 0.4 s. As shown in Fig. 13, when the supply voltage is 180 V, the DySC can effectively compensate for the voltage sag; however, when the supply voltage drops to 100 V, the load voltage becomes not sinusoidal as the maximum injected compensation voltage is limited by the low steady-state dc-link voltage. Fig. 13 also indicates that the DySC can only mitigate deep sags for a few line cycles depending on the energy stored in dc-link capacitors as its steady-state dc-link voltage is always lower than the peak value of the supply voltage. The graphics of the active and reactive power are also included in Fig. 13. When the supply voltage is 180 V, the dc-link voltage does not reach its steadystate value with limited simulation time, so the active power of the supply is lower than the load power and its value is about 1.6 kW. When the dc-link voltage reaches its steady-state value with 100 V supply voltage, the active power of the supply is about 1.65 kW which means that the load voltage is no longer maintained.

The simulation results of the proposed PB-AVQR topology under the same condition is shown in Fig. 14. As can be seen in Fig. 14, when supply voltage changes, the dc-link voltage precisely tracks V_{dc-set} according to (18) and it also remains enough high for the compensation even with a 100 V supply voltage. Fig. 14 also indicates that the transient response here is not very good, but this can be improved by increasing the set value for dc-link voltage. The active power of the supply during the steady-state compensation is 2 kW, and it is the same as the load power which means that the load voltage is effectively ensured. The reactive power during the steady-state compensation is about 1.1 kvar with 180 V supply and is about 1.4 kvar with 100 V supply. The reactive power of the proposed PB-AVQR is higher than that of the DySC due to the dc-link voltage adaptive control method. Additionally, the instantaneous value of the active and reactive power can be suppressed by properly designing $V_{\rm dc-set}$ and the charging time of the capacitors. Fig. 15 shows trigger pulses for thyristors under different grid voltage. The supply voltage is 180 V in Fig. 15(a) and is 100 V in Fig. 15(b). As shown in Fig. 15, the trigger angle becomes smaller to ensure the compensation energy needed when the grid voltage decreases.



Fig. 15. Trigger signals under different supply voltage values. (a) 180 V supply voltage. (b) 100 V supply voltage.



Fig. 16. 2 kW single-phase prototype of the proposed PB-AVQR.

C. Experimental Results

The single-phase prototype is shown in Fig. 16. There are namely three experimental results presented in this section: the compensation ability comparison between the DySC and the proposed PB-AVQR; the compensation performance of the PB-AVQR; the operating efficiency comparison between the SPB-AVQR and the PB-AVQR. In the experimental waveforms, V_S , V_L , V_{dc} , and I_L , respectively, represent the supply voltage, the load voltage, the dc-link voltage and the load current.

The compensation ability of the DySC for deep voltage sag is shown in Figs. 17 and 18. Fig. 17 gives the waveforms with



 $\frac{15 \text{A/div}; \text{CH3: } \nu_{dc}, 100 \text{V/div}; \text{CH4: } I_L,}{15 \text{A/div}; \text{time: } 10 \text{ms/div}}$

Fig. 17. Waveform of the DySC with a 100 V supply voltage.



(CH1: V_s, CH2: V_L, 250V/div; CH3: V_{dc}, 200V/div; time: 2s/div)

Fig. 18. Waveform of the DySC with fluctuation supply voltage.



Fig. 19. Waveform of the PB-AVQR with a 100 V supply voltage.

a 100 V supply voltage and 2 kW pure resistive load. In this situation, the dc-link voltage stabilizes at a relatively low level limited by the grid and the load voltage becomes non-sinusoidal as the injected voltage is restricted by the dc-link voltage. The supply voltage fluctuates between 80 and 250 V in Fig. 18. Waveforms show that the dc-link voltage changes with the variation of the source voltage during the compensation and the DySC fails to mitigate voltage sags that are lower than 50% of its nominal value due to its insufficient dc-link voltage.

The compensation ability of the proposed PB-AVQR under the same circumstances is presented in Figs. 19 and 20. Fig. 19 shows the waveforms obtained when the supply voltage is 100 V



Fig. 20. Waveform of the PB-AVQR with fluctuation supply voltage.



Fig. 21. Load voltage regulation curve and THD level.



Fig. 22. Compensation behavior with nonlinear load.

and the load voltage in this situation is well maintained as the dclink voltage stabilizes at a relatively high level. Fig. 20 presents the result with a fluctuation supply voltage between 80 and 250 V, and it indicates that although the dc-link voltage of the PB-AVQR changes according to the source, it will always remain high enough to compensate for deep voltage sags that are lower than half of its rated value.

Fig. 21 shows the regulation curve and total harmonic distortion (THD) level of the load voltage as a function of the source voltage. As can be seen from Fig. 21, the load voltage is well maintained within 1% of its nominal value and the THD level is properly controlled. The compensation behavior of the PB-AVQR with nonlinear load is given in Fig. 22. As shown in Fig. 22, the source voltage is 180 V and the load voltage



Fig. 23. Compensation performance with distorted grid.



Fig. 24. Transient response of the PB-AVQR.

after compensation is 222 V with a THD level of 1.4%. Fig. 23 presents the compensation performance of the PB-AVQR with distorted grid. The source voltage in Fig. 23 is 160 V with a 17% THD level and the load voltage after compensation is 221.6 V with a THD level of 1.0%. The transient response of the proposed topology is demonstrated in Fig. 24 and the supply voltage in this situation drops from 220 to 150 V. In this experiment, the dc-link set value is properly designed to a relatively high level according to what have been mentioned in the simulation, so the system exhibits a fast response.

Furthermore, the efficiency of the proposed PB-AVQR and SPB-AVQR is also tested on the experimental platform. The efficiency curves of the two topologies are provided by a PQ analyzer named HIOKI 3197 (made in Japan) and shown in Fig. 25. Each efficiency curve is consists of ten points with the supply voltage ranging from 150 to 250 V and each point is recorded during the steady-state compensation for at least 1 min under same conditions. As illustrated in Fig. 25, although the working principles are the same between these two topologies, they differ greatly in the operating efficiency. The operating efficiency here is mainly related to the dc-link voltage and charging current, so the PB-AVQR has a higher efficiency than the SPB-AVQR as its dc-link voltage is controlled by the thyristors during the compensation. Specific analysis of the dc-link voltage adaptive control method is discussed in [25].



Fig. 25. Efficiency curve of the two topologies.

V. CONCLUSION

This paper has presented a novel transformerless active voltage quality regulator with parasitic boost circuit to mitigate long duration deep voltage sags. The proposed PB-AVQR topology is derived from the DySC circuit and the compensation performance is highly improved without increasing the cost, weight, volume, and complexity. It is a relatively cost-effective solution for deep sags with long duration time compared with the traditional DVR topology with load-side-connected shunt converter as a series transformer is no longer needed. The working principle and circuit equations are given through theoretical analysis. Simulation and experimental results are presented to verify the feasibility and effectiveness of the proposed topology in the compensation for long duration deep voltage sags that are lower than half of its rated value. The operating efficiency of the proposed PB-AVQR system also remains at a relatively high level as the dc-link voltage adaptive control method is adopted. In a conclusion, the proposed PB-AVQR topology in this paper provides a novel solution for long duration deep voltage sags with great reliability and compensation performance.

REFERENCES

- Y. H. Chen, C. Y. Lin, J. M. Chen, and P. T. Cheng, "An inrush mitigation technique of load transformers for the series voltage sag compensator," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2211–2221, Aug. 2010.
- [2] M. F. McGranaghan, D. R. Mueller, and M. J. Samotyj, "Voltage sags in industrial systems," *IEEE Trans. Ind. Appl.*, vol. 29, no. 2, pp. 397–403, Mar./Apr. 1993.
- [3] A. Bendre, D. Divan, W. Kranz, and W. Brumsickle, "Equipment failures caused by power quality disturbances," in *Proc. IEEE IAS Conf. Record*, 2004, pp. 482–489.
- [4] M. F. Alves and T. N. Ribeiro, "Voltage sag: an overview of IEC and IEEE standards and application criteria," in *Proc. IEEE Transmiss. Distrib. Conf.*, 1999, vol. 2, pp. 585–589.
- [5] S. Subramanian and M. K. Mishra, "Interphase AC–AC topology for voltage sag supporter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 514– 518, Feb. 2010.
- [6] M. H. J. Bollen, Understanding Power Quality Problems, Voltage Sags and Interruptions. Piscataway, NJ, USA: IEEE Press, 2002.
- [7] A. Sannino, M. G. Miller, and M. H. J. Bollen, "Overview of voltage sag mitigation," in *Proc. IEEE Power Eng. Soc. Winter Meet.*, 2000, vol. 4, pp. 2872–2878.
- [8] S. M. Hietpas and M. Naden, "Automatic voltage regulator using an AC voltage-voltage converter," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 33– 38, Jan./Feb. 2000.

- [9] Z. Fedyczak, R. Strzelecki, and G. Benysek, "Single-phase PWM AC/AC semiconductor transformer topologies and applications," in *Proc. 33rd Annu. IEEE Power Electron. Spec. Conf.*, Jun. 2002, pp. 1048–1053.
- [10] J. Hoyo, J. Alcala, and H. Calleja, "A high quality output AC/AC cuk converter," in *Proc. 35th Annu. IEEE Power Electron. Spec. Conf.*, 2004, pp. 2888–2893.
- [11] J. Hoyo, H. Calleja, and J. Arau, "Three-Phase PWM AC/AC cuk converter for voltage sag compensation," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, 2006, pp. 1–5.
- [12] S. W. Middlekauff and E. R. Collins, "System and customer impact: Considerations for series custom power devices," *IEEE Trans. Power Del.*, vol. 13, no. 1, pp. 278–282, Feb. 1998.
- [13] J. Praveen, P. Bishnu, M. S. Venkateshwarlu, and H. V. Makthal, "Review of dynamic voltage restorer for power quality improvement," in *Proc. 30th Annu. IEEE Ind. Electron. Soc.*, 2004, pp. 749–752.
 [14] J. G. Nielsen and F. Blaabjerg, "A detailed comparison of system topolo-
- [14] J. G. Nielsen and F. Blaabjerg, "A detailed comparison of system topologies for dynamic voltage restorers," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1272–1280, Sep./Oct. 2005.
- [15] F. A. L. Jowder, "Design and analysis of dynamic voltage restorer for deep voltage sag and harmonic compensation," in *Proc. Inst. Eng. Technol. Gen. Transm. Distrib.*, 2009, vol. 3, no. 6, pp. 547–560.
- [16] T. Jimichi, H. Fujita, and H. Akagi, "A dynamic voltage restorer equipped with a high-frequency isolated DC-DC converter," *IEEE Trans. Ind. Appl.*, vol. 47, no. 1, pp. 169–175, Jan./Feb. 2011.
- [17] T. Jimichi, H. Fujita, and H. Akagi, "Design and experimentation of a dynamic voltage restorer capable of significantly reducing an energystorage element," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 817–825, May/Jun. 2008.
- [18] A. K. Sadigh, E. Babaei, S. H. Hosseini, and M. Farasat, "Dynamic voltage restorer based on stacked multicell converter," in *Proc. IEEE Symp. Ind. Electron. Appl.*, 2009, pp. 419–424.
- [19] A. K. Sadigh, S. H. Hosseini, S. M. Barakati, and G. Gharehpetian, "Flying capacitor multicell converter based dynamic voltage restorer," in *Proc.* 41st North Amer. Power Symp., 2009, pp. 1–6.
- [20] A. K. Sadigh, A. Hosseini, S. H. Farasat, and M. Mokhtarpour, "Voltage flicker mitigation with dynamic voltage restorer," in *Proc. 1st IEEE Power Electronic Drive Syst. Technol. Conf.*, 2010, pp. 388–392.
- [21] W. E. Brumsickle, R. S. Schneider, G. A. Luckjiff, D. M. Divan, and M. F. McGranaghan, "Dynamic sag correctors: Cost-effective industrial power line conditioning," *IEEE Trans. Ind. Appl.*, vol. 37, no. 1, pp. 212– 217, Jan./Feb. 2001.
- [22] D. M. Divan, G. Luckjiff, R. Schneider, W. Brumsickle, and W. Kranz, "Dynamic voltage sag correction," U.S. Patent 6 118 676, Sep. 2000.
- [23] D. M. Vilathgamuwa and H. M. Wijekoon, "Control and analysis of a new dynamic voltage restorer circuit topology for mitigating long duration voltage sags," in *Proc. 37th IAS Annu. Meet. Ind. Appl. Conf.*, 2002, vol. 2, pp. 1105–1112.
- [24] D. Divan, A. Bendre, W. Kranz, and R. Schneider, "Dual source dynamic sag correctors-a cost effective topology for enhancing the reliability of dual source systems," in *Proc. 38th IAS Annu. Meet.*, 2003, vol. 2, pp. 940–947.
- [25] G. C. Xiao, Z. L. Hu, L. Zhang, and Z. A. Wang, "Variable Dc-bus control strategy for an active voltage quality regulator," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf.*, 2009, pp. 1558–1563.
- [26] S. S. Choi, J. D. Li, and D. M. Vilathgamuwa, "A generalized voltage compensation strategy for mitigating the impacts of voltage sags/swells," *IEEE Trans. Power Del.*, vol. 20, no. 3, pp. 2289–2297, Jul. 2005.
- [27] A. E. Aroudi, M. Orabi, L. Martínez-Salamero, and T. Ninomiya, "Investigating stability and bifurcatios of a boost PFC circuit under peak current control," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2005, vol. 3, pp. 2835–2838.
- [28] W. Zhang, G. Feng, Y. F. Liu, and W. Bin, "DSP implementation of predictive control strategy for power factor correction (PFC)," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf.*, 2004, vol. 1, pp. 67–73.
- [29] K. L. Zhou and D. W. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 186–196, Feb. 2002.
- [30] G. F. Teng, G. C. Xiao, Z. Zeng, Z. H. Ye, F. Zhuo, and Z. A. Wang, "A digital control strategy based on repetitive and multi-loop control for an active voltage quality regulator," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 2656–2662.
- [31] C. N. Ho, H. S. H. Chung, and K. T. K. Au, "Design and implementation of a fast dynamic control scheme for capacitor-supported dynamic voltage restorers," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 237–251, Jan. 2008.



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