A Novel Non-Isolated Ultra-High Voltage Gain DC-DC Converter with Low Voltage Stress

Yong Cao, Vahid Samavatian, *Student Member, IEEE,* Kaveh Kaskani, *Student Member, IEEE*, Hamidreza Eshraghi

***Abstract*— Regarding to the inherent structure of some non-polluting resources such as fuel cell stacks and photovoltaic panels, the output exhibits a low voltage which cannot be employed in the common conventional utilizations. Accordingly, an interference DC-DC converter is extremely required. This paper demonstrates the feasibility of using an ultra-high voltage gain DC-DC converter in either the fuel cell or the photovoltaic applications. While keeping high voltage gain, the proposed topology illustrates low switches' voltage stress resulted in high efficiency. The continuous and discontinuous conduction operation modes as well as efficiency analysis are investigated. The prototype setup of 250 W and 400 V output voltage is implemented. The proposed DC-DC converter merits involving ultra-high voltage ratio, low switches' voltage stress and high efficiency are verified via experimental results.**

***Index Terms*— DC-DC converter, fuel cell stack, high efficiency, high voltage gain, photovoltaic panel.**

I. Introduction

IT goes without saying that with the ever-increasing electric consuming, the usage of distributed generators (DGs) are extensively required. Perfect non-polluting resources exploitation is undoubtedly one of the most pressing concerns confronting all electrical engineers. Such resources including photovoltaic (PV), fuel cell (FC) and the other flexible distributed generators (FDGs) exhibit a low unregulated output voltage [1, 2]. Accordingly, an interference power electronic converter is required. For making the output voltage usable in power system utilization, output voltage should be adjusted at a regulated high voltage [3, 4]. It stands to reason that an ultra-high gain DC-DC converter is necessary for meeting high voltage requirements.

Generally, high voltage DC-DC converters fall into two categories including isolated and non-isolated. Quite recently, considerable attention has been paid to the isolated high step-up DC-DC converters [4-7]. The thrust of [4-7] argument is to employ transformer with the turn ratio of larger than 1 in order to increase output voltage in comparison with the conventional transformerless DC-DC power converters. However, these isolated DC-DC converters have been confronted high switch stress issues leading to poor efficiency. To tackle this problem, either active or passive clamp has been employed [8, 9]. Although, from switch voltage stress point of view, this technique can improve the performance of isolated DC-DC converters, the final cost and control complexity always are the firm barriers for employing this technique. Not giving exhaustive account of isolated converters, the main goal of this paper is to propose non-isolated DC-DC converter.

Recent research indicates that a significant non-isolated converters have been employed for meeting the requirement of high voltage gain applications such as electric vehicles (EVs), FCs and PVs [10-14]. The literature on high voltage gain DC-DC converter demonstrates a variety of approaches. For examples, [10-13] have been proposed conventional cascaded boost converter, single-switch quadratic boost converter, quadratic three-level boost converter, quadratic three-level boost converter using a capacitor-inductor-diode cell, respectively. In these converters, since large number of active switches, capacitors, inductors and diodes are required, the control circuit has become much more complicated [14] while the efficiency has been also diminished [15].

Coupled inductor based high step-up converter is proposed in [16, 17] which are combining by Dickson multiplier cell and capacitor-diode stage respectively. Although robustness has been evident in these proposed converters, output diode and switches voltage stresses are extremely high leading to lower efficiency. Moreover, pulsating input current also leads to electromagnetic interference (EMI) problems. This can affect the control circuit. In [17], the number of active switches is also high leading to control complexity.

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As reported by Bist et al. [18], for making high voltage ratio, a newly proposed isolated Cuk derived DC-DC converter is launched. Although this converter provides a higher voltage ratio in comparison with conventional converters, the switch voltage stress is considerably high leading to lower efficiency and higher cost.

A switched-capacitor boost converter is proposed in [19]. Switch voltage stress is diminished leading to high efficiency. However, since in high power application the input inductor becomes larger the dynamic of converter becomes slow which is not suitable in high performance application. For tackling this problem, another modified switched capacitor DC-DC converter is launched in [20]. However, drawbacks including complex controlling circuit and considerable number of components make this converter not to be potential option for low voltage resources.

Pan et al. in [21] and Tseng et al. in [22] propose a quadrupler and coupled-inductor interleaved boost converter respectively. In [21], switch voltage stress becomes 25% of output voltage. Not using an extra transformer, the current sharing is done properly. However, the number of containing component is extremely high leading to complex designing procedure. In [22], not only is the switch voltage stress mostly high, but also the number of components is high. As reported by [23], an interleaved step-up converter based on diode–capacitor multiplier cells (DCMCs) is presented. This proposed converter has far lower number of active and non-active components. The more cells added the lower switch voltage stress. Of course this cascade connection DCMCs causes to efficiency become lower particularly in high power applications owing to considerable amount of multiplier diodes conduction losses.

In addition to aforementioned interleaved-based high step-up DC-DC converters, [24] proposes an interleaved boost converter employing two coupled inductors to accomplish ultra-high voltage gain. Although, this proposed converter exhibits high performance in high power applications, its control circuit is complicated because of its duty cycle's constraints and a necessary soft-start circuit providing initial charge of output capacitors. Proposed converter in [25] mitigates the constraint of duty cycles at the expense of employing higher number of components leading to lower efficiency and higher initial cost.

In recent papers by [26-29], high voltage gain DC-DC converters have been proposed based on voltage multiplier cells and the three-state switching cells. Higher efficiency, thanks to the soft switching scheme, over a wide load variation is the most important merits of propositioned converter. In addition, the duty cycle constraints is totally mitigated. But, a key limitation of these proposed converters is that the number of component, having low switch voltage stress, is considerable leading to higher cost.

Multi-cell switched-inductor/switched-capacitor combined and a new generalized ultra-gain DC-DC converter have been proposed in [30] and [31, 32] respectively. Although in these circuits coupled inductors do not employed, for making high voltage ratio the number of semiconductor devices is extremely high. This leads to complex controlling and expensive converters.

Floating output DC-DC converter are described in [33-35]. In [33], conventional boost is employed. Although the structure seems to be modular, some detriments including pulsating input current, high starting current, large number of required diodes and capacitors are evident. In [34, 35], interleaved topologies and cross connection of inductors are used. In these topologies, above-mentioned drawbacks are mitigated at the expense of losing ultra-high voltage ratio capability.

However, studies on non-isolated step-up DC-DC converters are still lacking low switch voltage stress, high efficiency and ultra-high voltage gain all together. Accordingly, this paper proposes a novel topology of DC-DC converter having benefited by low switch voltage stress, high efficiency and ultra-high voltage gain. This topology is based on switch capacitor along with voltage-doubler circuit leading to ultra-high voltage gain. Thanks to its structure, this topology can operate either in isolated or non-isolated scheme. However, the main purpose of proposing this topology is not the operation scheme. The proposed topology can readily cater the key features including ultra-high voltage gain and low switch voltage stress which is suitable for low voltage resources including FCs and PVs. Accordingly, the proposed converter can be a potential candidate for low voltage distributed generations.

The remainder of the paper is organized as follows. Section II belongs to introducing the structure and the principles of operations. While the steady state analysis in both DCM and CCM is thoroughly analyzed in section III and VI, respectively, section V is allotted to the design equation. Section VI covers efficiency analysis. Experimental results including efficiency and key waveforms are illustrated in section VII. Finally, a brief conclusion is drawn in section VIII.

II. Operation Principles

Structure of proposed DC-DC converter is depicted in Fig. 1. Regarding this figure, one can observe that two main switches (Power MOSFETs) are employed in cross connection between two input coupled inductors. In addition, three power diodes with three capacitors are used for switched capacitor circuit. Besides, including two power diodes with two capacitors, a voltage-doubler circuit is also employed for making converter work in ultra-high voltage gain manner.

The voltage-doubler circuit is triggered with two transformers with turn ratio of n ($= N_2/N_1$) connecting in series. The input of these two transformers are required to be periodically exited for avoiding core saturation occurrence. Accordingly, main switches should be located such shown in Fig. 1.

Switched capacitor circuit, consisting three capacitors and three diodes, is in charge of providing some of output voltage derived on conventional switched capacitor circuits [36]. Regarding input transformers this circuit is properly employed for achieving this goal.

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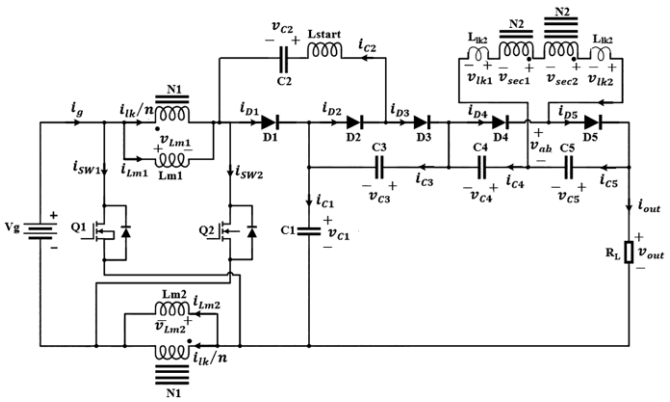

Fig. 1. Topology of proposed ultra-high voltage gain DC-DC converter

The main cause of cross connection of main switches is to charge magnetizing inductors in the parallel mode and then to discharge them in series for accomplishing ultra-high voltage gain.

For mitigating the starting problem, although, there exist few approaches, a small inductor is used connecting in series with C_2. Fig. 2 illustrates the key waveforms of proposed converter dividing the whole operation into 4 operation modes. These operation modes are discussed as following.

Interval 1 [t_0-t_1]: At the beginning of this time interval the gate activation signals are applied. Capacitors 1 and 3 discharge to the load while capacitor 2 is being charged from both input voltage and capacitor 1 through diode 2. In this time interval, voltage of coupled inductors are reached to the input voltage leading to charge magnetizing inductors. $V_{sec1,2}$ are corresponded to magnetizing inductor voltages and follow them without any delay. Due to the presence of transformer leakage inductors, V_{ab} is increasing to its nominal voltage with slight ramping delay. At the end of this time interval the voltage doubler circuit may triggered. It is easily seen that in this time interval V_{C4} is been changing its operation mode from charging to discharging.

Interval 2 [t_1-t_2]: In this time interval, capacitors 1 and 3 are continued to discharge to the load while capacitor 2 is being charged from both input voltage and capacitor 1 through diode 2. In this time interval, V_{ab} is increased to its nominal voltage (nV_g). The voltage doubler circuit start to charge C_5 while the demanded output energy is supplied by capacitor 4.

Interval 3 [t_2-t_3]: At the beginning of this time interval the gate activation signals are removed. Capacitor 2 discharges to the load while capacitors 1 and 3 are being charged. In this time interval, voltage of coupled inductors are reached to the negative value leading to discharge magnetizing inductors. $V_{sec1,2}$ are corresponded to magnetizing inductor voltages and follow them without any delay. Due to the presence of transformer leakage inductors, V_{ab} is decreasing to its nominal voltage with slight ramping delay. At the end of this time interval the voltage doubler circuit may triggered reversely done in mode 1. It is easily seen that in this time interval V_{C5} is been changing its operation mode from charging to discharging.

Interval 4 [t_3-t_4]: In this time interval, capacitor 2 is continued to discharge to the load while capacitors 1 and 3 are being charged. In this time interval, V_{ab} is decreased to its nominal voltage. The voltage doubler circuit start to charge C_4 while the demanded output energy is supplied by capacitor 5.

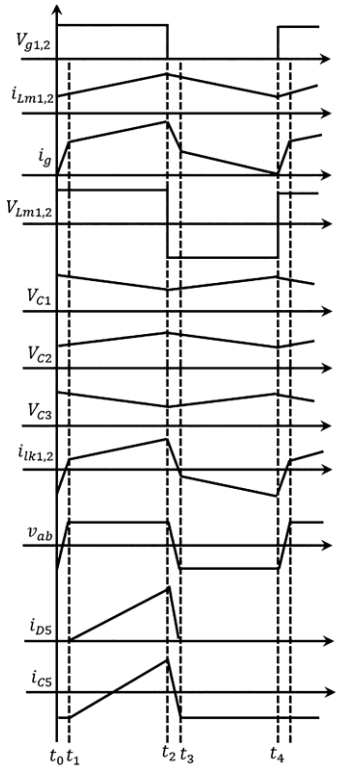

Fig. 2. Key waveforms of proposed DC-DC converter

III. Continuous Conduction Mode Operation

For analyzing the continuous conduction mode (CCM), one can suppose that there exist only two operation states without loss of precision: State I and State II including time interval [t_0-t_2] and [t_2,t_4], respectively. The switched capacitor part is independent of leakage inductance in the output of transformers based on our proposed model. Moreover, with the assumption that the capacitors of the voltage doubler circuit are large enough to supply the output voltage during intervals 1 and 3, considering only two operation modes is applicable.

A. State I

In this state, both main switches are turning on ignoring their turning-on delays. In this situation the both diodes 1 and 3 are turned off and only diode 2 is in forward bias making the capacitor 2 being charged while C_1 and C_3 are discharging. Magnetizing inductor voltage are

$$V_{Lm1} = V_{Lm2} = V_g \quad (1)$$

Capacitors' voltages are also obtained as following.

$$V_g + V_{C1} = V_{C2} \quad (2)$$

The input voltage of voltage doubler circuit V_{ab} is equals to (ignoring leakage inductance)

$$V_{ab} = 2nV_g \quad (3)$$

B. State II

In this state, both main switches are turning off while both

diodes 1 and 3 are turned on and only diode 2 is in reverse bias making the capacitor 1 and 3 being charged while C_2 is discharging. Magnetizing inductor voltage are

$$V_{Lm1} = V_{Lm2} = \frac{V_g - V_{C1}}{2} \quad (4)$$

Capacitors' voltages are also obtained as following.

$$V_{C3} = V_{C2} \quad (5)$$

$$V_{C1} = V_{C2} - V_g \quad (6)$$

The input voltage of voltage doubler circuit V_{ab} is equals to (ignoring leakage inductance)

$$V_{ab} = 2n\frac{V_g - V_{C1}}{2} \quad (7)$$

Regarding above-mentioned equations, one can find the output voltage ratio through following procedure.

Using equations (2), (5) and (6) and with regard to constant-capacitor-voltage, one can find the capacitors' voltage:

$$V_{C1} = \frac{V_{out1} - V_g}{2} \quad (8)$$

$$V_{C2} = V_{C3} = \frac{V_{out1} + V_g}{2} \quad (9)$$

Where

$$V_{out1} = V_{C1} + V_{C3} \quad (10)$$

Therefore, in the state II the magnetizing inductors' voltages are rewritten as following.

$$V_{Lm1} = V_{Lm2} = \frac{3}{4}V_g - \frac{1}{4}V_{out1} \quad (11)$$

Accordingly,

$$V_{ab} = 2n\left[\frac{3}{4}V_g - \frac{1}{4}V_{out1}\right] \quad (12)$$

Employing voltage-second balance principle [37] applied to both magnetizing inductors, one can find that

$$DV_g + (1-D)\left(\frac{3}{4}V_g - \frac{1}{4}V_{out1}\right) = 0 \quad (13)$$

Where D denotes the duty ratio of activation signals. Therefore, the voltage ratio of switch capacitor circuit may be calculated as follows.

$$\acute{G} = \frac{V_{out1}}{V_g} = \frac{3+D}{1-D} \quad (14)$$

Flashing back to the equation (12), by using equation (14) we have

$$V_{ab} = 2nV_g\left[\frac{3}{4} - \frac{1}{4}\frac{3+D}{1-D}\right] = 2nV_g\frac{D}{D-1} \quad (15)$$

Bu using equations (3) and (15), one can find capacitors' voltages of the voltage doubler circuit as follows.

$$V_{C4} = 2nV_g\frac{D}{1-D} \quad (16)$$

$$V_{C5} = 2nV_g \quad (17)$$

Accordingly

$$V_{out} = V_{out1} + V_{C4} + V_{C4} = V_g\left\{\frac{3+D}{1-D} + 2n\left[1 + \frac{D}{1-D}\right]\right\} \quad (18)$$

By simplifying, total voltage ratio can be obtained as

$$G = \frac{V_{out}}{V_g} = \frac{3+D+2n}{1-D} \quad (19)$$

Regarding the above-mentioned equation, one can easily find that the voltage ratio depends on two separated quantities. Making this equation much more clear, Fig. 3 illustrates the voltage ratio variations during the variations of both transformer turn ratio and switches' duty cycle. In this figure, an increase in the transformer turn ratio leads to the significant increase in voltage ratio. Accordingly, based on the required voltage gain, the transformer turn ratio can be employed as a constant quantity and applied as a design parameters.

For adjusting the output voltage under different load and input voltage conditions, duty cycle is a convenient choice and one can easily tune the output voltage through varying the duty cycle via a simple conventional controlling system. Fig. 4 depicts the variation of voltage ratio in terms of duty cycle variation under different transformer turn ratio. Regarding this figure, it is clear that output voltage adjustment can be achieved by tuning duty cycle.

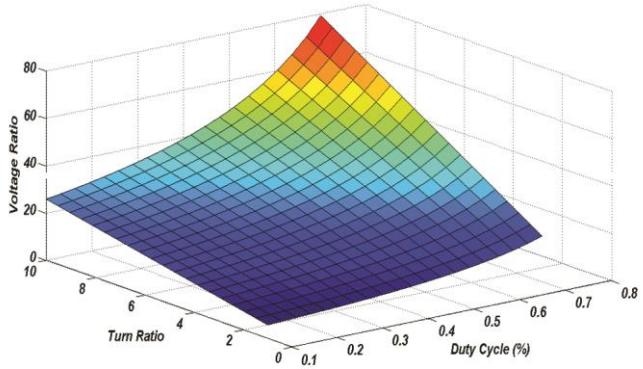

Fig. 3. 3-D voltage ratio in terms of transformer turn ratio and duty cycle

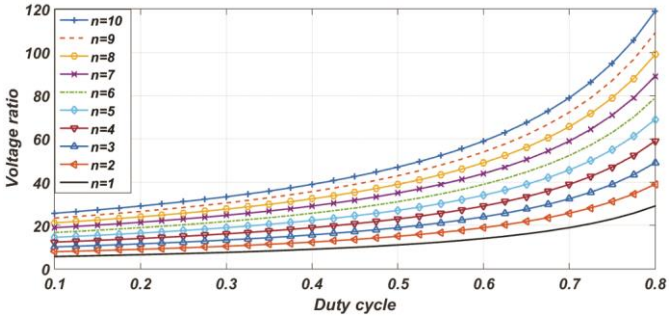

Fig. 4. Voltage ratio in terms of transformer turn ratio and duty cycle

Non-idealities always have inconsiderable effects on the converter voltage ratio. However, it is worth investigating these effects especially on voltage ratio. Since the voltage doubler circuit has high output voltage (regarding transformer turn ratio), accordingly, its diodes' forward voltage and on-resistance can be neglected without losing any accuracy. Suppose that transformers have the winding resistance of R_t, switched-capacitor-diodes forward voltage of V_d, diodes resistance of R_d and MOSFETs on-resistance of R_{ds}, therefore

$$G = \frac{\frac{3+D}{1-D} - 3\frac{V_d}{V_g}}{1 + \frac{2R_{ds}}{R_o}\frac{(1+D)^2}{D(1-D)^2} + \frac{2R_d}{R_o}\frac{(1+D)}{D(1-D)} + \frac{2R_L}{R_o}\frac{8}{1-D^2} + \frac{2n}{1-D}} \quad (20)$$

Where R_o is the output resistor associated to the connected load. It is noted that the procedure of calculation of this equation is beyond of our study and only the final result is expressed. Regarding this voltage ratio, one can find that in

the specific input voltage range and also with employing SCHOTTKY diodes, voltage gain is almost equal in both ideal and non-ideal circuit components.

For demonstrating the merits of proposed converter, it is helpful to compare our proposed converter with other recent papers dealing with high step-up DC-DC converter in many aspects. Accordingly, seven different DC-DC converters including conventional boost converter along with DC-DC converters proposed in [16], [17], [18], [22], [30] and [31].

Having a brief comparison among these converters' topology, the number of active switches and diodes are listed in Table. 1. A quantitative comparison is highly required for investigating on the merits of proposed converter. As a voltage ratio point of view, accordingly, the voltage ratio can be compared listed in Table. 1. With regard to this table, it is clear that voltage ratio of proposed converter is higher than mostly the others. As a voltage stress of power switches point of view, one can easily judge the privilege of proposed converter to the other mentioned converters. The power switches' voltage stress in these power converters can be estimated by the expressions listed in Table. 1.

TABLE I
TOPOLOGIES COMPARISON

Topology	Active Switches	Diodes	Voltage Ratio	Normalized Voltage stress (VS/V_g)
Proposed	2	5	$\frac{3+D+2n}{1-D}$	$\frac{1+G}{4+2n}$
Proposed in [16]	1	4	$\frac{3+nD}{1-D}$	$\frac{n+G}{n+3}$
Proposed in [17]	4	4	$\frac{4n+1}{1-D}$	$\frac{G}{4n+1}$
Proposed in [18]	2	2	$\frac{nD}{1-D}$	$\frac{G}{n}$
Proposed in [22]	2	6	$\frac{2n+2}{1-D}$	$\frac{G}{2n+2}$
Proposed in [30]	2	9	$\frac{3+5D}{1-D}$	$\frac{1+G}{4}$
Proposed in [31]	1	7	$\frac{5+D}{1-D}$	$\frac{1+G}{2}$
Conventional boost	1	1	$\frac{1}{1-D}$	G

Making the comparison much more clear, Fig. 5 demonstrates the voltage ratio of the aforementioned high step-up DC-DC converters in terms of main switch duty cycle. In this case, the turn ratio of couple inductor in all converters is considered 2. It can be easily observed that there is a yawning gap among the other topologies' voltage ratio and our proposed converter and the converter in [17] making them potential candidate for high step-up DC-DC converter. It should be mentioned that the proposed converter only has two main switches while the one in [17] has four switches. Therefore, as an economic and control simplicity point of view, the proposed converter is thoroughly reasonable.

Clearly comparing, Fig. 6 demonstrates the normalized voltage stress of power switches in these different DC-DC converters. This figure obviously shows that the proposed converter along with converter in [17] have the merits of lower voltage stress under different voltage ratios, particularly in high voltage ratios. However, the one in [17] has used 2 more clamp switches while our proposed converter has not. It can be found that by increasing transformer turn ratios, switches' voltage stresses become lower. Therefore, this specification directly results in higher efficiency being one of the paper claims.

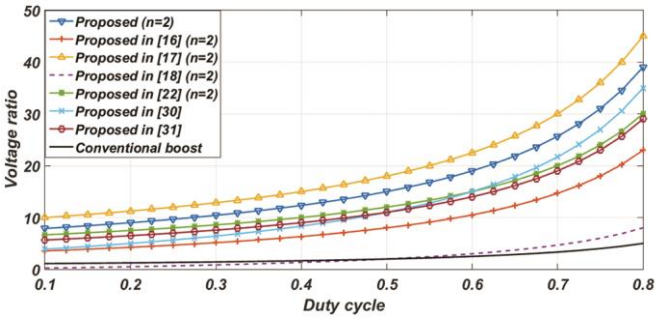

Fig. 5. Voltage ratio in terms of duty cycle

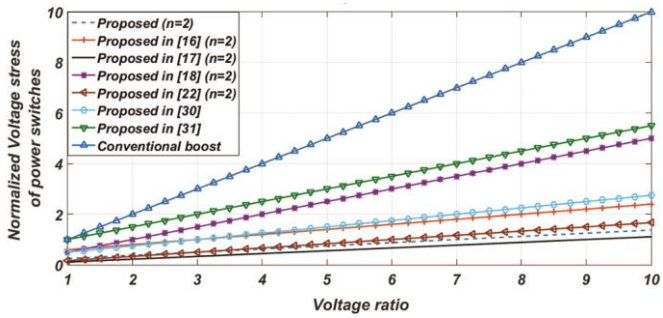

Fig. 6. Normalized voltage stress of power switches versus voltage ratio

It is clear that diodes voltage stresses are also important for evaluating an ultra-high voltage gain DC-DC converter performance. The expression described these voltage stresses are derived in (21)-(23). Regarding these equation, one can easily found that the voltage stresses during off states in all circuit diodes are low. Accordingly, the cost can be diminished and efficiency can be enhanced.

$$VS_{D1,2,3} = \frac{2}{1-D} V_g \tag{21}$$

$$VS_{D4} = 2nV_g \tag{22}$$

$$VS_{D5} = 2nV_g \frac{D}{1-D} \tag{23}$$

IV. DISCONTINUOUS CONDUCTION MODE OPERATION

Practically, light loads may occur and make the DC-DC converter work in discontinuous conduction mode (DCM). Therefore, in this section the behavior of the proposed converter in DCM will be discussed. The boundary load which cause DCM may specify regarding the circuit parameter. In DCM, magnetizing currents become discontinuous and make a new operation mode.

Fig. 7 shows these current. Time intervals DT_s and D_2T_s are exactly the state I and state II expressed in previous section, respectively. In DCM, there additionally exists another time interval, namely D_3T_s, which in all the semiconductor devices turn off and output power is only provided via C_1, C_3, C_4, C_5 capacitors.

DCM operation analysis should be started by investigating on Fig. 7. Magnetizing current peak can be calculated both in

DT_s and D_2T_s time intervals as follows:

$$i_{L\_P} = \frac{V_g}{L_m} DT_s \tag{24}$$

$$i_{L\_P} = \frac{V_{out1} - 3V_g}{L_m} D_2T_s \tag{25}$$

Regarding above equations, one can easily find that

$$D_2 = \frac{4\,V_g\,D}{V_{out1} - 3V_g} DT_s \tag{26}$$

Employing (16) and (17)

$$V_{out1} = \frac{2}{2+n} V_{out} - \frac{n}{2+n} V_g \tag{27}$$

Accordingly, (23) becomes

$$D_2 = \frac{2(2+n)\,V_g\,D}{V_{out} - (2n+3)V_g} DT_s \tag{28}$$

With regard to charge balance in capacitors, one can consider that average magnetizing current equals to average output current over one switching period. Therefore

$$\frac{V_{out}}{R_o} = \frac{V_g}{L_m} DT_s \frac{(D + D_2)}{2} \tag{29}$$

Where R_o is the equivalent load resistor. Employing (28) and defining $\tau = L_m f_s/R_o$ (f_s is switching frequency), following expression specify the voltage ratio in DCM:

$$G_{DCM} = \frac{V_{out}}{V_g} = \frac{(2n+3)\tau + \left(\frac{D^2}{2}\right) + \sqrt{\left\{(2n+3)\tau + \left(\frac{D^2}{2}\right)\right\}^2 + 2\tau D^2}}{2\tau} \tag{30}$$

If $(2n+3)\tau \gg \left(\frac{D^2}{2}\right)$, which occurs in small duty cycles, G_{DCM} reduces to the following expression:

$$G_{DCM} = \frac{V_{out}}{V_g} = \frac{(2n+3) + \sqrt{\{(2n+3)\}^2 + 2\frac{D^2}{\tau}}}{2} \tag{31}$$

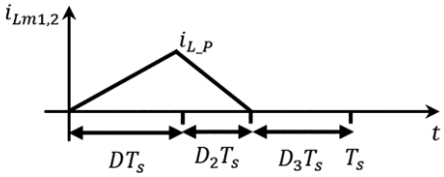

Fig.7. DCM operation of magnetizing currents

The boundary between DCM and CCM operation mode occurs when the half of magnetizing current variation ($\Delta I/2$) equals to the average current flowing to magnetizing inductor. Accordingly,

$$\frac{V_{out}}{R_o} = \frac{\Delta I}{2} = \frac{V_g}{2L_m} DT_s \tag{32}$$

Therefore

$$R_{crit} = R_o = \frac{V_{out}\,2L_m\,f_s}{DV_g} \tag{33}$$

With using (19), above equation becomes as follow:

$$R_{crit}(D,n) = \frac{(3+D+2n)\,2L_m\,f_s}{D(1-D)} \tag{34}$$

This equation shows that for $R_o > R_{crit}(D,n)$ DCM and for $R_o < R_{crit}(D,n)$ CCM operation will be occurred. Fig. 8 illustrates $R_{crit}(D,n)$ versus duty cycles (D) and turn ratio (n). f_s and L_m is selected 50 kHz and 520µH respectively according to Table. 3 in section VII. It can be easily observed that with the increase of turn ratio the boundary of DCM operation is exceeded. Therefore, the proposed converter can work in CCM within wider range of output power. With assumption of n=2, minimum critical load occurs approximately in $D = 0.483$ with $R_{crit} = 1557.6\,\Omega$.

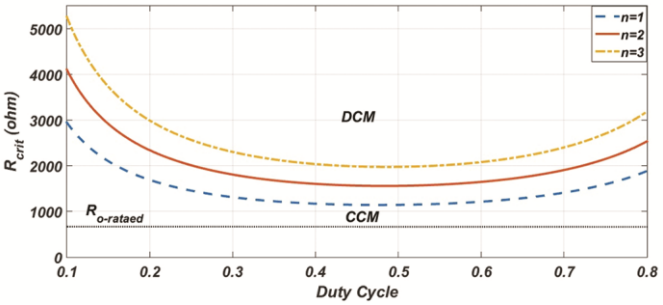

Fig.8. DCM operation of magnetizing currents

V. DESIGN EQUATIONS

One of the most pressing concern in the DC-DC converters is undoubtedly the design consideration of the converter components based on the constraints and requirements of applications and standards. The necessity of limited current ripple determines the value of transformer magnetizing inductors. When the switches is in conduction mode

$$L_{m1}\frac{di_{Lm1}}{dt} = L_{m2}\frac{di_{Lm2}}{dt} = V_g \tag{35}$$

If ΔI is the desired current ripple, then the following equation is valid for selecting transformer magnetizing inductors.

$$L_{m1} = L_{m2} = \frac{D(1-D)}{(3+D)\Delta I\,f_s} V_{out} \tag{36}$$

Where f_s is the converter switching frequency. In addition, for selecting the capacitors values of switched-capacitor circuit, charge balance theory is employed. When C_1, C_2 and C_3 are charging, the their electric charges can be expressed as following.

$$\Delta Q_1 = C_1\Delta V_{C1} = I_{out}(1 + \frac{1}{D})T_{on} \tag{37}$$

$$\Delta Q_2 = C_2\Delta V_{C2} = I_{out}(\frac{1}{D})T_{on} \tag{38}$$

$$\Delta Q_3 = C_3\Delta V_{C3} = I_{out}T_{on} \tag{39}$$

Where I_{out} and T_{on} are output current and switches' conduction time, respectively. ΔV_{Cx} is also desired capacitor voltage ripple.

By simplification, one can find following straightforward expression for capacitors determinations.

$$C_1 = \frac{P_{out}(1+D)}{\Delta V_{C1} f_s V_{out}} \tag{40}$$

$$C_2 = \frac{P_{out}}{\Delta V_{C2} f_s V_{out}} \tag{41}$$

$$C_3 = \frac{P_{out}D}{\Delta V_{C3} f_s V_{out}} \tag{42}$$

Where P_{out} is the load power. Using the same procedure, for the voltage doubler circuit, the following expressions can also be derived.

$$C_4 = \frac{P_{out}D}{\Delta V_{C4} f_s V_{out}} \tag{43}$$

$$C_5 = \frac{P_{out}(1-D)}{\Delta V_{C5} f_s V_{out}} \tag{44}$$

VI. Efficiency Analysis

It goes without saying that efficiency analysis has paramount of importance in power converter performance evaluation especially in high voltage gain converter. Therefore, in this section theoretical analysis of efficiency of the proposed DC-DC converter would be investigated. To calculate the overall efficiency of the converter, all the components power losses should be considered. Power switches, diodes and the equivalent series resistor (ESR) of the coupled inductors are the main sources of power losses in the proposed converter. Accordingly, considering individually the power loss of each device and accumulate them all together would lead us to efficiency evaluation. In the power switches point of view, power loss fall to two main categories, namely, conduction and switching power losses. Therefore

$$P_{Loss,Cond_Q} = \sum_{i=1}^{2} R_{on,i}\left(I_{\mathrm{Q,i},rms}{}^2\right) \tag{45}$$

$$P_{Loss,Sw_Q} = \sum_{i=1}^{2}\left\{P_{on,Sw_\mathrm{Q}} + P_{off,Sw_\mathrm{Q}}\right\} = \frac{f_{sw}}{2}\sum_{i=1}^{2}\left\{V_{\mathrm{Q,i}} I_{\mathrm{Qi}}\left(t_{ri} + t_{fi}\right)\right\} \tag{46}$$

Where i is the main switch no. $P_{Loss,Cond_Q}$ and P_{Loss,Sw_Q} are conduction and switching power loss of main switches, respectively. f_{sw} is switching frequency and t_{ri} and t_{fi} are rising time and falling time of associated switches, respectively. For calculating the diodes and inductor power losses, following equation would be employed.

$$P_{Loss,\mathrm{diode}} = \sum_{j=1}^{5}\left\{V_{D,j}\left(I_{\mathrm{D,j},ave}\right) + r_{D,j}\left(I_{\mathrm{D,j},rms}\right)\right\} \tag{47}$$

$$P_{Loss,inductor} = \sum_{k=1}^{2}\left(I_{\mathrm{L,k},rms}{}^2\right) R_{L,k} \tag{48}$$

Where j and k are the diodes and coupling inductor no, respectively. $P_{Loss,\mathrm{diode}}$ and $P_{Loss,inductor}$ are diode and inductor ESR power losses, respectively. V_D is forward voltage of the diodes and R_D is resistance of the diodes in their conducting operation. R_L is also the winding equivalent resistance of coupling inductors. Accordingly, total power loss can be evaluated as following:

$$P_{Loss} = P_{Loss,Cond_Q} + P_{Loss,Sw_Q} + P_{Loss,\mathrm{diode}} + P_{Loss,inductor} \tag{49}$$

Assuming that the both main switches and coupling inductors are equal, the effective value of each component current can be calculated as follows:

$$\begin{cases} I_{L1,2,rms} = \sqrt{I_L{}^2 + \Delta i^2{}_{\mathrm{Lp-p}}/12} \\ I_{Q_1,rms} = I_{Q_2,rms} = \sqrt{D}\sqrt{I_L{}^2 + \Delta i^2{}_{\mathrm{Lp-p}}/12} \\ I_{D_\mathrm{j},rms} = I_{Dj}\sqrt{D/3} \\ I_{D_\mathrm{j},ave} = 0.5\, D\, I_{Dj} \end{cases} \tag{50}$$

A voltage and current ripple are considered as given in the next section. The parameter values are listed in Table. 2. Therefore, the efficiency for different input voltages and output power (at a fixed output voltage here is 36 V) can be readily evaluated.

TABLE II
PARAMETERS' VALUES OF ESR, SWITCHES AND DIODES

Parameter	Value	Parameter	Value
R_{on}	0.0037 Ω	f_s	50 KHz
$R_{on}(max)$	0.0045 Ω	t_r	67 ns
R_L	0.05 Ω	t_f	88 ns
R_d	2.2 Ω	V_D	0.6 V

Fig. 9 has shown the above-mentioned calculations graphically. Regarding this figure, it is clear that the minimum efficiency is occurred in the full load operation while its maximum is occurred in the light loads. Obviously, with the increase of load conduction and switching power losses of active devices would increase leading to efficiency decreasing.

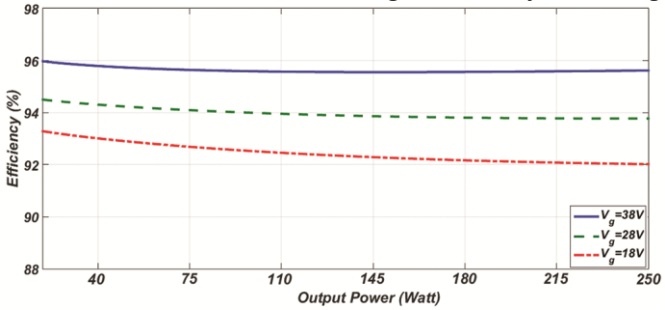

Fig. 9. Energy conversion efficiency for Vo = 400 V as a function of the output power for different input voltage levels.

VII. Experimental Result

The proposed ultra-high step-up converter is employed for adjusting the input voltage around a desired output voltage by means of tuning duty cycle. As it mentioned earlier, this converter has the merits of high voltage ratio and relatively high efficiency owing to low voltage stress. Following specifications are considered in implementing of this converter.

Input Voltage	$V_g = 18\sim38\ V$	Output Power	$P_{out} = 250\ W$
Output Voltage	$V_{out} = 400\ V$	Current Ripple	$\Delta I = 1\ A$
Switching Frequency	$f_s = 50\ KHz$	Voltage Ripple	$\Delta V = 5\ V$

The switching frequency is selected with the trade of between EMI problems and the size of passive components. In this paper the transformer turn ratio is considered 2 (one can use another turn ratio with regard to the desired application). Accordingly, regarding input voltage range, the switches' duty cycle are limited in $0.306 \le D \le 0.655$. It should be noted that the passive components and the active ones can be easily evaluated and the final results are listed in Table. 3.

Employing above-mentioned components, this converter is implemented for a 250 W and 400 V application. The input voltage has been varying between 18 to 38 V. For controlling system, a microcontroller ATMEGA16L is used and each MOSFET is driven by a separate ICL7667 using isolated DC-DC converters and optocouplers. It is worth mentioning that TEKTRONIX/TDS2014B oscilloscope has been used for

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measuring parameters' waveforms.

The illustrated experimental waveforms demonstrates the steady-state operation of the converter in the boundary modes: an input voltage equals to 18 V and the other equals to 38 V under the full load conditions.

TABLE III
COMPONENTS FOR PROPOSED CONVERTER

Component	Description	Type/Value
$Q_1 and\ Q_2$	MOSFET	IRFB4110Pbf
$D_1 to\ D_5$	SCHOTTKY Diode	MBR20200CT
$L_{m1} and\ L_{m2}$	Magnetizing Inductor	520 µH/15A
C_1	Capacitor	4.7 µF/160V
C_2	Capacitor	3.3 µF/160V
C_3	Capacitor	2.2 µF/160V
C_4	Capacitor	2.2 µF/160V
C_5	Capacitor	2.2 µF/160V

Fig. 10a depicts output voltage and the capacitors voltages of doubler circuit in the first operation mode ($V_g = 18\,V$). As it shown in this figure the voltage ripple of capacitors are restricted to the desired voltage ripples. In the top boundary mode ($V_g = 38\,V$), the corresponded waveforms are shown in Fig. 10b. This figure also indicates the acceptable voltage ripples.

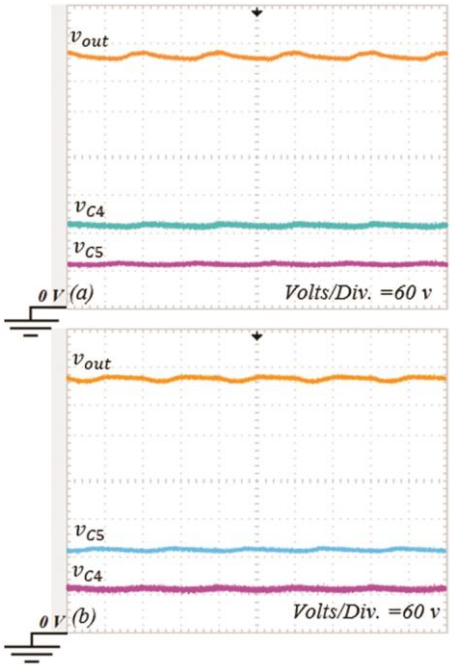

Fig. 10. Output voltage and capacitors voltages of doubler circuit. (a) $V_g = 18\,V$, (b) $V_g = 38\,V$.

Fig. 11a illustrates the capacitors voltages of switched-capacitor circuit in the first operation mode ($V_g = 18\,V$), while, the corresponded waveforms in the top boundary mode ($V_g = 38\,V$) are depicted in Fig. 11b. As it shown in this figure the voltage ripple of capacitors are also restricted to the desired voltage ripples. The maximum voltage ripple is about 4.4 V which belongs to the Capacitor 1 in the $V_g = 18\,V$.

Input, the magnetizing inductors currents and leakage current in both operation modes are illustrated in Fig. 12. In the Fig. 12a corresponded to $V_g = 18\,V$ the current ripples are acceptable. The same is true for Fig. 12b associated with $V_g = 38\,V$. Regarding this figure, in the both boundary modes, the waveforms are exactly the same as the analytical discussion carried out in section II. In addition, this figure validates the specific waveforms of proposed converter in Fig. 2.

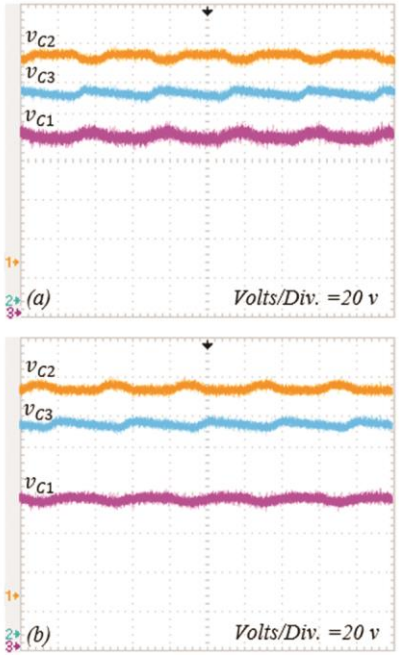

Fig. 11. The capacitors voltages of switched capacitor circuit. (a) $V_g = 18\,V$, (b) $V_g = 38\,V$.

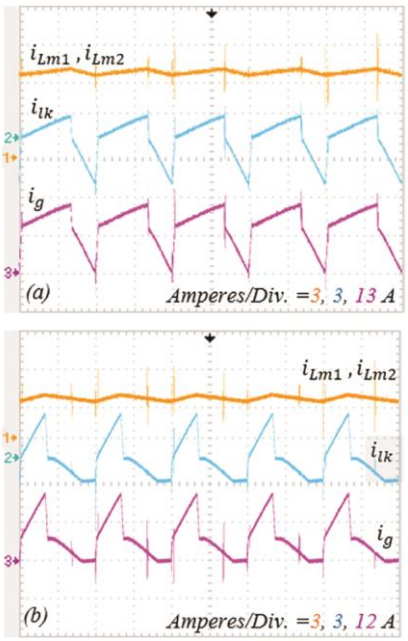

Fig. 12. Input, the magnetizing inductors currents and leakage currents. (a) $V_g = 18\,V$, (b) $V_g = 38\,V$.

Main switch voltage and current are illustrated in Fig. 13. Fig. 13a depicts these parameters for $V_g = 18\,V$, while Fig. 13b depicts them for $V_g = 38\,V$. Regarding these waveforms, the switch voltage stress within this input voltage rang is limited to maximum 60V.

Fig. 14 depicts the calculated and experimental voltage ratio

curve of proposed converter within the input voltage variation rang, namely, 18V to 38V. This experiment has been done by increasing the input voltage from 18V to 38V by step variation of 2V. The experimental voltage gain has become a little lower than calculated voltage ratio, expressed in (20), owing to the parasitic elements in the converter.

Regardless of conversion type, the energy conversion efficiency plays the vital role for any energy conversion system. Efficiency traces are gained experimentally and shown in Fig. 15 as a function of the output power for different input voltage levels. As it can be observed from Fig. 12, the maximum efficiency is occurred in the low output power which is owing to low switches conduction loss. With output power increasing, the energy conversion efficiency lessened due to the sharp increase in conduction loss. In addition, the efficiency becomes higher with the rise in input voltage owing to the small duty cycle being able to be employed with higher input voltage.

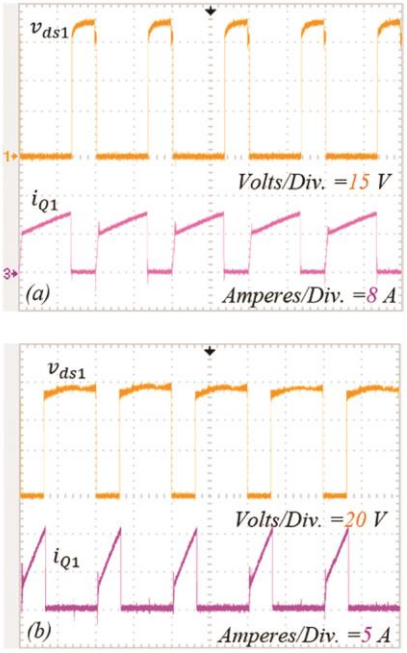

Fig. 13. Main switch voltage and current waveforms. (a) $V_g = 18\,V$, (b) $V_g = 38\,V$.

VIII. Conclusion

A novel ultra-high voltage ratio DC-DC converter is presented. A combination of voltage doubler circuit with the especial switched capacitor circuit is employed. The principle and the steady-state operation of the proposed converter is conducted and additionally the modeling equations are obtained for CCM and DCM operations. Experimental results validate the prefiguration enhancements in the proposed DC-DC converter performance, including high efficiency owing to low voltage stress and ultra-high voltage gain. Moreover, the measurements of proposed converter efficiency indicate that the maximum efficiency can be achieved in the light load and higher input voltage.

A comparison with some aforementioned topologies, although the part counts of the proposed DC-DC converter have been increased, enhanced performance and higher efficiency far outweigh this drawback. The ability of ultra-high voltage ratio along with the high efficiency makes this converter a suitable choice for many low voltage applications, like PV panel and FC.

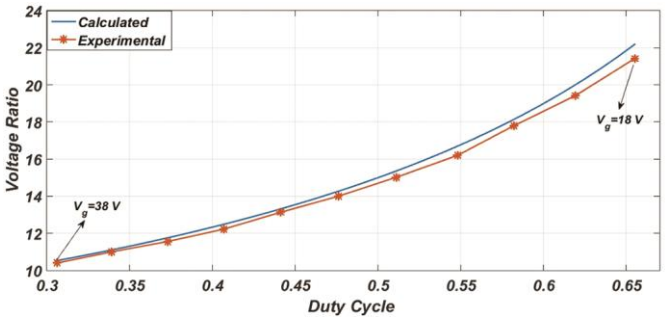

Fig. 14. Calculated and experimental voltage gain

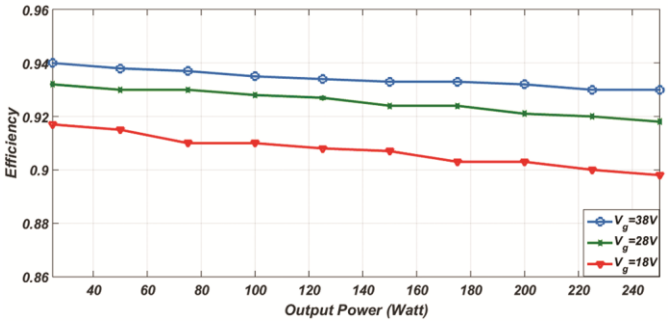

Fig. 15. Energy conversion efficiency for Vo = 400 V as a function of the output power for different input voltage levels.

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