Two-Phase Interleaved Critical Mode PFC Boost Converter With Closed Loop Interleaving Strategy

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***Abstract*—This paper presents a two-phase interleaved critical mode (CRM) power factor correction (PFC) boost converter with a novel closed loop interleaving technique. This new interleaving technique makes each phase work at ideally CRM. Natural current sharing and precise 180° phase shift are achieved. The scheme can be easily integrated into a PFC control chip. Full-order averaged model of CRM boost is derived to analyze the stability of the converter. The loop response and stability of the closed-phase regulation loop have been analyzed. A 400 W two-phase interleaved CRM PFC boost converter prototype is built. This proposed scheme is verified by simulation and experimental results.**

***Index Terms*—Boost, critical mode (CRM), interleaving, power factor correction (PFC), two phase.**

I. Introduction

DUE to the wide utilization of ac/dc power supply in electric systems, the problem of input harmonic current has been a big concern. This leads to the demand for electrical equipments to comply with the European Norm EN61000-3-2. Boost power factor correction (PFC) regulator has been used as a popular solution to suppress current harmonics, achieve unity power factor (PF), and utilize full line power. Typically, fixed switching frequency and continuous conduction mode (CCM) boost rectifier is widely used in high power offline power supplies because of the continuous input current. However, there are still some existing problems that prevent the conventional PFC circuit from obtaining high efficiency. For example, the main switch and rectifier are under hard switching conditions. Also, the fast rectifier's reverse recovery related loss is significant, due to the high-dc output voltage.

One technique to achieve higher efficiency for PFC is to operate the boost converter at the boundary of discontinuous conduction mode (DCM) and CCM, as shown in Fig. 1. Usually, it is called critical mode (CRM) operation. Since the inductor current reaches zero at the end of off time, the rectifier does not have reverse recovery charge. However, the inductor peak current is twice the average current and additional input current filter is required. Because of these drawbacks, the critical mode operation is usually implemented in PFC converter under 300 W. Interleaving two or more phases PFC regulator has been proved as a practical way to supply higher power, as shown in Fig. 2. The interleaved multiphase converter could reduce input ripple current, output capacitor ripple current, and electromagnetic interference (EMI) filter size [1]. The switching frequency of CRM PFC is variable; there is no clock signal available for synchronization. Hence, the interleaving design is more challenging.

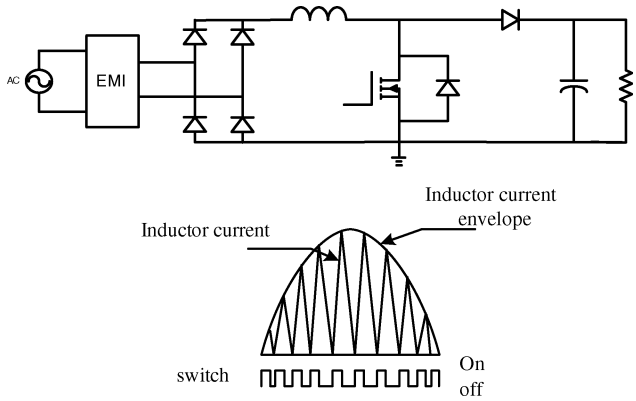

Fig. 1. CRM boost PFC rectifier and inductor current.

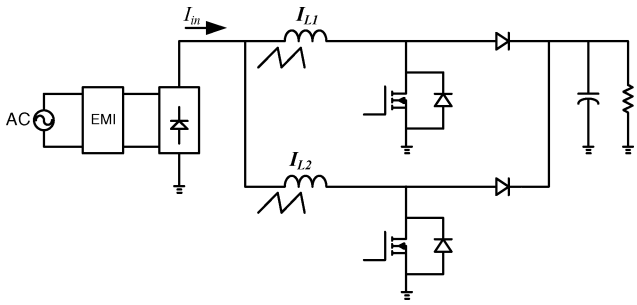

Fig. 2. Two-phase interleaved boost.

Generally, there are two categories of interleaving techniques [2]–[6], [16], [17]. One approach is the open loop solution. One phase is used as master phase and the other phase is the slave phase. Turn-ON or OFF instant of the main switch in slave phase is delayed by half instant period from that of the master phase [2], [3], [16]. Paper [16] summarizes the methods of open loop synchronization: Turn-ON or OFF instant synchronization with either current mode or voltage mode control. Paper [16] concludes that only turn ON instant synchronization with current mode control is a stable implementation method. Theoretically, both two phases should work at ideally critical mode. However, if there is inductance mismatch of boost inductor, the slave phase is working at DCM or CCM instead of critical mode. The implementation method requires that inductance of slave phase

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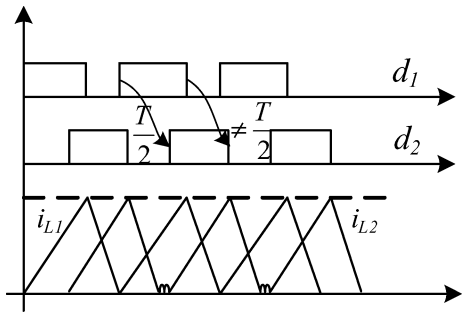


Fig. 3. Interleaving technique in [2] and [16].

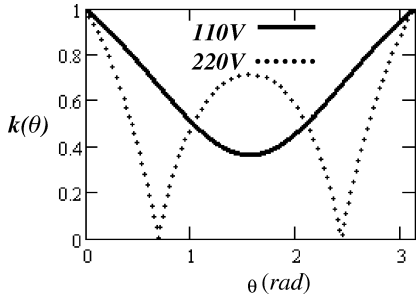


Fig. 4. Input ripple current reduction versus phase angle at different input voltage $V_o = 400$ V.

is always smaller than that of master phase to avoid the CCM operation of slave phase. Hence, the slave phase is working at DCM, which hurts the PF and total harmonic distortion (THD) performance of the converter. Each phase inductor current of this method is shown in Fig. 3 [2]. In addition, the implementation scheme should identify the master and slave during the initialization phase [16]. The other approach is the closed loop solution [4]–[6], [17]. Paper [4] presents a simple interleaving design by using the logic configuration. It has 50% maximum duty cycle limitation. In paper [5] and [17], a conventional phase locked loop (PLL) interleaving approach is proposed. There is a low-pass filter and a compensation network in the phase locked loop. As a result, the interleaving loop response is slow and the passive components are very hard to integrate into a PFC control chip.

This paper presents a novel closed loop interleaving strategy for the multiphase CRM PFC converter [7]. The master phase is free running. Phase shift between the master and slave phase is regulated by changing the period of slave phase cycle-by-cycle. Especially, this closed-loop interleaving scheme does not require any low-pass filter and compensation *RC* network. Even if there is inductance mismatch, the converter still can achieve exactly 180° phase shift and work at ideally critical mode. This proposed interleaved boost converter exhibits fast phase regulation, accurate 180° phase shift, and ideally critical mode operation. This converter has the natural current sharing characteristic. Also, the phase regulation loop response and stability are analyzed in a mathematical way. Furthermore, the stability of the converter is proved by deriving the full-order averaged model.

To verify the principle of the proposed multiphase CRM boost interleaving architecture, a two-phase interleaved boost PFC converter is developed. This converter has two phases, while each phase has the same power rating. Both two phases operate at ideally critical mode with 180° phase shift.

This paper is organized as follows: the benefits of multiphase interleaved CRM boost PFC converter compared with single phase CRM and CCM converter are reviewed in Section II. The control architecture and implementation scheme of a two-phase interleaved CRM boost converter with the novel interleaving technique are presented in Section III. Full-order averaged model of CRM boost is derived and the stability of the converter is also analyzed in Section III. Simulation results are presented in section IV. Experimental results of the converter are shown in Section V. Section VI is the conclusion. An Appendix is also provided.

II. Benefits Review of Interleaving Technique

There are two issues of the CRM PFC converter: 1) the input ripple current, which is two times the average input current; 2) the large differential mode (DM) EMI filter. The interleaving technique can reduce the DM-EMI filter size with the inductor ripple current cancellation [1].

A. Input Ripple Current Cancellation and Duty Cycle or Phase Angle

Fig. 2 is a two-phase interleaved boost converter. The phase inductor currents are 180° out of phase; they cancel each other to reduce the input ripple current. The ratio between the input ripple current and the individual phase inductor current is

$$k(d) = \frac{1-2d}{1-d}(d < 0.5) \qquad k(d) = \frac{2d-1}{d}(d \geq 0.5). \quad (1)$$

The best-input ripple current cancellation happens at 50% duty cycle. In the CRM PFC converter, duty cycle is variable with input line voltage and phase angle changing. $k(\theta)$, which is the ratio between the input ripple current and individual phase inductor current versus phase angle in CRM PFC converter, is expressed by

$$\begin{cases} k(\theta) = 1 - \dfrac{t_{\text{OFF}}}{t_{\text{ON}}}, & \text{if } t_{\text{OFF}} < t_{\text{ON}} \\ k(\theta) = 1 - \dfrac{t_{\text{ON}}}{t_{\text{OFF}}}, & \text{if } t_{\text{OFF}} \geq t_{\text{ON}} \end{cases}$$

where

$$\frac{t_{\text{OFF}}}{t_{\text{ON}}} = \frac{\left|\sqrt{2}V_{\text{in}}\sin(\theta)\right|}{V_0 - \left|\sqrt{2}V_{\text{in}}\sin(\theta)\right|}. \quad (2)$$

The ratio $k(\theta)$ is shown in Fig. 4. The inductor ripple current cancellation is not 100% in half-line cycle, but it is dramatically decreased.

B. DM Noise Reduction

The DM noise is related to the input ripple current. Fig. 5(a) is the simulated input ripple current spectrum of a 400 W single phase CRM converter in Saber simulator and Fig. 5(b) is the input ripple current spectrum of a 400 W two-phase interleaved

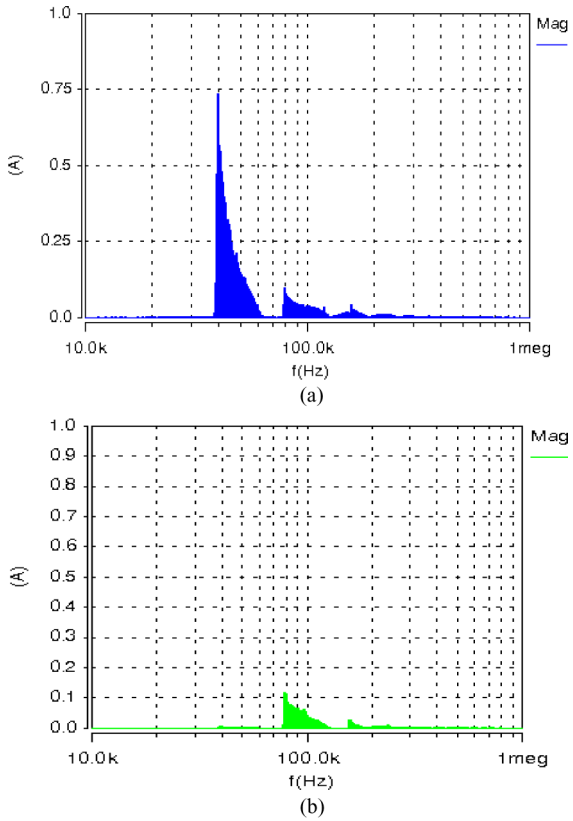


Fig. 5. (a) Simulated input ripple current spectrum of a single-phase 400 W CRM PFC converter $L = 200\ \mu$H. (b) Simulated input ripple current spectrum of a two-phase interleaved 400 W CRM PFC converter $L = 200\ \mu$H.

CRM converter. DM noise of a two-phase interleaved converter is much smaller than that of single phase CRM converter, as shown in Fig. 5(b). Therefore, the DM-EMI filter size can be smaller.

III. Architecture of a Novel Closed Loop Interleaving Technique

Precise interleaving and good current sharing are the basic requirements of the multiphase converter. In critical mode PFC converter, phase inductor current is determined by the on-time of main switch and the inductance. The current difference of each phase is caused by the inductance mismatch. Natural current sharing can be achieved in the CRM boost PFC converter. However, to achieve precise interleaving is challenging when the switching frequency is variable.

A. Novel Interleaving Strategy of Critical Mode PFC

Fig. 6 is the voltage mode control scheme of a two-phase CRM boost regulator with the novel phase interleaving design. v_c is the error voltage of voltage loop. On-time of each phase is generated by the common error voltage. Turn-on edge of each phase is determined by the zero current detection. To achieve good input ripple current cancellation, the two inductor currents should be 180° out of phase. As shown in Fig. 7, i_{L1} is the master phase inductor current and i_{L2} is the slave phase inductor current. s_1 and s_2 are the corresponding turn-ON edges of the main switch in individual phase. An artificial ramp is synchronized with s_1. The ramp amplitude represents the period of master phase. The ramp voltage at s_2 instant indicates the phase shift. If there is 180° phase shift, ramp voltage at S_2 instant must be one half of the ramp amplitude. The novel closed loop interleaving method can make s_2 remain in the middle of the ramp in each cycle. Therefore, 180° phase shift is achieved.

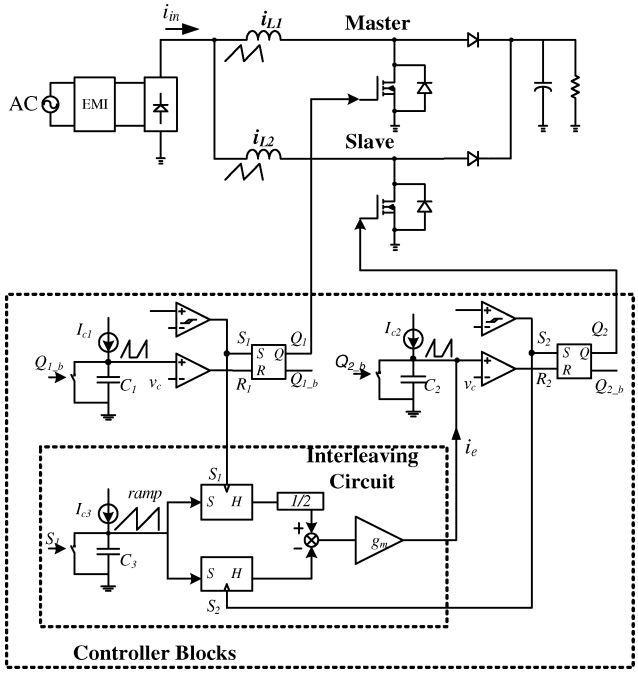


Fig. 6. Proposed control architecture with novel interleaving technique.

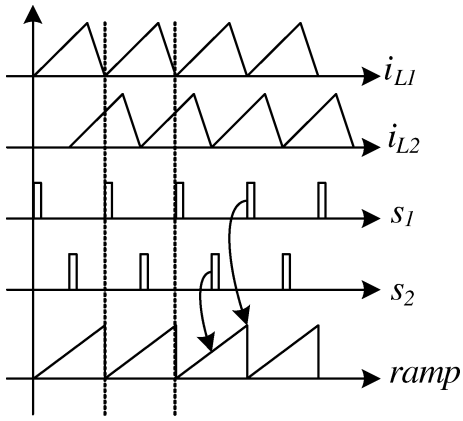


Fig. 7. Proposed interleaving technique.

The interleaving circuit of Fig. 6 is the heart of this control architecture. The artificial ramp, which is synchronized with s_1, is generated by a current source I_{c3} and a small capacitor C_3. At the rising edge of s_1 and s_2, voltages of the ramp are sensed and held separately. The voltage v_{s1} sensed by s_1 represents period of master converter and the voltage v_{s2} sensed by s_2 represents the phase shift between master phase and slave phase. The voltage difference between v_{s2} and $v_{s1}/2$ is the phase error voltage Δv_ϕ, which is proportional to the error phase shift. If the error phase shift is zero, ideally 180° phase shift is achieved. This phase error voltage is transferred to phase error current i_e by a g_m block. Error current i_e is injected back to slave

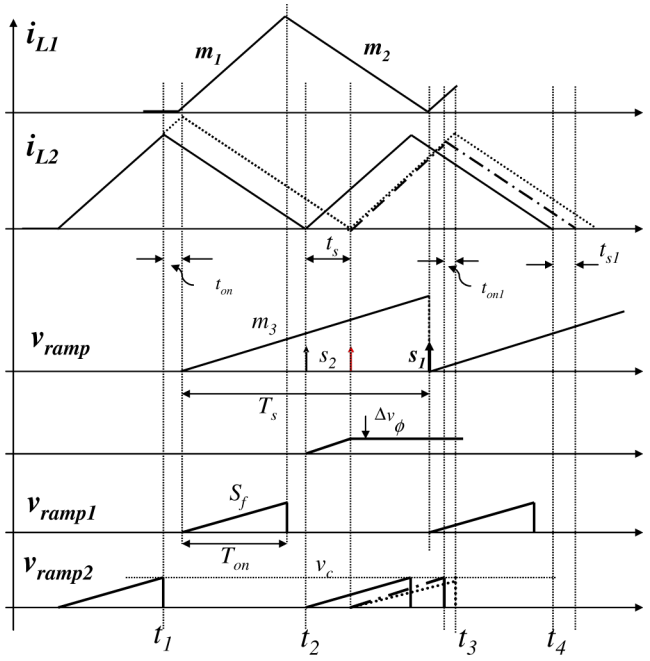


Fig. 8. Phase shift regulation.

phase capacitor C_2 or sourced from C_2. Therefore, the period of the slave phase is changed to achieve the phase regulation. This closed-phase regulation loop is a typical negative feedback loop. Gain of the g_m block determines the response and stability of the closed-phase regulation loop. By choosing suitable value of g_m, this closed-phase regulation loop can achieve one switching cycle regulation. The implementation strategy does not have passive compensation components and low-pass filter. Therefore, this interleaving block can be integrated into the control chip easily.

Stability and response of the phase correction loop can be analyzed by a mathematical way [8]. Fig. 8 shows the phase regulation with $\Delta t_{\rm ON}$ perturbation in the slave phase. i_{L1} and i_{L2} are the master and slave phase inductor currents. $v_{\rm ramp}$ is the artificial ramp. $v_{\rm ramp1}$ and $v_{\rm ramp2}$ are the corresponding master and slave phase fixed on-time charging ramps. Since the PFC converter is working at a quasi steady state, assumptions are made here that the nearby two switching cycle periods are equal and the converter has precise 180° phase shift. If there is a small $\Delta t_{\rm ON}$ perturbation of slave phase at time t_1, the period perturbation will happen at time t_2 and the error period is Δt_s. At the same time, Δt_s is proportionally transferred to the error phase shift voltage Δv_ϕ, which is shown in Fig. 8. The dotted curve in i_{L2} shows this perturbation. If these two phases are free running, this period error Δt_s will be kept forever.

Fortunately, with the novel interleaving technique, the negative phase correction feedback injects a small current to the slave phase capacitor C_2 based on the phase error voltage Δv_ϕ. As a result, ON time of the slave phase is reduced at time t_3 and $\Delta t_{\rm ON}$ perturbation is reduced to $\Delta t_{\rm ON1}$ as shown in Fig. 8. The dotted-dashed lines in i_{L2} and $v_{\rm ramp2}$ show the regulation. Finally, at time t_4, the period or phase error will be Δt_{s1}. If Δt_{s1} is smaller than Δt_s, the phase correction loop is stable. In order to stabilize the phase correction loop, the worst situation of g_m has to be determined. Expressions of Δt_s, Δv_ϕ and the phase error current i_e at time t_2 are included in (3). The error signals $\Delta t_{\rm ON1}$ at time t_3 and Δt_{s1} at time t_4 are expressed in (4). Due to the stability condition of the phase regulation loop in (5), g_m has to satisfy (6). In (6), S_f and m_3 are constant values and g_m is inversely proportional to m_3. In the scheme design, $T_{\rm ON}$ varies with input line rms voltage and the worst situation of g_m happens in low line (110 V) input. The larger g_m, the faster phase regulation is achieved

$$\begin{cases} \Delta t_s = \left(1+\dfrac{m_1}{m_2}\right)\Delta t_{\rm ON} \\ \Delta v_\phi = -m_3\left(1+\dfrac{m_1}{m_2}\right)\Delta t_{\rm ON} \\ i_e = -g_m \Delta v_\phi \\ s_e = \dfrac{i_e}{C_2} = \dfrac{g_m}{C_2} m_3 \left(1+\dfrac{m_1}{m_2}\right)\Delta t_{\rm ON} \end{cases} \tag{3}$$

$$\begin{cases} \Delta t_{\rm ON1} = \dfrac{V_c}{S_f} - \dfrac{V_c}{S_f + s_e} \\ \Delta t_{s1} = \Delta t_s - \left(1+\dfrac{m_1}{m_2}\right)\Delta t_{\rm ON1} \\ \dfrac{\Delta t_{s1}}{\Delta t_s} = 1 - \dfrac{\Delta t_{\rm ON1}}{\Delta t_{\rm ON}} \\ \qquad = 1 - \dfrac{T_{\rm ON}\,(g_m/C_2)\,m_3\,(1+(m_1/m_2))}{S_f + (g_m/C_2)\,m_3\,(1+(m_1/m_2))\,\Delta t_{\rm ON}}. \end{cases} \tag{4}$$

Stability condition of phase correction loop is

$$\begin{cases} 0 < \dfrac{\Delta t_{s1}}{\Delta t_s} < 1 \\ 0 < \dfrac{\Delta t_{\rm ON1}}{\Delta t_{\rm ON}} < 1 \end{cases}. \tag{5}$$

The worst case of g_m is obtained when $\Delta t_{\rm ON} \to 0$, then

$$g_m \le \frac{C_2 S_f}{m_3(1+(m1/m2))T_{\rm ON}} = \frac{C_2 S_f (V_o - V_{\rm in})}{m_3 T_{\rm ON} V_o}. \tag{6}$$

For the converter in Fig. 6, the slave phase converter has an additional phase correction loop. g_m determines the phase correction loop response and stability. In addition to the phase correction loop response and stability, stability of the slave phase converter becomes a concern due to the additional phase regulation loop compared with the master phase converter.

B. Averaged Small Signal Model of CRM Boost

For CRM control, the inductor current always starts from zero in one switching cycle. In most of the modeling analysis publications, the control to output transfer function is simplified as a first order system and inductor current is not stated as a status variable [8]–[10]. In this paper, which considered the frequency variation, a full-order averaged model for CRM boost converter is derived [11]–[14]. In addition, the full-order averaged model of the slave phase converter with phase regulation loop is analyzed.

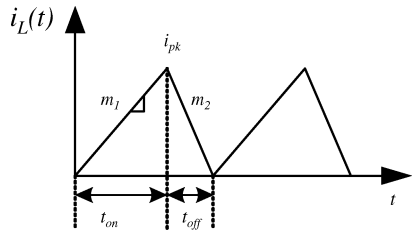


Fig. 9. Inductor current of CRM boost.

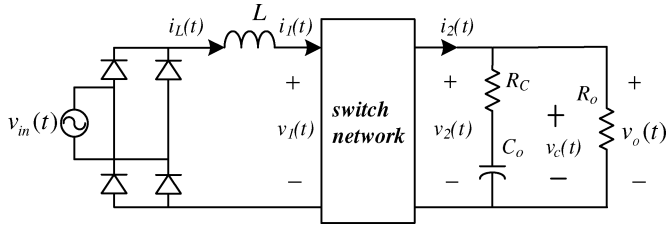


Fig. 10. Boost converter with two-switch network.

1) Reduced-Order Averaged Model of CRM Boost: Operation mode of CRM differs from CCM. ON time $t_{\rm ON}$ is fixed. $t_{\rm OFF}$ is not independent, but rather has algebraic dependency on state and control variables due to the voltage-second balance in one switching cycle (see Fig. 9). The switch and diode (see Fig. 1) can be viewed as a general switch network in Fig. 10 [8]. Construction of a small signal ac model involves averaging, perturbation, and linearization.

The averaged input current $\langle i_1(t)\rangle$ and output current $\langle i_2(t)\rangle$ of the switch network in Fig. 10 is

$$\langle i_1(t)\rangle = \frac{\langle v_{\rm in}(t)\rangle\, t_{\rm ON}}{2L} \qquad \langle i_2(t)\rangle = \frac{\langle v_{\rm in}(t)\rangle\, t_{\rm ON} t_{\rm OFF}}{2Lt_s}$$

where

$$\langle v_{\rm in}(t)\rangle = \langle v_1(t)\rangle \quad t_s = t_{\rm ON} + t_{\rm OFF} \qquad t_{\rm OFF} = \frac{v_{\rm in}}{v_o - v_{\rm in}} t_{\rm ON}. \tag{7}$$

Applied perturbation and linearization to $\langle i_1(t)\rangle, \langle i_2(t)\rangle, t_{\rm OFF}$, and t_s, the first-order ac terms on both sides remain as

$$\begin{cases} \hat{i}_1 = \dfrac{T_{\rm ON}}{2L}\hat{v}_{\rm in} + \dfrac{V_{\rm in}}{2L}\hat{t}_{\rm ON} \\ \hat{i}_2 = \dfrac{T_{\rm ON}T_{\rm OFF}}{2LT_s}\hat{v}_{\rm in} + \dfrac{T_{\rm OFF}V_{\rm in}}{2LT_s}\hat{t}_{\rm ON} + \dfrac{V_{\rm in}T_{\rm ON}}{2LT_s}\hat{t}_{\rm OFF} - \dfrac{V_{\rm in}T_{\rm ON}T_{\rm OFF}}{2LT_s^2}\hat{t}_s \end{cases} \tag{8a}$$

$$\begin{cases} \hat{t}_{\rm OFF} = \dfrac{V_{\rm in}}{V_o - V_{\rm in}}\hat{t}_{\rm ON} - \dfrac{V_{\rm in}T_{\rm ON}}{(V_o - V_{\rm in})^2}\hat{v}_o + \dfrac{V_o T_{\rm ON}}{(V_o - V_{\rm in})^2}\hat{v}_{\rm in} \\ \hat{t}_s = \dfrac{V_o}{V_o - V_{\rm in}}\hat{t}_{\rm ON} - \dfrac{V_{\rm in}T_{\rm ON}}{(V_o - V_{\rm in})^2}\hat{v}_o + \dfrac{V_o T_{\rm ON}}{(V_o - V_{\rm in})^2}\hat{v}_{\rm in} \end{cases} \tag{8b}$$

$\hat{t}_{\rm OFF}$ and $\hat{t}_s$ in (8a) can be replaced by (8b). Hence, $\hat{i}_2$ is written as

$$\hat{i}_2 = \frac{T_{\rm ON}V_{\rm in}}{LV_o}\hat{v}_{\rm in} + \frac{V_{\rm in}^2}{2LV_o}\hat{t}_{\rm ON} - \frac{V_{\rm in}^2 T_{\rm ON}}{2LV_o^2}\hat{v}_o. \tag{8c}$$

Note that $\hat{v}_o = \hat{i}_2 R_o((R_c + (1/sC))/R_o + (R_c + (1/sC)))$ and $\hat{t}_{\rm ON} = (1/S_f)\hat{v}_c$.

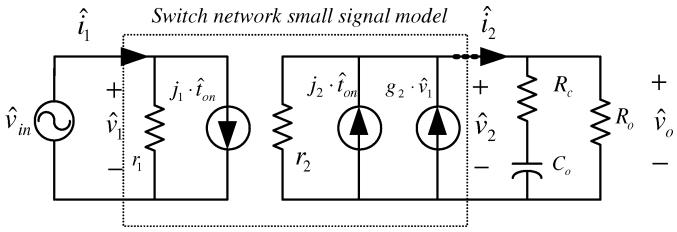


Fig. 11. Reduced order averaged small signal model of Boost PFC.

According to $\hat{i}_1$ in (8a) and $\hat{i}_2$ in (8c), the general switch network in Fig. 10 can be replaced by the reduced order averaged small signal ac model in Fig. 11 where j_1, j_2, and g_2 are the corresponding coefficients.

In (8a), $\hat{i}_1$ is not a status variable, $G_{id}(s) = V_{\rm in}/2L$. Hence, the control $\hat{v}_c$ to inductor current $\hat{i}_L$ transfer function is independent of inductor current dynamics.

Based on (8c), if $\hat{v}_{\rm in} = 0$, control $\hat{v}_c$ to output $\hat{v}_o$ transfer function $G_{vc}(s)$ for resistive load is obtained as

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = \frac{V_o R_o}{S_f}\frac{(1 + R_c C_o s)}{(2LM^2 + T_{\rm ON}R_o) + R_o C_o (2LM^2 + R_c T_{\rm ON})s}. \tag{9}$$

2) Full-Order Averaged Model of CRM Boost: In several publications [11]–[14], small signal response measurement clearly shows second order dynamics at high frequency. Full-order averaged model can correctly predict high frequency response. In this paper, an additional fast phase regulation loop is applied to slave phase converter. Hence, to analyze stability of the converter, a full-order averaged model is necessary.

In the derivation of full-order averaged model, the voltage second balance is not applicable in one switching cycle any more [13]. Considered the time delay between $\Delta t_{\rm ON}$ ($\hat{t}_{\rm ON}$) and $\Delta t_{\rm OFF}$ ($\hat{t}_{\rm OFF}$), Δt_s ($\hat{t}_s$) in Fig. 8, $\hat{t}_{\rm OFF}$ and $\hat{t}_s$ are expressed by [13]

$$\begin{cases} \hat{t}_{\rm OFF} = \hat{t}_{\rm ON}\left[-\left(\delta(t) + \dfrac{V_o}{V_o - V_{\rm in}}\delta\left(t - T_{\rm OFF}\right)\right)\right] \\ \qquad\qquad - \dfrac{V_{\rm in}T_{\rm ON}}{(V_o - V_{\rm in})^2}\hat{v}_o + \dfrac{V_o T_{\rm ON}}{(V_o - V_{\rm in})^2}\hat{v}_{\rm in} \\ \hat{t}_s = \dfrac{V_o}{V_o - V_{\rm in}}\hat{t}_{\rm ON}\delta\left(t - T_{\rm OFF}\right) - \dfrac{V_{\rm in}T_{\rm ON}}{(V_o - V_{\rm in})^2}\hat{v}_o \\ \qquad + \dfrac{V_o T_{\rm ON}}{(V_o - V_{\rm in})^2}\hat{v}_{\rm in}. \end{cases} \tag{10}$$

The input current differential function and output current in Fig. 10 are represented by

$$\begin{cases} \langle i_1'(t)\rangle = \langle i_L'(t)\rangle = \dfrac{t_{\rm ON}\langle v_{\rm in}(t)\rangle + t_{\rm OFF}\left[\langle v_{\rm in}(t)\rangle - \langle v_{\rm o}(t)\rangle\right]}{t_s L} \\ \langle i_2(t)\rangle = \dfrac{\langle v_{\rm in}(t)\rangle\, t_{\rm ON} t_{\rm OFF}}{2Lt_s}. \end{cases} \tag{11}$$

Applied perturbation and linearization to (11) as usual and then substituting the Laplace transformation of (10) into (11),

the first-order ac terms on both sides remain in

$$\begin{cases} L\dfrac{d\hat{i}_L}{dt} = \dfrac{V_o}{T_s}\left(1-e^{-sT_{\rm OFF}}\right)\hat{t}_{\rm ON} \\ \hat{i}_2 = \dfrac{T_{\rm ON}V_{\rm in}}{LV_o}\hat{v}_{\rm in} - \dfrac{V_{\rm in}^2 T_{\rm ON}}{2LV_o^2}\hat{v}_o \\ \quad + \left(\dfrac{V_{\rm in}\left(2V_{\rm in}-V_o\right)}{2LV_o} + \dfrac{V_{\rm in}}{2L}\dfrac{\left(V_o-V_{\rm in}\right)}{V_o}e^{-sT_{\rm OFF}}\right)\hat{t}_{\rm ON} \end{cases} . \tag{12}$$

In (12), the inductor current is a status variable and is only related to $\hat{t}_{\rm ON}$. Sun *et al.* [13] explains the inductor current dynamics in one switching period. Specially, $\hat{i}_L$ happens only in a switching period since the inductor current always starts from zero in every switching cycle. Based on (8a) and (12), the input and output current of the two port network can be expressed by

$$\begin{cases} \hat{i}_1 = \dfrac{T_{\rm ON}}{2L}\hat{v}_1 + \left[\dfrac{T_{\rm ON}}{2L}\dfrac{V_o}{T_s}\left(1-e^{-sT_{\rm OFF}}\right) + \dfrac{V_{\rm in}}{2L}\right]\hat{t}_{\rm ON} \\ \hat{i}_2 = \dfrac{T_{\rm ON}V_{\rm in}}{LV_o}\hat{v}_1 - \dfrac{V_{\rm in}^2 T_{\rm ON}}{2LV_o^2}\hat{v}_o + \left(\dfrac{T_{\rm ON}V_{\rm in}}{LT_s}\left(1-e^{-sT_{\rm OFF}}\right)\right. \\ \quad \left. + \dfrac{V_{\rm in}\left(2V_{\rm in}-V_o\right)}{2LV_o} + \dfrac{V_{\rm in}}{2L}\dfrac{\left(V_o-V_{\rm in}\right)}{V_o}e^{-sT_{\rm OFF}}\right)\hat{t}_{\rm ON} \end{cases} . \tag{13}$$

Compared with (8a) and (8c), the coefficients j_1 and j_2 have been replaced by the corresponding coefficients j_1' and j_2'. According to (13), the control to inductor current transfer function $G_{\rm id}(s)$ is

$$G_{\rm id}(s) = \frac{\hat{i}_L}{\hat{t}_{\rm ON}} = \frac{V_o\left(1-e^{-sT_{\rm OFF}}\right)}{LT_s s} \tag{14}$$

where

$$e^{-sT_{\rm OFF}} \approx \frac{1-\left(s/\left(2/T_{\rm OFF}\right)\right)}{1+\left(s/\left(2/T_{\rm OFF}\right)\right)}.$$

Meanwhile, with the assumption $\hat{v}_{\rm in}=0$, the full-order transfer function $G_{vc}(s)$ is

$$G_{vc}(s) = \frac{V_o R_o}{S_f}\left(\frac{1+\left(s/\left(2/T_{\rm OFF}\right)\right)\left(3-2V_0/V_{\rm in}\right)}{1+\left(s/\left(2/T_{\rm OFF}\right)\right)}\right) \times \frac{\left(1+R_cC_os\right)}{\left(2LM^2+T_{\rm ON}R_o\right)+R_oC_o\left(2LM^2+R_cT_{\rm ON}\right)s}. \tag{15}$$

Fig. 12 shows the reduced order and full-order control to output transfer function $G_{vc}(s)$ magnitude and phase Bode plot. In Fig. 12, frequency responses of the full-order averaged model and reduced order model match each other exactly at low frequencies. The full-order averaged model has a right half plane zero and a pole beyond 10 kHz. The right half plane zero is caused by the delay item $e^{-sT_{\rm OFF}}$ in $\hat{t}_{\rm OFF}$ and $\hat{t}_s$. In Fig. 12, gain curve crosses the zero axes again at frequency 20 kHz. Hence, compensator of the voltage loop should be carefully designed since gain of the stable closed voltage loop only can cross zero axes one time. Otherwise, the Bode plot cannot be used to identify the loop stability.

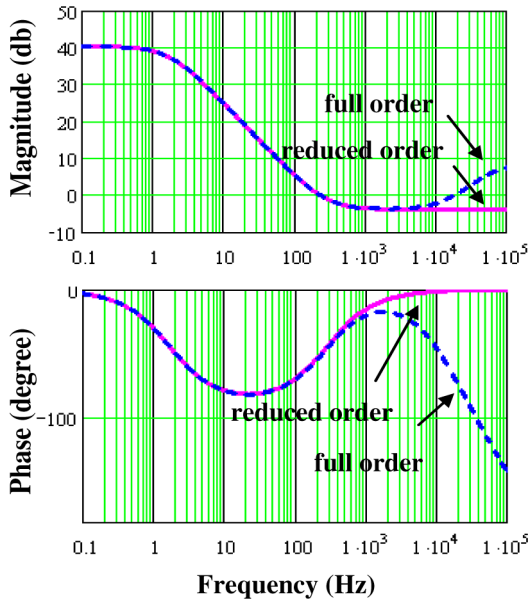


Fig. 12. Magnitude and phase of the reduced order and full order $G_{vc}(s)$.

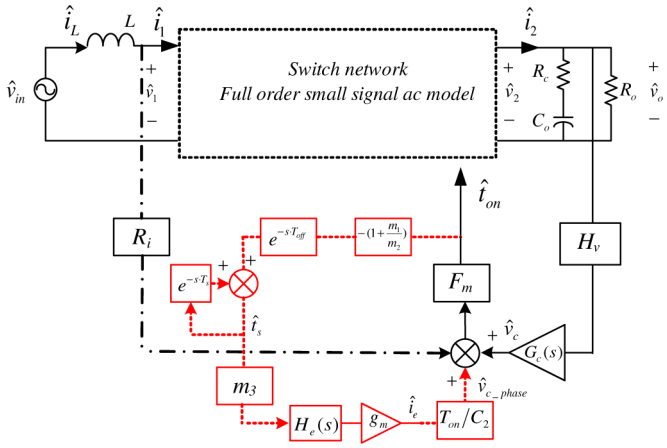


Fig. 13. Averaged small signal model of the slave phase with the novel closed phase correction loop.

3) Full-Order Averaged Model of Slave phase Converter with Novel Phase Correction Loop: The small signal model of the slave phase converter including the phase correction loop is shown in Fig. 13. The dashed-dotted line indicates the current loop. In this paper, fixed on time control, which is a voltage mode control, is implemented. This is why the current loop response is not included. The small signal model of the phase regulation loop is expressed with dashed line in Fig.13 because the phase regulation loop is only used to calibrate the phase shift. The loop response and the stability of the phase regulation loop are analyzed in the following.

Based on Fig. 13, the transfer function of the phase regulation loop can be expressed as

$$T_{\rm pll}(s) = -\left(1+\frac{m_1}{m_2}\right)e^{-sT_{\rm OFF}}\frac{1}{1-e^{-sT_s}}m_3 g_m H_e(s)\frac{T_{\rm ON}}{C_2}F_m. \tag{16}$$

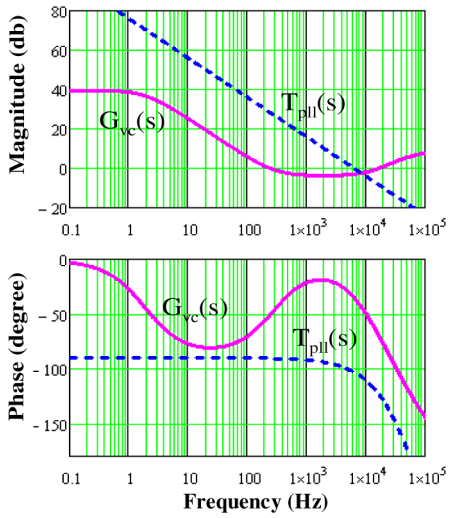


Fig. 14. Magnitude and phase of phase regulation loop ($g_m = 40$ μS) and the full-order $G_{vc}(s)$ of the slave phase.

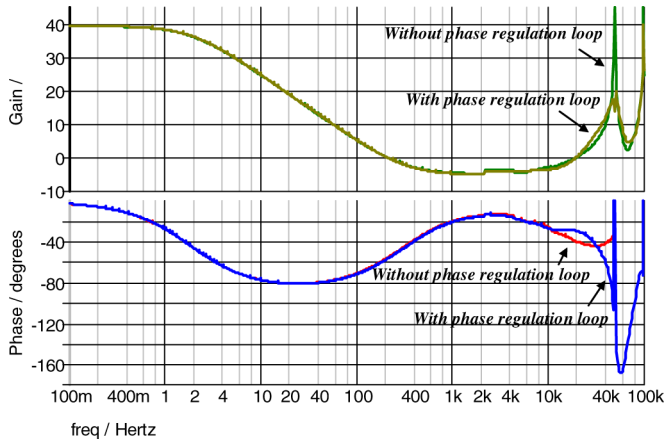


Fig. 15. Magnitude and phase of the full order $G_{vc}(s)$ with phase correction loop and voltage loop $T_v(s)$.

The derivation of (16) is in the Appendix. In (16), $e^{-sT_{\rm OFF}}$ represents the delay of $\hat{v}_\phi$ (Δv_ϕ) from $\hat{t}_{\rm ON}$ ($\Delta t_{\rm ON}$), as shown in Fig. 8. $H_e(s) = \left(1 - e^{-sT_s}\right)/(sT_s)$, which is caused by the sample and hold block in phase regulation loop (see Fig. 6).

The analyzed loop gain and phase of the phase regulation loop in the slave phase converter are shown in Fig. 14. The bode plot of $T_{\rm pll}(s)$ indicates that the phase regulation loop has an infinite pole characteristics and is always stable. The bandwidth of the phase regulation loop is around 10 kHz, which is 1/4 of the minimum switching frequency of the PFC converter. Compared with the closed voltage loop (required bandwidth <120 Hz) in the PFC converter, the bandwidth of the phase regulation loop is 100 times higher. Hence, this phase regulation loop can be ignored in the voltage loop analysis of the PFC converter and modulator gain of the slave phase is a constant (F_m).

Fig. 15 is the simulated gain and phase of the full order $G_{vc}(s)$ of the slave phase converter with and without phase regulation loop in SIMPLIS simulator. There is a slightly difference between these two curves beyond half minimum switching frequency (20 kHz). Fig.15 proves that the phase regulation loop does not change the modulator gain and affect the converter's stability of the slave phase converter.

For the voltage loop of PFC converter, the crossover frequency must be below 120 Hz to eliminate double line frequency output ripple. A conventional compensator $-(s + z_1)/(s)$ is used to compensate the voltage loop. Based on Fig. 15, from the modeling point of view, conclusions are made here: a two-phase interleaved CRM boost could be simplified as a single phase boost; the equivalent inductance is one half of each phase inductance and the output capacitor is double of each phase. Furthermore, the reduced order control to output small signal model can be used to predict the two-phase converter's stability, since the zero and pole in full order control to output small signal model happen at a much higher frequency than the voltage loop bandwidth.

IV. Simulation of Two-Phase Interleaved CRM PFC Boost Converter

Based on Fig. 6, the simulated input and individual inductor current of a two phase 400 W PFC converter are shown in Fig. 16(a) and (b). The input ripple current is significantly reduced compared with individual phase inductor current. Regarding the input current, this converter appears to be working at CCM. This converter achieves precise 180° phase shift and the peak to peak ripple current is 40% of average input current.

The transient phase regulation is shown in Fig. 17(a) and (b). In Fig. 17(a), both two phases are free running when the enable signal is high. The maximum input current ripple is two times each phase peak current. When the enable signal is low, the closed-phase regulation loop is applied; the input ripple current is dramatically reduced. Fig. 17(b) shows the transient phase regulation in one cycle. After one cycle regulation of slave phase, these two phases achieve 180° interleaving.

V. Experiment Results of Two-Phase Interleaved CRM PFC Boost Converter

The hardware demo of a 400 W two-phase interleaved boost converter is shown in Fig. 18. In the power stage, $C_o = 330$ μF and the phase inductors have ±5% tolerance, $L_1 = 430$ μH and $L_2 = 460$ μH, respectively. The controller of this converter is built by discrete components based on Fig. 6. The constant ON time is related to the capacitor C_1 and C_2. Two bandgap current sources I_{C1}, I_{C2}, and ±5% tolerance capacitors are used to determine the constant on-time. $I_{C1} = I_{C2} = I_{C3} = 100$ μA, $C_1 = C_2 = 680$ pF, $C_3 = 1000$ pF, where C_1 and C_2 also have ±5% tolerance. In the transistor level integrated circuits design, I_{C3} and C_3 can be scaled down to 1 μA and 10 pF. C_1 and C_2 are OFF chip capacitors. The artificial ramp maximum amplitude is 5 V.

In the converter, the minimum switching frequency is 40 kHz and $T_{\rm ON} = 15$ μs at low line input (110 V). Based on (6), the maximum g_m gain is 40 s. Output current range of the g_m block is ±20 μA, which is limited by the commercial discrete g_m amplifier design. If the maximum output current of g_m block is

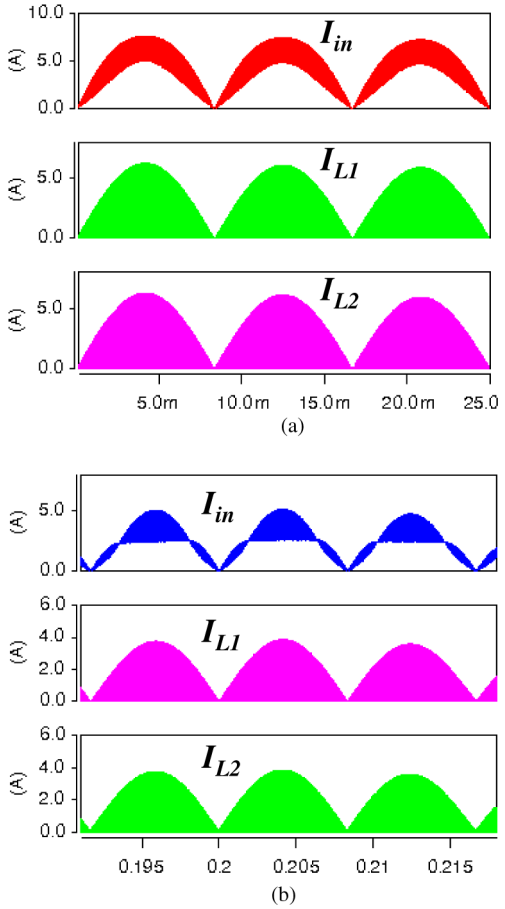


Fig. 16. (a) Input and individual phase inductor current, $V_{\rm in} = 110$ V. (b) Input and individual phase inductor current $V_{\rm in} = 220$ V.

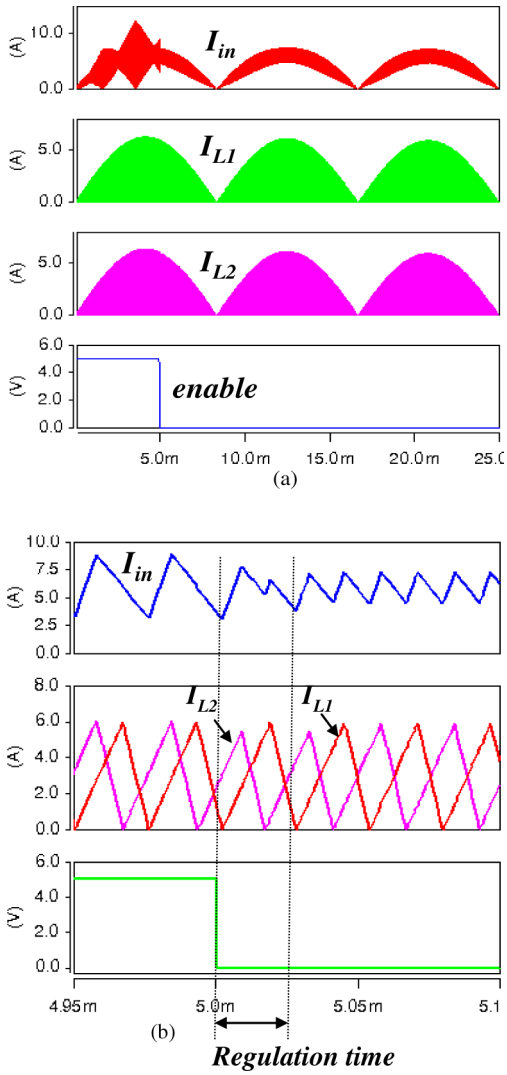


Fig. 17. (a) Transient phase regulation. (b) Transient phase regulation in one cycle.

$\pm 100\ \mu$A, the ideal one cycle phase regulation (see Fig. 17) can be obtained. The experimental transient phase regulation with the nonideal g_m block will be shown in Fig. 21.

Fig. 19(a) shows the experimental phase inductor currents and the corresponding gate drive signals at steady state. These two phases are working at ideally critical mode and the phase shift is 180°. The input current and master phase inductor current are shown in Fig. 19(b). The input ripple current is much smaller than the individual phase inductor current. There is a minor amplitude variation of input ripple current, which is caused by each phase inductance mismatch.

Fig. 20 is the input current and master phase inductor current of several line cycles when the input is 110 V. The peak-to-peak input ripple current is 40% of the peak value, which matches the simulation very well. The zero-crossing distortion of the input current is caused by the input rectifier bridge voltage drop, the delay of zero-voltage detection (ZCD) circuit, and the resonant capacitor that is in parallel with the main switch to achieve the soft switching. The current sensing voltage range, which is from inductor's secondary winding, is ± 20 V. It is much higher than the break down voltage of analog circuit [15]. A Zener and diode are used to clamp the ZCD positive and negative voltage. The parasitic capacitance of Zener diode is around 200 pF, which

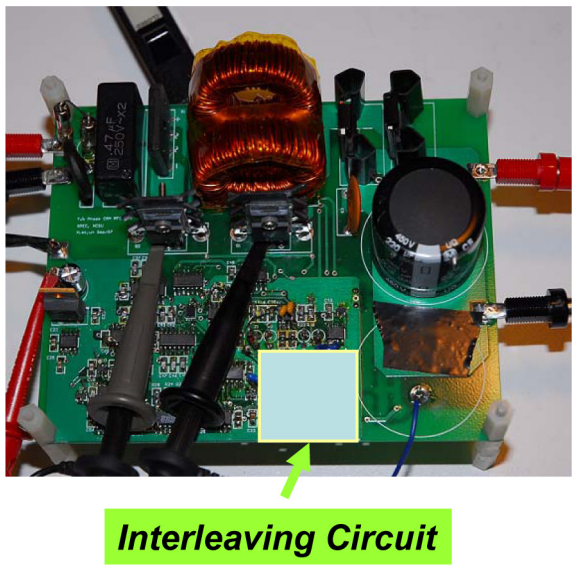


Fig. 18. Hardware of the 400 W two-phase critical mode interleaved PFC converter.

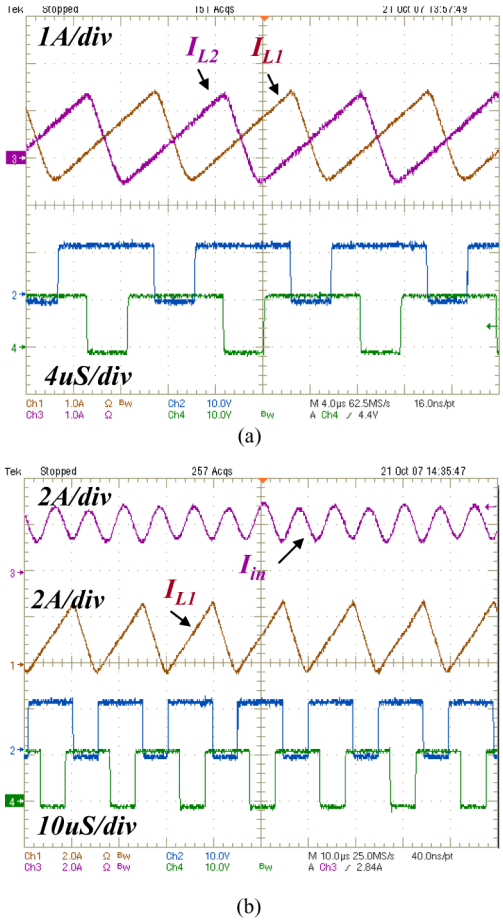


Fig. 19. (a) Inductor current and corresponding gate drive signal. (b) Input current, master phase inductor current and gate drive signal.

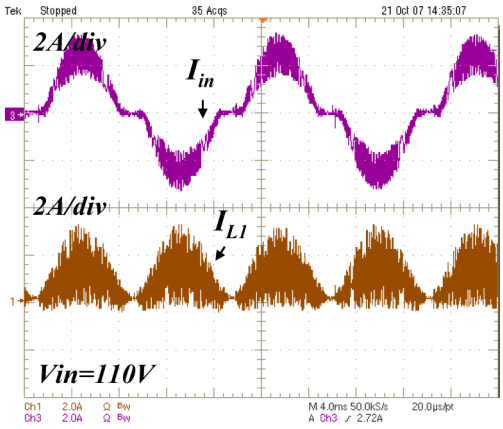


Fig. 20. Input current and master phase inductor current $V_{\rm in} = 110$ V.

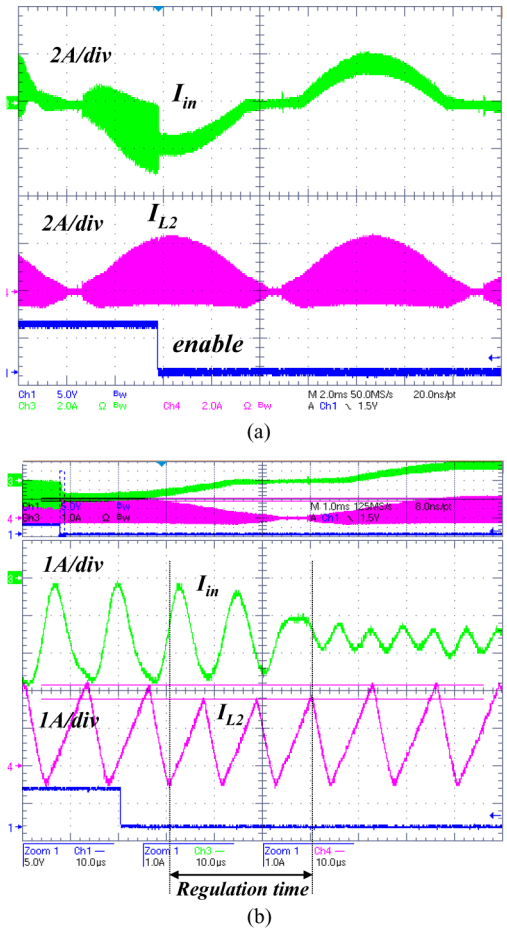


Fig. 21. (a) Experimental transient phase regulation. (b) Experimental transient phase regulation, expanding waveform of Fig. 29(a).

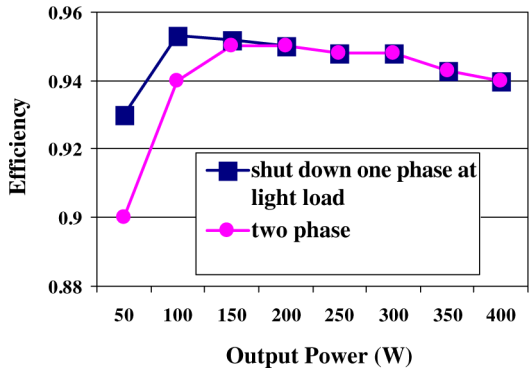


Fig. 22. Efficiencies of single phase and two-phase operation at light load condition $V_{\rm in} = 110$ V.

introduces a big delay to the main switch turn ON edge. This problem will not happen in the integrated control chip.

Fig. 21(a) and (b) shows the experimental transient phase regulation. In Fig. 21(a), when the enable is high, there is no interleaving between two phases and the input ripple current is very large. The phase regulation loop is applied when the enable is low. As a result, the input ripple current is only 40% of the average input current. Fig. 21(b) is the expanding picture of Fig. 21(a). Due to the output current limitation of the g_m block, 180° phase shift is achieved by two cycle regulation. Based on Fig. 21(a) and (b), a conclusion can be made, this new closed phase correction loop has very fast response and the experimental results match the simulations very well.

Another advantage of the two-phase converter is to improve the power efficiency at light load condition by shutting down one phase. Fig. 22 shows the experimental power efficiency of the

two-phase converter. In the light load condition, if one phase is shut down, the converter's efficiency has over 3% improvement.

VI. Conclusion

In this paper, a two-phase interleaved CRM PFC boost converter with a new closed loop interleaving technique is presented. This interleaving method results in several advantages, which include: ideally 180° phase shift, critical working mode of two phases, and simplicity to be integrated to a control chip. A two-phase boost PFC converter is built to verify the presented approach. It is found that the input ripple current is dramatically reduced by applying this interleaving method. In the high power application, interleaving PFC preregulators would be a very promising choice.

Appendix

Derivation of (16)

In Fig. 6, if there is a perturbation $\Delta t_{\rm ON}$ in slave phase converter, $i_e = g_m \Delta v_\phi H_e(s) = g_m m_3 \left(\left(1-e^{-sT_s}\right)/(sT_s)\right)\Delta t_s$, where Δt_s can be obtained based on Fig. 8.

In Fig. 8

$$\Delta t_s = \left(1+\frac{m_1}{m_2}\right)\Delta t_{\rm ON} e^{-sT_{\rm OFF}}.$$

Due to the phase regulation loop $\Delta v_\phi = m_3 \Delta t_s \rightarrow i_e = g_m \Delta v_\phi \rightarrow \Delta t_{\rm ON1}$, $\Delta t_{s1} = \Delta t_s - (1+\frac{m_1}{m_2})\Delta t_{\rm ON1} e^{-sT_{\rm OFF}}$, where $e^{-sT_{\rm OFF}}$ represents the delay of $\hat{v}_\phi(\Delta v_\phi)$ from $\hat{t}_{\rm ON}(\Delta t_{\rm ON})$, as shown in Fig. 8.

g_m is chosen as a fixed value in the controller, hence, the phase regulation loop may not correct the error phase shift in one cycle due to the variable input voltage. The error phase shift could be corrected by couple cycles

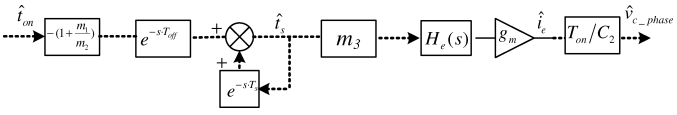
$$\Delta v_{\phi 1} = m_3 \Delta t_{s1} \rightarrow i_e = g_m \Delta v_{\phi 1} \rightarrow \Delta t_{\rm ON2}$$

$$\Delta t_{s2} = \Delta t_{s1} - \left(1+\frac{m_1}{m_2}\right)\Delta t_{\rm ON2} e^{-sT_{\rm OFF}}.$$

In the kth switching cycle after the perturbation of $\Delta t_{\rm ON}$

$$\Delta t_{s(k)} = \Delta t_{s(k-1)} - \left(1+\frac{m_1}{m_2}\right)\Delta t_{{\rm ON}(k)} e^{-sT_{\rm OFF}}.$$

According to these expressions, the small signal model from $\hat{t}_{\rm ON}$ to $\hat{i}_e$ can be shown in the block diagram in the *s* domain.



$H_e(s)$ is caused by the sample and hold circuit. Therefore, the transfer function of the phase regulation loop is

$$T_{\rm pll}(s) = -\left(1+\frac{m_1}{m_2}\right) e^{-sT_{\rm OFF}} \frac{1}{1-e^{-sT_s}} m_3 g_m H_e(s) \frac{T_{\rm ON}}{C_2}.$$

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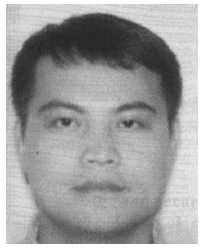

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