Topology Characteristics Analysis and Performance Comparison for Optimal Design of High Efficiency PFC Circuit for Telecom

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Abstract—**This paper is selecting typical PFC topology that can be application design of high-capability power of high efficiency, high power factor correction (PFC) performances, and review its operating characteristics, and analyze the actual performance differences to manufacture 2kwatt grade product under the same conditions. The first topology is average current mode control (ACM) PFC that the performance is excellent and applications examples are various in conventional PFC circuit methods. The second topology is related to Interleaved PFC of dual boost way that has the advantages of current ripple performance improvement and current stress reduction properties. Third and fourth topology is back to back bridgeless (BTBBL) PFC and semi-bridgeless (SBL), and the object of topologies is to improve loss of bridge diode. PSIM simulation was used for comparison of topology and prototype was designed with power density standard of more 1.35kW/dm^3 under 1U size low-profile conditions. To minimize the performance comparison errors, design conditions such as board space, heat-sink and PCB pattern synchronize to the maximum. It should be note that topology efficiency and power factor performance difference was identified objectively through comparing tests.**

Keywords – PFC; Power factor correntionl; Average current mode; Iterleaved; Backt to back; Semi-bridgeless; Bridgeless

I. INTRODUCTION

It is common technical challenge to use efficient energy in the all industrial field. Hence, efficiency performance of PSU must take into consideration for developers. The efficiency performance is more important in case that power consumption is larger systems. Recent efficiency performance of the PFC circuit has been upgrading continuously by performance improvement of the switch components like FET and diode and the material development of magnetic components along with topology research having improved power flow. As result of research, the study on high-efficiency PFC circuits with more 99% has been released [1-3].

On the other hand, it is easy to overlook additional problems to new proposed topology having affected by conventional circuit. Therefore, it needs to check that there is improvement effect in some degree in practice and there is no trade-off of other performance element when using equally high-performance parts on new proposed topology. In this study, to evaluate the performance of each topology when designing high-capacity high-density, performance was compared by applying the design to meet more 1.35kW/dm^3 power density on 1U specifications which is the thin standard size of power device for communications. Especially, PSU for communication and server system of targeted application field must meet a high-efficiency performance because of continuous and long-term operating characteristics. In addition, PSU to meet demanding design conditions such as low-profile, high-density and high-performance serves as the circuit role model of other application fields.

II. PFC STAGE OF PSU

The PSU for communication generally is designed as two stage structure of PFC stage and DC-DC stage as shown in figure 1 to meet the electrical requirements like input voltage range, the power capacity and output noise characteristics. To compare the performance of the PFC circuits selected in this paper, the EMI filter, link-capacitor, controller and auxiliary power located inside dotted line of figure 1 have been designed together.

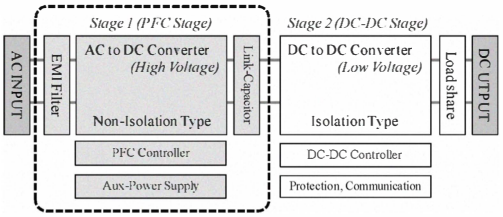

Figure 1. Circuit structure of PSU for telecom

A. Type of PFC topology

PFC circuit is designed in various ways in accordance with power part circuit structure and control algorithms. There is PFC circuit that has in high practical applications is in figure 2.

B. Inductor current control method

Boost converter has been applied widely when designing the PFC stage of medium, high capacity PSU. On the other hand, boost PFC is divided into discontinues conduction mode

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(DCM), boundary conduction mode (BCM), continues conduction mode (CCM) depending on current control way of inductor. The inductor current control method affects the size of inductor, the size of circulating currents and efficiency, power factor, noise characteristics become different. Also, EMI filter design standard is changed. DCM and BCM are recommended below 200~300watt in many design cases, the selection of the CCM way is recommended on more capacity.

CCM is also re-divided into control manner such as peak current mode control (PCM), variable hysteresis current mode control (VHCM), average current mode control (ACM). In particular, to control the instrumented inductor current, the high power factor improvement is shown by controlling in FET on/off manner on upper limit and lower limit of the standard current in average current mode control.

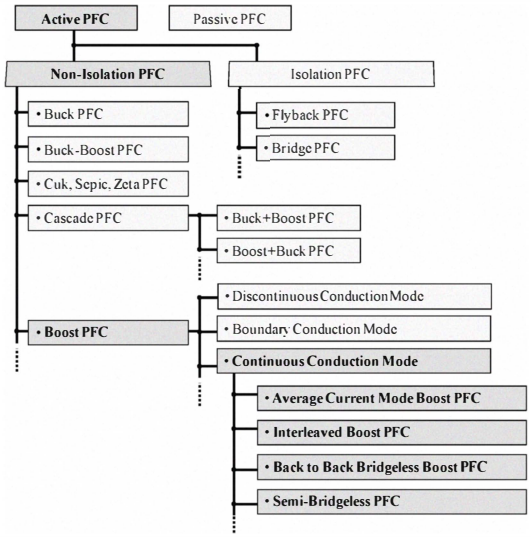


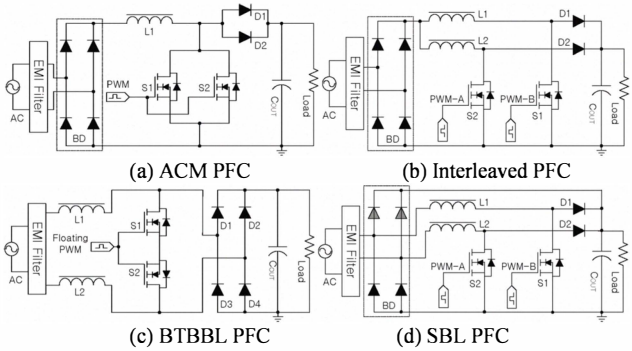
Figure 2. Classification of PFC topology

C. *Selection of topology*

The main contribution of this paper is performance comparison of high topology appropriate to 2kwatt grade high-density output. So in general 300~500watt capacity of more than 95% efficiency in the performance and possible PFC average current mode control boost PFC (herein after ACM PFC) is best suited to the reference topology. Meanwhile, loss analysis research for improving the efficiency of ACM PFC has been done widely. As a result of our study, it can provide a loss ratio of bridge diode's loss having nearly 50% in approximately 700watt power capacity in the rest of the parts except the EMI filter loss [4]. In other words, circuit structure that can reduce bridge diode loss is desirable for efficiency performance improvement circuit of PFC. Therefore, recently spotlighting two topology of bridgeless ways were chosen in the paper. Each topology is back to back bridgeless boost PFC (herein after BTBBL PFC) and semi-bridgeless boost PFC (herein after SBL PFC) [4-6]. Finally, selected topology is interleaved boost PFC (herein after Interleaved PFC). Interleaved PFC is dual structure of the ACM PFC, controls PWM phase shift. Conduction current stress of power devices is low, has the advantage of reducing the output current ripple.

III. TOPOLOGY CHARACTERISTICS

To confirm the basic characteristics of selected four kinds of topologies, PSIM simulation was utilized. Basic control method of each topology is the same as the average current mode control. The control of figure 4 has been commonly used in each topology. Controller's Vin-P and Vin-N are the input line voltage feedforward signal. Vout is the output voltage feedback signal. L-I is an inductor circulation current signal. At the time ACM PFC and BTBBL PFC has been used without changing the controller, only synthesis of the signal was changed and run because interleaved PFC and SBL PFC need respective inductor current control. Switching frequency was set equally at 60 kHz. In addition, with reference to datasheet of the actual selected parts V_F and each switch parts were applied the internal impedance. Inductor and output capacitor also applies used values when the actual prototype was produced.



(a) ACM PFC (b) Interleaved PFC

(c) BTBBL PFC (d) SBL PFC

Figure 3. Equivalent circuit of high efficiency topology

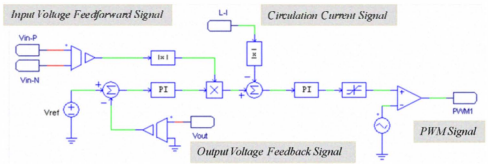


Figure 4. Basic controller of average current mode control

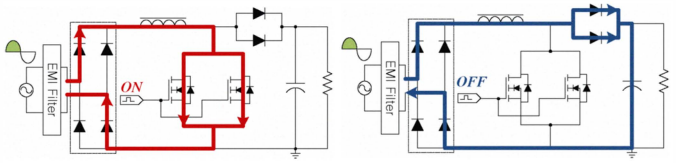
TABLE I. COMPONET CONSTITUENT OF EACH TOPOLOGY

	ACM PFC	Interleaved PFC	BTBBL PFC	SBL PFC
Bridge diode	1	1	0	0.5
Inductor	1(3ea)	2(4ea)	2(4ea)	2(4ea)
FET	1	2	2	2
Diode	1	2	4	2
Current transformer	1	2	1	2
Driver	1	2	1(floating)	2
PWM channel	1	2	1	2

A. *Characteristics of ACM PFC*

Figure 3(a) is the basic circuit structure of the ACM PFC. One bridge diode for input voltage rectification, one FET, one diode and one inductor are basic parts and one inductor current sensor is used for current control. But, in this paper for 2kwatt output FET and diode were used respectively two considering allowable current capacity and thermal performance. Thus, for the simulation was also used respectively two in parallel. Figure 5 is FET on/off operation

flow by input state of ACM PFC. Stable operation can be found until output voltage reaches the normal state. The controller gain for figure 6 simulation result was used equally to the rest of the topology. Figure 7 is the result waveform to be working to improve well the power factor as simulation circuit diagram and average current mode.



(a) Positive input FET turn-on (b) Positive input FET turn-off

(c) Negative input FET turn-on (d) Negative input FET turn-off

Figure 5. Operating mode of ACM PFC

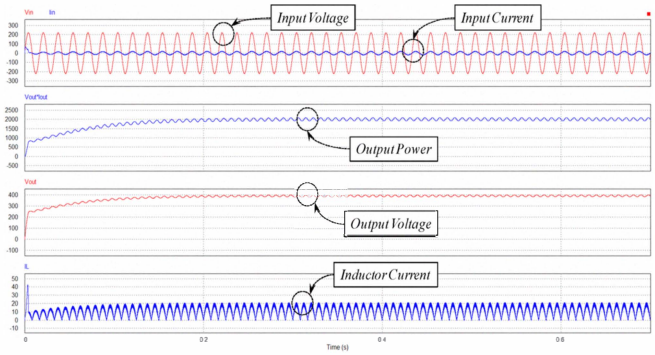
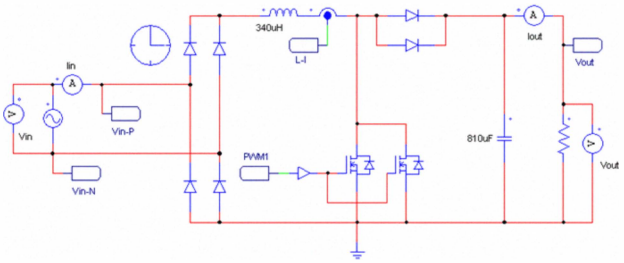
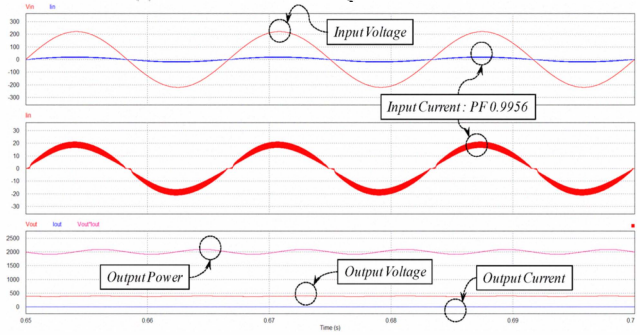


Figure 6. Start up characteristics waveform of basic controller



(a) Simulation circuit diagram of ACM PFC

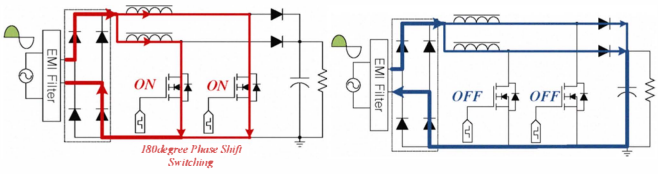


(b) Input voltage, input current and output power

Figure 7. Simulaton of ACM PSIM

B. *Characteristics of Interleaved PFC*

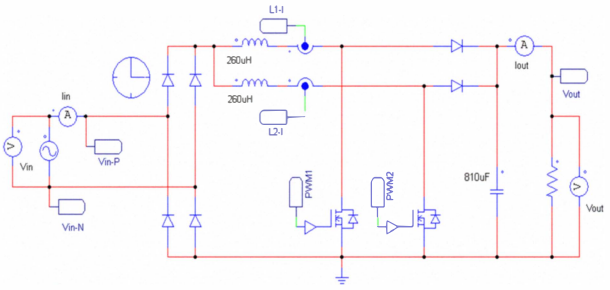
Figure 3(b) is the basic circuit structure of the Interleaved PFC. Circuit layout is the same as configured ACM PFC with the dual boost. Therefore, current conducted on each boost flows quarter. In addition, the controller makes PWM signal to operate by 180 degree phase shift. As a result, effects that current ripple is offset can be enlarged. Figure 8 shows FET on/off operation flow by the input state of Interleaved PFC. Figure 9 shows the simulation circuit of Interleaved PFC and the simulation results of 180 degree phase shift. In contrast, it can be seen that the power factor improvement performance is lower than 180 degrees phase shift result of figure 10(a) if look at the results after 90 degree phase shift as shown in figure 10(b), input current ripple can be seen large. In other words ripple trade-off effect can be seen largest to do phase shift as 360 degrees divided by the number of boost circuits.



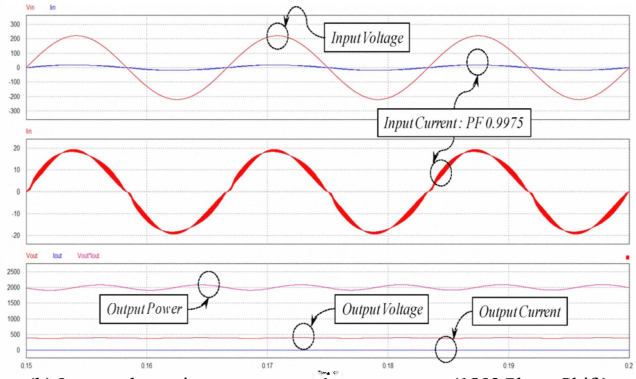
(a) Positive input FET turn-on (b) Positive input FET turn-off

(c) Negative input– FET turn-on (d) Negative input FET turn-off

Figure 8. Operating mode of Interleaved PFC

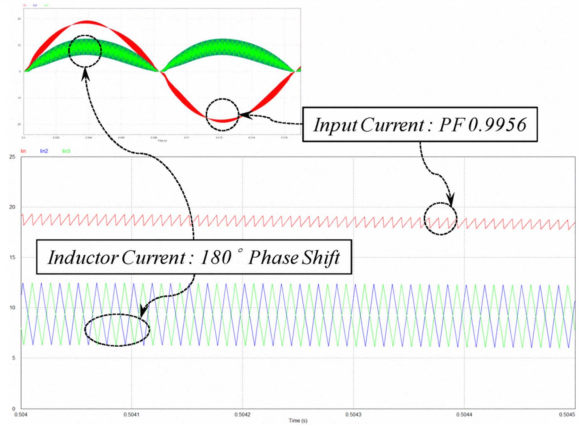


(a) Simulation circuit diagram of Interleaved PFC

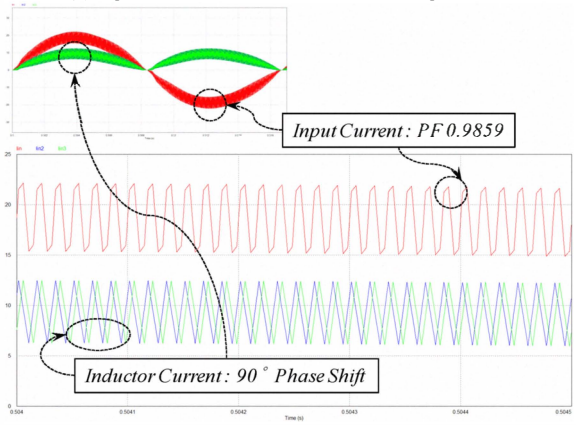


(b) Input voltage, input current and output power (180° Phase Shift)

Figure 9. Simulation of Interleaved PFC



(a) Input current characteristic when 180° phase shift

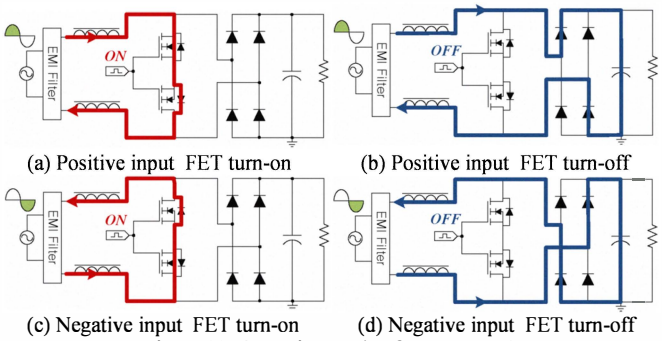


(b) Input current characteristic when 90° phase shift

Figure 10. Input current according to the phase shift angle of Interleaved PFC

C. *Characteristics of BTBBL PFC*

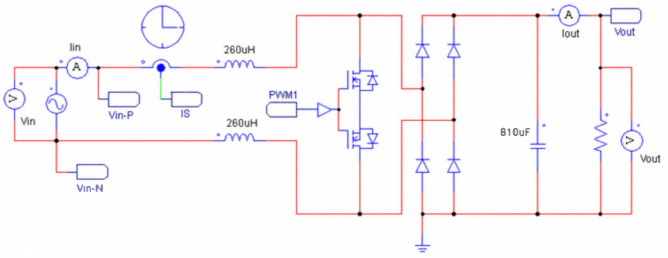
BTBBL PFC is shown as Figure 3(c). BTBBL PFC is topology like bidirectional switch bridgeless boost PFC, dual boost AC switch boost PFC [4-7]. Inductor is directly connected to each line of input. In particular, it is the bridgeless way which does not use bridge diode at all and utilizes the feature that the circulating current on the output side than the circulating current on the input side flows smaller by inductor standard. However, common mode noise is generated largely because there are no connection parts between ground of link voltage on output side and input line [8]. Figure 11 is FET on/off operation flow by input state of BTBBL. Figure 13 is the basic simulation circuit diagram of BTBBL PFC and simulation result waveform.



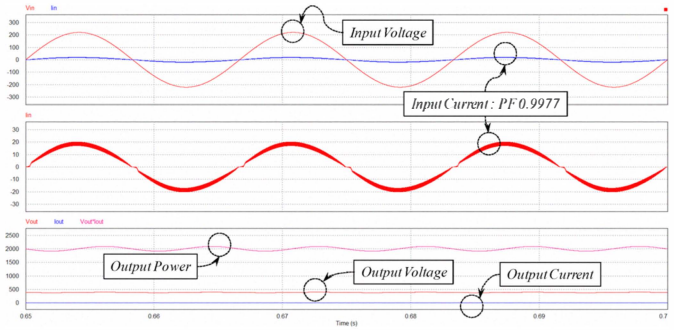
(a) Positive input FET turn-on (b) Positive input FET turn-off

(c) Negative input FET turn-on (d) Negative input FET turn-off

Figure 11. Operating mode of BTBBL PFC



(a) Simulation circuit diagram of BTBBL PFC

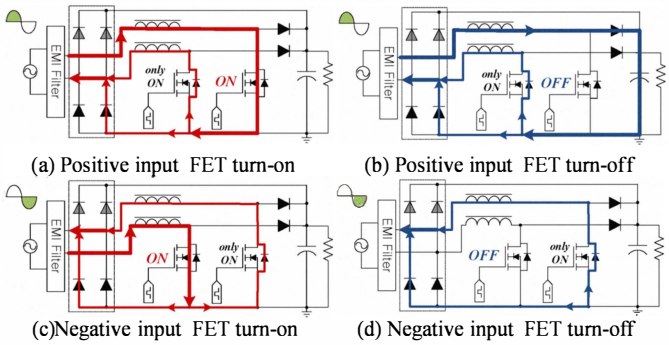


(b) Input voltage, input current and output power

Figure 12. Simulation of BTBBL PFC

D. *Characteristics of SBL PFC*

SBL PFC is shown as figure 3(d) SBL PFC is the most practical structure of bridgeless PFC topologies. In other words, SBL PFC enhances the current cycle paths by utilizing bridge diode located in input line and improves the common mode noise. Only bridge diode operates differently with its role in the ACM PFC [4-6]. In addition, two diodes on common cathode side of bridge diode are used as inrush diode features. Meanwhile SBL PFC is the same parts configuration as Interleaved PFC and is similar to the wiring structure. Interleaved PFC and SBL PFC were produced through simple wiring structure changes by using same PCB, which had been produced actually on this study. Figure 13 is FET on/off operation flow by input state of Interleaved PFC. Figure 14 is the basic simulation circuit diagram of SBL PFC and the simulation waveform. Figure 15 is result measuring the current waveform of each FET when not using bridge diode on the input side. While FET is switching on the positive line FET, FET of negative line is conducted reverse current like switching cycle through the body diode. In addition, circulating current is conducted with all switching cycle sectors of on/off as well as on section.

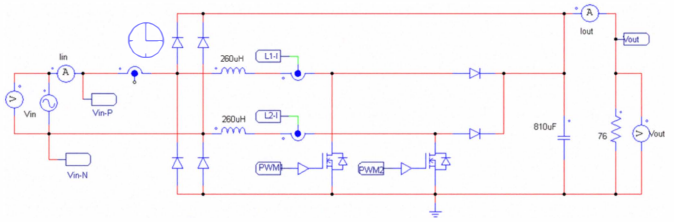


(a) Positive input FET turn-on (b) Positive input FET turn-off

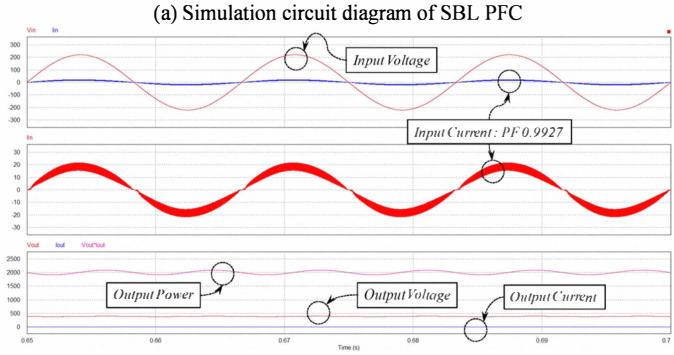
(c)Negative input FET turn-on (d) Negative input FET turn-off

Figure 13. Operating mode of SBL PFC

While, if there is bridge diode, the non-switching current is conducted through body diode of FET in negative line. At that time, the current of switching cycle is conducted in the bridge diode. Currents of body diode and bridge diode flow on the split depending on conduction characteristics of each component and inductor and contribute to efficiency improvement.

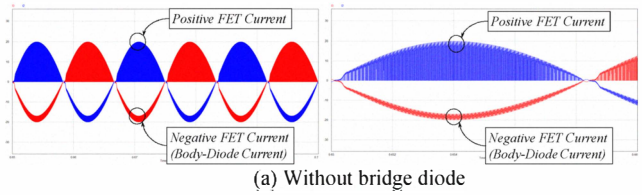


(a) Simulation circuit diagram of SBL PFC

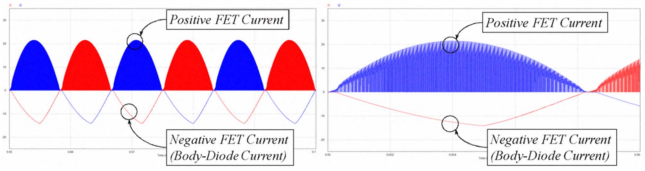


(b) Input voltage, input current and output power

Figure 14. Simulation of SBL PFC



(a) Without bridge diode



(b) With bridge diode

Figure 15. Current characteristics by the presence of bridge diode

IV. DESIGN AND EXPERIMENTAL TEST RESULT

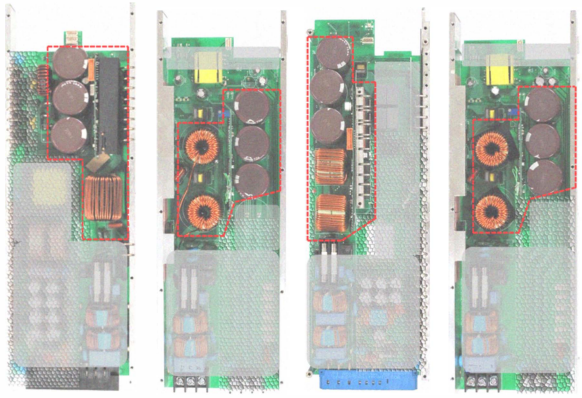
A. *Design Conditions*

The input conditions of prototype were designed based on the universal input voltage. However, 60% range of the maximum output power like general PSU for communication was allowed to be derating within 110VAC range. And the maximum output is capable of designing on more than 180Vac. The external dimension size was designed with 109mm by 41.5mm by 327mm including DC-DC stage. Meanwhile, to evaluate only the performance of PFC topology the parts of DC-DC stage were disconnection.

Figure 16 is an image of the fabricated prototype. Volume of mounting space heat, heat-sink of each PFC was applied equally as possible. IC for dedicated PFC was used as control circuit. ACM PFC and BTBBL PFC needed one PWM was used with UCC2854, Interleaved PFC and SBL PFC required two PWMs was used with UCC28070. FET was also used equally with a series of CoolMOS C6 and diode was used with 600V class silicon carbide diode in the same way. Meanwhile, because BTBBL PFC needs floating gate driver opto-coupler driver circuit isolation possible was applied. Inductor was used the high flux core of metal powders material. Table 2 is the major components lists of power-part device.

TABLE II. DESIGN COMPONENTS

	ACM PFC	Interleaved PFC	BTBBL PFC	SBL PFC
Bridge diode	RBV2506	RBV2506	-	RBV2506
Inductor	340uH	260uH*2	260uH*2	260uH*2
FET	IPW60R070C6	IPW60R070C6	IPW60R070C6	IPW60R070C6
Diode	STPSC1206D	STPSC1206D	STPSC1206D	STPSC1206D
Current transformer	(100:1)	(100:1)*2	ACS714	(100:1)*2
Driver	Direct One Channel	Direct Two Channel	Opto-coupler One Channel	Direct Two Channel
PWM controller	UCC2854	UCC28070	UCC2854	UCC28070



(a) ACM PFC (b) Interleaved PFC (c)BTBBL PFC (d)SBL PFC

Figure 16. Prototypes of four topologies

B. *Experimental result*

Figure 17-20 is voltage measurement waveforms of FET drain-source voltage when each topology outputs 2kwatt. Experimental condition of four topologies is equal. ACM PFC tests waveform of figure 17 can be seen typical average current mode control PFC waveform. Figure 18 is Interleaved PFC test waveforms and ripple of input current like simulation results can be seen little. Figure 19 is a test waveform of BTBBL PFC. Ripple components can be seen large in most input current range. In particular, the largest ripple is identified on input current peak points. Figure 20 is the SBL PFC tests waveform and current ripple has confirmed small next Interleave PFC. There is difference of ripple size and noise ingredients in all topologies, but input current waveform of high power factor improvement performance can be seen.

Figures 21-22 shows the result of the performance comparison tests. The measurement equipment were used with 61505 for input power supply of CHROMA ATE INC., EL-Load PLZ1003WH load in three parallel for output electronic load of KIKUSUI ELECTRONICS CORP., and WT1600 for power meter of Yokogawa Electric Corp. Measurement conditions are input 220Vac, output 390Vdc, load step

100watt, maximum output 2kwatt and switching frequency is 60 kHz.

Figure 21 is a comparison graph of the efficiency results. Measurement result is that the highest efficiency of ACM PFC is 97.89% in 900watt and Interleaved PFC is 97.80% in the 1500watt. BTBBL PFC was 97.90%, in a 700watt and SBL PFC was 98.14% in the 1300watt. At that time, Interleaved PFC was measured with lower efficiency result than ACM PFC in load interval to less than approximately 1600watt. And in case of BTBBL PFC, efficiency decline is large in more load than about 900watt. Meanwhile, the efficiency of SBL PFC was measured with the highest efficient performance in all load segments. Especially in approximately 30-80% load area, efficiency of over 98% was measured and range of efficiency was measured with the smallest. SBL PFC also has the highest average efficiency. In the graph of Figure 22, power factor result of ACM PFC and SBL PFC is the highest and the difference is less than the measurement error range. Meanwhile, wide of change in BTBBL PFC power factor is the biggest.

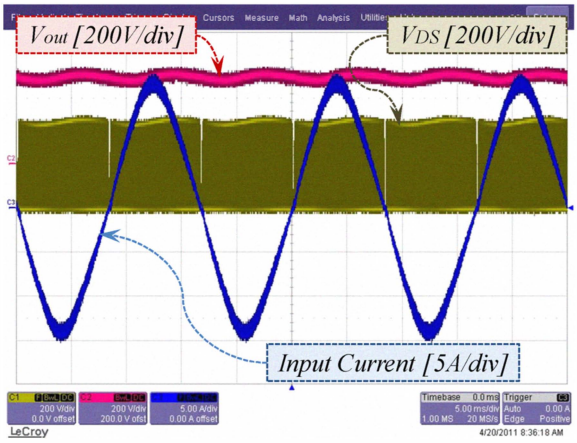


Figure 17. Experimental waveform of ACM PFC

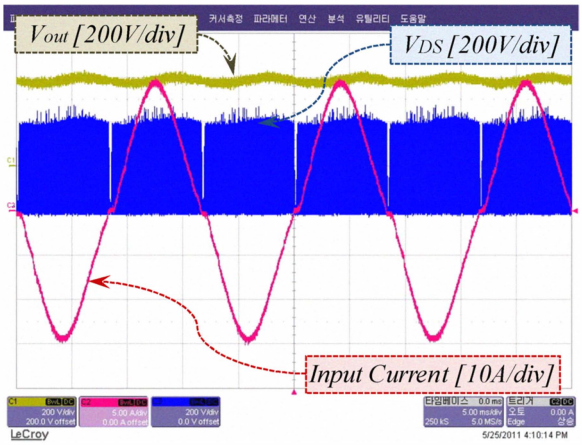


Figure 18. Experimental waveform of Interleaved PFC

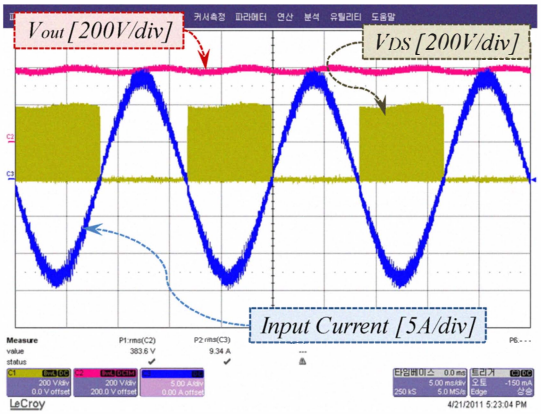


Figure 19. Experimental waveform of BTBBL PFC

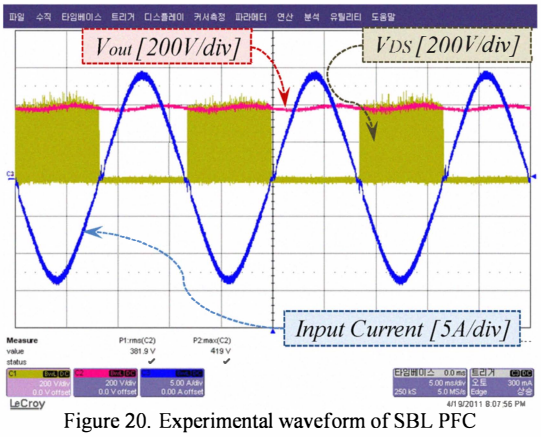


Figure 20. Experimental waveform of SBL PFC

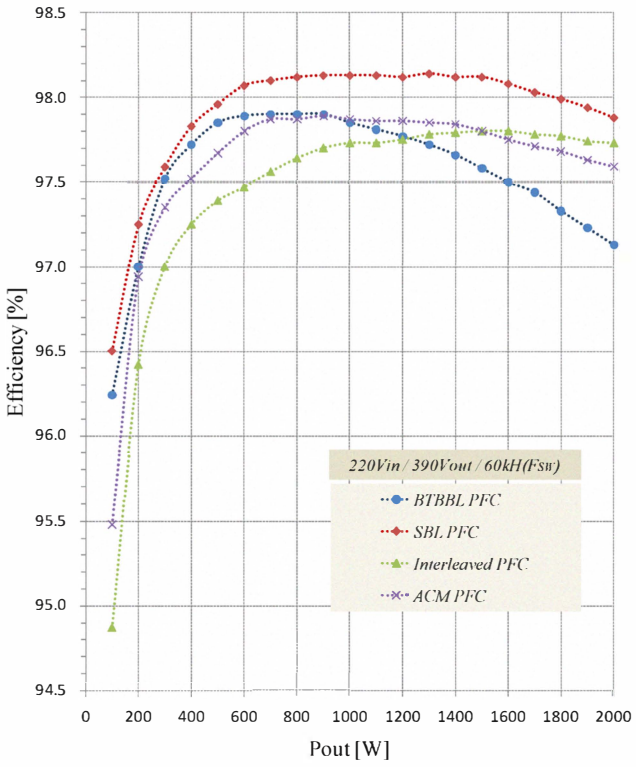


Figure 21. Efficiency result

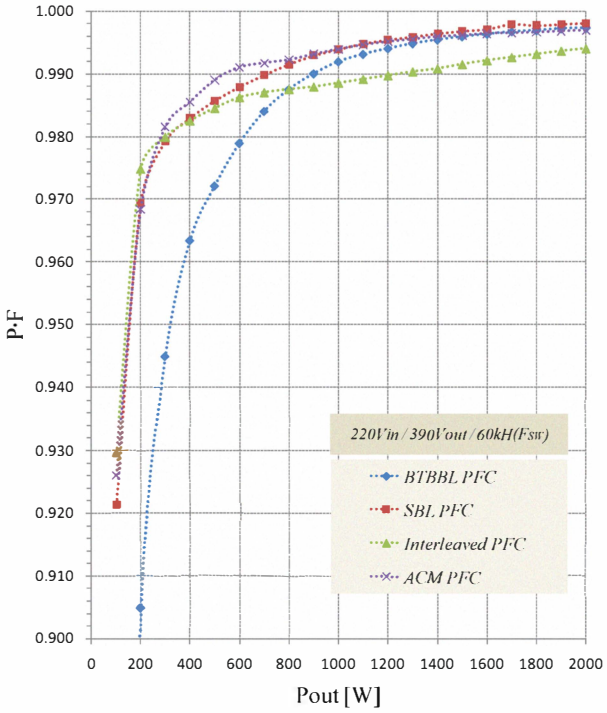


Figure 22. PFC result

TABLE III. EXPERIMENTAL RESULT OF ALL TOPOLOGIES

	ACM PFC	Interleaved PFC	BTBBL PFC	SBL PFC
Average efficiency	**97.59%**	97.43%	97.54%	**97.91%**
Peak efficiency	97.89%	97.80%	**97.90%**	**98.14%**
Average P·F	**0.9886**	0.9852	0.9706	**0.9881**
Over P·F 0.99	600watt	1300watt	900watt	800watt
Over P·F 0.98	300watt	400watt	700watt	400watt

V. SUMMARY

Efficiency performance was measured on ACM PFC approximately 96.48% at 10% light loads, over 97.89% over medium loads. Efficiency performance of ACM PFC is high secondly and PFC performance is the highest. PFC performance over 0.99 was measured over 30% load interval.

As a simulation results, Interleaved PFC made sure that ripple performance varies depending on the phase shift angle. Actually as test results of 180 degree phase shift, the smallest input current ripple characteristics can be confirmed among four types of topologies. However, efficiency and power factor performance are the lowest.

BTBBT PFC has the lowest input current ripple characteristics. And in the load segment more than about 40%, there is characteristic that the range of efficiency decline is large. In addition, full-load efficiency is the lowest.

SBL PFC was excellent Input current ripple characteristics next Interleaved PFC. Besides the highest efficiency performance was measured in all loads range, efficiency of 98% was measured over 30% load. Power factor characteristics were similar to ACM PFC.

In this paper, four high-performance topologies for PFC were design and compared. As an experiment result of this study, SBL PFC average efficiency has improved 0.32% compared to ACM PFC and PFC has enhanced 0.0005. Considering measurement error, it is judged that PFC has the same average performance. While, average performance of Interleaved PFC and BTBBL PFC were low compared to ACM PFC. In the future, conditions of various input and output voltage and switching frequency will be conducted for the evaluation.

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