Electrical Power and Energy Systems 104 (2019) 230–245

Contents lists available at ScienceDirect

Electrical Power and Energy Systems

journal homepage: www.elsevier.com/locate/ijepes

Simultaneous control and protection schemes for DC multi microgrids systems☆

Ali Abdali, Reza Noroozian*, Kazem Mazlumi

Department of Electrical Engineering, Faculty of Engineering, University of Zanjan, P.O. Box 45371-38791, Zanjan, Iran

ARTICLE INFO

Keywords:
DC microgrid (DCμG)
Hysteresis Current Control (HCC)
Fault detection
Fuzzy inference system (FIS)
Distributed generation (DG)

ABSTRACT

This paper proposes a novel simultaneous control interface and protection scheme for DC microgrids (DCμG) interconnected systems, although the interconnections could be possible via two power electronic systems such as DC/DC converter. Each DCμG presented in this paper is supplied by AC grid as well as battery bank unit, distributed generation (DG) unit and AC load unit. The proposed control interface is based on a developed suitable small signal model for each DCμG that provides proper power flow control and cancellation of interactions between DCμG. Also, the presented protection scheme for fast fault detection in DC link is based on fuzzy inference system (FIS), so that faults could be detected as quickly as possible in few milliseconds. In fact, the aim of this paper is simultaneous protection and control interface for DC multi microgrids, so that the performance of the controller and protection system is separate, yet integrated together. As such, DC multi microgrid performance under different events, such as change in active power of DGs and short circuit is not in trouble and disorder. Simulation results indicate the remarkable effectiveness of the proposed control interface and protection scheme for DCμG interconnected systems. For validation of the capability and feasibility of FIS fault detection scheme, simulated network and protection algorithm are implemented in laboratory-scale. The implementation results demonstrate that FIS protection scheme can swiftly detect faults within a few milliseconds.

1. Introduction

The interest in distributed resource systems including distributed generation (DG) and energy storage resources is increasing due to technical, economical, reliability and environmental merits. Local aggregation of distributed resources and electrical loads results in a microgrid (μG) [1,2]. Microgrid systems are small-scale power grids that consist of renewable energy resources and loads [3–5].

In order to meet energy, reliability, power quality, power back-up and peak shaving and to allow sharing of resources within a common infrastructure, multiple microgrids are interconnected thus providing a power park [6]. The DC microgrids (DCμGs) concept and consequently, DC power parks have provided a new paradigm for future power distribution systems. This is due to the fact that modern DG systems (e.g., fuel cells, micro-turbines, photovoltaic arrays and wind power systems), storage systems (e.g., batteries, supercapacitors, and flywheels) and modern electrical loads (e.g., sensitive loads, electronic loads and AC drives) have DC link stages for interconnection to the AC distribution network. As a result, DCμGs provide the best solution for integrating the DC link stages of these devices. In [7], control and load-dispatching strategies for a microgrid with a DC/AC inverter was proposed. Also in [8,9], mathematical modeling of DC microgrid using SM hysteresis controller and hierarchical microgrid control were presented, respectively.

In [10–12], it has been shown that DCμGs are preferable to both power frequency and high-frequency AC microgrids from technical, economical and reliability viewpoints. In [12–14], several DCμG configurations are investigated based on small signal modeling. However, an acceptable small signal model for DCμGs which can effectively represent the dynamic performance of the original system has not been developed. In this paper, detailed, small signal and steady-state models of the investigated DCμG including DC/DC interconnection converter are developed. In this scheme, a DC/DC converter is used for the interconnection of two DCμGs. The main objective of this paper is to develop suitable control interfaces for both interconnection systems that can provide proper power flow control and cancellation of interactions between the DCμGs.

The advantage of AC microgrids is the possibility of using DG sources directly which are based on AC voltages; however, synchronization, reactive power control, and voltage stability are among their

☆ This work was supported by the University of Zanjan.

* Corresponding author.
E-mail addresses: ali_abdali@znu.ac.ir (A. Abdali), noroozian@znu.ac.ir (R. Noroozian), kmazlumi@znu.ac.ir (K. Mazlumi).

https://doi.org/10.1016/j.ijepes.2018.06.054
Received 4 June 2017; Received in revised form 11 March 2018; Accepted 27 June 2018
Available online 13 July 2018

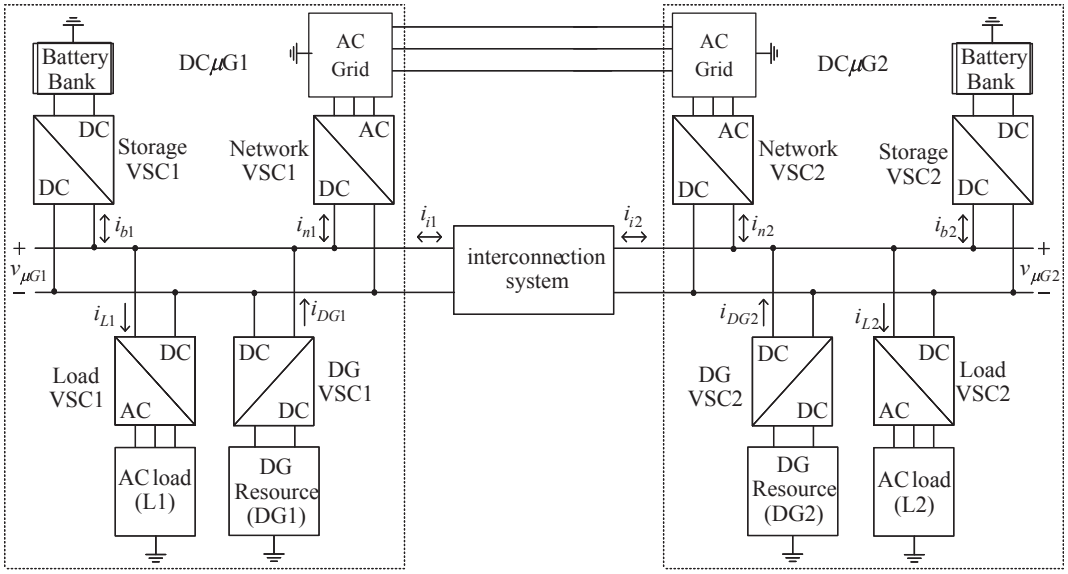

Fig. 1. The general structure of a DCμG and DC power park.

drawbacks. Nevertheless, DC microgrids are considered to be a feasible solution since they are small grids with fewer transmission losses. Furthermore, they lack the defects of AC systems, and the size of AC-DC-AC converters used may be significantly reduced [6]. Notwithstanding its remarkable privileges, the protection of DC microgrids is challenging and in addition, there is no published standard, guidance or experience in this regard [15]. In the distribution system, the ability to accurate fault detection has the benefits of quick repair and restoration which reduces the electricity outage time [16]. The presence of power electronic devices controls current to a certain extent during fault conditions which in turn makes fault detection difficult [16,17].

Various fault protection solutions have been proposed for LVDC distributed systems including overcurrent protection [15,18,19], derivatives of current [15], under-voltage and directional protection [18]. However, the dynamics of voltage and current were not considered, and this method leads to an unnecessary outage of sources and loads in DC microgrids. It is worth noting that [20,21] have investigated the classical and conventional protection methods such as overcurrent protection, which due to microgrids instantaneous and continuous changes are not applicable, thus novel methods and algorithms should be applied. Also, M. Shahidehpour et al. [22] demonstrated that hierarchical protection method and local differential protection method are more effective protection methods for the microgrids. The hierarchical protection has advantage for wide area protection but in contrast to the microgrid changes such as short-circuit levels changes under different situations, it is inefficient. Although differential protection is robust against microgrids changes, there are problems which will be discussed subsequently.

In [23], an event-based protection scheme for a multi-terminal hybrid DC power system was proposed. Also, in [24], a non-unit protection scheme for DC microgrid based on local measurements was presented. The time of fault detection of these proposed protection schemes is close to one hundred of milliseconds, which is not appropriate for a DCμGs system.

In [25], high-speed differential protection for radial DCμGs distribution systems based on natural characteristics of second derivatives DC differential current measurements was proposed. If this scheme is implemented on the multi-DCμGs, it causes increase in the time of fault detection. In addition, a differential method of fault detection and isolation in LVDC ring-bus microgrids was proposed in [26]. This method used a specific threshold for fault detection. The fault detection speed is dependent on the time window and protection algorithm chosen. The problem of differential protection in DCμGs is the difficulty in choosing the thresholds. However, the time of fault detection of differential method is totally dependent on the choice of the threshold value. An increase in the threshold value increases the time of fault detection, which causes increase in the time of fault detection. This value is determined based on the operators' experience; that is, the defect of protection method is based on human actions and consideration and not intelligence. The aim of the present research is to provide a scheme in which human actions and considerations would not affect fault detection. Therefore, a fast fault detection method using fuzzy inference system (FIS) is presented.

In the rest of the paper, DCμGs modelling is presented in Section 2. In Section 3, the interconnection systems for DCμGs is studied. In Section 4, the proposed control interface for VSCs in interconnection system is investigated. The proposed fault detection method for DC multi microgrids based on FIS is presented in Section 5. Simulation results is noted in Section 6. FIS protection is implemented and tested in a laboratory-scale to assess the enforceability and feasibility of the proposed algorithm in Section 7. The supplementary points and validation of the laboratory prototype implementation, as well as the considerations of the real scale prototype implementation are stated in Section 8.

2. DCμG modeling

The general structure of a DCμG is presented in Fig. 1. All DCμG converters are Voltage Source Converter (VSC). The DCμG has a lossless DC bus structure formed by using a common capacitive terminal for its VSCs. Thus, the DCμG voltage should be maintained within specified limits to ensure the stable and continuous operation of the VSC systems [10–14]. The AC distribution network (i.e., AC grid), distributed resource and load are connected to the inductive terminals of the VSCs.

The controllers of the network VSC and the storage VSC employ DC voltage droop regulator in order to maintain the DCμG voltage within specified limits as required by the VSCs, because this is the only common signal for power balancing in DC bus [11–13]. The characteristic of DC voltage droop is generally expressed by the reference power as a droop function of the DCμG voltage. Therefore, the power regulation modules for network VSC and storage VSC incorporate instantaneous power regulation based on droop controller.

The DG VSC controller regulates the DG active power to meet its technical and economical requirements which usually consider DG

maximum/optimum power/efficiency constraints [11,13]. In renewable sources, the main purpose of power management strategies is to utilize the maximum power according to source availability. In non-renewable sources, the active power management strategies consider various criteria such as maximum efficiency conditions. The load VSC can be controlled by voltage-frequency control strategy, which regulates the voltage and the frequency of AC load. This converter has no loop to regulate the DC bus voltage [10–14]. Therefore, the load VSC has a load voltage regulator module in order to control the load supply voltage. The active powers of the DG VSC and the load VSC are independent of DC bus voltage changes. The network and storage VSCs connected in parallel, can be modeled by current sources controlled by a DCμG voltage signal. Furthermore, the power reference for bidirectional network and storage VSCs is provided by DC voltage regulator. During islanding operation, the voltage regulation is achieved by the energy storage system. The control strategy of network and storage VSCs is based on feedback from the DCμG voltage and the reference value for the DC bus voltage. If the DC bus voltage is low, thus the power should be injected to the DC bus by the storage system or the AC grid. If the DC bus voltage is high, the addition power in DC bus must recharge the battery and in the case of redundancy, the power should be returned to AC grid. As it can be seen in Fig. 2, we have:

$$I_n(s) + I_b(s) - C_{dc} s V_{\mu G}(s) = I_L(s) - I_{DG}(s) \tag{1}$$

$$I_n(s) = \frac{V_{refn}(s) - \frac{\omega_{lp}}{s+\omega_{lp}} V_{\mu G}(s)}{R_n} \tag{2}$$

$$I_b(s) = \frac{V_{refb}(s) - \frac{\omega_{lp}}{s+\omega_{lp}} V_{\mu G}(s)}{R_b} \tag{3}$$

where I_n and I_b are the output currents of the network and storage VSCs, respectively. C_{dc} is the total equivalent capacitance of converters connected to the DC bus. V_{refn} and R_n are DC reference voltage and the equivalent resistance of the network VSC, respectively. V_{refb} and R_b are DC reference voltage and the equivalent resistance of the storage VSC, respectively. ω_{lp} is the break-over frequency of the low pass filter (LPF in Fig. 2(a)). Using equations (1), (2) and (3), we have:

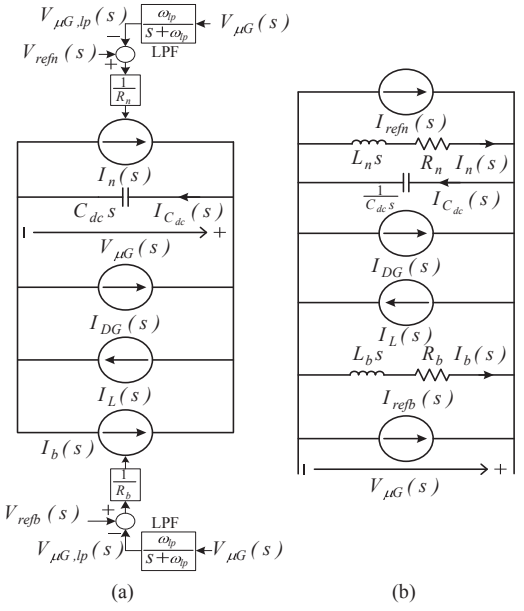

Fig. 2. (a) DC side dynamic model, (b) Developed small signal model for DCμG.

$$V_{\mu G}(s) = \frac{\frac{1}{R_n C_{dc}}(s+\omega_{lp})}{s^2 + \omega_{lp} s + \frac{(R_n+R_b)\omega_{lp}}{R_n R_b C_{dc}}} V_{refn}(s) + \frac{\frac{1}{R_b C_{dc}}(s+\omega_{lp})}{s^2 + \omega_{lp} s + \frac{(R_n+R_b)\omega_{lp}}{R_n R_b C_{dc}}} V_{refb}(s) + \frac{\frac{1}{C_{dc}}(s+\omega_{lp})}{s^2 + \omega_{lp} s + \frac{(R_n+R_b)\omega_{lp}}{R_n R_b C_{dc}}} (I_{DG}(s) - I_L(s)) \tag{4}$$

The characteristic equation of the closed loop transfer function is the following equation:

$$p(s) = s^2 + \omega_{lp} s + \frac{(R_n + R_b)\omega_{lp}}{R_n R_b C_{dc}} \tag{5}$$

The desired characteristic equation can be expressed as:

$$p(s) = s^2 + 2\zeta_n \omega_n s + \omega_n^2 \tag{6}$$

where ζ_n and ω_n are, the desired closed loop damping and bandwidth, respectively. The value of DC bus equivalent capacitors determines the performance of the DC voltage control system. The total required DC bus capacitor (C_{dc}) can be determined by using equations (5) and (6):

$$C_{dc} = \frac{(R_n + R_b) 4\zeta_n^2}{R_n R_b \omega_{lp}} \tag{7}$$

In order to develop a simple electrical circuit representing the small signal model for the DCμG, we define:

$$I_n(s) = \frac{V_{refn}(s)}{R_n} - \frac{1}{\frac{R_n}{\omega_{lp}} s + R_n} V_{\mu G}(s) = I_{refn}(s) - \frac{1}{L_n s + R_n} V_{\mu G}(s) \tag{8}$$

$$I_b(s) = \frac{V_{refb}(s)}{R_b} - \frac{1}{\frac{R_b}{\omega_{lp}} s + R_b} V_{\mu G1}(s) = I_{refb}(s) - \frac{1}{L_b s + R_b} V_{\mu G}(s) \tag{9}$$

Substituting equations (8) and (9) in equation (1), a novel DCμG small signal model is developed shown in Fig. 2(b). The aforementioned equations can be written for the steady state condition as:

$$I_n + I_b = I_L - I_{DG} \tag{10}$$

$$I_n = \frac{V_{refn} - V_{\mu G}}{R_n} \tag{11}$$

$$I_b = \frac{V_{refb} - V_{\mu G}}{R_b} \tag{12}$$

Substituting equations (11) and (12) in equation (10), we have:

$$V_{\mu G} = \frac{R_b V_{refn} + R_n V_{refb} + R_b R_n (I_L - I_{DG})}{R_n + R_b} \tag{13}$$

For steady-state, active power related to the network and storage VSCs, P_n and P_b, we have:

$$P_n = V_{\mu G} I_n = \frac{V_{\mu G}(V_{refn} - V_{\mu G})}{R_n} \tag{14}$$

$$P_b = V_{\mu G} I_b = \frac{V_{\mu G}(V_{refb} - V_{\mu G})}{R_b} \tag{15}$$

Using equations (13) and (11), we have:

$$I_n = \frac{R_b (I_L - I_{DG})}{R_n + R_b} + \frac{V_{refn} - V_{refb}}{R_n + R_b} \tag{16}$$

Using equations (13) and (12), we obtain:

$$I_b = \frac{R_n (I_L - I_{DG})}{R_n + R_b} - \frac{V_{refn} - V_{refb}}{R_n + R_b} \tag{17}$$

In order to prevent circulating currents between the network VSC and the storage VSC, we have:

$$V_{refn} = V_{refb} = V_{ref\mu G} \tag{18}$$

where $V_{ref\mu G}$ is the reference DCμG voltage. The DCμG voltage droop,

$\delta_{\mu G}$, can be defined as follows:

$$\delta_{\mu G} = \frac{V_{refn} - V_{\mu G}}{V_{refn}} = \frac{V_{refb} - V_{\mu G}}{V_{refb}} \tag{19}$$

The equations (14) and (15) can be rewritten in the following form:

$$P_n = \frac{\delta_{\mu G}(1-\delta_{\mu G})V_{refn}^2}{R_n} \tag{20}$$

$$P_b = \frac{\delta_{\mu G}(1-\delta_{\mu G})V_{refb}^2}{R_b} \tag{21}$$

The DCμG droop coefficient is selected to obtain an acceptable DCμG voltage droop at rated power operation. At rated power conditions, equations (20) and (21) can be rewritten as follows:

$$P_{n,rated} = \frac{\delta_{\mu G,n}(1-\delta_{\mu G,n})V_{refn}^2}{R_n} \tag{22}$$

$$P_{b,rated} = \frac{\delta_{\mu G,n}(1-\delta_{\mu G,n})V_{refb}^2}{R_b} \tag{23}$$

$$R_n = \frac{\delta_{\mu G,n}(1-\delta_{\mu G,n})V_{refn}^2}{P_{n,rated}} \tag{24}$$

$$R_b = \frac{\delta_{\mu G,n}(1-\delta_{\mu G,n})V_{refb}^2}{P_{b,rated}} \tag{25}$$

where $\delta_{\mu G,n}$ is the nominal DCμG voltage droop, $P_{n,rated}$ is the rated power of the network VSC, and $P_{b,rated}$ is the rated power of the storage VSC. Using equations (7), (18), (24) and (25), we have:

$$C_{dc} = \frac{2\zeta_n^2(P_{b,rated} + P_{n,rated})}{\omega_{lp}\delta_{\mu G,n}(1-\delta_{\mu G,n})V_{ref\mu G}^2} \tag{26}$$

Using equations (26), the design of DC bus equivalent capacitors depends on the DC voltage control system and the power related to the network and storage VSCs, since a high-performance DC voltage control system leads to a reduction of the DC bus voltage ripple and increases the system stability. Since the power reference for network and storage VSCs are provided by DC voltage regulator, the load power and DG power swings have influence on DCμG voltage. Therefore, the value of DC bus equivalent capacitor is dependent on the parameters only related to the network VSC and storage VSC.

3. Interconnection systems for DCμGs

Fig. 1 shows the DC power park which has been studied in this paper. The DC power park in Fig. 1 includes DCμG1 and DCμG2 which have the general structure of DCμG. Considering technical and controller design issues, VSC system is preferable to current source converters. Thus, the interconnection system in Fig. 1 incorporates one VSC topology as DC/DC interconnection converter. The distance between DCμG1 and DCμG2 is neglected. DC/DC interconnection system would be presented in the following.

According to Fig. 2, the dynamic model of the DC power park shown in Fig. 1 is derived and depicted in Fig. 3. The interconnection system can be modeled by controlled current sources, I_i, by DCμGs voltages signal. In addition, the power reference regulator for bidirectional interconnections VSC is controlled by power management system. In Fig. 3, we have:

$$I_{n1}(s) + I_{b1}(s) - C_{dc1}sV_{\mu G1}(s) = I_{L1}(s) + I_i(s) - I_{DG1}(s) \tag{27}$$

$$I_{n2}(s) + I_{b2}(s) - C_{dc2}sV_{\mu G2}(s) = I_{L2}(s) - I_i(s) - I_{DG2}(s) \tag{28}$$

$$I_{n1}(s) = \frac{V_{refn1}(s) - \frac{\omega_{lp}}{s+\omega_{lp}}V_{\mu G1}(s)}{R_{n1}} \tag{29}$$

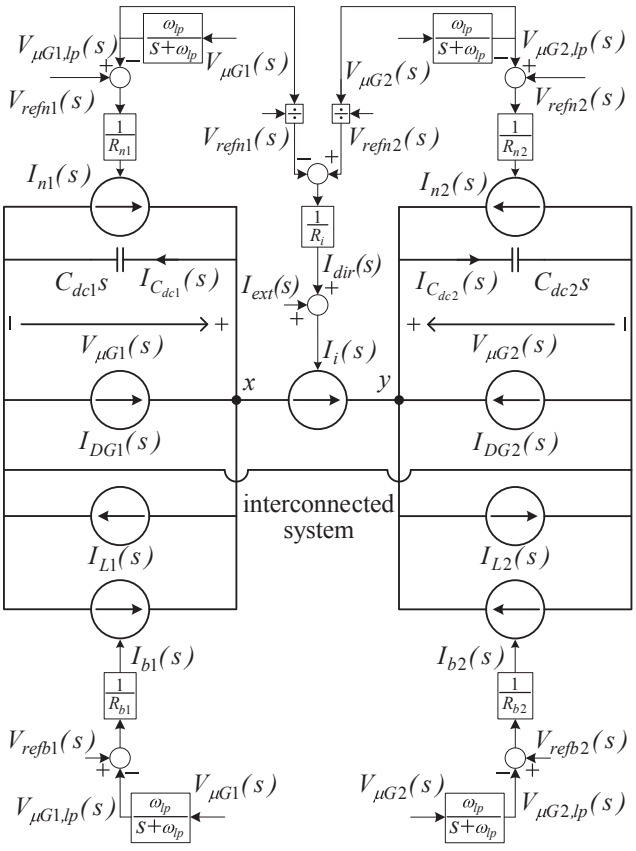

Fig. 3. DC side dynamic model.

$$I_{b1}(s) = \frac{V_{refb1}(s) - \frac{\omega_{lp}}{s+\omega_{lp}}V_{\mu G1}(s)}{R_{b1}} \tag{30}$$

$$I_{n2}(s) = \frac{V_{refn2}(s) - \frac{\omega_{lp}}{s+\omega_{lp}}V_{\mu G2}(s)}{R_{n2}} \tag{31}$$

$$I_{b2}(s) = \frac{V_{refb2}(s) - \frac{\omega_{lp}}{s+\omega_{lp}}V_{\mu G2}(s)}{R_{b2}} \tag{32}$$

Considering equations (27)–(32), the DCμG voltage $V_{\mu G1}$, the DCμG voltage $V_{\mu G2}$ can be obtained as follows:

$$\begin{aligned} V_{\mu G1}(s) = {} & \frac{\frac{1}{R_{n1}C_{dc1}}(s+\omega_{lp})}{s^2 + \omega_{lp}s + \frac{(R_{n1}+R_{b1})\omega_{lp}}{R_{n1}R_{b1}C_{dc}}}V_{refn1}(s) \\ & + \frac{\frac{1}{R_{b1}C_{dc1}}(s+\omega_{lp})}{s^2 + \omega_{lp}s + \frac{(R_{n1}+R_{b1})\omega_{lp}}{R_{n1}R_{b1}C_{dc1}}}V_{refb1}(s) \\ & + \frac{\frac{1}{C_{dc1}}(s+\omega_{lp})}{s^2 + \omega_{lp}s + \frac{(R_{n1}+R_{b1})\omega_{lp}}{R_{n1}R_{b1}C_{dc1}}}(I_{DG1}(s) - I_{L1}(s) - I_i(s)) \end{aligned} \tag{33}$$

$$\begin{aligned} V_{\mu G2}(s) = {} & \frac{\frac{1}{R_{n2}C_{dc2}}(s+\omega_{lp})}{s^2 + \omega_{lp}s + \frac{(R_{n2}+R_{b2})\omega_{lp}}{R_{n2}R_{b2}C_{dc}}}V_{refn2}(s) \\ & + \frac{\frac{1}{R_{b2}C_{dc2}}(s+\omega_{lp})}{s^2 + \omega_{lp}s + \frac{(R_{n1}+R_{b1})\omega_{lp}}{R_{n2}R_{b2}C_{dc2}}}V_{refb2}(s) \\ & + \frac{\frac{1}{C_{dc2}}(s+\omega_{lp})}{s^2 + \omega_{lp}s + \frac{(R_{n2}+R_{b2})\omega_{lp}}{R_{n2}R_{b2}C_{dc2}}}(I_{DG2}(s) - I_{L2}(s) + I_i(s)) \end{aligned} \tag{34}$$

The aforementioned equations can be written for the steady state

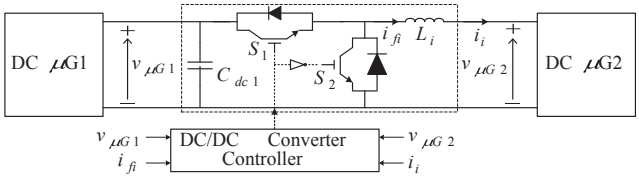

Fig. 4. DC/DC interconnection converter structure.

condition as:

$$V_{\mu G1} = \frac{R_{b1}V_{refn1} + R_{n1}V_{refb1}}{R_{n1} + R_{b1}} + \frac{R_{b1}R_{n1}(I_{DG1} - I_{L1} - I_i)}{R_{n1} + R_{b1}} \quad (35)$$

$$V_{\mu G2} = \frac{R_{b2}V_{refn2} + R_{n2}V_{refb2}}{R_{n2} + R_{b2}} + \frac{R_{b2}R_{n2}(I_{DG2} - I_{L2} + I_i)}{R_{n2} + R_{b2}} \quad (36)$$

The resistive voltage droop, R_i for the DC/DC VSC, can be obtained from the Thevenin equivalent circuit across terminals x and y in Fig. 3 as follows:

$$R_i = \frac{R_{b1}R_{n1}(R_{b2} + R_{n2}) + (R_{b1} + R_{n1})R_{b2}R_{n2}}{(R_{b1} + R_{n1})(R_{b2} + R_{n2})} \quad (37)$$

Droop characteristics of the network VSC and storage VSC for each microgrid (R_{n1}, R_{b1}, R_{n2} and R_{b2}) is obtained by using equations (24) and (25), respectively.

3.1. Interconnection systems configuration

Fig. 4 illustrates the DC/DC interconnection converter structure proposed for the interconnection system of Fig. 1. The DC/DC interconnection converter is a one leg DC/DC VSC with IGBT switches. Considering the technical notes of VSCs, the DC/DC interconnection converter can technically be implemented and controlled by an interconnected system of two DCμGs with different DC voltage levels. DCμG1 is assumed to have a higher DC voltage level than DCμG2. Thus, DCμG2 is connected to the inductive terminal of the DC/DC interconnection converter.

4. Proposed control interface for VSCs in interconnection system

Considering technical and economic issues which are generally considered in the interconnection of electric power systems, the following objectives are assumed for the design of suitable control interface for VSCs of DC/DC interconnection:

- Proper regulation of active power flow between DCμGs
- Cancellation of interactions between DCμGs

The first objective is set in order to make the active power transfer between the DCμGs follow a scheduled reference value. The second objective is set in order to cancel the effects caused by DG resources and loads in each DCμG on the other DCμG resulting in decoupled and independent operation of the DCμGs. Control interfaces of the interconnection VSCs should have a fast dynamic response in order to properly regulate the power flow between the DCμGs. Consequently, the controllers of the interconnection VSCs should have the following characteristics in order to achieve the above-mentioned objectives:

- Fast dynamic response
- Insensitivity to system parameters variations

The controllers of the VSCs in DC/DC interconnection structure shown in Fig. 4 are designed as power regulators in this paper. The power regulator of a VSC includes the current calculator and the Pulse Width Modulation (PWM) system. The reference power is the input to the current calculator and the current calculator specifies the reference current for the closed-loop PWM system. For each VSC in the interconnected system, an instantaneous power based on the current calculator and a Hysteresis Current Control (HCC) PWM scheme are proposed. HCC has the following particular advantages [27]:

- HCC is the simplest PWM system.
- HCC has an excellent dynamic performance.
- HCC is insensitive to system parameters variations.

Instantaneous power based on the current calculator has the following advantages [28]:

- Instantaneous power based on the current calculator has much faster dynamic response than average power-based methods.
- Instantaneous power based on the current calculator does not reflect the disturbances of the VSC inductive terminal to its capacitive terminal.

As it can be seen, the proposed power regulator provides fast dynamic response and decoupled operation of the subsystems at the capacitive and inductive sides of DC/DC VSCs. As a result, the proposed power regulator is the simplest system which satisfies the required characteristics for DC/DC VSC controllers in the interconnection system of DCμGs.

The small signal model of the DC/DC interconnection converter is shown in Fig. 5(a). This converter is represented by a current source, i_{fi}^{ref}. The DC/DC converter manages the amount of the current transferred between of the DCμGs. In Fig. 5(a), input signals of the converter controller are DCμG1 voltage $v_{\mu G1}$, output current i_i, output currents for this converter i_{fi}, DCμG2 voltage $v_{\mu G2}$. L_i is the inductive terminal inductor. Fig. 5(b) shows the proposed power regulator scheme for DC/DC interconnection converter in this paper. In Fig. 5(b), the power flow direction can be set in two ways. One way is to set the direction so that only one direction is allowed (i_{dir}). The other way is by specifying the minimum and maximum power transfer limits (P_{ext}). The reference current for the power transfer is indicated by i_{ext}. For normal operation, the power direction is set to flow from the higher to the lower (relative to the reference) voltage level. Because load power and DG power swings in each microgrid have influence for DCμG voltage. This would cause a change of reference power direction by using the resistive voltage droop, R_i of the converter stage. In this paper, the following equation is proposed for instantaneous power based on current calculator of DC/DC interconnection converter:

$$i_{fi}^{ref} = i_{dir} + i_{ext} = \frac{(v_{\mu G1,pu} - v_{\mu G2,pu})}{R_i} \pm \frac{P_{ext}}{V_{refn2}} \quad (38)$$

It must be noted that i_{fi}^{ref} and i_{fi} are the inputs of the two-level hysteresis comparator of the HCC system. The switching frequency of HCC systems is variable. Thus, the maximum switching frequency of the VSCs with HCC should be limited to an acceptable value. This issue is considered in the design of the inductor L_i in Fig. 6. Fig. 6 shows the current and voltage waveforms for DC/DC VSC with HCC. The current i_{fi} tends to cross the lower hysteresis band, where the IGBT S_1 is switched on. The rising current (i_{fi}^{+}) then touches the upper band, where the IGBT S_2 is switched on. h is fixed hysteresis band. Neglecting the resistance, the following equations can be written in switching intervals t_1 and t_2, respectively.

$$\frac{di_{fi}^{+}}{dt} = \frac{(v_{\mu G1} - v_{\mu G2})}{L_i} \quad (39)$$

$$\frac{di_{fi}^{-}}{dt} = -\frac{v_{\mu G2}}{L_i} \quad (40)$$

From the geometry of Fig. 6, we can write:

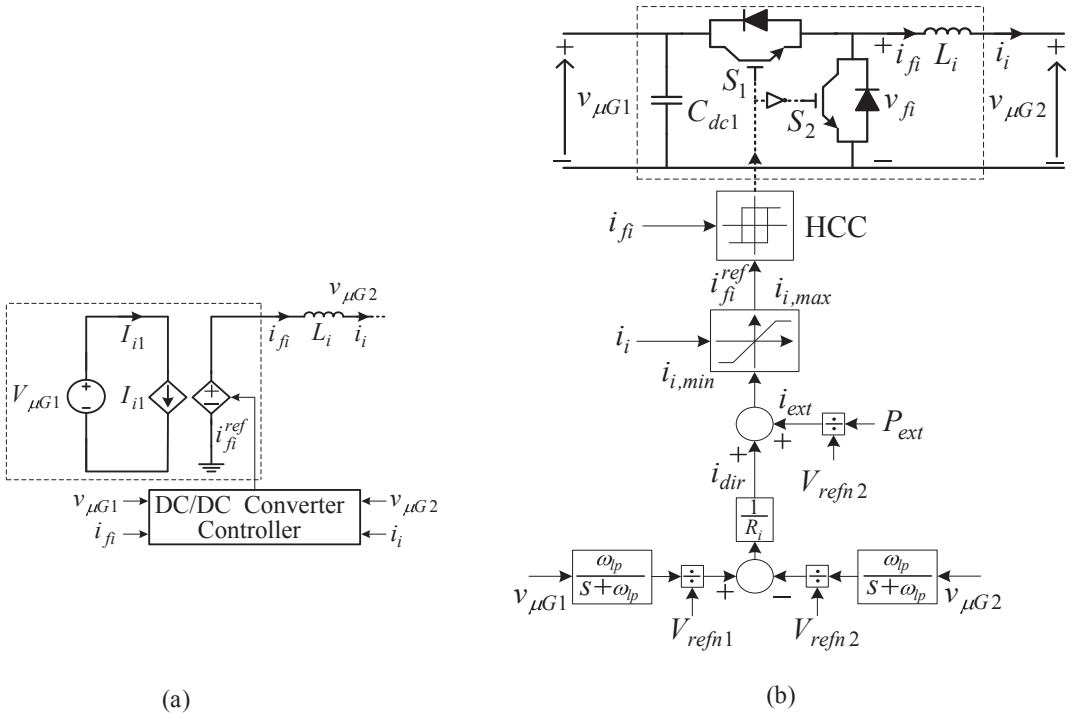

Fig. 5. Small signal model of DC/DC interconnection converter (a) Control interface scheme of DC/DC interconnection converter (b).

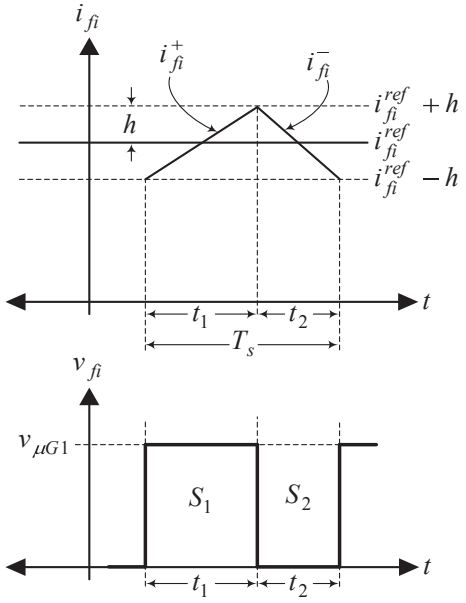

Fig. 6. Current and voltage waveforms with HCC.

$$\frac{d(i_{fi}^{+}-i_{fi}^{ref})}{dt}.\ t_1 = 2h \tag{41}$$

$$\frac{d(i_{fi}^{-}-i_{fi}^{ref})}{dt}.\ t_2 = -2h \tag{42}$$

$$t_1 + t_2 = T_s = \frac{1}{f_s} \tag{43}$$

where f_s is the switching frequency. Using equations (39) to (43), the following equation is obtained according to the HCC concept:

$$h = \frac{v_{\mu G1}}{4L_i f_s} \tag{44}$$

The maximum switching frequency is obtained by $v_{\mu G1} = V_{\mu G1,\max}$ in equation (44) as follows:

$$f_{s,\max} = \frac{V_{\mu G1,\max}}{4L_i h} \tag{45}$$

where $f_{s,\max}$ is the maximum switching frequency, and $V_{\mu G1,\max}$ is the maximum steady state capacitive terminal voltage of the DC/DC VSC. Thus, the inductor L_i for each DC/DC VSC of the interconnected system is obtained using equation (44) as follows:

$$L_i = \frac{V_{ref\mu G1}}{4hf_{s,n}}\cdot(1+\delta_{\mu G1}) \tag{46}$$

where $f_{s,n}$ is the acceptable switching frequency of the DC/DC VSC. $V_{ref\mu G1}$ and $\delta_{\mu G1}$ are the reference voltage and nominal droop of the DCμG1 connected to DC/DC VSC, respectively.

5. Proposed FIS fault detection method for DC multi microgrids

There are two common faults in the DC system which are Line to Line (LL) fault, and Line to Ground (LG) fault. An LL fault is one where short-circuit occurs between positive and negative poles in a network, while an LG fault is one where short-circuit occurs between one line of the system, either positive or negative and the ground. A protection method for DC microgrid systems was proposed in [26]. The suggested protection scheme consists of master controller, slave controllers and freewheeling diode path. The master controller calculates and monitors the difference between input and output currents, and slave controllers are responsible for measurement of these currents:

$$I_{diff} = I_{in} - I_{out} \tag{47}$$

where I_{in} and I_{out} are input and output currents of each DC link segment. As earlier mentioned, the major debility of this scheme is the utilization of a threshold for detecting faults. This value is specified based on operator's experience, and can obviously affect fault detection speed.

Each DC link is persistently monitored and its current is measured by the two slave controllers. The speed and precision of fault detection of the master controller are dependent on the fault detection algorithm.

Consider the two following cases:

1) high threshold
2) low threshold

In the first case, it is assumed that a high threshold is set. The fault current magnitude depends on system resistance and fault current path. If the impedance at fault location is high or a high resistance exists in the fault current path, the peak of fault current decreases. Hence, the master controller will be unable to detect high impedance faults.

On the other hand, the threshold value can be reduced to overcome this problem. Reducing the threshold value causes the main controller to make a mistake decision and trip the system due to power swings, while in fact, no fault has occurred. In such a situation in which threshold value is set low, fault detection has lower precision. Accordingly, it is proposed that another criterion be added as the expert system in the decision-making unit. Based on fuzzy logic, FIS tries to make the best decision for any system mode. In addition, another criterion for fault detection for systems connected to DC multi microgrids interconnected systems is presented and specified in the next section. An intelligent fuzzy controller is then used as a substitute for the previous controller, in which it can detect faults as quickly as possible.

5.1. Definition criterion of rate of change of differential current and criterion of current direction for low impedance fault detection

For a defining of the new criterion, suppose the low impedance fault such as F1 occurs in Segment A (Seg.A in Fig. 7), which is to be investigated. The input current to faulted segment is calculated as follows:

Input current (I_{in}) = $I_{\mu G}$ + $I_{fault1,F1}$

where $I_{fault1,F1}$ is the fault current entering the faulted point due to F1 occurrence. The output current from the faulted is determined as follows:

Output current (I_{out}) = $I_{\mu G}$ + $I_{fault2,F1}$

where $I_{fault2,F1}$ is the fault current entering faulted point from Seg.B. Fig. 7 indicates these currents. It can be inferred that in the low impedance fault condition, the current on the DCμG1 increases, since fault current is added to the $I_{\mu G}$. However, the current on the load side decreases. Hence, the following two modes can be concluded (Table 1).

Table 1
Conditions of input and output currents in each segment.

Without Fault	Fault Occurrence
$I_{in} = I_{MG}$ $I_{out} = I_{MG}$	$I_{in} > I_{MG}$ $I_{out} < I_{MG}$

In normal situation, the current flowing through each segment is identical. When a low impedance fault occurs, either the input or output current quickly rises, implying that its rate of change has become positive. Meanwhile, the rate of change of current on the other side of the segment turns negative. The categorization is represented as rules which will be fed to the FIS so that decisions at every moment would be made according to these rules. A FIS protection scheme for LVDC ring-bus was presented in [29], but the specific and accurate form of the proposed FIS protection scheme for DC multi microgrids systems is as follows:

- **Rule 1:** IF I_{in} and I_{out} are equal → THEN no fault has occurred.
- **Rule 2:** IF I_{in} and I_{out} are decreasing → THEN no fault has occurred.
- **Rule 3:** IF I_{in} and I_{out} are increasing → THEN no fault has occurred.
- **Rule 4:** IF Iin is increasing and Iout is decreasing ($\frac{di_{in}}{dt} > 0$ and $\frac{di_{out}}{dt} < 0$) → THEN a fault has occurred.
- **Rule 5:** IF Iin is decreasing and Iout is increasing, ($\frac{di_{in}}{dt} < 0$ and $\frac{di_{out}}{dt} > 0$) → THEN a fault has occurred.
- **Rule 6:** IF Iin and Iout are entering, THEN a fault has occurred, even if no another rule is true.

These 6 rules help the FIS make the most appropriate, precise decision based on the criterion of the rate of change of current and criterion of current direction. The 6 rules as new criterions are included in Table 2 and Table 3 for determining the proposed FIS scheme. The current direction criterion has priority over the rate of change criterion, and if a fault is detected based on the current direction, the output of the other criterion not be calculated and fault detection is notified immediately. The ✓ symbols in the Table 2 and Table 3 indicate more important outputs, meaning that fault occurrence is definite. The proposed FIS scheme is the main controller, and the differential method acts as a backup controller supervising this intelligent system. Presented rules are provided in the multi-stage flowchart. According to the

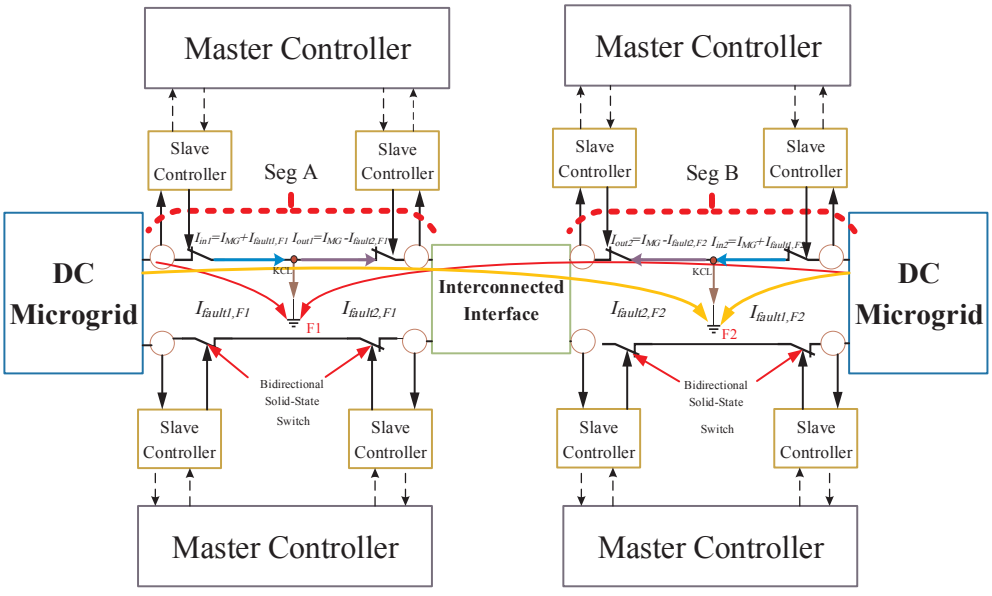

Fig. 7. Current flow direction in faulted segment.

Table 2
The current directions in each segment.

I_{in} Direction	I_{out} Direction	Fault Occurrence
Entering	Exiting	×
Exiting	Entering	×
Entering	Entering	✓

Table 3
The rate of current change in each segment.

I_{in}	I_{out}	Fault Occurrence
0	0	×
Decreasing ↘	Decreasing ↘	×
Increasing ↗	Increasing ↗	×
Increasing ↗	Decreasing ↘	✓
Decreasing ↘	Increasing ↗	✓

fault detection flowchart of Fig. 8, fault detection based on the differential method is the last layer of the protection system and plays a backup role for algorithm primary layers.

Fuzzy inference systems (FIS) can formulate the behavior of a phenomenon or process only in the form of using descriptive and empirical rules without the need to recognize the exact and analytical model. In contrast to regression and neural network models, even FISs can also be used to simulate the behavior of a process without the process data. Consequently, the FIS is a tool for formulating a process using specific and accurate rules, and if 'p', then 'q' conditions (Rules 1 to 6). The type of FIS used in this paper is Mamdani with the following structure:

$$R_i:\ If\ x_1\ is\ \widetilde{A}_{i1}\ and\ (or)\ x_2\ is\ \widetilde{A}_{i2}\ and\ (or)...x_m\ is\ \widetilde{A}_{im}\ Then\ y_i = \widetilde{N}_i\ (i = 1, 2, ..., C)$$

Fuzzy rules were used to determine the proper output, which are defined for the protection algorithm and constructed using 'AND' and 'OR' operators, as well as using the center of gravity (COG) method. Membership functions intended for fuzzification and defuzzification of measured data (input and output currents of each segment) are triangular with equal distributions in an interval of $[-1,1]$. To avoid errors in decision-making, the number of consecutive cycles for fault occurrence confirmation is also defined in 3 cycles. In other words, a fault occurrence command is issued by the master controller when at least one of the fuzzy rules results in the three consecutive simulation steps.

6. Simulation results

The simulation time was adjusted to 2 s and the LG fault is applied in the positive pole at 1.2 s. The considered DCμG with simultaneous control and FIS protection schemes are simulated in MATLAB/Simulink environment. The type of solver used is 'ode23tb (stiff/TR-BDF2)' type. Furthermore, the type of sampling is variable-step type and the maximum step size is 10^{-4} and minimum step size is auto type. The DC power parks presented in Fig. 1 have been modeled and simulated. DCμG1 and DCμG2 in both DC power parks are modeled using the averaged model of DCμGs illustrated in Fig. 2(b). The DC/DC VSCs in an interconnected system of both DC power parks that are modeled in detail, i.e. by considering the switching action of their IGBT switches. The DCμGs model data, DCμGs calculated design data and DC/DC

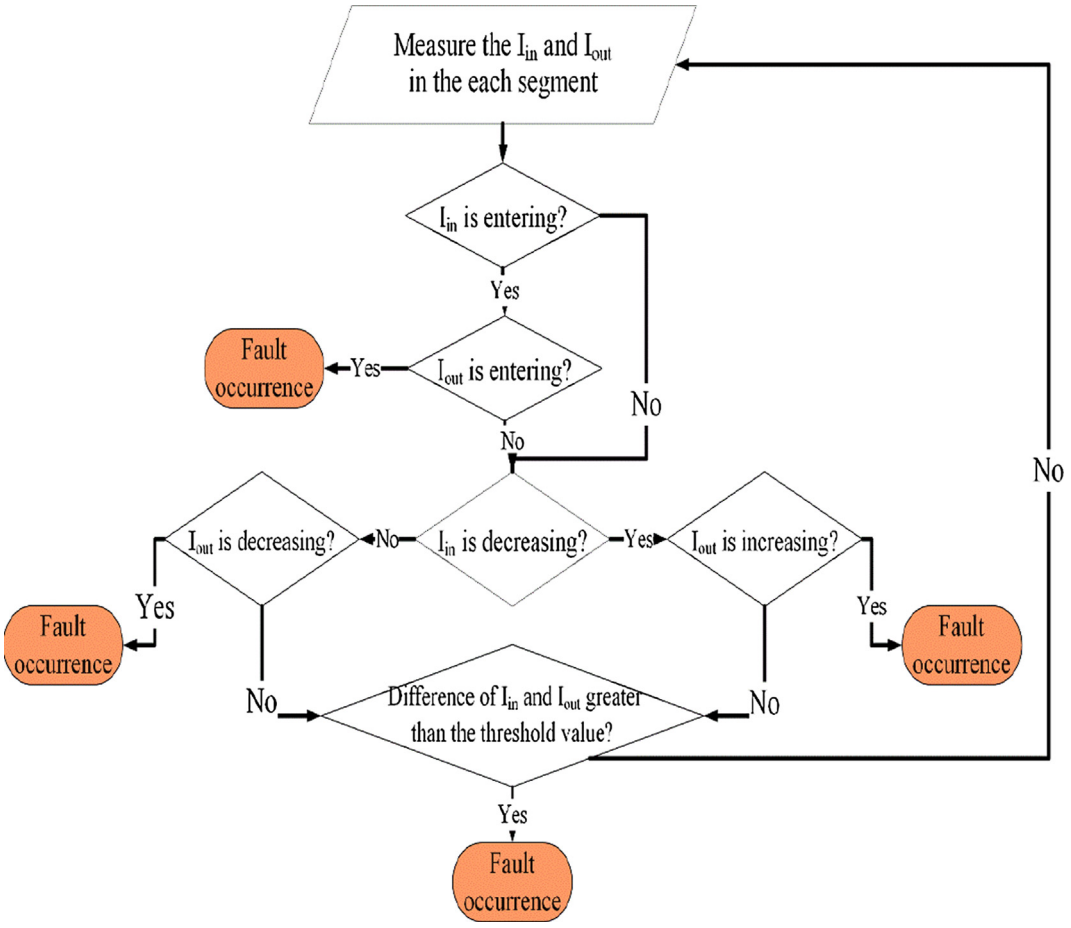

Fig. 8. Flowchart of multi-stage fault detection using FIS in each DC microgrid segment.

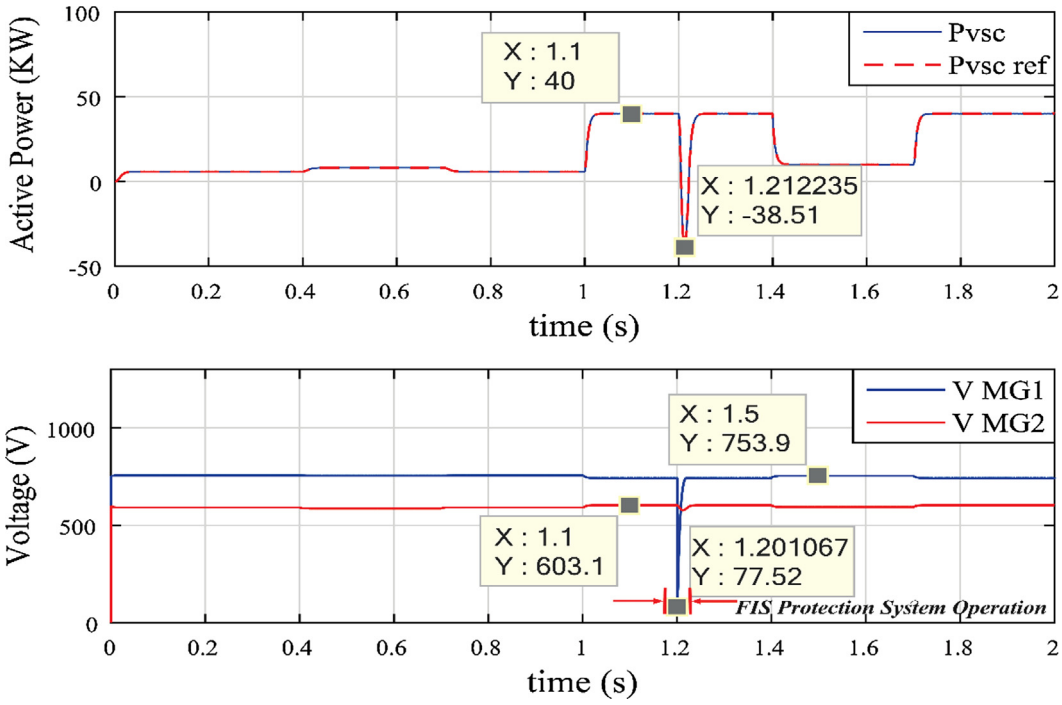

Fig. 9. Transfer power reference and instantaneous power (top), DC bus voltage of DCμG1 and DCμG2 (bottom).

interconnection converter model data are given in the Appendix. An LG fault is applied at t = 1.2 s first in seg. A, then in seg. B as can be seen in Fig. 7. The fuzzy rules for the protection algorithm are defined using "AND", "OR" operators.

The DC/DC interconnection converter performance under changes of the voltage droop controller and scheduled transfer power reference is studied. The DG and load powers in both DCμGs are presumed to have their rated values. Fig. 9 (top) shows the scheduled transfer power reference and the instantaneous active power of the DC/DC interconnection converter. As shown in Fig. 9 (top), when $0 < t < 1$ s, the DC/DC interconnection converter is operated by voltage droop controller (R_i). When, $1\text{ s} < t < 1.4$ s, DC/DC interconnection converter is operated in scheduled transfer power reference (P_{ext}). As illustrated in Fig. 9 (top), the active power of the DC/DC interconnection converter effectively follows the transfer power reference, even in short circuit moments. This indicates the effectiveness of the proposed control system for the DC/DC interconnection converter in proper regulation of power flow between two DCμGs.

The DCμG bus voltages of DCμG1 and DCμG2 are illustrated in Fig. 9 (bottom). As can be seen, the DCμG bus voltages are maintained within specified limits. As shown in Fig. 9 (bottom), in the final steady state condition, we have $V_{\mu G1} = 753.9$ V, $V_{\mu G2} = 603.1$ V. These results can be verified by equations (35) and (36). According to Fig. 9 (bottom), the voltage of DCμG1 reduced due to fault (F1) occurrence in Seg. A DC link. However, the FIS protection system detects fault very quickly in 1.067 ms. Then, the faulted DC link segment is isolated and the needed voltage and active power of the DCμG1 are provided by energy storage system and AC grid and the network is quickly restored. Therefore, it is observed that there is no defects and malfunctions in the simultaneous operation of control interface and FIS protection scheme.

Fig. 10 (top) depicts the variations of the active power in AC grid (P_{n1} and P_{n2}) and in battery storage banks (P_{b1} and P_{b2}), as well as power associated with AC loads connected to the DC bus (P_{L1} and P_{L2}) and the output power of DG units injected to the DC bus (P_{DG1} and P_{DG2}). As can be observed, the active power of the network VSCs and storage VSCs changes during the power transfer variations, because the recent converters act as a DC voltage regulator. According to Fig. 10, it can be seen that after the fault occurrence in the link DC, the active power in AC grid (P_{n1} and P_{n2}) and in battery storage banks (P_{b1} and P_{b2}) increases for a few milliseconds. Since the fault occurred in the DCμG1, increase of active power on this side is more. After fault detection, faulted DC link is isolated and the performance of the two DCμG will be in islanding mode. Also in this mode, it is observed that there is no defects and malfunctions in the simultaneous operation of control interface and FIS protection scheme. Simulation results show the effectiveness of the proposed control interface and FIS protection scheme for the DC/DC interconnection converter in the exact regulation of power transfer between the DCμGs and its independence from disturbances of both DCμGs and faults.

In following, supposed that fault (F2) has occurred in Seg.B. Fig. 11 (top) shows the scheduled transfer power reference and the instantaneous active power of the DC/DC interconnection converter in this circumstance. As shown in Fig. 11 (top), the active power of the DC/DC interconnection converter effectively follows the transfer power reference, even in short circuit moments. This indicates the effectiveness of the proposed control system for the DC/DC interconnection converter in proper regulation of power flow between two DCμGs.

The DCμG bus voltages of DCμG1 and DCμG2 are illustrated in Fig. 11 (bottom). As can be seen, the DCμG bus voltages are maintained within specified limits. As shown in Fig. 11 (bottom), in the final steady state condition, we have $V_{\mu G1} = 741.7$ V, $V_{\mu G2} = 603.1$ V. According to the Fig. 11 (bottom), the voltage of DCμG2 reduced due to fault (F2) occurrence in Seg.B DC link. However, the FIS protection system detects

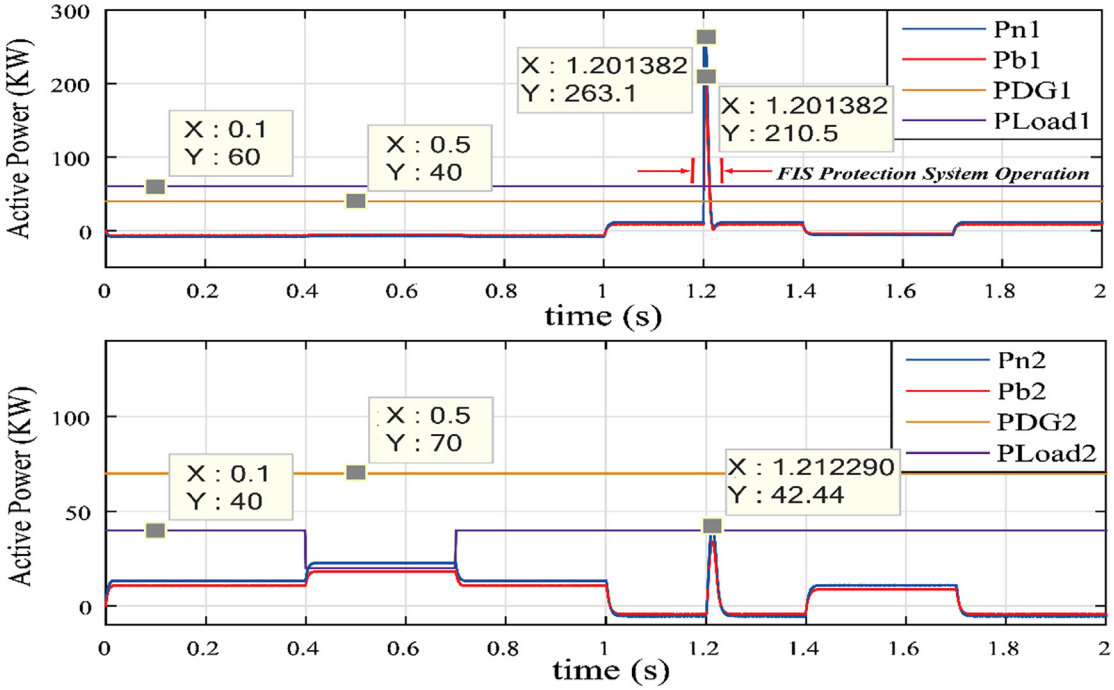

Fig. 10. Active power variations in DCμG1 (top), Active power variations in DCμG2 (bottom).

fault very quickly in 0.776 ms. Then the faulted DC link segment isolated and needed voltage and active power of the DCμG1 are provided by energy storage system and AC grid and the network is quickly restored.

Fig. 12 (top) depicts the active power variations in DCμG1 and DCμG2. As can be seen, the active power of the network VSCs and storage VSCs change during the power transfer variations, because the recent converters act as a DC voltage regulator. According to Fig. 12 can be seen, after the fault occurrence in the link DC, P_{n1}, P_{n2}, P_{b1} and P_{b2} increase for a few milliseconds. Since the fault occurred in the DCμG2, increasing of active power on this side is more. After fault detection, faulted DC link is isolated and the performance of two DCμG will be in islanding mode. Also in this mode, it is observed that there is no defects and malfunctions in simultaneous operation of control interface and FIS protection scheme. Simulation results show the effectiveness of the proposed control interface and FIS protection scheme for the DC/DC interconnection converter in the exact regulation of power transfer between the DCμGs and its independence from disturbances of both DCμGs and faults.

Fig. 13 depicts DC bus voltage of DCμG1 and DCμG2 for F1 fault occurrence in the presence of FIS and differential protection systems. The DCμG voltage restoration has lasted about 100 ms in the presence of differential protection which is not proper for DC system at all. Whereas, this amount is approximately 20 ms for FIS protection. By using the intelligent FIS protection, DCμGs voltages experience much smaller maximum values, causing fewer damage to the microgrid

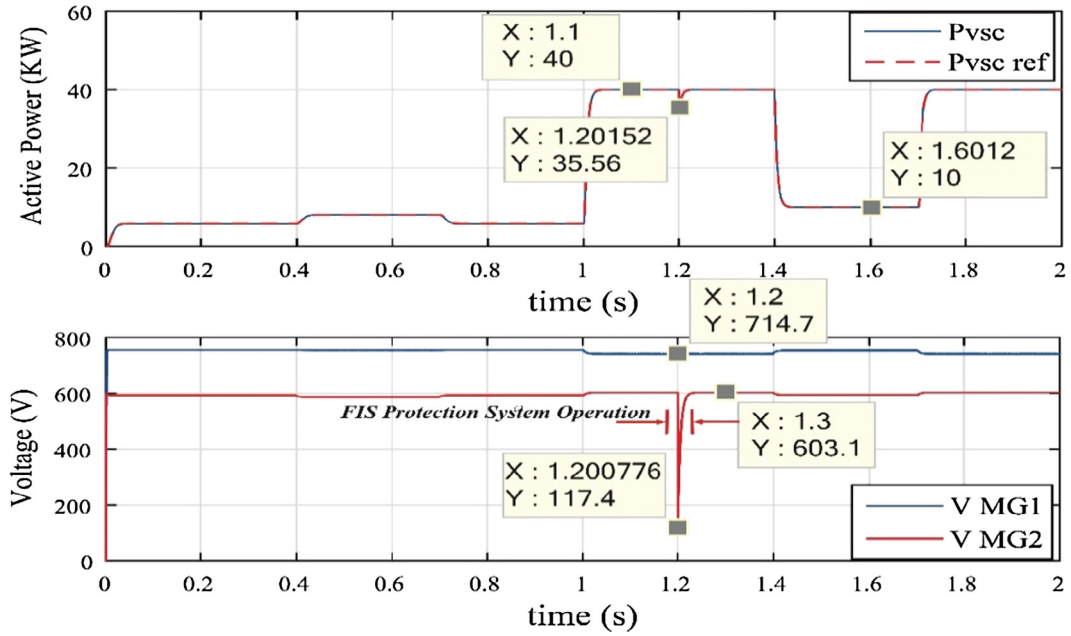

Fig. 11. Transfer power reference and instantaneous power (top), DC bus voltage of DCμG1 and DCμG2 (bottom).

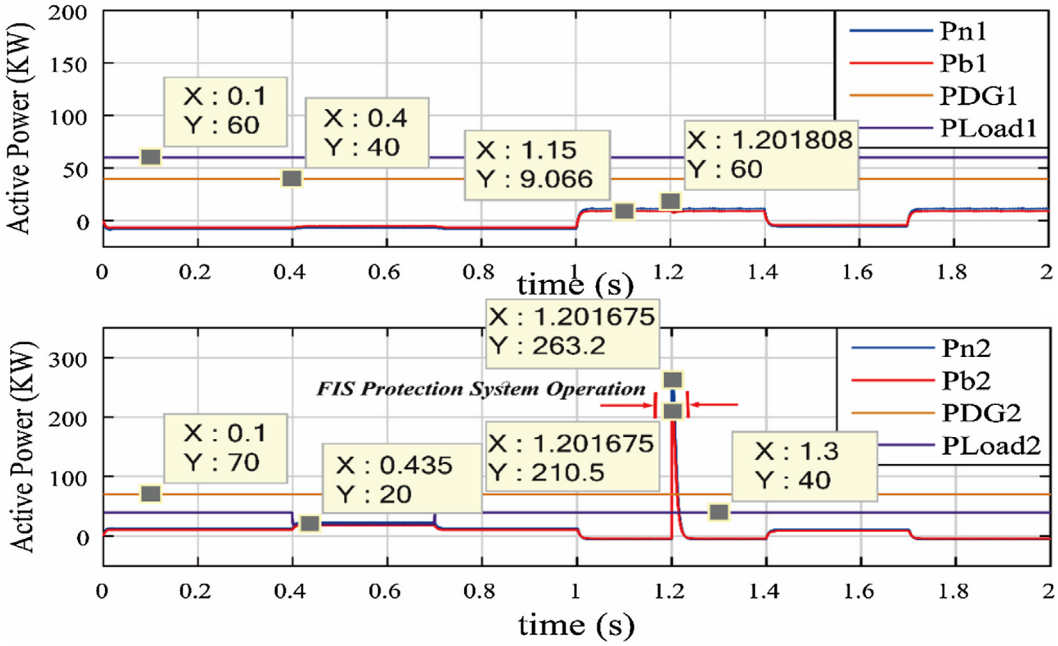

Fig. 12. Active power variations in DCμG1 (top), Active power variations in DCμG2 (bottom).

equipment.

Fig. 14 indicates the input current from the DCμG 1 to seg.A due to F1. As can be seen, in the FIS protection, F1 is detected faster and within 2 ms, and the isolation command is issued by the controller and the seg.A is isolated. By using FIS protection, smaller peak of fault currents are experienced that cause less damage to the microgrid equipment. Meanwhile, for differential protection, the fault is detected in 69 ms, and the peak of fault current is more than 1.5 times the FIS protection.

In Fig. 15 (top), fault current flow comparison is shown in the freewheeling branch. FIS protection by the fast fault detection and preventing an increase in fault current caused a smaller fault current (less than 1.5 times) in the freewheeling branch compared to differential protection. This means reducing the cost of protection and the possibility of using smaller diodes. Fig. 15 (bottom) shows the voltage of the switches. The use of FIS protection reduces the maximum voltage on the switches, which allows their installation costs as well as the utilization of switches with lower rated insulation.

A detailed report of the FIS and differential time reaction in 3 section including DCμG1 current, freewheeling path current and switch voltage are presented in Table 4.

7. Experimental validation

In the previous section, numerical simulation results are presented. After investigation of the numerical simulation results and because the faults are detected in a few milliseconds, the question is that, is the proposed simultaneous control and protection scheme applicable and enforceable in real scale of DCμGs? Nowadays, due to the high speed of analysis and processing of microcontrollers, the advancement of

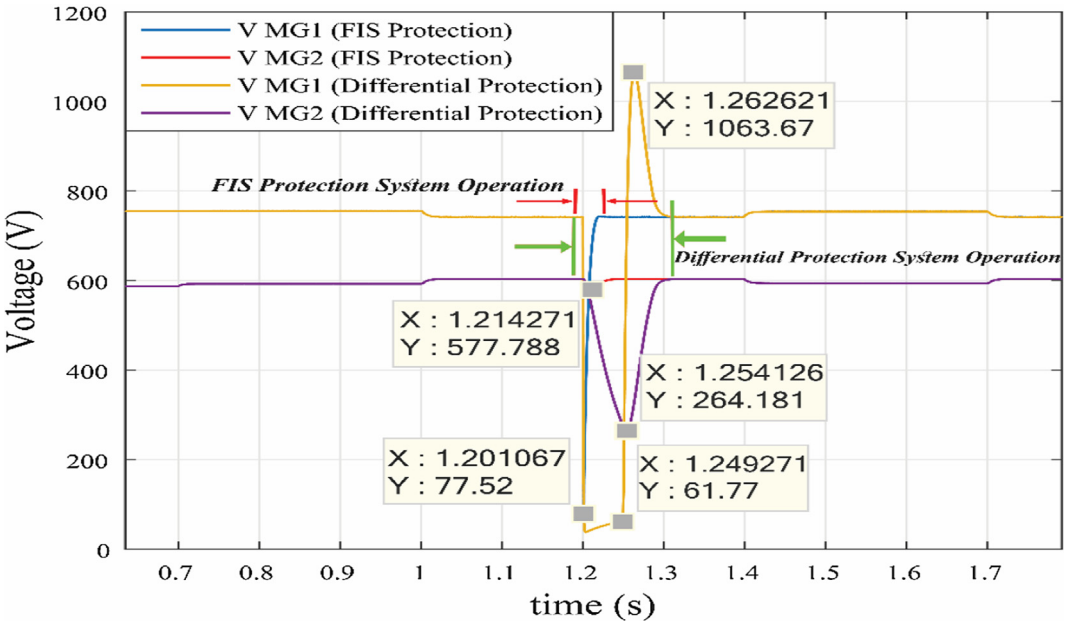

Fig. 13. DC bus voltage of DCμG1 and DCμG2.

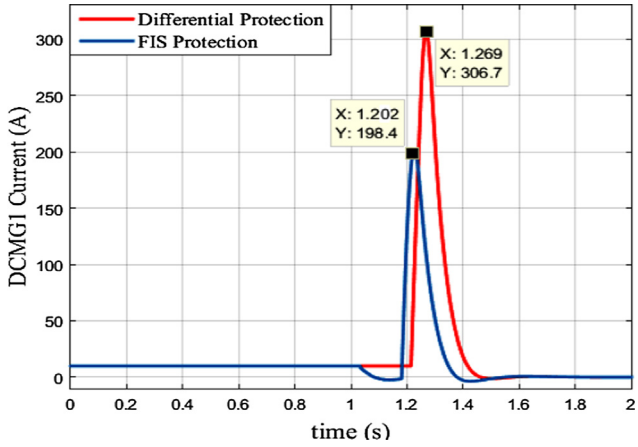

Fig. 14. DCμG 1 side current in seg.A.

semiconductor technology and the fast switching of power electronic devices, it is expected that the simultaneous control and protection scheme for DCμGs are feasible and enforceable. Nevertheless, a simple laboratory-scale experiment setup in 12:1 scale from the simulation DCμG architecture is constructed to assess the feasibility of the proposed FIS protection scheme with actual hardware. Due to hardware limitations in the 12:1 ratio, the implementation of the DCμGs control scheme has been neglected. However, the performance of the control system is in the range of seconds and has a slower dynamic than the protective system, hence the implementation ability of control scheme is clear and evident. The structure has a source-load structure of Fig. 7, but only with a positive pole to simulate an LG fault. The utilized equipment, specifications and relevant explanations of the used devices are given in Table 5.

The architecture of the experimental test setup is displayed in Fig. 16. Differential fault detection threshold value has been considered as 10% of the simulations value. In this test, the analog to digital (A/D) conversion of the current measurement is accomplished in the 50 μs interrupt service routine. Microcontroller and IGBTS gate drivers are shown in Fig. 17. Bright LEDs of current measurement modules represent the right connection between current sensor and the microcontroller. The test structure has two sources as DC multi-microgrids. In normal circumstance, the DCμG 1 source supplies 30 W (30 V, 1 A) and the DCμG 2 source supplies 25 W (25 V, 1 A). It should be noted that during a fault occurrence, until the current limiter of the power supply is activated, the current reaches about ten amps. Also, due to fast dynamic of protective system, implementation of the interconnection system of DCμG is neglected. An LG fault was applied in the middle of the DC link in seg. A in 1.2 s. The input and output currents of this segment are monitored by the ACS 712-30 current measurement module and sent to the microcontroller. The microcontroller as the intelligent protective system should detect the fault occurrence.

Table 4
The FIS and Differential Time Reaction.

Items	FIS Protection	Differential Protection
Time of fault detection	2 ms	69 ms
Peak current of freewheeling branch (during fault occurrence)	142.7 A	220.1 A
Time of fault current damping in freewheeling branch	1.407 s	1.517 s
Peak voltage of switch (during fault occurrence)	848.1 V	970.3 V

Fig. 18 shows the input current from the DCμG 1 to the seg. A due to F1. As can be observed, in the FIS protection, F1 is detected faster and within 17 ms, and the isolation command is issued by the controller and the seg. A is isolated. By using FIS protection, smaller peak of fault currents are experienced that cause less damage to the microgrid equipment. Meanwhile, for differential protection, the fault is detected in 77 ms, and the peak of fault current is more than 1.3 times the FIS protection. As can be seen, although, 3rd order low-pass filter and an optocoupler are used, nevertheless experimental environment is still very noisy, but there is no disturbance in the performance of the fault

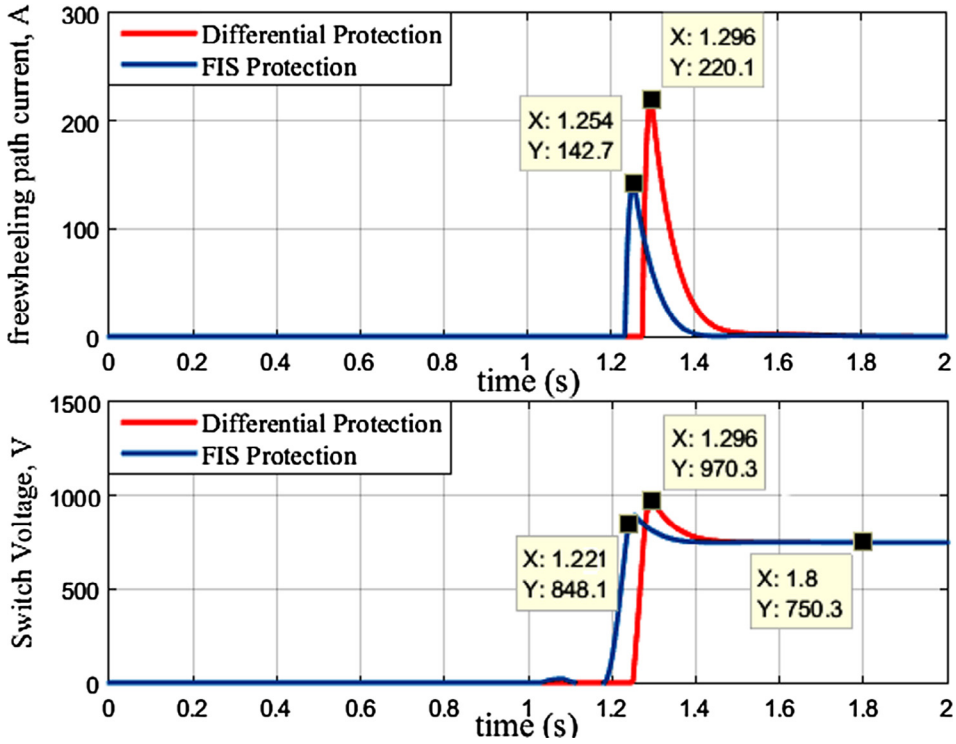

Fig. 15. Fault current in the freewheeling path (top) and Voltages of the switches in fault occurrence (bottom).

Table 5
Used equipment and corresponding descriptions.

Equipment	Descriptions
Two channels of 30-V 3-A power supply MASTECH HY3005-2	Used for modelling of DCμG1 and DCμG2 source supplies
10 Ω, 30 Watt wirewound resistor	Used for resistive DC load
Three 15 μH ferrite-core inductor	Used for DC link inductance
Six 220 pF ceramic capacitor	Used for DC link capacitor discharges
Four IGBT STGW38IH130D modules	Used to make bidirectional switches
One IGBT IKW40N120H3	Used to employ the LG fault
Diode FEP30GP, 2 Ω wirewound resistor	Used for freewheeling diode paths
Diode FEP30GP, 10 μF electrolytic capacitor, 12 Ω resistor	Used for RCD snubbers that suppress voltages overshoot due to the DC link inductance effect
TI's TMS320F28335 Microcontroller	Used for fault detection method implementation
Three ACS 712-30 current measurement modules	For sampling current, a 3rd order low-pass filter (LPF), analog-to-digital converter
Three TC427CPA microchip, ULN2003 APC buffer	Used for IGBTs gate drivers Important note: The IGBTs gate drivers was implemented in the Darlington Coupling for simultaneous operation of the IGBT switches
Two HCPL-7840 optocoupler	Used for separation of analog ground from digital ground, noise reduction
CP2102 modules	Used for connection of the microcontroller to the computer via USB port
One channel of 30-V 3-A power supply MASTECH HY3005-1	Used for energy storage modelling
Hyper Terminal software V1.9b	Used for view and use data and information on a computer

detection algorithm. The proposed FIS scheme in the real implementation acted well and detects the faults faster than the differential method.

In Fig. 19 (top), fault current flow comparison is shown in the freewheeling branch. FIS protection by the fast fault detection and preventing an increase in fault current caused a smaller fault current in the freewheeling branch compared with differential protection. This means reducing the cost of protection and the possibility of using smaller diodes. Fig. 19 (bottom) shows the voltage of the switches. Using FIS protection reduces the maximum voltage on the switches, which allows their installation costs as well as allowing the utilize of switches with lower rated insulation.

A detailed report of the FIS and differential time reaction in 3 section including DCμG1 current, freewheeling path current and switch voltage are presented in Table 6.

8. Discussion and consideration

This section describes the supplementary points and validation of the laboratory prototype implementation, as well as the considerations

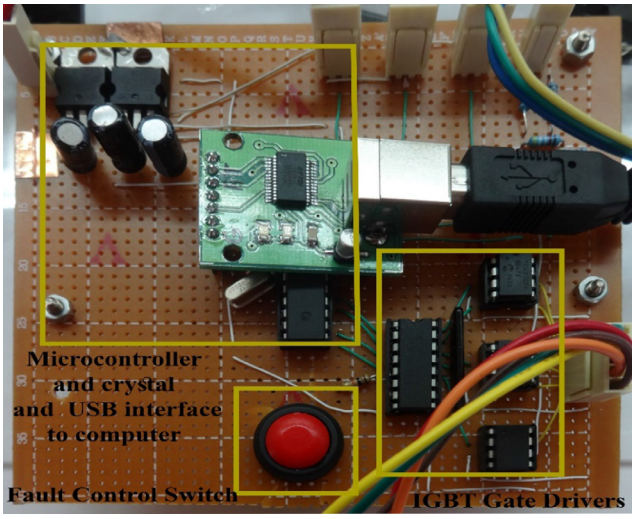

Fig. 17. Microcontroller and IGBTS gate drivers.

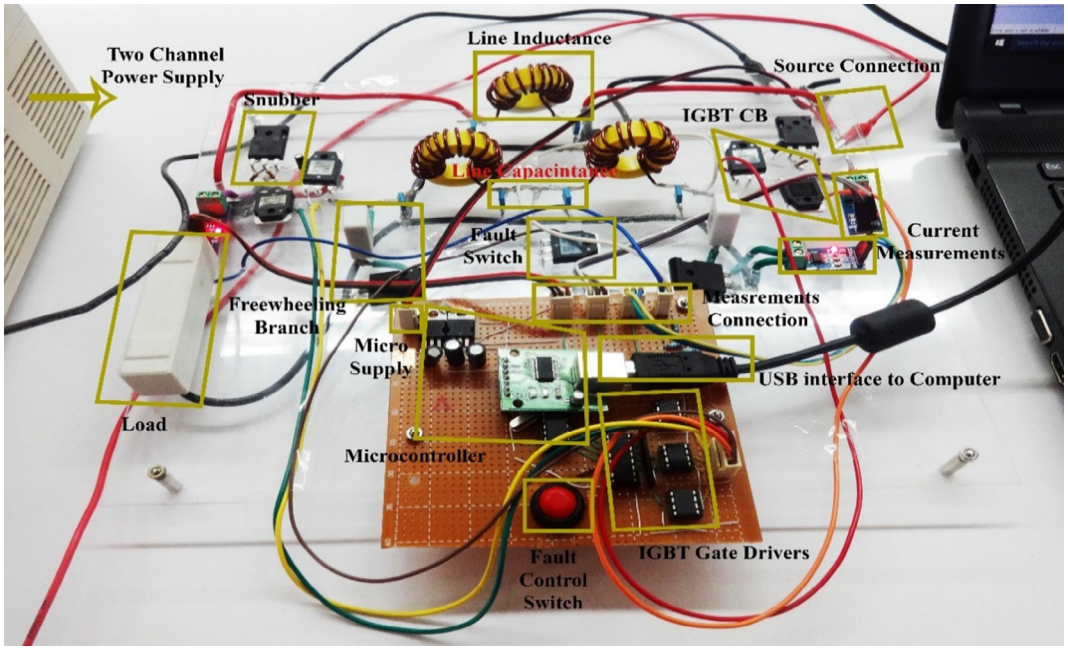

Fig. 16. The architecture of the experimental test setup and microcontroller.

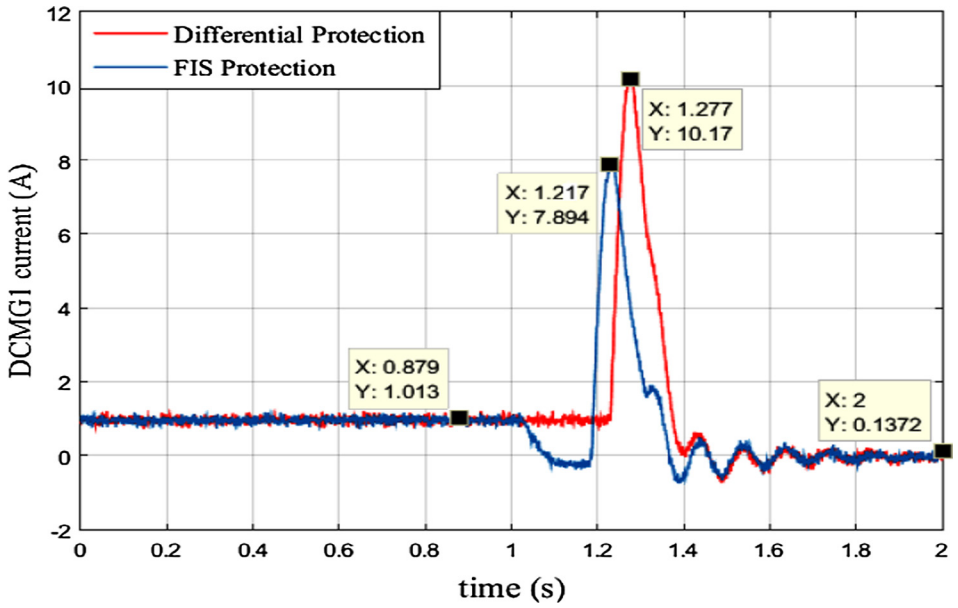

Fig. 18. DCμG 1 side current in seg.A.

of the real scale prototype implementation. The sample network used in this paper is DC Multi Microgrids. The pointed-out network should have at least two DC DGs or two AC DGs, whose voltages were converted to DC voltages via VSCs for each DCμG. There is also a need for energy storage system in these networks and loads are generally considered as DC load. Considering the implementation of laboratory network in 1:12 ratio, and also due to the laboratory limitations, we have been tried to use equipment that is most similar to the simulated network in order to claim that the results are valid. In this regard, two DC DGs and energy storage system are implemented by three DC power supplies. DC loads have also been implemented by the DC resistor. In the simulated

Table 6
The FIS and Differential Time Reaction.

Items	FIS Protection	Differential Protection
Time of fault detection	17 ms	77 ms
Peak current of freewheeling branch (during fault occurrence)	5.524 A	7.444 A
Time of fault current damping in freewheeling branch	1.394 s	1.486 s
Peak voltage of switch (during fault occurrence)	34.57 V	36.19 V

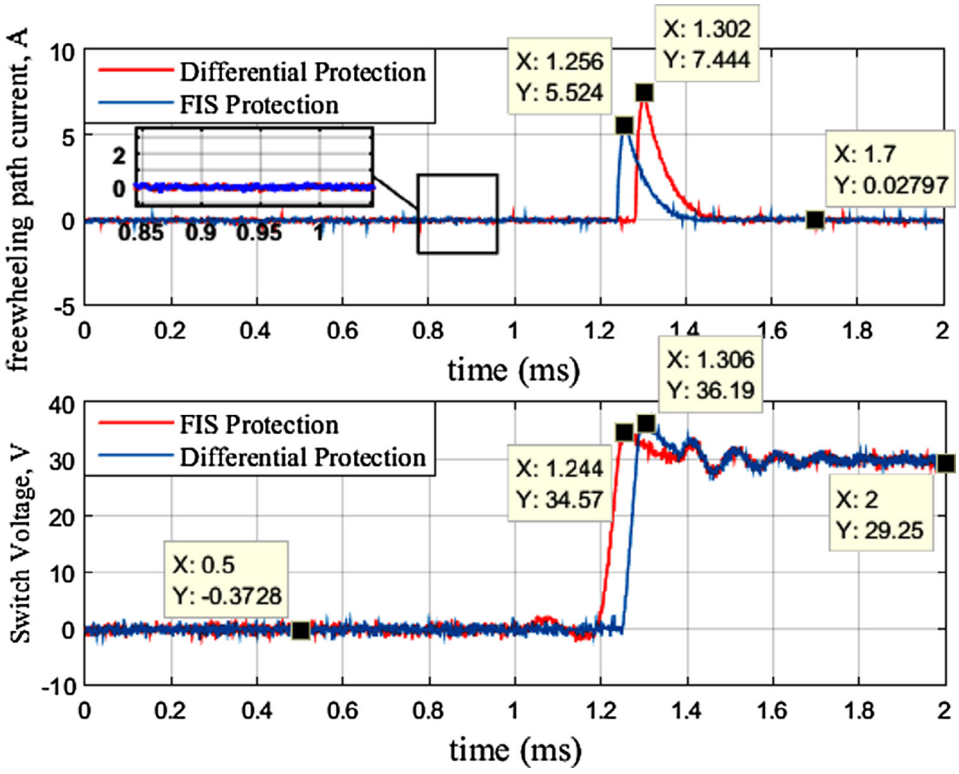

Fig. 19. Fault current in the freewheeling path (top) and Voltages of the switches in fault occurrence (bottom).

Table 7
DCμGs model data.

DCμG parameters	DCμG1	DCμG2
Reference DC voltage [V]	750	600
DG rated power [kW]	60	40
Energy storage rated power [kW]	40	40
Network VSC rated power [kW]	50	50
Load rated power [kW]	40	70
Nominal DC voltage droop	0.05	0.05

Table 8
DCμGs calculated design data.

Calculated DCμG design parameter	DCμG1	DCμG2
Storage VSC droop coefficient [Ω]	0.6680	0.4275
Network VSC droop coefficient [Ω]	0.5344	0.3420
DCμG capacitor [mF]	17.917	27.996

Table 9
DC/DC interconnection converter data.

Rated power [kW]	40
HCC hysteresis band [A]	2
Acceptable switching frequency [kHz]	10

network, the solid-state circuit breakers like IGBTs are used, which IGBTs are also used in practical implementation as back to back to make bidirectional switches. It is noticeable that similar models of the simulation network have been used for implementation of DC link inductance, DC link capacitor discharges, freewheeling paths, RCD snubbers and IGBTs gate drivers that values and supplementary explanations are given in Table 5. The FIS and differential fault detection algorithm are rewritten in the DSP software environment, and algorithms are configured in the TMS320F28335 microcontroller. Also, the results are transferred to the computer through the CP2102 modules USB interface. By comparing the results, it can be seen that the figures of the DC microgrid and the freewheeling branch current and the voltages of switches are very similar for simulation and practical implementation, and there is nuance which is negligible and indicates the validity of the laboratory prototype implementation.

As noted above, we tried to employ the special equipment to make laboratory prototype more similar to simulated network and needs the least possible changes to real scale prototype implementation. Nevertheless, some considerations should be taken into account in the real scale prototype implementation. The first and most important point is that when the fault occurs, the solid-state breakers that are used at the beginning and the end of each section to protect the DC microgrid should operate simultaneously. To achieve this goal, the current values measured and monitored by the slave controllers at the beginning and the end of each section must be synchronized. As a result, we require high-speed communications and synchronization like PMU for real scale prototype implementation [23,24]. The next issue is that the presence of power electronic devices controls current to a certain extent during fault conditions, which in turn makes fault detection difficult [30–32]. To overcome this problem must use two-level VSC that does not limit current. The last point is that, in the real scale prototype implementation, the quantities and capacity of the utilized equipment, especially the solid-state breakers (IGBTs), should be selected in accordance with the DCμGs voltage level, which can tolerate voltages and currents transient.

9. Conclusion

Simultaneous protection and control schemes for DC multi microgrids systems have not been studied in previous papers. In this paper, a DC/DC VSC system is developed for interconnection of DC microgrids in a DC power park. Suitable control interfaces are proposed for the proposed interconnection systems. Simulation results show the effectiveness of the proposed control interface in proper regulation of instantaneous power transfer and cancellation of interactions between the interconnected DC microgrids. In addition, this paper is proposed as a novel fast fault detection method for DC microgrids interconnected systems. The proposed method is based on fuzzy inference system (FIS). The proposed protection method included expert controllers which are able to detect faults more quickly than the other existing methods. Fast fault detection is the advantage of the proposed method which reduces system protection costs and allows the use of equipment with lower insulation withstand. Also, by the implementation of FIS protection scheme, it can be inferred that FIS scheme is reliable, and the enforceable and efficiency, speed and precision of the FIS scheme are demonstrated compared to the differential protection.

Appendix

The DCμGs model data are given in Table 7. As a result, using equations (23), (24) and (27), the DCμGs design data are calculated as given in Table 8. Also, the DC/DC interconnection converter model data are given in Table 9.

References

[1] Hammons TJ. Integrating renewable energy sources into European grids. Int J Electr Power Energy Systems 2008;30(8):462–75. https://doi.org/10.1016/j.ijepes.2008.04.010. ISSN 0142-0615.

[2] Ma WJ, Wang J, Lu X, Gupta V. Optimal operation mode selection for a DC microgrid. IEEE Trans Smart Grid 2016;7(6):2624–32.

[3] Tan Xingguo, Li Qingmin, Wang Hui. Advances and trends of energy storage technology in Microgrid. Int J Electr Power Energy Systems 2013;44(1):179–1915. https://doi.org/10.1016/j.ijepes.2012.07.015. ISSN 0142-0615.

[4] Wang Z, Chen B, Wang J, Kim J. Decentralized energy management system for

networked microgrids in grid-connected and islanded modes. IEEE Trans Smart Grid 2016;7(2):1097–105.
[5] Bracale A, Caramia P, Carpinelli G, Mancini E, Mottola F. Optimal control strategy of a DC micro grid. Int J Electr Power Energy Systems 2015;67:25–38. https://doi.org/10.1016/j.ijepes.2014.11.003. ISSN 0142-0615.
[6] Cook MD, Parker GG, Robinett RD, Weaver WW. Decentralized mode-adaptive guidance and control for DC microgrid. IEEE Trans Power Delivery 2017;32(1):263–71.
[7] Huang X, Wang Z, Jiang J. Control and load-dispatching strategies for a microgrid with a DC/AC inverter of fixed frequency. Int J Electr Power Energy Systems 2012;43(1):1127–36.
[8] Rashad M, Ashraf M, Bhatti AI, Minhas DM, Ahmed BA. Mathematical modeling and stability analysis of DC microgrid using SM hysteresis controller. Int J Electr Power Energy Systems 2018;95:507–22.
[9] Bevrani, H., Francois, B., & Ise, T. Hierarchical microgrid control. Microgrid Dynamics and Control, 221–265.
[10] Mahmoodi M, Gharehpetian GB, Abedi M, Noroozian R. Control systems for independent operation of parallel connected DG units in distribution DC systems. In: Proc. First Int. Power and Energy Conf., Putrajaya, Malaysia, 2006, pp. 220–224.
[11] Pirooz Azad S, Iravani R, Tate JE. Stability enhancement of a DC-segmented AC power system. IEEE Trans Power Delivery 2015;30(2):737–45.
[12] Karlsson P, Svensson J. DC bus voltage control for a distributed power system. IEEE Trans Power Electron 2003;18(6):1405–12.
[13] Ito Y, Zhongqing Y, Akagi H. DC micro-grid based distribution power generation system. In: The 4-th int. conf. on power electronics and motion control, IPEMC, 2004, p. 1740–1745.
[14] Johnson BK, Lasseter R. An industrial power distribution system featuring UPS properties. In: Proc. 24th Ann. IEEE PESC, 1993, p. 759–765.
[15] Salomonsson D, Soder L, Sannino A. Protection of low-voltage dc microgrids. IEEE Trans Power Delivery 2009;24(3):1045–53.
[16] Sohrab Mirsaeidi, Dalila Mat Said, Mohd. Wazir Mustafa, Mohd. Hafiz Habibuddin, Kimia Ghaffari, An analytical literature review of the available techniques for the protection of micro-grids, Int J Electr Power Energy Systems, 58, 2014, 300–306, ISSN 0142–0615.
[17] Ren J, Venkata S, Sortomme E. An accurate synchrophasor based fault location method for emerging distribution systems. IEEE Trans Power Delivery 2014;29(1):297–8.
[18] Saeedifard M, Graovac M, Dias R, Iravani R. DC power systems: challenges and opportunities. In: IEEE PES General Meeting, p. 1–7, IEEE, 2010.
[19] Salonen P, Nuutinen P, Peltoniemi P, Partanen J. LVDC distribution system protection solutions, implementation and measurements. In: Power Electronics and Applications, 2009. EPE'09. 13th European Conference on, p. 1–10, IEEE, 2009.
[20] Lin X, Zhang R, Tong N, Li X, Li M, Yang D. Regional protection scheme designed for low-voltage micro-grids. Int J Electr Power Energy Systems 2015;64:526–35.
[21] Lien KY, Bui DM, Chen SL, Zhao WX, Chang YR, Lee YD, et al. A novel fault protection system using communication-assisted digital relays for AC microgrids having a multiple grounding system. Int J Electr Power Energy Systems 2016;78:600–25.
[22] Che L, Khodayar ME, Shahidehpour M. Adaptive Protection System for Microgrids: Protection practices of a functional microgrid system. IEEE Electrification Mag 2014;2(1):66–80.
[23] Farhadi M, Mohammed OA. Event-based protection scheme for a multiterminal hybrid DC power system. IEEE Trans Smart Grid 2015;6(4):1658–69.
[24] Meghwani A, Srivastava SC, Chakrabarti S. A non-unit protection scheme for DC microgrid based on local measurements. IEEE Trans Power Delivery 2017;32(1):172–81.
[25] Fletcher SD, Norman PJ, Fong K, Galloway SJ, Burt GM. High-speed differential protection for smart DC distribution systems. IEEE Trans Smart Grid 2014;5(5):2610–7.
[26] Park J-D, Candelaria J. Fault detection and isolation in low voltage dc-bus microgrid system. IEEE Trans Power Delivery 2013;28(2):779–87.
[27] Kazmierkowski MP, Malesani L. Current control techniques for three-phase voltage-source PWM converters: a survey. IEEE Trans Ind Electron 1998;45(5):691–703.
[28] Prodanovic M, Green TC. Control and filter design of three-phase inverters for high power quality grid connection. IEEE Trans Power Electron 2003;18(1):373–80.
[29] Abdali A, Mazlumi K, Noroozian R. Fast fault detection and isolation in low-voltage DC microgrids using fuzzy inference system. In: 2017 5th Iranian Joint Congress on Fuzzy and Intelligent Systems (CFIS), Qazvin, 2017, pp. 172–177. doi: 10.1109/CFIS.2017.8003678.
[30] Mohanty R, Balaji USM, Pradhan AK. An accurate noniterative fault-location technique for low-voltage DC microgrid. IEEE Trans Power Delivery 2016;31(2):475–81.
[31] Ericsen T, Hingorani N, Khersonsky Y. Power electronics and future marine electrical systems, IEEE Trans Ind Appl, vol. 42, pp. 155–163, Ja2006.
[32] Cuzner R, Venkataramanan G. The status of dc micro-grid protection. In: Industry Applications Society Annual Meeting, 2008. IAS '08. IEEE, pp. 1–8, Oct 2008.