Phase Locked Loop System for FACTS

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***Abstract*—This research addresses the special requirements of phase locked loops (PLLs) for a typical application with FACTS elements. A new PLL system that uses adaptation algorithms is developed with the aim of improving speed of responses, robustness to AC voltage depressions, and harmonic rejection. The adaptive PLL consists of the three control units that individually control frequency, phase angle, and voltage magnitude. The voltage controller output is used to compensate for reduced gain caused by the ac voltage magnitude depressions. The output phase angle and its derivative, the frequency signal, are controlled in two independent control systems in order to enable elimination of frequency and phase error without compromising transient responses. The simulation results are compared with a PLL available with the PSB MATLAB block-set and noticeable improvements are demonstrated. In particular, settling time and overshooting are significantly lower with conditions of reduced ac voltage magnitude.**

***Index Terms*—Frequency locked loops, modeling, phase-locked loops, power system control, thyristor circuits, tracking.**

I. Introduction

A. Background

PHASE locked loops (PLL) with all ac/dc converters take an important role in providing a reference phase signal synchronized with the ac system. This reference signal is used as a basic carrier wave for deriving valve-firing pulses in control circuits. The actual valve-firing instants are calculated using the PLL output as the base signal and adding the desired valve firings [1], [2]. Typically, the desired firings are calculated in the main control circuit achieving regulation of some output system variables. The dynamically changing reference from a PLL therefore influences actual firings and it plays an important role in the system dynamic performance.

Modern FACTS and HVDC elements have ever-increasing requirements on speed of response, performance, robustness, fault-recovery, and power quality. Their control systems are becoming sophisticated and the role of PLL structure/dynamics in meeting these requirements is becoming an important research topic [1]–[3] although it is still insufficiently investigated. Research in [1]–[3] studies the influence of PLL dynamics inside FACTS/HVDC, and [1] demonstrates that an increase in HVDC inverter PLL gains deteriorates the system stability, whereas [3] proves that *10* times reduced SVC PLL gains make responses very poor. Further in line with the above research, this paper seeks to develop a new PLL that would improve FACTS performance and that would be suitable for operating demands and conditions faced by various FACTS elements.

Manuscript received March 24, 2003.

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Digital Object Identifier 10.1109/TPWRS.2003.814885

Historically viewed, the first converters with transmission systems (HVDC systems) employed the individual phase firing controls using zero-crossing detection synchronizing circuits [4]. They were found to be prone to harmonic instabilities, and they were replaced with a more robust equidistant firing pulse method, employing the voltage-controlled oscillator [5]. This method has evolved to the three-phase, trans-vector-type PLL [6] that is popular with HVDC and FACTS [1]–[3], [7]. The trans-vector-type PLL has excellent internal harmonic cancellation and fairly good transient responses but it is deficient in the following: 1) Unbalanced ac voltages cause pronounced second harmonic generation, 2) Gain is reduced with lower ac voltages, 3) It is sensitive to ac voltage harmonics and speed of response must be reduced in order to prevent harmonic propagation. 4) It is unable to follow individual phase angles. Recent research [8] attempts to improve transient response of the trans-vector PLL using lead-lag compensation but the robustness, the unbalanced faults, and other issues are unresolved. Among various designs to improve robustness and positive sequence tracking, lot of praise deserves the discrete robust PLL developed with power system block-set (PSB) on MATLAB platform [9], [10] (the methodology is applied with the three-phase and single-phase PLL available as the standard unit in the PSB library in SIMULINK). This PLL design, referred here as the PSB PLL, uses the specially developed unit variable frequency average (VFA) that eliminates harmonics. It demonstrates excellent second harmonic elimination including conditions with single-phase faults and superb elimination of external ac voltage harmonics but, as shown below, it has an unfavorable transient response and very poor phase angle tracking under reduced voltages.

The desired PLL should possess generic properties: rapid response, accurate indication of unbalanced conditions, and robustness in terms of unaffected responses under voltage magnitude reduction or harmonic presence on the input ac signal.

B. Three-Phase Against Single-Phase PLL for FACTS

The design presented here can be applied to a single-phase PLL or to a three-phase configuration. Primarily, the single-phase design is addressed for the reasons presented below.

Many FACTS and HVDC converters use a three-phase PLL configuration that measures a three-phase signal (voltages or currents) and derives a single phase-reference signal. The distinct phase-references for individual phases are then calculated by adding or subtracting $2\pi/3$ radians. Such a design has the advantage of internal harmonic cancellation, but it suffers from poor representation of single-phase transients. In reality, such a PLL will give an average phase angle over three phases that poorly represents the individual phase angles.

In addition, in case of voltage unbalance, this PLL generates various harmonics.

A single-phase PLL gives a particular phase angle reference irrespective of the conditions on the other two phases, and therefore, allows better individual phase control of the ac system. It is presumed here that three single-phase PLL units would give a more accurate indication of the system dynamics. The central issue that has hampered single-phase PLL utilization is that a single-phase design normally generates second harmonic (there is no internal harmonic cancellation). Second harmonics in PLL are very difficult to eliminate and if eliminated, a very sluggish design typically results.

This research proposes a single phase PLL design that overcomes these obstacles and largely meets specific performance requirements as described below.

II. Design Objectives

PLLs normally use multiplication of two *sine* signals: v- the input signal, and the PLL output signal v_p, to obtain the phase error signal [11]

$$\begin{aligned} v =& V\sin(\omega t + a) \\ v_p =& V_p\cos(\omega_p t + a_p) \end{aligned} \tag{1}$$

where V, V_p are the magnitudes of the input and the PLL output, respectively, ω and ω_p are the frequencies of the input and output, and a, a_p are the phases of the input and output signal. The error signal can be derived as

$$\begin{aligned} e =& v \times v_p \\ e =& 0.5VV_p\sin\left((\omega-\omega_p)t + a - a_p\right) + \\ &+ 0.5VV_p\sin\left((\omega+\omega_p)t + a + a_p\right). \end{aligned} \tag{2}$$

The above error signal is processed in a feedback loop that involves filtering and a control stage. The control stage eliminates phase error, improves performance, and generates the PLL output v_p [11].

Observing (2), several specific characteristics are noted with the view of FACTS applications: 1) because of the relatively low main frequency, the second harmonic can have significant impact on the loop dynamics, 2) the loop gain is variable since ac faults reduce V, and 3) input harmonics on v can be expected to propagate through the feedback loop via V and they have frequencies that may interfere with the control loop. Additional control challenges are observed including: nonlinear gain, requirements for zero phase, but also frequency errors, and possible harmonic proliferation through the feedback loop.

Considering the practical application for FACTS and the above error signal analysis, the main design objectives are postulated:

- rapid response and zero error for the output angle and the output derivative. In FACTS applications, good phase angle but also frequency tracking are important;
- robustness to ac system voltage depressions, since it is important that PLL responses are sufficiently fast during faults and transients. Ideally, the PLL dynamic responses should be unaffected by the voltage magnitude (V) changes;

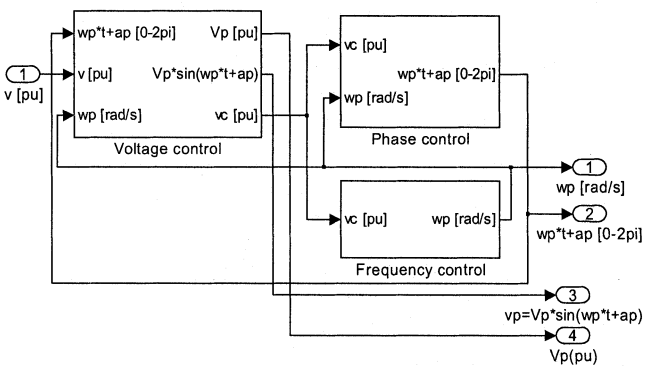


Fig. 1. PLL schematic.

- unaffected, robust response under the input ac system harmonics. These ac harmonics in the host network are a realistic expectation with the increasing use of power electronics. The harmonics on the input signal are multiplied with the feedback signal in (2), causing an array of other harmonics and nonlinear responses, depending on the system gain.
- Minimal presence of harmonics on the PLL output signal, since they can cause problems at other control levels outside the PLL. This implies total elimination of the second harmonic in (2) and filtering of any other harmonics on the input signal.

III. Adaptive PLL Structure

The underlying design assumption is that a PLL can meet the objectives only if it possesses complete information on the input signal (i.e., magnitude V, frequency ω and phase a). The proposed design generates these three components in three feedback control units. These components are used to regenerate the *sine* signal that should be a close replica of the input signal v.

Fig. 1 shows the PLL structure outlining the three main units: the voltage controller, the frequency controller, and the phase angle controller. The phase angle and the frequency controller in essence produce the same signal but in different frequency domains since $\omega = da/dt$. However, if these two signals are separately controlled and then blended in a suitably developed control loop, we are able to get very good transient responses, by means of adding two slow and robust signals. Adding two slow signals improves robustness, given that each signal is individually low-pass filtered. It is noted that in the traditional approach [6], [8], [9], a single feedback controller is used that needs to ensure good tracking of frequency and frequency integral (phase angle) and this implies a degradation in performance.

The design is labeled an adaptive PLL since the voltage control output is used to correct gain in the phase and frequency controller. The voltage controller output follows variations in the input signal magnitude, and this compensates for V in (2), in a typical adaptive control manner.

A generic control design approach for the PLL system in Fig. 1 does not exist, since it is a multivariable adaptive nonlinear system. The system is constructed by sequentially designing each of the three units as shown in the following sections.

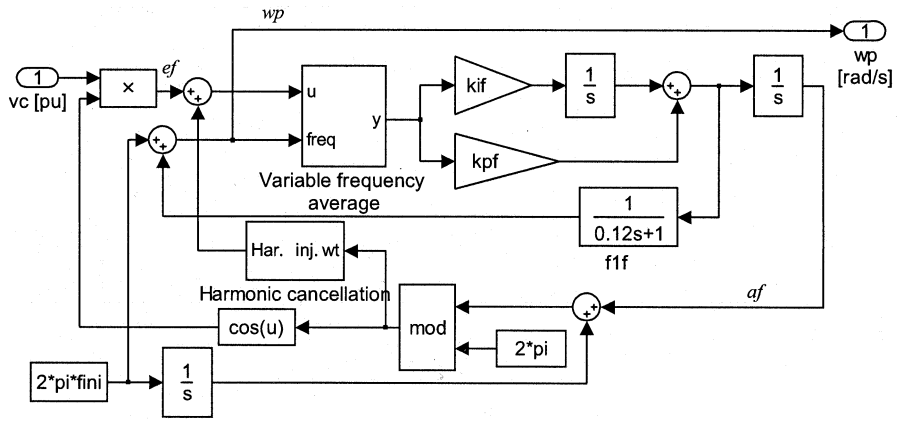


Fig. 2. Frequency control module block diagram.

IV. System Design

A. Frequency Control

The frequency controller structure is shown in Fig. 2. It is a PLL system similar to the one used in [6], [8], [9]. The open loop must have two integrators in order to ensure frequency tracking (i.e., with one integrator only phase angle tracking is possible). The closed loop control is achieved using the phase angle a_f; however, the output of the unit is the frequency value ω_p. The frequency output ensures that the PLL is capable of longer-term tracking of the input frequency. This output is filtered in the low pass f_{1f} to reduce the signal bandwidth. The slow dynamics of the output are required to avoid interactions with dynamics of the phase control unit.

The controller uses multiplication of two *sine* signals that give an error e_f, containing the second harmonic as in expression (2). The second harmonic is eliminated using the harmonic cancellation module, which is discussed in Section IV.D.

Because of the high controller gains, even small harmonics on the input signal can be magnified to a noticeable magnitude. The error signal harmonics are eliminated in the module variable frequency average (VFA) as described in Section IV.E.

The block "Mod" is a standard SIMULINK block that converts a ramp signal into a saw-tooth signal of period 2π. The variable f_{ini} is the initial frequency, or to be precise, the initial guess of the expected frequency.

The initial design is performed by isolating the unit, where the input v_c is set as an ideal *sine* signal. The small signal analytical, linearized model is developed to study stability and to determine the controller gains. The state-space model is

$$\begin{aligned}
\overset{\circ}{x}_1 &= -600x_1 - 1.5e5x_2 - 1.5e7x_3 - x_6 + a \\
\overset{\circ}{x}_2 &= x_1 \\
\overset{\circ}{x}_3 &= x_2 \\
\overset{\circ}{x}_4 &= x_3 \\
\overset{\circ}{x}_5 &= k_{if}50x_1 + k_{if}0.75e7x_3 \\
\overset{\circ}{x}_6 &= k_{pf}50x_1 + k_{pf}0.75e7x_3 + x_5 \\
a_f &= x_6
\end{aligned} \tag{3}$$

where the first four states belong to the VFA model that includes a third order Pade approximation of the delay element. The states x_5 and x_6 represent the controller and the integrator dynamics. The root locus technique is used with the model (3) to calculate the initial controller gains k_{if}, k_{pf}, with respect to stability and performance.

B. Phase Control

The phase controller resembles the frequency control unit as shown in Fig. 3. It however uses the frequency ω_p, which is output from the frequency controller, as the base frequency. Since the phase controller need not track frequency changes, the module has a single integrator in the feedback loop, and this significantly improves speed of response and reduces overshoots. The phase controller adjusts for the phase angle transients by adding a signal onto the frequency controller output.

The phase control system is designed by isolating the unit with the assumption that v_c is an ideal *sine* signal and that ω_p is a constant. The initial controller gains k_{ip}, k_{pp} are calculated using a suitable analytical model as shown below

$$\begin{aligned}
\overset{\circ}{x}_1 &= -k_{ip}x_3 + k_{ip}a \\
\overset{\circ}{x}_2 &= -\frac{1}{0.006}x_2 - \frac{k_{pp}}{0.006}x_3 + \frac{k_{pp}}{0.006}a \\
\overset{\circ}{x}_3 &= \frac{0.5}{0.008}x_1 + \frac{0.5}{0.008}x_2 - \frac{1}{0.008}x_3 \\
a_{ph} &= x_3.
\end{aligned} \tag{4}$$

The filter f_{3p} is required for stability reasons but the time constant should be as low as practically possible (also the time constant of f_{2p}) since it affects dynamics in the feedback loop. The filters f_{1p}, f_{4p}, and f_{5p} improve transient response and their values are adjusted at the final optimization stages. Note that in this control system, the error signal can be added to the output to improve transients, and filter f_{1p} further contributes phase overshoot reduction.

The VFA element introduces significant phase-lag in the controller, and for this reason it is taken out of the control loop. The differentiator VFA block is similar to the variable frequency average as discussed in Section IV.D. The harmonic cancellation unit eliminates the second harmonic.

It is underlined that this controller does not track frequency variation, and therefore, the output can be low-pass filtered (using VFA) to derive a signal with relatively slow dynamics. This method allows moderate gains and good robustness.

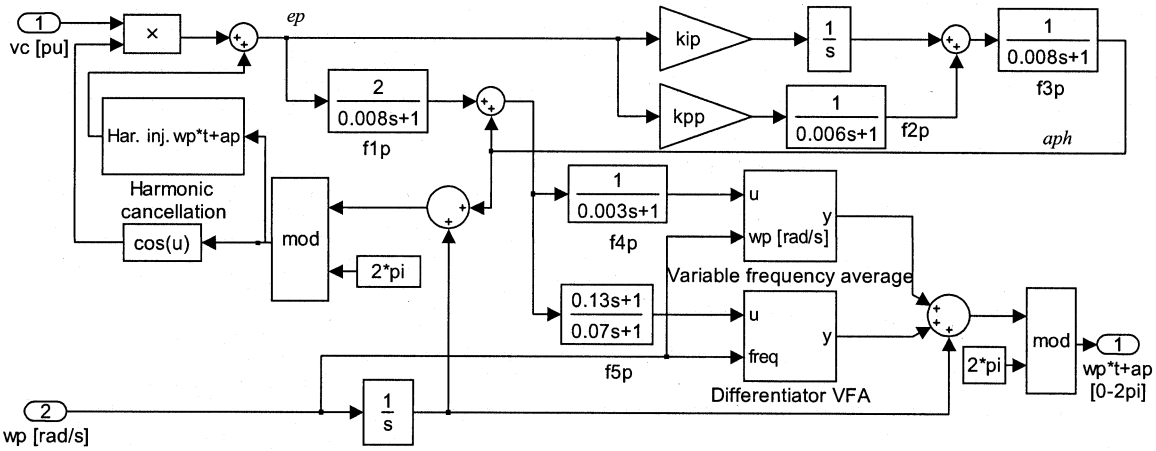


Fig. 3. Phase control module block diagram.

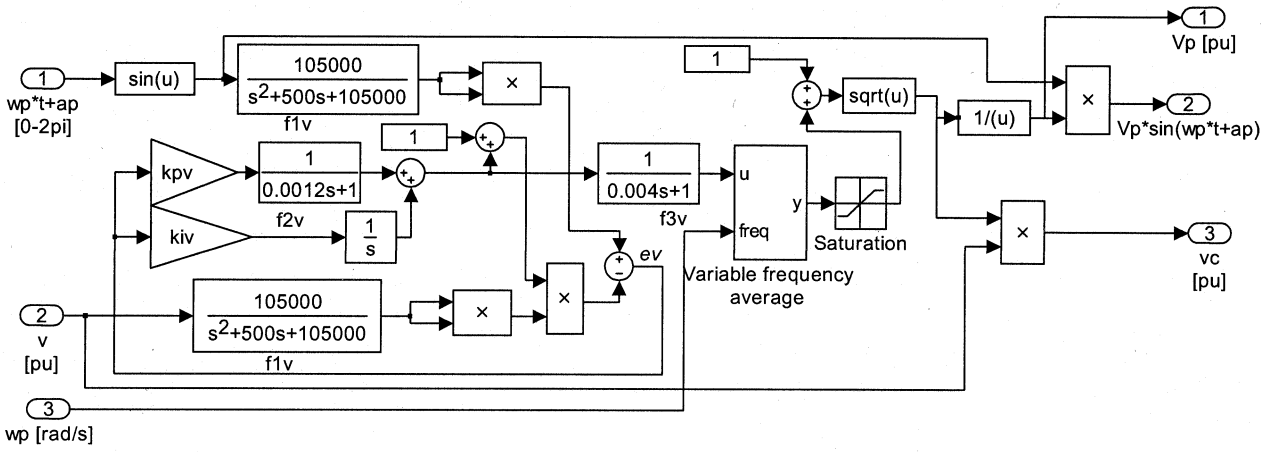


Fig. 4. Voltage control module block diagram.

C. Voltage Control

The voltage controller block diagram is shown in Fig. 4. It uses the phase angle signal $\omega_p{}^*t + a_p$ from the phase control unit as the phase reference. A sinusoidal signal is generated and assuming accurate operation of the phase controller, this signal will be a close replica of the input voltage. Taking square, a signal is obtained proportional to the input signal magnitude with an additional second harmonic

$$v_p^2 = \frac{1}{2}V_pV_p + \frac{1}{2}V_pV_p\cos(2\omega_p t + 2a_p). \tag{5}$$

If the input signal v is also squared, the error e_v in Fig. 4 is obtained as

$$e_v = \frac{1}{2}(V_p^2 - V^2). \tag{6}$$

It is seen that the second harmonic is naturally eliminated in (6), under the assumption of good phase tracking. Since there is no need for second harmonic filtering in the control loop, a higher control bandwidth can be employed.

Because of the squaring of the *sine* signal in (5), all noise harmonics will also be converted to dc signal and this affects the error e_v. As a result, the input harmonics will introduce a steady state error (offset). To eliminate this offset, the filter f_{1v} is added. It is essential that the same filter be used with both input signals (v and v_p). The filter is of second order with a cut off close to *50 Hz*.

The VFA unit is included to eliminate harmonics on the output signal and it is placed outside the main control loop to improve control speed. The square root function of the voltage controller output multiplies the input signal v to compensate for the magnitude deviation. The output of the voltage control unit is the corrected voltage signal v_c that will have unit magnitude (assuming fast PLL action). This signal is passed to the frequency and phase controllers.

The system stability and performance are ensured firstly by isolating the unit and by adjusting the controller gains k_{pv}, k_{iv}, and the filter f_{1v}. This is performed using a suitable analytical model, that resembles the model (4), and the design rules for a PI controller.

The final tuning of all the PLL controller gains and parameters is performed with the above three control units connected. The three loops interact and nonlinear simulation is the most suitable design approach. Because of the large number of parameters, the MATLAB nonlinear control (NCD) block-set optimization is used, with the performance index J as the main

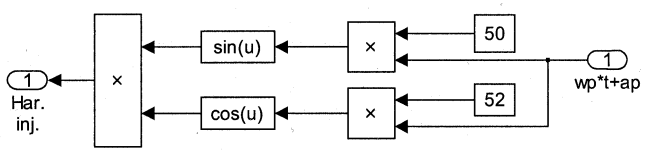


Fig. 5. Harmonic cancellation module block diagram.

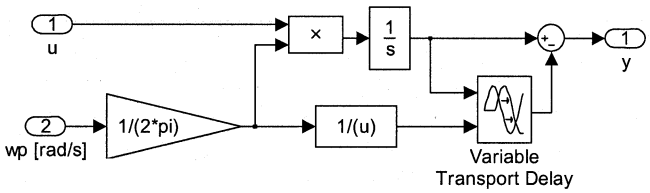


Fig. 6. Variable frequency average.

optimization function. The index J is introduced to penalize deviation from the reference value

$$J = \frac{1}{T}\sqrt{\int_0^T (a - a_P)^2} \tag{7}$$

where the time interval is taken as $T = 0.3$ s. The final controller gains are shown in the Appendix.

D. Harmonic Cancellation Module

The harmonic cancellation module is show in Fig. 5, and it uses the trigonometric identity

$$\sin\left[50\left(\omega_p t + a_p\right)\right] \times \cos\left[52\left(\omega_p t + a_p\right)\right] = \\ = \frac{1}{2}\sin\left[102\left(\omega_p t + a_p\right)\right] - \frac{1}{2}\sin\left[2\left(\omega_p t + a_p\right)\right] \tag{8}$$

to generate the second harmonic. The second harmonic is of the same magnitude and phase as the one generated inside the phase/frequency controller, assuming sufficiently fast phase and frequency control ($\omega = \omega_p$, $a = a_p$). The *102nd* harmonic is naturally eliminated in the low-pass control circuit.

E. Variable Frequency Average Module

The VFA unit, as shown in Fig. 6, resembles the module used with PSB PLL [9], [10], but a very similar configuration called moving average filter has also been used with ALSTOM PLL/sensor systems [12]. It effectively eliminates all harmonics of the input frequency, though on the downside it also introduces noticeable delay in the control circuit. The dynamics of this element can be studied with the Pade approximation, assuming that the delay time constant is $Td = 0.02$ s, as given by the first four equations in the model (3).

With the differentiator VFA module in Fig. 3, the structure is similar to that in Fig. 6, except that the integrator and the gain before the integrator are removed.

V. Simulation Results

A. Performance Testing

1) Frequency and Phase Responses: The phase-angle tracking and input frequency tracking performance are confirmed first. Fig. 7 shows the response following a *5-deg.* step change in the phase angle of the input signal. It is seen that the designed system is able to follow the reference with a settling time of approximately *40 ms* (5% criterion). The improvement over the PSB PLL is clearly evident. Table I summarizes performance comparison between the two controllers, and it is seen that in all aspects, the adaptive PLL shows better performance.

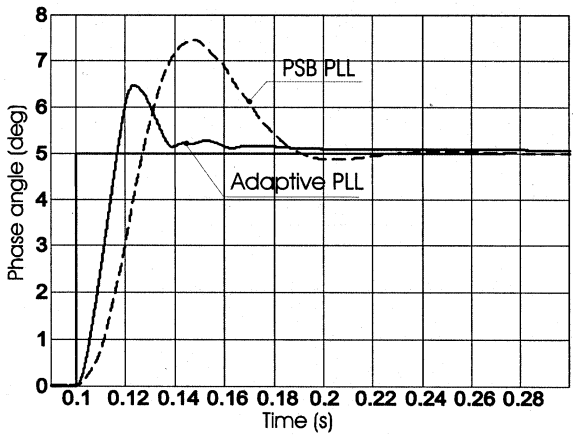


Fig. 7. PLL response after $+5$ deg. phase angle step change.

TABLE I
Performance Comparison for Phase Step Input

PLL	Index J	Settling time (ms)		Overshoot (%)
		(5%)	(2%)	
PSB PLL	0.044	80	120	49
Adaptive	0.026	40	100	29

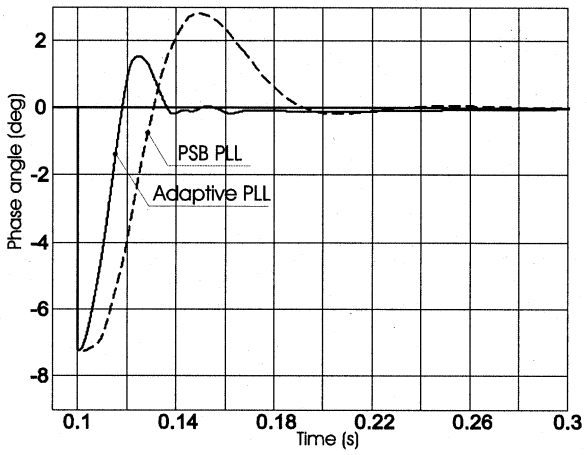


Fig. 8. PLL response after $+0.2$ Hz frequency step change.

Fig. 8 shows the response after a *0.2-Hz* step frequency change. In this case, the output angle is shown relative to the new frequency and in the ideally fast control case, the phase angle should stay at zero. It is seen that the new PLL system is able to track the frequency change with zero steady-state error. The settling time and overshooting are much smaller than in the case of the PSB PLL. The improvement in response with the adaptive PLL is attributed to the system structure that enables frequency tracking in one control unit and separate phase tracking in another control system.

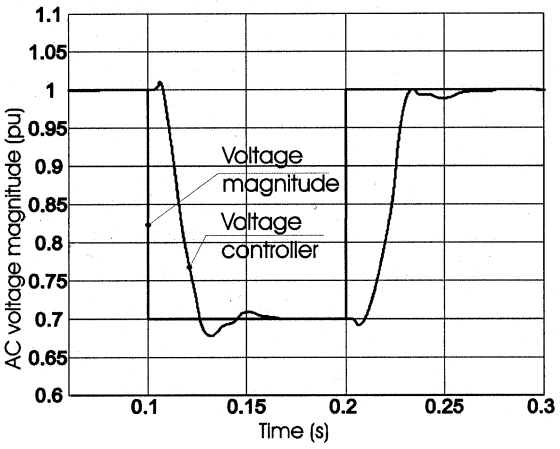


Fig. 9. Voltage controller response. Inputs: at *0.1 s* voltage magnitude depression to *0.7 p.u.*, at *0.2-s* voltage recovery to *1 p.u.*

It is noted that the system behaves as nearly linear system for solely phase or frequency inputs [11], and any higher or lower magnitude phase or frequency input produces transients of a similar shape to those in Figs. 7 and 8.

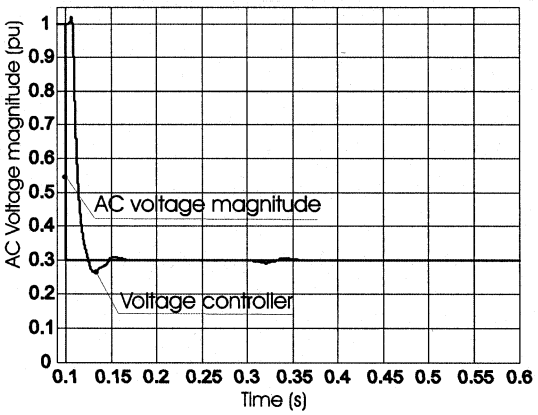
Fig. 9 demonstrates the voltage controller performance. The input signal magnitude V is stepped with unaltered phase or frequency values. It is seen that the voltage controller is able to track the input voltage magnitude with zero steady-state error and with settling time below two cycles. Voltage sags and faults will typically last several cycles in a power system, and the voltage controller should settle within the fault period to enable adequate gain at the recovery transient. The overshoot in Fig. 9 is below *10%*.

For a positive voltage step change, the response is somewhat different as a consequence of a different gain. More complex testing with additional phase and frequency changes are presented in the next section.

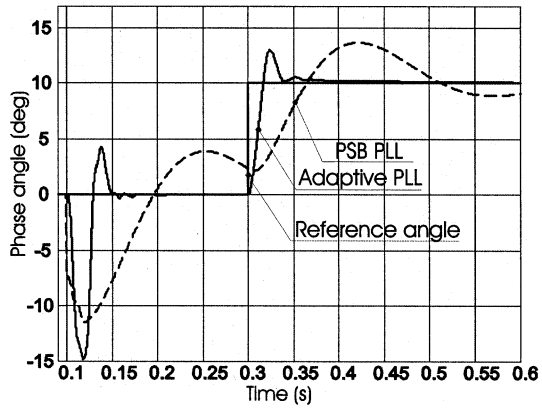
2) Tests With Voltage Sags—Robustness: It is desirable that a PLL be able to follow the phase angle and the frequency during periods of voltage depressions and to have fast response at the fault recovery stage transient. This is difficult to achieve because of the reduced PLL loop-gain with a reduced voltage. A typical PLL will have a significantly slower response for voltage depression duration.

In Fig. 10, the two PLLs are tested with reduced voltage conditions. As the voltage magnitude reduces to *0.3 p.u.* at *0.1 s*, the PSB PLL experiences reduced gain and the responses are very poor. A step reference of *10 deg.*. is applied under reduced voltage at *0.3 s* and the PSB PLL takes nearly *1 s* to settle to the new reference angle. The adaptive PLL, on the contrary, is able to fully adjust the system gain in less than *50 ms* [Fig. 10(a)]. After the gain is adjusted, the response of the main phase controller is very similar to the case with *1-p.u.* voltage and the settling time is very short.

Fig. 11 shows the responses with voltage reduction to *0.1 p.u.* for a duration of five cycles. The PLL output *sine* signal (v_p) is shown and it is evident that complete synchronization is very fast. The recovery stage introduces longer PLL settling time, but full synchronization is always achieved below *50 ms*.



(a)



(b)

Fig. 10. PLL response after phase step change during voltage depression. Inputs: at *0.1-s* voltage reduction to *0.3 p.u.*, at *0.3-s* phase angle step $+10$ deg. (a) Voltage controller output. (b) PLL phase output.

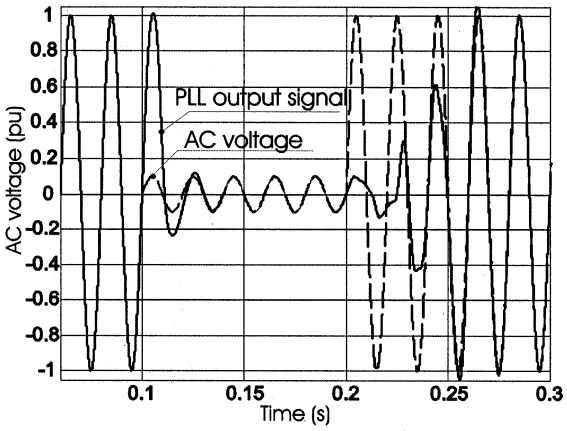
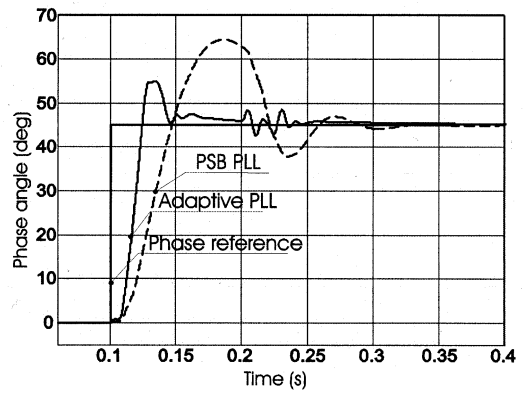


Fig. 11. PLL response during severe voltage depressions. Inputs: at *0.1-s* voltage magnitude reduction to *0.1 p.u.*, at *0.2-s* voltage recovery to *1 p.u.*

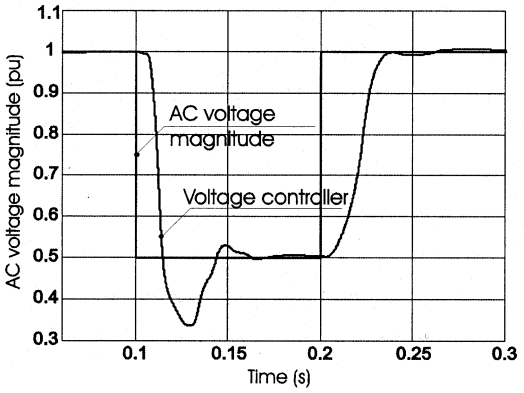
Fig. 12 shows PLL system tests for simultaneous application of two inputs: at *0.1 s*, the voltage magnitude is reduced to *0.5 p.u.* and a phase step of *45 deg.* is applied. Satisfactory responses are observed.

B. Testing With Input Harmonics

This section investigates PLL responses assuming the input voltage is polluted with harmonics, which would represent quite



(a)



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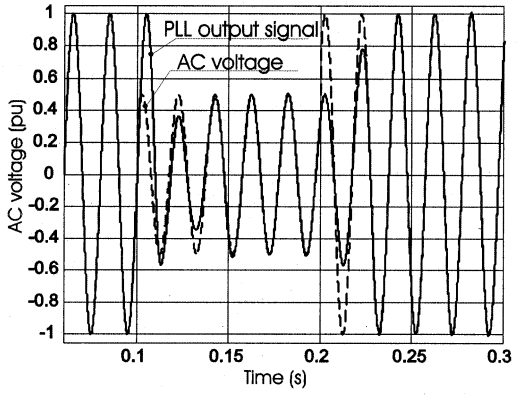
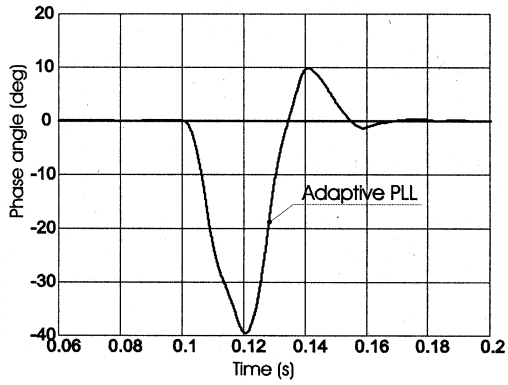


(c)

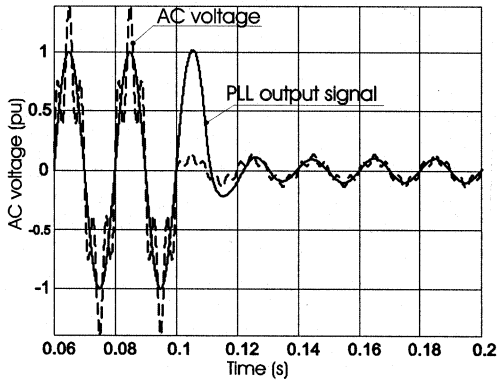
Fig. 12. PLL response to multiple inputs. Inputs: at *0.1-s* voltage depression to *0.5 p.u.* and phase step $+45$ deg., at *0.2-s* voltage recovery to *1 p.u.* (a) phase angle output (extended timescale). (b) Voltage controller output. (c) PLL generated *sine* signal.

realistic operating conditions for FACTS applications. If the input voltage has harmonics, there are two possible problems: 1) The responses might be affected in terms of transient performance or steady-state error; 2) The PLL output signal may contain an unacceptably high harmonic level. These are performance measures in the tests below.

With the understanding that typical harmonic voltage amplitudes would be expected below *1–2%*, the PLL system is tested here for much higher harmonic magnitudes, and in particular for the lower order harmonics, to better illustrate the system robustness.



(a)



(b)

Fig. 13. PLL response to voltage depression with the ac voltage having *40% 5th* harmonic. Input: at *0.1-s* voltage magnitude depression to *0.1 p.u.* (a) PLL phase angle. (b) PLL *sine* signal output.

TABLE II
STEADY STATE CONTROLLER ERROR UNDER INPUT HARMONIC PRESENCE

Harmonic injection on AC voltage		Voltage offset (%)	Phase offset (deg)
Order	Magnitude		
2^{nd}	10%	0.1	0.23
	20%	0.3	0.9
3^{rd}	10%	1	0.15
	20%	2	0.3
5^{th}	10%	0.09	0.002
	20%	0.15	0.008

Fig. 13 presents the PLL responses for voltage depression under an onerous control scenario with the input voltage containing *40%* fifth harmonic. It can be concluded from this figure and other similar tests completed that the responses are not affected or very little changed if input harmonics are present, and also that the PLL output phase angle has no noticeable harmonic level.

Because of the squaring function in the voltage controller, a harmonic on the input signal will produce a dc error signal and this will induce a steady-state error in the voltage controller and also in the phase angle controller. The filters f_{1v}, as discussed above, contribute to eliminate this error. With the present settings, the offset error values are measured for *10%* and *20%* harmonic magnitude and the results are summarized in Table II. It is seen that in the worst case of *20%* second harmonic, the

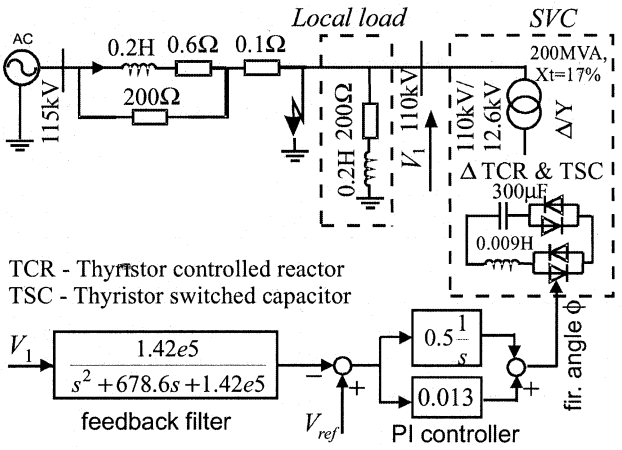


Fig. 14. Electrical test system. PLL is used to synchronize TCR valve firings with the *110-kV* bus voltage.

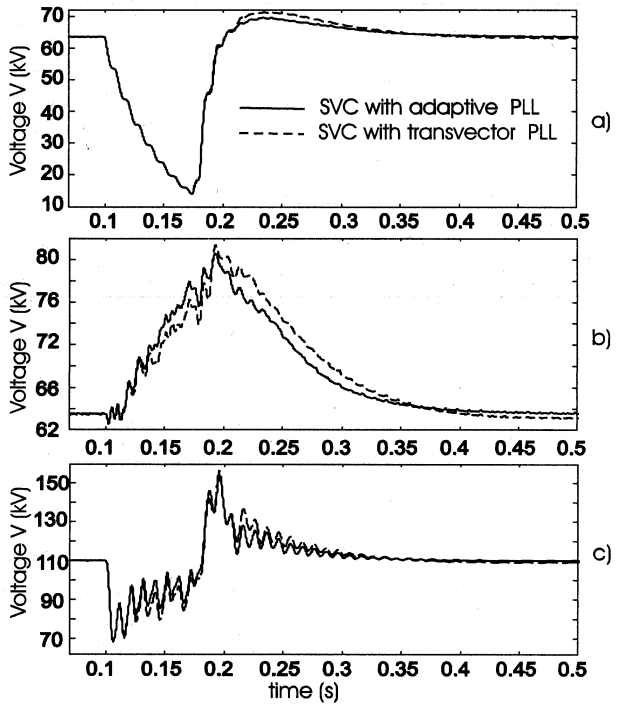


Fig. 15. EMTDC simulation of *110-kV* bus voltage response following a *60-ms* low-impedance single-phase fault. (a) Phase A (faulted phase) rms voltage. (b) Phase B rms voltage. (c) Three-phase rms voltage.

offset is *0.9 deg*. Further tests with a more realistic harmonic magnitude of *1–2%*, demonstrate that in the worst scenario of *2%* second harmonic the error is below *0.03 deg*. It is concluded that these results would be acceptable in practical applications. The design is therefore suitable for a range of FACTS elements but also for their applications with a high harmonic presence, like active filtering, or with highly nonlinear loads.

C. Testing With a FACTS Element

The adaptive PLL is also simulated on the EMTDC/PSCAD platform with a simple test system employing a six-pulse SVC element. The test system is shown in Fig. 14 and it is based on the SVC tutorial case in [7]. The SVC thyristor controlled reactor (TCR) valve firings are synchronized in two different ways: 1) using the original PLL from the EMTDC library (transvector type); and 2) using three adaptive PLL units, where all other parameters are maintained unchanged.

A low-impedance single-phase fault is simulated and the responses are shown in Fig. 15. It is clear that the adaptive PLL enables better fault recovery as demonstrated by the reduced overshootings. It is observed that the SVC is in saturation during the fault period and it actually affects the voltage only several cycles after the fault. In this post-fault interval (after the *0.2 s* time instant), the adaptive PLL achieves faster tracking of the individual phase voltages and this enables the main PI voltage controller to attain regulation of the *110-kV* bus voltage with better transient responses.

VI. Conclusions

The main challenges in PLL design for applications with FACTS can be summarized as the need to perform with zero steady-state error for phase angle and for frequency inputs, good performance under voltage depressions, and with voltage harmonics, and filtering of the input harmonics. A suitable approach to meet the above requirements is the adaptive PLL structure that regulates system gain in an adaptive control manner. The adaptive PLL consists of three control units: the phase controller, the frequency controller, and the voltage controller (Table III), which work in parallel to produce three output variables defining the input *sine* signal. The tests with phase and frequency inputs demonstrate settling time and overshooting far below those with presently used PLL systems. Further tests with phase steps under voltage depressions also demonstrate that responses settle in the period below *50 ms* and much improvement over the PLL used in PSB MATLAB block-set is observed. The testing with harmonic content on the input signal confirms objectives of robust responses and minimal harmonic propagation through the system. Additional testing with application to a SVC element demonstrates superiority over the conventional PLL systems.

Appendix

TABLE III
Controller Data

Phase control module		Frequency control module		Voltage control module	
Kip	$500s^{-1}$	*Kif*	$2000s^{-1}$	Kiv	$60000V^{-2}s^{-1}$
Kpp	*2*	*Kpf*	*100*	Kpv	$10\ V^{-2}$

Acknowledgment

The author is grateful to Dr. L. Xu, and Dr. B. Andersen of ALSTOM T&D, U.K. for their contribution in this research.

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