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Digital Closed-Loop Control Strategy To Maintain The Phase Shift of a Multi-Channel BCM Boost Converter for PFC Applications

Robert T. Ryan, *Member, IEEE,* Diarmuid N. Hogan, Richard J. Morrison and John G. Hayes, *Senior Member, IEEE.*

***Abstract*—This paper presents a novel closed-loop digital control scheme to maintain proper interleaving operation of a multi-channel boundary-conduction-mode (BCM) boost converter used in power-factor-correction (PFC) applications. The proposed control scheme is suitable for implementation on a low-cost microcontroller. This is made possible by executing the control scheme at a constant sampling rate that is much slower than the maximum switching frequency of the converter. The performance of the control scheme is further improved by using an adaptive gain that scales with the on-time of the converter, which provides optimal phase-shift control and stability under all operating conditions. The digital closed-loop control scheme is validated experimentally on a 3-channel 1 kW prototype ac-dc converter. The converter has an output voltage of 400 V and a universal input voltage range of 85 V to 265 V. The prototype converter uses a low-cost microcontroller while demonstrating correct interleaving operation.**

***Index Terms*—Interleaved boost converter, boundary-conduction mode, critical-conduction mode, power factor correction, valley switching.**

NOMENCLATURE

v_{line}	Input line voltage.
v_{in}	Rectified input voltage.
v_{gs}	Gate-source voltage.
v_{gsn}	Gate-source voltage of the n$^{\text{th}}$ channel.
v_o	Output voltage.
V_{EA}	Error-amplifier output voltage.
V_{EAn}	Adjusted error-amplifier output voltage.
v_{ramp}	Analog PWM-generation ramp voltage.
v_{ds}	MOSFET drain-source voltage.
v_{zcd}	ZCD-circuit output voltage.
v_L	Boost-inductor voltage.
i_{line}	Input line current.
i_{in}	Rectified input current.
i_L	Boost-inductor current.
i_{Ln}	Boost-inductor current of the n$^{\text{th}}$ channel.
i_o	Boost-converter output current.
i_e	Turn-off-adjustment feedback current.
t_{on}	MOSFET on-time.
t_{onn}	MOSFET on-time of the n$^{\text{th}}$ channel.
t_{psn}	Phase shift of the n$^{\text{th}}$ channel.
t_{sw1}	Switching period of channel one.
t_{refn}	Reference phase shift of the n$^{\text{th}}$ channel.
$t_{\Delta n}$	On-time perturbation of the n$^{\text{th}}$ channel.
t_1	Time at which $i_L = 0$.
T_m	Phase-shift-control execution period.
PWM_n	PWM signal of the n$^{\text{th}}$ channel.
ZCD_n	ZCD signal of the n$^{\text{th}}$ channel.
$TBPRD$	PWM time-base period register.
$TBCTR$	PWM time-base counter register.
D_Q	MOSFET body diode.
C_{ds}	MOSFET drain-source capacitance.
C_o	Boost-converter output capacitance.
C_{in}	Boost-converter input capacitance.
L	Boost-converter inductance.
n	Index number of the boost-converter channel.
N	Total number of boost-converter channels.
k	Number of switching cycles completed.
K	Number of switching cycles completed during the period T_m.
k_m	Phase-shift-controller gain.
i	Number of executions of the phase-shift-control algorithm.

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R. T. Ryan is with the Power Electronics Research Laboratory (PERL), School of Engineering, University College Cork, Cork, Ireland (e-mail: robertryan@umail.ucc.ie)

J. G. Hayes is with the Power Electronics Research Laboratory (PERL), School of Engineering, University College Cork, Cork, Ireland (e-mail: john.hayes@ucc.ie)

R. J. Morrison is with Excelsys Technologies, 27 Eastgate Buisness Park, Little Island, Cork, Ireland (e-mail: richardmorrison@aei.com)

D. N. Hogan is with Excelsys Technologies, 27 Eastgate Buisness Park, Little Island, Cork, Ireland (e-mail: diarmuidhogan@aei.com)

I. INTRODUCTION

THE BCM boost converter is a popular topology used for PFC applications at power levels below 300 W [1]. This is due to advantages such as soft switching, low-magnetic volume, and a simple control structure that only requires a slow single voltage compensator to regulate the output voltage [2]. At higher power levels the single-channel BCM boost converter suffers from high peak-to-peak input-current ripple, which increases the rms input current and reduces the converter's efficiency. The high input-current ripple at higher powers also increases differential-mode (DM) electromagnetic interference (EMI) [3], [4], thus requiring the converter to use a large DM EMI filter. Interleaving to create a 2-channel BCM boost converter is a

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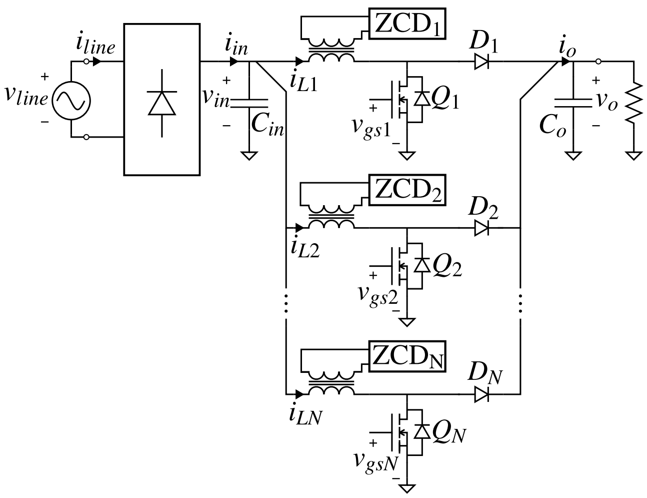

Fig. 1. Simplified circuit schematic of a multi-channel BCM boost converter.

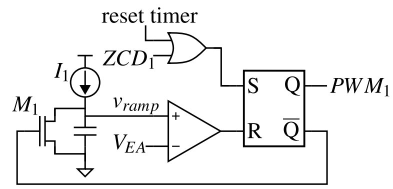

Fig. 2. PWM generation of the master channel using analog circuitry.

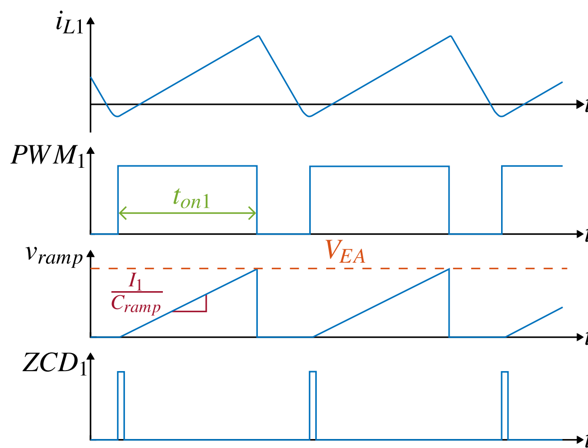

Fig. 3. Master channel constant-on-time PWM generation using analog circuitry.

common technique used to reduce the input-current ripple, thus extending the power level of the BCM boost converter to 600 W [5]. For higher power levels the CCM boost converter becomes more advantageous, due to its naturally low input-current ripple and low peak inductor current [6]. The use of the BCM topology can be extended to higher power levels by interleaving more channels together. In this paper, a closed-loop digital control scheme is designed for maintaining correct interleaving operation of a multi-channel BCM boost converter shown in Fig. 1.

A. Existing Analog Closed-Loop Solutions

Fig. 2 demonstrates how the PWM signal PWM_1 that controls MOSFET Q_1 is generated for the master channel using analog circuitry and constant-on-time control (COTC) [2]. Fig. 3 shows the corresponding timing diagram for the circuit. The signal PWM_1 is set by the signal ZCD_1 which is created by a zero-current-detection (ZCD) circuit. The ZCD circuit detects when the energy stored in the drain-source capacitor of Q_1 has discharged back into the input capacitor C_{in}. This causes the inductor current i_{L1} to become negative before the turn-on instant of the switch. The switch is turned off after an on-time of t_{on1} has elapsed. This is implemented by using the constant-current source I_1, transistor M_1 and a capacitor to make a ramp signal that is compared to the voltage V_{EA}, to trigger the switch's turn-off instant. The voltage denoted V_{EA} is the output of the voltage error amplifier, which is proportional to the on-time and is adjusted by the voltage compensator to maintain the output voltage at its setpoint value.

For the correct interleaving operation of a multi-channel BCM boost converter, a phase shift of $\frac{n-1}{N} \times 360°$ must be maintained between the inductor currents of each channel, where N is the number of boost converter channels that are enabled, and n is the index number of a particular channel. However, the switching frequency of the BCM boost converter varies with input voltage and output power [7]. This makes interleaving of a multi-channel BCM boost converter a challenging design task.

In existing analog solutions [8]–[11], the phase shift is sensed and a feedback network is formed to adjust the turn-off instant of the slave channel MOSFET to maintain the desired phase shift. The closed-loop method uses ZCD circuits to trigger MOSFET turn-on of all interleaved channels, thus ensuring perfect valley switching of all switches under all conditions, and therefore lower switching losses. Using a separate ZCD circuit for each channel also ensures the converter cannot enter continuous-conduction mode (CCM), which may cause damage to components. The Phase-Locked-Loop (PLL) method is a commonly adopted analog closed-loop control scheme [8], [11]. This method is shown in Fig. 4. In this method the phase shift is sensed by passing the ZCD signals of the master and slave channel through a flip flop. This creates a square wave with a mean value proportional to the ratio of the phase shift of the n^{th} channel t_{psn} to the switching period t_{sw1} of the master channel. This square wave is passed through a RC low-pass filter and subtracted from a constant voltage setpoint proportional to $\frac{n-1}{N}$ to create an error signal. The current i_e is then generated proportional to the error signal, and is used to adjust the turn-off instant of the slave channel by adjusting the slope of the v_{rampn} signal used in the PWM generation. Selecting the correct gain value for k_m ensures the phase shift tracks the desired setpoint. The turn-off instant of the slave channel can also be adjusted by adding a voltage to the V_{EA} signal of the slave channel.

The downside of the PLL method is that the use of the

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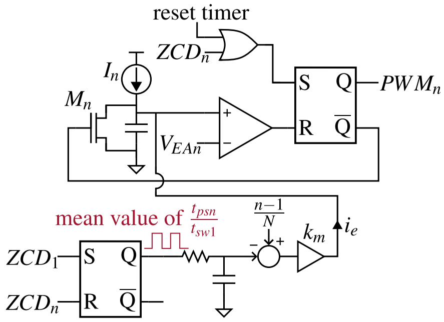

Fig. 4. Phase-shift control and PWM generation of a single slave channel using analog circuitry with the PLL method and turn-off adjustment by altering the PWM generation ramp signal.

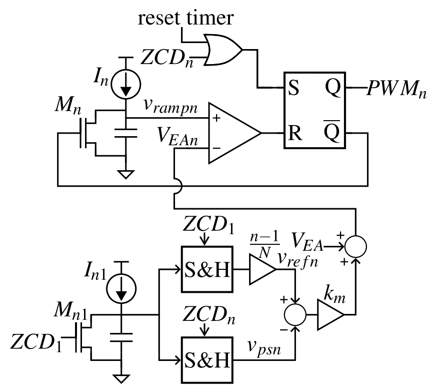

Fig. 5. Phase-shift control and PWM generation of a single slave channel using analog circuitry with the closed-loop method and turn-off adjustment by altering the voltage error amplifier signal.

low-pass filter to sense the phase shift leads to a slow dynamic response of the control loop and can lead to significant phase error. In [10] a closed-loop scheme is adopted where the phase shift and switching period are sensed using sample-and-hold blocks. This method is more advantageous than the closed-loop PLL method as it does not require low-pass filtering of the sensed phase shift, thus improving the tracking performance of the control loop. This method is depicted in Fig. 5. The constant current source I_{n1}, transistor M_{n1} and ramp capacitor are used to generate a ramp signal. This ramp signal is then fed into two separate sample-and-hold blocks triggered by ZCD_1 and ZCD_n. The output of the sample-and-hold triggered by ZCD_1 is a voltage proportional to the switching period of the master channel. The signal is scaled by the factor $\frac{n-1}{N}$ to generate the reference signal of the control loop, and is denoted v_{refn}. The output of the sample-and-hold block triggered by ZCD_n is a voltage proportional to the current phase shift between the master channel and the n^{th} slave channel. This voltage is denoted v_{psn}. An error signal is generated by subtracting v_{psn} from v_{refn}. A closed feedback loop is formed by adjusting the error signal by a gain of k_m, and adding the signal to the voltage error signal to adjust the switches turn-off instant. It is also possible to adjust the switches turn-off instant by adjusting the slope of the PWM ramp signal of the slave converter as in Fig. 4.

B. Other Existing Solutions

It is also possible to interleave multiple channels of a BCM boost converter using an open-loop method [12]–[14]. The open-loop method works by assigning one of the interleaved channels as the master and the others as the slaves. The master works as a standalone converter with its own ZCD circuit, therefore the master channels MOSFET turn-on instant is always triggered by it's own ZCD circuit. The turn-on instants of the MOSFETs in the slave channels are obtained by delaying the ZCD signal of the master channel with a time delay of $\frac{n-1}{N} \times t_{sw1}$. The open-loop method suffers from severe sub-harmonic oscillations when implemented using voltage-mode control for duty cycles greater than 0.5 [14], meaning it must be implemented with current-mode control which requires additional sense circuitry. The slave converter must have a lower inductance than the master channel to prevent it entering into CCM. As a result, the open-loop method also requires the ability to sense which channel has the lowest inductance. If there is only a small mismatch in the boost inductance of each channel the slave converter operates slightly in DCM, and valley switching is ensured. However, if there is significant mismatch between the boost inductances of both channels, the slave channel operates in DCM and loses its valley-switching operation.

Several examples of digitally-controlled interleaved BCM boost converters already exist in literature. These examples maintain their phase shift by either open-loop master-slave control [15], or by the use of feed-forward algorithms to estimate the converter's switching period [16], however this method also does not ensure BCM operation and valley switching if the system is disturbed.

There are very few examples of 3-channel interleaved BCM boost converters [16], [17] described in literature, compared to 2-channel interleaved BCM boost converters [8]–[15]. Similarly, although there are many commercially available analog PFC control integrated circuits (ICs) available on the market for 2-channel BCM boost converters, such as the FAN9611, UCC28063 and NCP1631, there are currently no PFC control ICs for more than 2 channels. Using a digital microcontroller makes it possible to build an interleaved BCM boost converter with more than 2 channels, provided the microcontroller has sufficient suitable peripherals for the number of channels.

C. Proposed Digital Closed-Loop Solution

In this paper, a digital closed-loop solution is proposed to maintain the correct phase shifts for a multi-channel BCM boost converter. The last few decades have seen significant improvement in microcontroller and digital-signal-processor technologies, with better CPUs and dedicated power electronics peripherals at lower costs. Digital microcontroller technology is also less prone to temperature and process variations. Digital control also gives the designer much more design flexibility, for instance in [2] the output voltage transient reponse of a 2-channel BCM boost converter is

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improved with digital control by using an adaptive gain to increase the systems bandwidth at low input voltage. These advantages have led to the widespread adoption of digital control by power supply designers [18].

The implementation of the phase-shift feedback control, and the PWM generation of the master and a single slave channel, as described in this paper, are shown in Fig. 6. The switching period of the master channel is measured by feeding the ZCD_1 signal of the master channel into a capture peripheral on the microcontroller. The capture peripheral has a digital timer independent of the CPU that can be used to measure the time between the ZCD pulses. As a result, it is possible to measure the switching period of the master channel every switching period. This is equivalent to the sample-and-hold method used in the analog solution of Fig. 6. The feedback control is accomplished by executing a feedback algorithm in the microcontroller CPU. The feedback algorithm reads the sensed switching period and phase shift from each capture peripheral. It then calculates the reference for each slave channel t_{ref_n} based on the sensed switching period of the master channel. The phase-shift error is determined by subtracting the sensed phase shift from the reference phase shift. The phase-shift error is used to adjust the on-time of each channel to ensure the desired phase shift is maintained. This method uses a similar feedback control as the analog solution shown in Fig. 6. The analog solution has an advantage that the turn-off instant of the slave channels are updated by the feedback network on every switching cycle. Attempting to update the turn-off instant of the microcontroller cycle by cycle requires a very expensive microcontroller. This is because the phase-shift algorithm executed by the CPU would have to run in an interrupt every switching instance, and therefore the microcontroller needs to execute the phase-shift control algorithm faster than the minimum switching period of the boost converter. This would require a microcontroller with a powerful CPU and high clock frequency, which is more expensive. A better solution is to run the phase-shift control algorithm at a fixed sampling period T_m which is much lower than the minimum switching period of the converter. This enables a much cheaper microcontroller to be used.

The microcontroller uses a compare or PWM peripheral to generate the PWM signals of each boost converter channel. The timing diagram of Fig. 7 demonstrates how the PWM peripheral for each channel is configured. The PWM signal is configured to turn on when the counter register of the PWM timer $TBCTR$ has a value of $TBPRD - t_{onn}$, where $TBPRD$ is the constant value stored in the period register of the PWM peripheral. The PWM peripheral is also configured to load the $TBCTR$ register with a value of $TBPRD - t_{onn}$ when the ZCD signal is triggered. When the $TBCTR$ reaches a value of $TBPRD$ the PWM signal is set low, and the counter restarts. Using this method results in the PWM signal of each channel having a natural reset timer. If the ZCD signal is not triggered, the $TBCTR$ continues counting until it reaches a value of $TBPRD - t_{onn}$. This method is helpful as sometimes the ZCD signal is not triggered, for instance during converter start-up or at very light load when the on-time becomes zero.

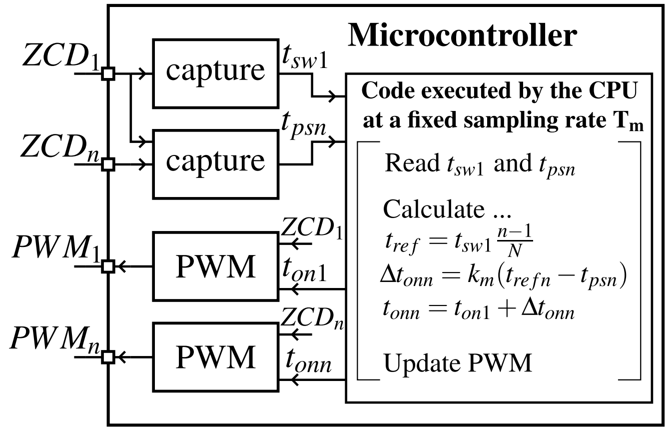

Fig. 6. Phase-shift control and PWM generation of the master and a single slave channel using digital circuitry with the closed-loop method and turn-off adjustment made by altering the slave channels on-time.

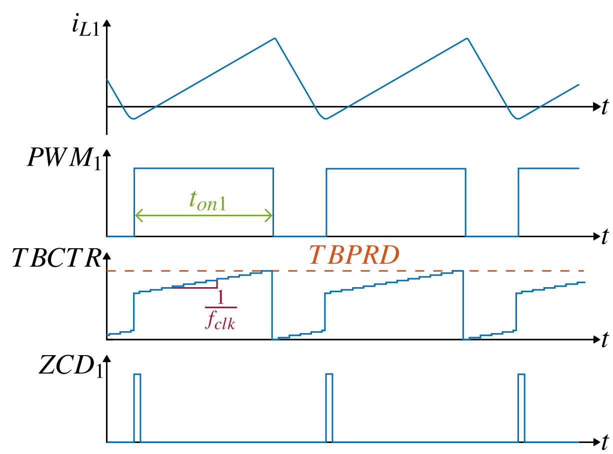

Fig. 7. Timing diagram for the PWM generation of the master channel using digital circuitry.

This paper is divided into four different sections as follows. Section I provides a brief review of how the valley-switching operation works and how it reduces power losses. Section II describes the operation and design of the phase-shift control loop. Section IV demonstrates the experimental results of a prototype 1 kW multi-channel BCM converter, demonstrating correct interleaving action for 2-channel and 3-channel operation.

II. Valley Switching

The main advantage of using a closed-loop control scheme to maintain the correct phase shifts is that each channel has its own ZCD circuit which ensures valley-switching operation is always maintained. This reduces switching losses. The valley switching of the BCM converter can be explained by looking at a single channel of the boost converter with the MOSFET drain-source capacitance C_{ds} as shown in Fig. 8.

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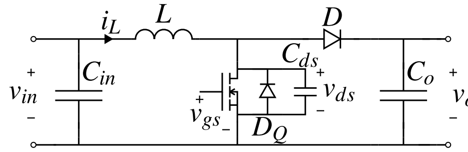


Fig. 8. A single channel of the interleaved boost converter including the MOSFET drain-source capacitance and body diode.

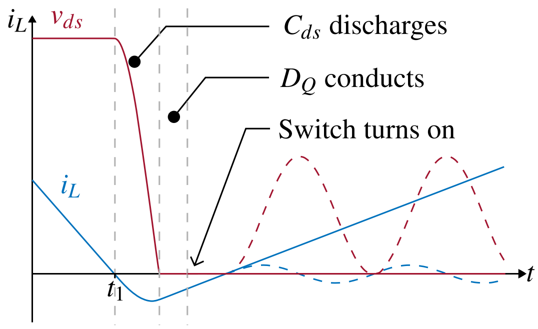


Fig. 9. Zero-voltage switching $v_{in} < \frac{1}{2}v_o$.

Fig. 9 and Fig. 10 show the behaviour of the drain-to-source voltage v_{ds} and inductor current i_L during MOSFET turn-off. As the inductor current discharges to zero, the diode D is forward biased, therefore $v_{ds} = v_o$, where v_o is the output voltage. Once i_L reaches zero the MOSFET remains off, and the capacitance C_{ds} begins to discharge through boost inductor L into the input capacitor C_{in}. During this region $i_L(t)$ and $v_{ds}(t)$ can be described using (1) and (2) respectively, where the time t_1 is defined in Fig. 9 and Fig. 10;

$$i_L(t) = -\omega_r C_{ds}(v_o - v_{in})sin(\omega_r(t - t_1)) \tag{1}$$

$$v_{ds}(t) = v_{in} + (v_o - v_{in})cos(\omega_r(t - t_1)) \tag{2}$$

where v_{in} is the input voltage and $\omega_r = 1/\sqrt{LC_{ds}}$ is the circuit's resonant frequency. Zero-voltage switching is achieved when $v_{in} < \frac{1}{2}v_o$. Once v_{ds} fully discharges to 0 V, the negative inductor current forces the MOSFET's body diode D_Q to conduct. The ZCD circuit then triggers the switch to turn on while $v_{ds} = 0$, as shown by the solid lines of Fig. 9. If the MOSFET remains off, the circuit enters DCM as shown by the dashed lines of Fig. 9.

If $v_{in} > \frac{1}{2}v_o$, then C_{ds} does not fully discharge, but instead reaches a valley at $v_{ds} = 2v_{in} - v_o$ as shown in Fig. 10. The ZCD ensures that the switch turns on at this valley to minimize the switching losses.

The valley switching is achieved in the experimental prototype by using the ZCD circuit shown in Fig. 11. The ZCD circuit consists of an auxiliary winding on the boost inductor, a current-limiting resistor R_{zcd}, a capacitor C_{zcd} that adds a small amount of low-pass filtering and a zener diode D_z that clamps the voltage v_{zcd} to between 0 and 5 V, so that it can be input to a microcontroller pin. Fig. 12 shows a timing diagram of the inductor current, inductor voltage v_L and the voltage v_{zcd} created by the ZCD circuit. The voltage v_{zcd} is a square wave, with a falling edge that corresponds to the instant the boost converter MOSFET should be turned on

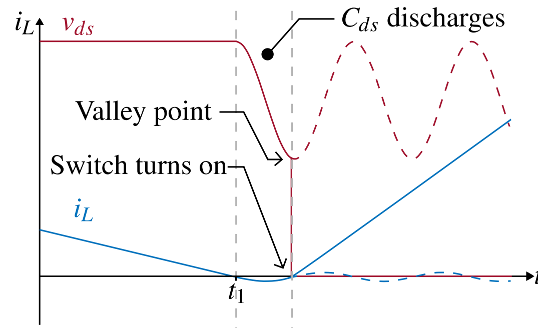


Fig. 10. Near-zero-voltage switching $v_{in} > \frac{1}{2}v_o$.

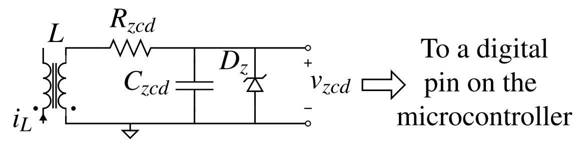


Fig. 11. Zero-current-detection circuit.

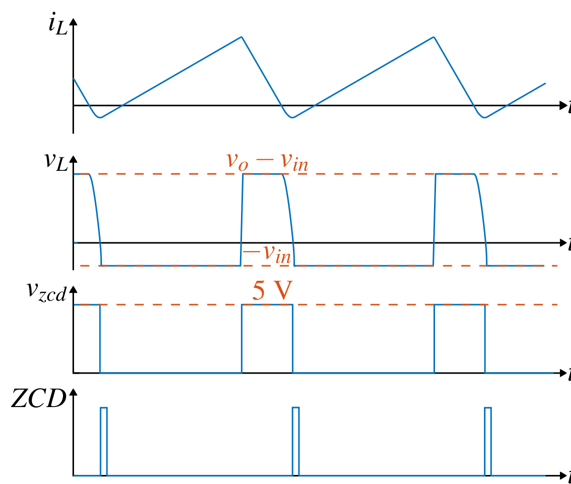


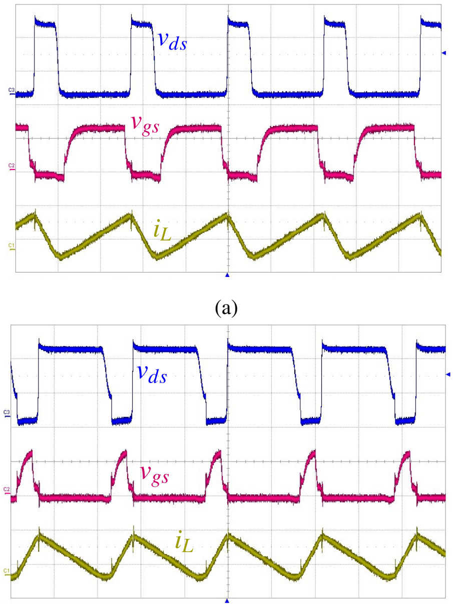
Fig. 12. Timing diagram for the ZCD generation.

to achieve valley switching. The voltage v_{zcd} is connected to a regular digital pin on the microcontroller, and the PWM peripheral is configured to trigger MOSFET turn-on on a falling edge of this signal. This method is advantageous because it does not require a comparator, which makes the implementation cheaper. Requiring an external comparator would add cost and, also, any available comparators in the microcontroller can now be used for safety functions, such as over-voltage and over-current protections.

Fig. 13 shows experimental results of the prototype converter operating in BCM with valley switching when $v_{in} =$ 100 V and $v_{in} =$ 300 V.

III. Phase-Shift Control

In this section the design of the phase-shift control algorithm is discussed. The phase-shift control is responsible for maintaining the correct phase shift between the boost inductor currents.



(b)

Fig. 13. v_{ds}, v_{gs} and i_L waveforms showing valley switching for (a) v_{in} = 100 V and (b) v_{in} = 300 V (v_{ds}: 200 V/div, v_{gs}: 10 V/div, i_L: 2 A/div, timebase : 2 µs/div).

The output voltage of the boost converter described in this paper is regulated using constant-on-time control (COTC) [2]. By this method, the sensed output voltage is subtracted from a constant reference to generate an error signal, which is input to a voltage compensator. The voltage compensator calculates the required on-time t_{on} so that the output voltage tracks the reference signal.

The time-averaged input-current drawn by the converter can be calculated using;

$$i_{in} = \frac{N}{2}\frac{v_{in}}{L}t_{on} \tag{3}$$

Given that N and L are constant in (3), the converter has near unity power factor provided t_{on} is near constant, therefore i_{in} equals a constant multiplied by v_{in}. This is the basis of COTC.

The phase-shift control algorithm takes the on-time calculated by the voltage compensator and adjusts it to calculate the individual on-time for each channel of the converter to maintain the desired phase shift between the different channels.

A. System Model

To design the phase-shift control algorithm, it is necessary to first develop a mathematical system model describing how adding a perturbation of $t_{\Delta n}$ to the individual on-time of a slave channel effects the phase shift t_{psn} between the master and the n_{th} slave channel of the converter. The effect of adding the perturbation $t_{\Delta n}$ to t_{onn}, so that $t_{onn} = t_{on1} + t_{\Delta n}$ is shown in Fig. 14 over a single switching cycle of the inductor currents i_{L1} and i_{Ln}. In order to simplify our analysis, it is assumed that the effects of the resonance between the boost inductor and MOSFET drain-source capacitance are negligible. If $t_{psn}[k]$ is the phase shift between the master and n_{th} slave channel during the k^{th} switching cycle, the phase shift of the $(k+1)^{th}$ switching cycle can be calculated by,

$$t_{psn}[k+1] = t_{psn}[k] + \frac{t_{\Delta 1} t_{sw1}}{t_{on1}} \tag{4}$$

where t_{sw1} is the switching period of the master channel. This change in the phase shift is graphically displayed in Fig. 14.

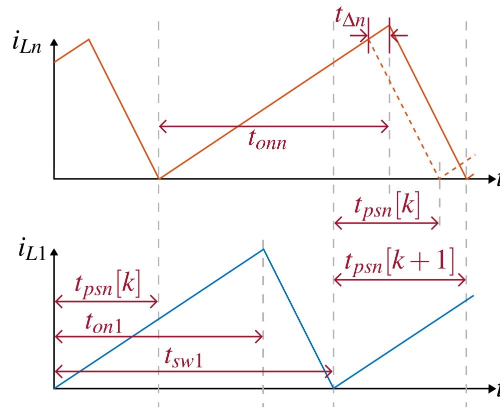


Fig. 14. Change in phase shift due to an on-time perturbation $t_{\Delta n}$.

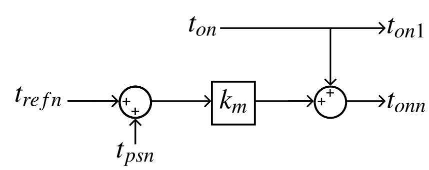


Fig. 15. Phase-shift control loop block diagram structure.

By expanding (4) over a total of K switching cycles, the phase shift of the $(k+K)^{th}$ switching cycle can also be calculated by (5), where it is assumed the t_{sw1} and t_{on1} remain constant over the K switching cycles.

$$t_{psn}[k+K] = t_{psn}[k] + K\frac{t_{\Delta n} t_{sw1}}{t_{on1}} \tag{5}$$

The open-loop system model is now described by (5). This equation is in the next subsection to design a closed feedback loop to control the phase shift t_{psn}.

B. Closed-Loop Control

Closed-loop control is used to ensure that the phase shift t_{psn} tracks a reference phase shift t_{refn}. Fig. 15 shows the proposed structure of the phase-shift control loop. The error signal given by $t_{refn} - t_{psn}$ is multiplied by the gain k_m to form a proportional controller, and the result is added to the on-time t_{on1} to give the on-time t_{onn} for that slave channel.

The value of k_m must be selected to obtain the best tracking performance while still ensuring the stability of the system under all operating conditions. Based on Fig. 15 the phase-shift control algorithm can be described by the following equation.

$$t_{onn} = t_{on1} + k_m(t_{refn} - t_{psn}[k]) \quad (6)$$

Substituting $t_{\Delta n} = t_{onn} - t_{on1}$ into (6), the following expression is obtained.

$$t_{\Delta n} = k_m(t_{refn} - t_{psn}[k]) \quad (7)$$

By combining (7) with the expression obtained earlier in (5), the effect the phase-shift control feedback has on the phase shift t_{psn} after K switching cycles can be obtained as follows.

$$t_{psn}[k+K] = t_{psn}[k] + Kk_m \frac{t_{sw1}}{t_{on1}}(t_{refn} - t_{psn}[k]) \quad (8)$$

The phase-shift control algorithm given in (6) is executed at a constant sampling rate, with a sampling period of T_m. A total of $K = T_m/t_{sw1}$ switching cycles occur over a single execution of the phase-shift control algorithm. A time-averaged approximation is taken by substituting this value of k into (8). As a result, the value of the phase shift t_{psn} after a single execution of the algorithm can be obtained as follows.

$$t_{psn}[i+1] - t_{psn}[i] = k_m \frac{T_m}{t_{on1}}(t_{refn} - t_{psn}[i]) \quad (9)$$

where i is an integer number describing the number of executions of the phase-shift control algorithm which have taken place. For ideal phase-shift tracking, the value of t_{psn} after a single execution of the algorithm should equal t_{refn}. Therefore, (9) becomes

$$t_{refn} - t_{psn}[i] = k_m \frac{T_m}{t_{on1}}(t_{refn} - t_{psn}[i]) \quad (10)$$

By re-arranging (10), the value of k_m that gives the best tracking performance can be calculated by

$$k_m = \frac{t_{on1}}{T_m} \quad (11)$$

C. Phase-Shift Control Stability

The phase-shift control loop remains stable provided that after a single execution of the phase-shift control algorithm, the phase shift t_{psn} stays bound to the region $0 < t_{psn} < t_{sw1}$. Re-arranging (9), the following equation can be found to describe the phase shift t_{psn} after $(i+1)$ execution cycles of the control algorithm,

$$t_{psn}[i+1] = k_m \frac{T_m}{t_{on1}}(t_{refn} - t_{psn}[i]) + t_{psn}[i] \quad (12)$$

The phase shift $t_{psn}[i]$ is bound to the region $0 < t_{psn}[i] < t_{sw1}$. The worst-case scenario occurs when either $t_{psn}[i] = 0$ or $t_{psn}[i] = t_{sw1}$. Looking first at the case where $t_{psn}[i] = 0$, $t_{psn}[i+1]$ is given by

$$t_{psn}[i+1] = k_m \frac{T_m}{t_{on1}} t_{refn} \quad (13)$$

Applying this result to the inequality $0 < t_{psn}[i+1] < t_{sw1}$, the following inequality can be obtained for the values of k_m for which the system is stable.

$$0 < k_m < \frac{t_{on1}}{T_m}\frac{t_{sw1}}{t_{refn}} \quad (14)$$

Now looking at the case where $t_{ps1}[i] = t_{sw1}$, $t_{psn}[i+1]$ is given by,

$$t_{psn}[i+1] = k_m \frac{T_m}{t_{on1}}(t_{refn} - t_{sw1}) + t_{sw1} \quad (15)$$

Again, applying the result from (15) to the inequality $0 < t_{psn}[i+1] < t_{sw1}$, a second inequality can be obtained for the values of k_m for which the system remains stable.

$$0 < k_m < \frac{t_{on1}}{T_m}\frac{t_{sw1}}{t_{sw1} - t_{refn}} \quad (16)$$

The inequalities given in (14) and (16) now describe the values of k_m for which stability is achieved in terms of the tracking reference t_{refn}. The reference signal is calculated from the switching period t_{sw1} by $t_{refn} = t_{sw1}\frac{n-1}{N}$. Substituting this value for t_{refn} into the inequalities (14) and (16) gives the following.

$$0 < k_m < \frac{t_{on1}}{T_m}\frac{N}{n-1} \quad (17)$$

$$0 < k_m < \frac{t_{on1}}{T_m}\frac{N}{N-n+1} \quad (18)$$

However, n is an integer number, with a value in the region $2 \leq n \leq N$. The strictest condition to satisfy (17) occurs when n is at its maximum value of $n = N$. Similarly for (18), the strictest condition occurs when n is at its minimum value of $n = 2$. Applying the strictest condition for n to both (17) and (18) results in the following single inequality.

$$0 < k_m < \frac{t_{on1}}{T_m}\frac{N}{N-1} \quad (19)$$

For 2-channel operation $N = 2$, therefore k_m must satisfy $0 < k_m < 2\frac{t_{on1}}{T_m}$ to remain stable. Fig. 16 demonstrates the waveshape of the input current drawn by the converter in 2-channel operation when k_m satisfies the stability inequality and when k_m is increased so that it no longer satisfies this inequity.

Fig. 16 is taken at an output power of 225 W, and an input rms voltage of 200 V. Under this condition the measured on-time t_{on1} is 0.9 µs. For the initial two half-line cycles the gain k_m is set to a value of $k_m = \frac{1.04\,\mu s}{T_m}$. Therefore the stability inequality given by $0 < k_m < \frac{1.8\,\mu s}{T_m}$ is satisfied, and the input current maintains the correct interleaving with low peak-to-peak current ripple. Then, the gain k_m is increased to $k_m = \frac{2.08\,\mu s}{T_m}$ so that the stability inequality is not satisfied. The phase-shift control loop is no longer able to maintain correct interleaving and the input current has a very large peak-to-peak ripple. For the last half-line cycle shown in the

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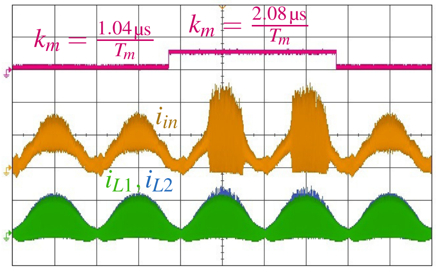


Fig. 16. Input current i_{in} and inductor currents i_{L1} and i_{L2} when the gain k_m is toggled from a value of $k_m = \frac{1.04\,\mu s}{T_m}$ to a value of $k_m = \frac{2.08\,\mu s}{T_m}$ at P_o = 225 W, t_{on} = 0.9 µs and a rms line voltage of 200 V. (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div, timebase : 5 ms/div).

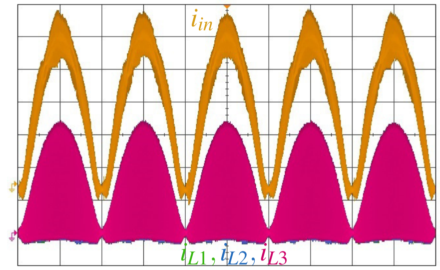
figure, k_m is reduced again to $k_m = \frac{1.04\,\mu s}{T_m}$ and the system becomes stable once more.

D. Adaptive Gain

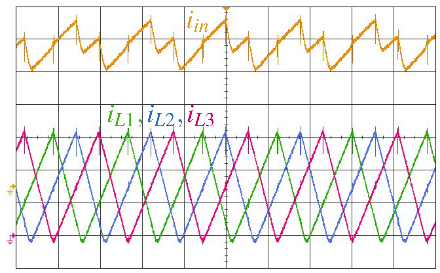
If a proportional control scheme is used where k_m has a constant value, then k_m must be set to satisfy the stability inequality (19). Therefore, the value of k_m is designed based on the minimum on-time $t_{on(min)}$ that occurs for multi-channel operation and can be calculated by $k_m = \frac{t_{on(min)}}{Tm}$. A minimum on-time exists because at lighter loads the converter turns off channels until only a single channel is operating. At low power levels this value for k_m works fine because its value is close to the value that gives best tracking performance described by (11). However, when the converter is operating at high power levels and low input voltage the on-time dramatically increases. As a result, the chosen value for k_m becomes much less than the value given by (11). This effect is shown in Fig. 17 when the on-time is at its maximum operating value at P_o = 700 W and an rms line voltage of 115 V. This is the maximum rated power of the prototype converter at low line. The value of k_m has been set to $\frac{0.8\,\mu s}{T_m}$.

The input current shown in Fig. 17 has a large peak-to-peak input-current ripple. This is caused by the poor tracking performance of the phase-shift control at this condition. This problem can be overcome by introducing an adaptive gain that scales the value of k_m with the operating on-time t_{on1} using the value of k_m obtained in (11). Thus, for best tracking performance the proportional gain k_m is replaced with a multiplier block that multiples the error signal by t_{on1} and a proportional gain of $1/T_m$, as is shown in Fig. 18.

Fig. 19 shows the same waveforms as Fig. 17 at the same operating condition but when an adaptive gain is used for k_m. By comparing the waveforms of Fig. 17 to Fig. 19 it is clear using an adaptive gain dramatically reduces the input current peak to peak ripple, and improves the tracking performance of the phase-shift control loop. As well as this, given that the the value of k_m used for the adaptive gain always satisfies the stability inequality given in (19), it is evident the use of an adaptive gain always ensures the phase-control loop remains stable for all values of t_{on}.



(a)



(b)

Fig. 17. i_{L1}, i_{L2}, i_{L3} and i_{in} when all 3 boost converter channels are enabled at P_o = 700 W and a rms line voltage of 115 V when k_m is a constant gain (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div).

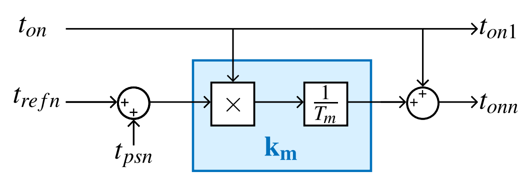
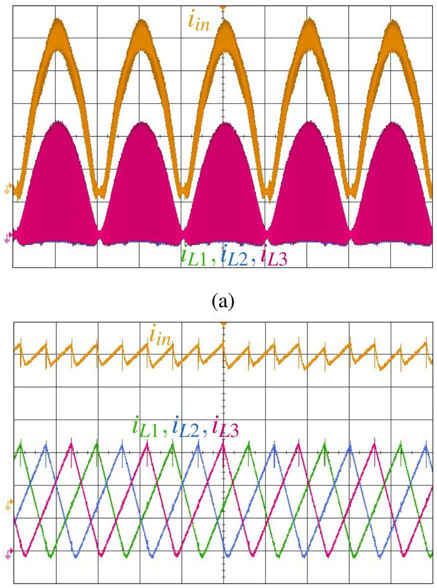


Fig. 18. Phase-shift control loop block diagram structure when an adaptive gain is used.

E. Appropriate Value for T_m

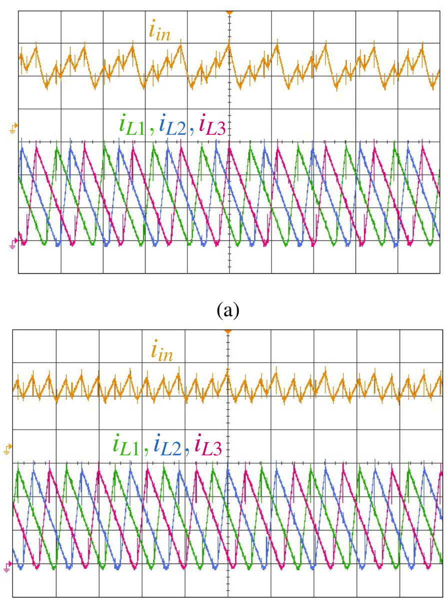
Choosing an appropriate value of the rate of execution of the phase-shift control algorithm is important, because the slower the control algorithm, the less computational power is required to execute it. Therefore, the cheaper the microcontroller that can be used. However if the the value of T_m is set too slow, there exists significant quantization error in the phase-shift control loop. This phenomenon is worst at low levels of on-time and switching period, which exist at high input voltage, and the lowest power level for the operation of a given number of channels. Fig. 20 demonstrates the waveshape of the input current and inductor currents when 3 channels of the boost converter are enabled, at an output power of 600 W, and an input rms line voltage of 230 V.

This is the near worst-case operating condition for the quantization noise created when T_m is too slow, as it is near the maximum input voltage and minimum power for 3-channel operation. Below this power level the converter switches to 2-channel operation, therefore the switching period and on-time are increased and this type of quantization error reduces. In Fig. 20(a) the value of T_m is set to 30 µs,



(b)

Fig. 19. i_{L1}, i_{L2}, i_{L3} and i_{in} when all 3 boost converter channels are enabled at P_o = 700 W and a rms line voltage of 115 V when k_m is an adaptive gain (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div).



(b)

Fig. 20. i_{L1}, i_{L2}, i_{L3} and i_{in} when all 3 boost converter channels are enabled at P_o = 600 W and a rms line voltage of 230 V (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div, timebase : 5 µs/div). (a) When T_m is set to have an execution frequency of 34 kHz (b) and when T_m is set to have an execution frequency of 100 kHz.

whereas in Fig. 20(b), the value of T_m is set to 10 µs. It is clear from comparing both figures, that having T_m set to too low a value results in poor tracking performance.

TABLE I
LIST OF PARAMETERS

Parameter	Value
Microcontroller	XMC1402-Q040X0032
Boost inductance L	130 µH
Input rms voltage	85 V to 265 V
Output voltage	400 V
Switching frequency	100 kHz to 550 kHz
Sampling period T_m	14.3 µs
Output Power P_o	0 W to 1000 W

IV. EXPERIMENTAL RESULTS

A 3-channel BCM boost converter prototype was built to verify the proposed control scheme. The main parameters of the 3-channel boost converter are given in Table. I. The microcontroller runs the code for the voltage-loop in a slow 5 kHz interrupt. The code for the phase-shift control is run in a faster 70 kHz interrupt.

Fig. 21 shows the inductor currents and input current when operating at a low input rms line voltage of 115 V in 2-channel operation. Near-perfect interleaving operation is maintained at this operating condition. Fig. 21(c) shows the same waveshapes, but at the zero-crossing point of the line voltage, demonstrating the control scheme also works well at this point.

Fig. 22 shows the converter operating at 500 W with an input rms line voltage of 230 V. Near-perfect interleaving operation can be observed when operating in 2-channel mode at this operating condition, as demonstrated by the perfect shape of the input current i_{in}, and the low peak-to-peak current ripple.

Similarly, Fig. 23 shows the converter operating with 3 channels enabled at the full rated output power of 1000 W with an input rms line voltage of 230 V. There is near-perfect interleaving operation at this operating condition, as demonstrated again by the low peak-to-peak current ripple of the input current.

At lighter loads, either one or two channels of the converter are shut-off to improve the converter's efficiency and also reduce the switching frequency of the converter which increases drastically at lighter loads. Therefore, the phase-shift control algorithm needs to be capable of operating with either one channel enabled, two channels enabled, or with all three channels enabled. Fig. 24 shows the waveshape of the inductor currents and input currents when the converter transitions from 3-channel to 2-channel operation.

At the instant the phase-shift control loop changes from 3-channel operation to 2-channel operation, the third channel is disabled, and the on-time t_{on} is scaled by a factor of $3/2$. This keeps the average instantaneous input current the same. The phase-shift control loop which controls t_{ps3} is disabled and the reference of the phase-shift control loop controlling t_{ps2} is stepped from $t_{sw1}/3$ to $t_{sw1}/2$. It then takes the controller two to three cycles of the phase-shift control algorithm execution to transition from a 120° phase shift,

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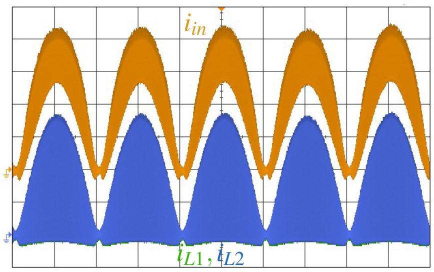
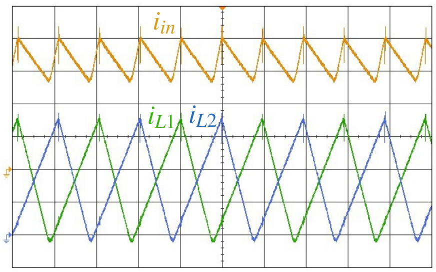
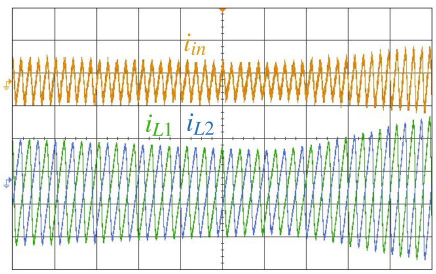


(a)

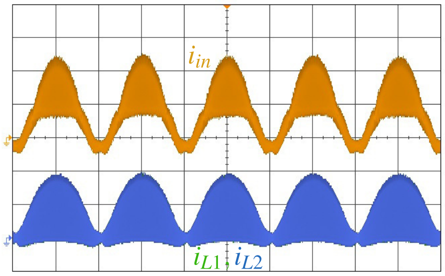


(b)

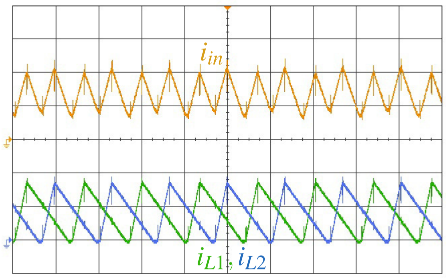


(c)

Fig. 21. i_{L1}, i_{L2} and i_{in} when 2 boost converter channels are enabled at P_o = 500 W and a rms line voltage of 115 V (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div). And (c) at the zero-crossing point of the line voltage (i_{in}: 200 mA/div, i_{L1}: 100 mA/div, i_{L2}: 100 mA/div, timebase : 20 µs/div) .

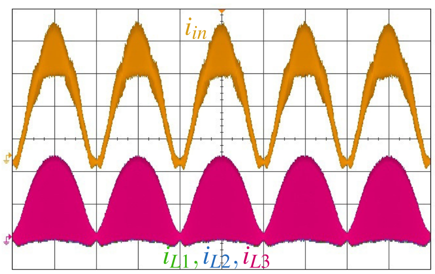


(a)

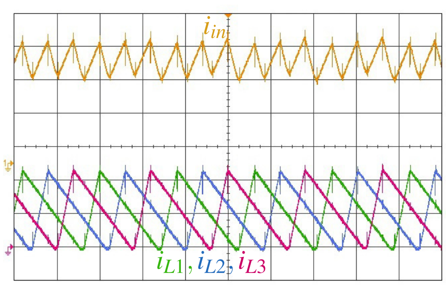


(b)

Fig. 22. i_{L1}, i_{L2} and i_{in} when 2 boost converter channels are enabled at P_o = 500 W and a rms line voltage of 230 V (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div).



(a)



(b)

Fig. 23. i_{L1}, i_{L2}, i_{L3} and input current i_{in} when all 3 boost converter channels are enabled at P_o = 1000 W and a rms line voltage of 230 V (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div).

to a 180° phase shift. A similar transition occurs when the converter transitions from 2-channel to 3-channel operation.

Fig. 25 shows the inductor currents as the converter transitions from single-channel operation to 2-channel operation. When the second channel and phase-shift control loop for t_{ps2} are re-enabled, t_{ps2} has a random initial value in the range $0 < t_{ps2} < t_{sw1}$. The phase-shift control loop takes two to three executions before t_{ps2} settles to it's reference at $t_{sw1}/2$. This transition is shown in Fig. 25.

The main advantage of disabling boost converter channels at lower power levels is that it increases the converter's efficiency at lighter load. The efficiency of the prototype converter is given in Fig. 26(a) for an input rms line voltage of 230 V, while Fig. 26(b) gives the efficiency for a rms line voltage of 115 V. It is clear that at lighter load, reducing the number of channels increases efficiency. This is mainly due to the lower switching frequency which reduces switching losses and inductor core losses.

A similar effect is seen when comparing the power factor in 1-channel, 2-channel and 3-channel operation. This comparison against output power is given in Fig. 27(a) for an rms line voltage of 230 V, and in Fig. 27(b) for an rms line voltage of 115 V. In is evident from these figures that disabling the number of channels at lighter load increases the power quality of the converter. At higher power levels it

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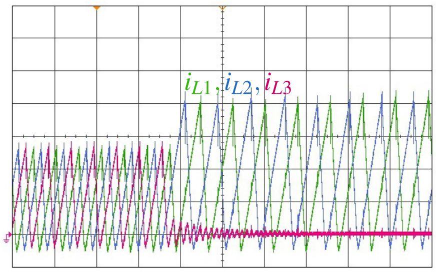

Fig. 24. i_{L1}, i_{L2} and i_{L3} when entering 2-channel BCM (i_{L1}: 1 A/div, i_{L2}: 1 A/div, i_{L3}: 1 A/div, timebase : 30 µs/div).

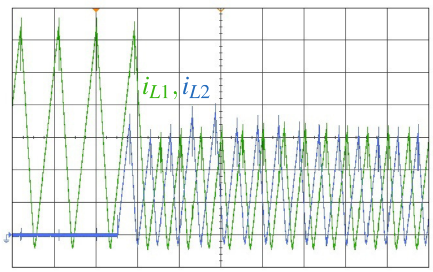

Fig. 25. i_{L1} and i_{L2} when entering 2-channel BCM (i_{L1}: 1 A/div, i_{L2}: 1 A/div, timebase : 30 µs/div)

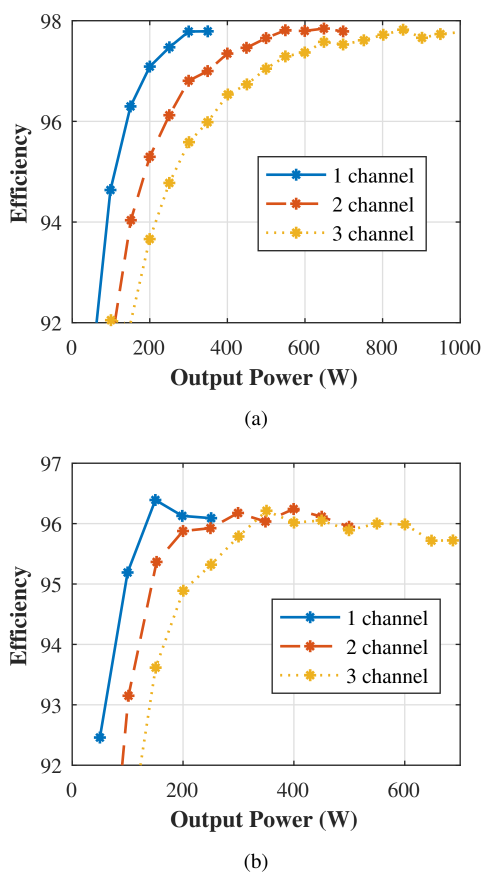

Fig. 26. Efficiency against output power for 1-channel, 2-channel and 3-channel operation at (a) an input rms line voltage of 230 V and (b) an input rms line voltage of 115 V.

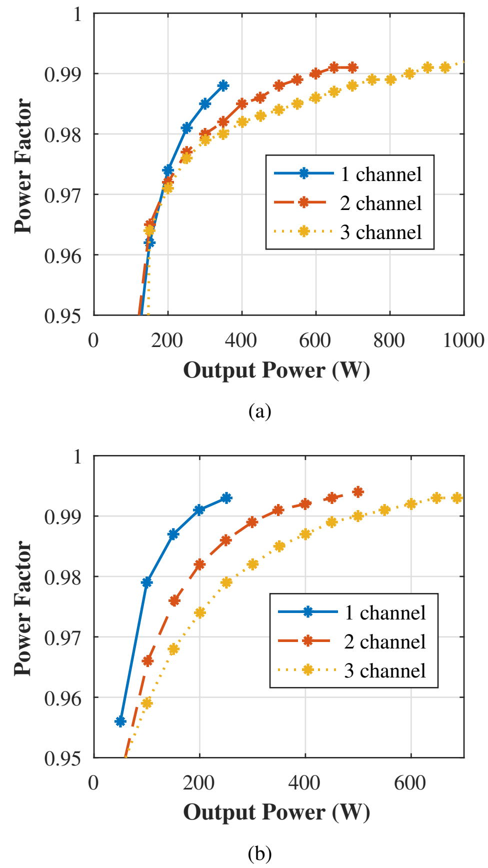

Fig. 27. Power factor against output power for 1-channel, 2-channel and 3-channel operation at (a) an input rms line voltage of 230 V and (b) an input rms line voltage of 115 V .

is better to use multiple channels to reduce current stress and thermal stress in components as well as the DM conducted EMI drawn by the converter.

V. Conclusion

A closed-loop digital control strategy which maintains correct interleaving operation of a multi-channel BCM boost converter has been presented. The importance of using separate ZCD circuits for each channel of the interleaved converter to maintain valley-switching operation has been discussed, and detail of how the ZCD circuit interfaces with the microcontroller were given.

A digital closed-loop control scheme to maintain correct interleaving operation of the converter was proposed. A mathematical analysis was derived to find the gain of a proportional controller which provided the best tracking performance and maintained stability of the control loop. An adaptive gain was incorporated into the control loop to give best tracking performance and ensure stability under all operating conditions.

Finally, the experimental results of a prototype 3-channel converter were shown, demonstrating correct interleaving operation of the converter operating in 2-channel and 3-channel modes.

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Robert T. Ryan received the B.E. degree from University College Cork (UCC), Cork, Ireland in 2015, where he is currently working toward the Ph.D. degree in the Power Electronics Research Laboratory in the field of ac-dc power converters for power factor correction applications. His main research focus is using of digital control to improve the performance and control of ac-dc converters, while maintaining low costs. His other research interests include the use of wide-bandgap semiconductors, design of high-frequency magnetic components, dc-dc isolated resonant converters and EV on-board charging.

Richard J. Morrison Richard J.Morrison received the B.E. degree from University College (UCC), Cork, Ireland in 1988, and has focused on power converter development for most of his career. He was conferred with a Ph.D. by UCC in 2000 for his work on power-factor-corrected interruptible-power-supply topologies. He is currently employed by Excelsys, an Advanced Energy company, as a design engineer for modular ac/dc supplies.

Diarmuid N. Hogan received his B.E. degree from the University of Bolton, England in 1995, and shortly thereafter joined Computer Products Ireland (which subsequently became Artesyn Technologies in 1998). He specialised in the design and development of dc-dc and ac-dc switch-mode power supplies and rose through the ranks of the Custom Power Group to become a Senior Design Engineer leading the development of power solutions for large telecoms companies. He joined Excelsys Technologies (subsequently to become an Advanced Energy company) in 2006 and has formed a world class power development team to create best in class innovative modular power supply solutions for the high reliability market. Diarmuid has Chartered Engineer status with Engineers Ireland since 2012 and currently sits on the Technical Committee of the European Power Supply Manufacturers Association (EPSMA).

John G. Hayes received the B.E. degree from University College Cork (UCC), the M.S.E.E. degree from the University of Minnesota, Minneapolis - St. Paul, the M.B.A. degree from California Lutheran University, and the Ph.D. from University College, Cork in 1986, 1989, 1993 and 1998, respectively. From 1986 to 1988, John held a research fellowship for power electronics under Prof. Ned Mohan at the University of Minnesota.

From 1988 to 1990, he worked at Power One Inc. (now ABB Solar), of Camarillo, CA, designing linear and switching ac-dc power converters. In 1990, He joined General Motors Advanced Technology Vehicle (formerly Hughes Aircraft Company and Delco Electronics), in Culver City, and later Torrance, CA, where he worked extensively as a design engineer and technical manager in the fields of propulsion drives and battery charging for electric vehicles, especially for heavy-duty vehicles and the General Motors EV1 electric car. From 1995 to 1997, he pursued a PhD part-time as a Howard Hughes Corporate Fellow while continuing to work as a design engineer at GM. Subsequently, he worked as a technical manager on EV battery chargers and infrastructure.

John joined the academic staff at UCC in late 2000 and currently teaches power engineering and power electronics and drives. His research interests are power electronics, machines, and magnetics for automotive, and energy applications. John directs the Power Electronics Research Laboratory (PERL) at UCC. The focus of PERL in recent years has been on industrial collaborations with global leaders, such as Analog Devices, United Technologies, General Motors, Moog, Excelsys, and SMA. John and his co-authors received the William M. Portnoy Award for best paper at IEEE ECCE 2011. John is the lead author, with co-author Dr. Abas Goodarzi, CEO of US Hybrid in Los Angeles, on *Electric Powertrain: Systems, Power Electronics and Drives for Electric, Hybrid and Fuel Cell Vehicles*. The publisher is John Wiley & Sons and the book was launched in early 2018.