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Digital-Based Interleaving Control for GaN-based MHz CRM Totem-pole PFC

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***Abstract*—This paper presents a comparison between the performances of different interleaving control methods for gallium-nitride (GaN) devices based MHz critical conduction mode (CRM) totem-pole power factor correction (PFC) circuit. Both closed-loop interleaving and open-loop interleaving are good for the 70 kHz CRM PFC; but for a MHz frequency CRM PFC with microcontroller (MCU) implementation, open-loop interleaving outperforms closed-loop interleaving with only a small and non-amplified phase error. After software optimization, the phase error of the open-loop interleaving is smaller than 3 degree at 1MHz, when the control is implemented by a 60 MHz low cost MCU. Significant ripple cancellation effect and differential-mode (DM) filter size reduction is achieved with good interleaving. For a 1.2 kW MHz totem-pole PFC, the DM filter size is reduced to one quarter when compared to the counterpart of a 100 kHz PFC. Last but not least, the stability of the open-loop interleaving is also analyzed indicating that the MHz CRM totem-pole PFC with voltage-mode control, open-loop interleaving, and turn-on instant synchronization can maintain critical mode operation with better stability compared to the 70 kHz CRM PFC.**

***Index Terms*— Interleaving, GaN, MHz, totem-pole PFC, MCU, DM filter**

I. INTRODUCTION

The totem-pole bridgeless power-factor-correction (PFC) circuit is becoming popular attributing to the emerging high voltage gallium-nitride (GaN) devices [1-6]. Enhancement mode GaN (e-GaN) device has no internal anti-parallel body diode, and thus reverse recovery effect is eliminated. Depletion mode GaN device in cascode structure (cascode GaN) has small reverse recovery effect contributed only by the body diode of low voltage Si MOSFET in the cascode structure. So both e-GaN and cascode GaN have significantly reduced reverse recovery effect compared to Si MOSFET in similar voltage and current rating. Furthermore, GaN device has significantly better figure-of-merit and smaller switching related loss. Taking all of the superior properties of GaN device into consideration, the simple and symmetric totem-pole bridgeless PFC topology which is not practical for Si MOSFET is suddenly widely adopted with GaN device. Hard switching GaN-based totem-pole PFC is demonstrated [1, 6] in good efficiency with 50 kHz or 100 kHz switching frequency.

According to [7-10], the soft switching operation is important in order to achieve a MHz frequency operation for 600 V GaN devices. Critical conduction mode (CRM) is the simplest way to achieve soft switching; and when applied to a boost-type PFC circuit, it is easy to achieve a good power factor with a CRM operation.

A 1.2 kW 1-3 MHz GaN-based CRM totem-pole PFC was built with close to 99% peak efficiency and more than 200 W/in^3 power density [11-13]. Figure 1 shows the circuit diagram of the two-phase interleaved totem-pole PFC with cascode GaN devices. In totem-pole PFC topology, S_{11}, S_{12}, S_{21}, and S_{22} are cascode GaN devices operating at high frequency while S_{N1} and S_{N2} are Si MOSFETs switching at line frequency. S_{11} and S_{12} form phase 1 while S_{21} and S_{22} form phase 2. In positive line cycle when the input voltage is positive, S_{N1} is always on and S_{N2} is always off; then for each phase the bottom switch is the control switch and the top switch is operating as synchronous rectifier. In negative line cycle, the functions of two switches in a half bridge are swapped therefore the topology has symmetric characteristic. S_{N1} and S_{N2} are also considered as line frequency synchronous rectifier with lower conduction loss and better control of negative current to realize ZVS of all high frequency control switches. The two phases usually operate with 180-degree phase shift to have ripple cancellation benefit for the total input current. The totem-pole PFC topology is considered as simplest boost-type bridgeless PFC topology with symmetry and good EMI characteristics.

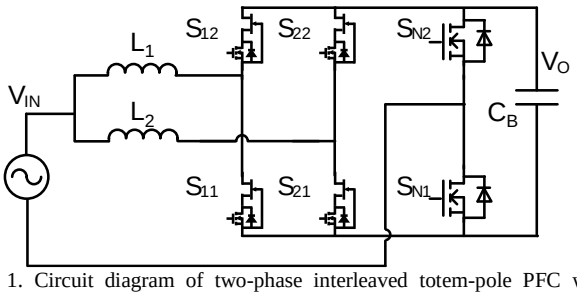

Fig. 1. Circuit diagram of two-phase interleaved totem-pole PFC with cascode GaN devices

The MHz frequency impact of the PFC is not limiting but has an even more significant impact on the input filter design. According to [14], when the switching frequency is higher, (e.g. above 400 kHz), the smaller the filter size.

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Paper [11-13] demonstrates that from 100 kHz to 1 MHz, the DM filter is simplified from 2 stages to 1 stage and the volume is reduced by 50%. It also claims that if a two-phase PFC is interleaved with a 180 degree phase shift then another 50% volume reduction is expected.

The challenge of interleaving control for a CRM PFC is that the nature of the circuit is variable frequency operation. For a given input and load condition, the frequency varies 3-5 times in a half line cycle. For different input or load conditions, the frequency range varies as well. According to literature, there are generally two categories of interleaving control methods proposed for the variable frequency CRM PFC: closed-loop interleaving [15-19] and open-loop interleaving [20-25]. For 70 kHz both methods work well in maintaining a minimal value in the phase error. . However, when the frequency is pushed 10 times higher to multi-MHz, the interleaving control becomes a new challenge.

In this paper, the impact of interleaving control on a MHz CRM totem-pole PFC and DM filter is introduced in Section II. The performance comparison between closed-loop interleaving and open-loop interleaving for MHz totem-pole PFC is then discussed in Section III. The optimization and experimental results of open-loop interleaving is presented in Section IV. Finally, the stability analysis of open-loop interleaving is elaborated in Section V.

II. Impact of Interleaving Control on MHz Totem-Pole PFC and its DM Filter

CRM PFC suffers from large current ripples. For a single phase CRM PFC, the input current ripple is always more than two times higher than its average current. Multi-phase interleaving techniques are widely used so that the total input current ripple is reduced, which is beneficial to have a lower conduction loss, a longer capacitor lifetime, and most importantly, a smaller input filter size.

For a two phase interleaved CRM PFC, when the phase shift is 180 degrees, the first order components in the input current is totally canceled while only second order and higher orders components exist. With the proposed DM noise model for CRM PFC [26], the DM noise spectrum is predicted for the dual-phase MHz totem-pole PFC (Figure 2). It is clearly shown that the ripple cancellation effect is very sensitive to phase error. Even just a few degrees phase error leads to a quick increase of the first order noise components, while the critical value is 5 degree and 1 degree for 1-stage DM filter and 2-stage DM filter respectively.

The critical value is chosen as 5 degrees, because when a 1-stage DM filter is used and the phase error is lower than 5 degree, the 40 dB/dec line firstly touches the DM noise at 2 MHz point. However, when the phase error is higher than 5 degree, it is the 1 MHz point who dominates the filter design. Thus it means the DM filter design cannot fully benefit from interleaving. For a 2-stage DM filter design, the critical value is 1 degree because 2-stage has 80 dB/dec attenuation, and thus it is more likely to be dominated by the 1 MHz point of the DM noise.

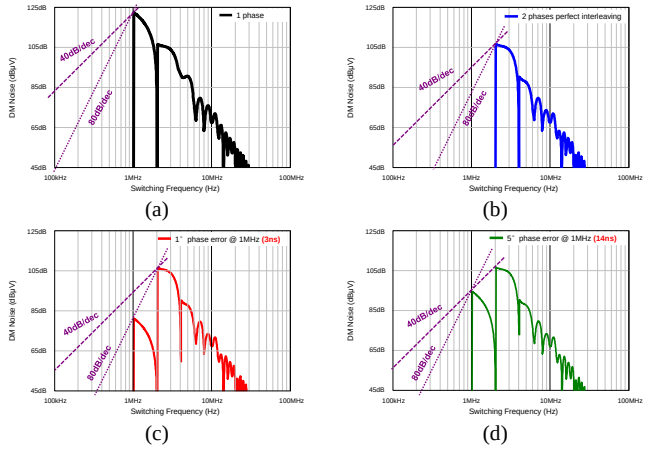

Fig. 2. Predicted DM noise spectrum for 1.2 kW MHz totem-pole PFC. (a) one phase; (b) 2 phases with perfect interleaving; (c) 2 phases with 1 degree phase error; and (d) 2 phases with 5 degree phase error

So in order to have full benefits on the DM filter, the phase error should be kept smaller than the critical value. Previously it is not a big issue to maintain a small phase error in frequency range like 70 kHz or 130 kHz PFC, however, when it increases to a multi-MHz frequency, it is really a challenge to make the phase error smaller than the critical value because only a few nano-second delay error leads to a significantly large phase error.

III. Performance Comparison between Closed-loop Interleaving and Open-loop Interleaving for MHz CRM Totem-Pole PFC

According to literature, previously proposed different interleaving control methods are divided into two categories: closed-loop interleaving and open-loop interleaving. In this paper, a master-slave relationship between two phases, and the voltage-mode control are applied to both cases. Particularly the turn-on instant synchronization is used in an open-loop interleaving analysis. Figure 3 and Figure 4 illustrate the concept of two interleaving control methods.

The voltage mode controlled CRM PFC is usually preferred because no instantaneous or average current sensing is required. The bandwidth of the voltage loop is much smaller than the line frequency so avoid double-line frequency ripple in the output. The voltage mode controlled CRM PFC is also referred to as constant on-time CRM PFC since the peak current is roughly two times of the average current and unity power factor is achieved naturally with a constant on-time in a line cycle. In this paper, voltage mode is used for both closed-loop interleaving case and open-loop interleaving case.

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For the closed-loop interleaving shown in Figure 3, the turn-on instants of both phases are triggered by the zero-current-detection (ZCD) signals. Thus soft-switching is guaranteed for both phases. The on-time of the master phase is determined solely by the voltage loop. The phase error between two phases is sensed and used to adjust the on-time of the slave phase so that the phase error can be minimized. Essentially there is a closed inner control loop as marked by the blue arrows. This method is also referred to as phase-locked-loop (PLL) based interleaving method.

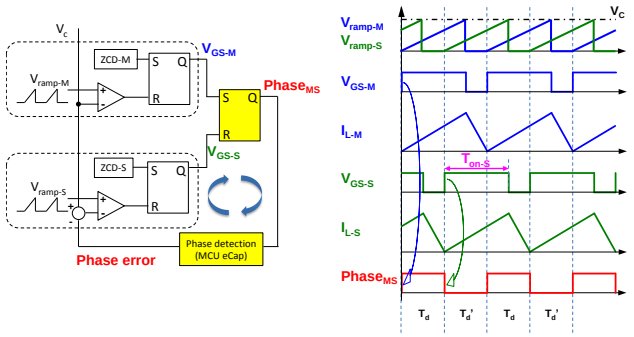

Fig. 3. Control diagram and typical waveforms of closed-loop interleaving with master-slave relationship and voltage-mode control

For the open-loop interleaving shown in Figure 4, the turn-off instants (or the on time) of both phases are determined by the voltage loop. However, only the turn-on instant of the master phase is triggered by the ZCD signal. For the slave phase, the instantaneous switching period of the master phase is detected, and then one-half of the sensed period is sent to the slave phase to determine the turn-on instant. One drawback of this method is soft-switching cannot be guaranteed in the slave phase without other performance trade off. Therefore the closed-loop interleaving method is usually preferred at low frequency (e.g. 70 kHz or 130 kHz) CRM PFC design.

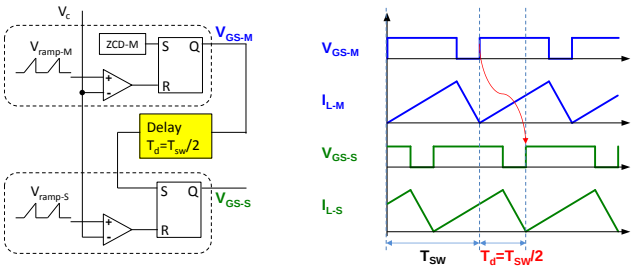

Fig. 4. Control diagram and typical waveforms of open-loop interleaving with master-slave relationship, voltage-mode control, and turn-on instant synchronization

For the system control implementation, no commercial controller supporting a MHz CRM PFC operation was available at the time of this research was conducted. Discrete components based analog control was tried for the first time, however they did not offer good enough control accuracy for interleaving, therefore a MCU based control is considered a viable alternative to achieve good performance and reasonable cost.

A 60 MHz MCU is used in the hardware demonstration. When the interleaving control is implemented by the MCU, there are two limitations. The first limitation is that the interleaving control cannot be done cycle by cycle. As shown in Figure 5, different control functions are executed in a series sequence so that the total control cycle takes 240 system clock cycles to complete. This is equivalent to 4 μs with a 60 MHz MCU so that the control cycle is much longer than the switching cycle. As a result, the interleaving control is performed once in each 4 μs.

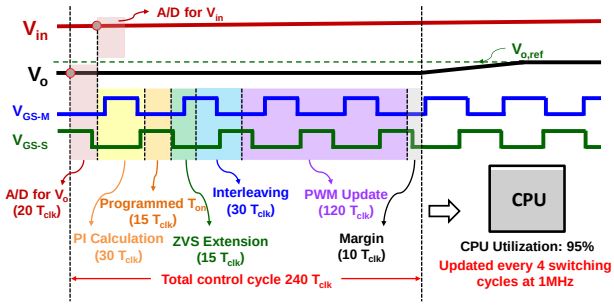

Fig. 5. MCU control implementation sequence (V_{GS-M} and V_{GS-S} are the gate driving signal of the control switch of the master phase and the slave phase respectively)

The second limitation is that all the control signals are synchronized to the MCU system clock. Then the switching period and delay time are all integer compared to the clock cycle. So even the nature of the CRM PFC is continuously smooth changing frequency but when implemented by MCU, the actual frequency is discrete.

When the two limitations combine together, a phase error oscillation is observed with the closed-loop interleaving method. Figure 6 shows the simulation waveform. There is significant oscillation in the half line cycle input current which indicates that the interleaving is not accurate. The zoom-in waveform further illustrates how the phase error is amplified and keeps oscillating. The phase error between two phases is increased or decreased by one clock cycle in each switching cycle. This is the minimum variation of phase error as switching period must be an integer number of clock cycle, and the minimum variation of switching period is one clock cycle as well. The on-time variation of salve phase is adaptively calculated and implemented by the high resolution PWM submodule of MCU to achieve a minimum switching period variation and thus a minimum phase error variation. The adaptively controlled on-time is critical because larger on-time variation may result in more than one clock cycle switching period variation; while smaller on-time variation may result in the same switching period so that no phase error adjustment can be observed.

Due to this limitation, there is up to a 24 degree phase error at 1 MHz which is far larger than the critical value and thus, makes the closed-loop interleaving unacceptable. The 24 degree phase error is a worst case value because the

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phase error can oscillate between positive and negative four clock cycles at 1 MHz switching frequency condition.

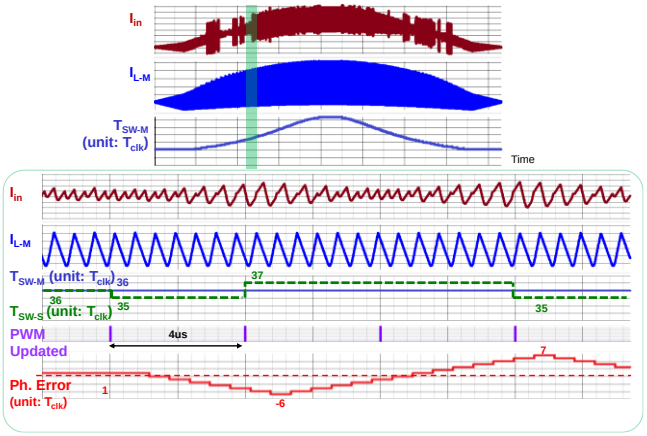


Fig. 6. Simulated closed-loop interleaving of MHz CRM totem-pole PFC (T_{SW-M} and T_{SW-S} are the switch period of the master phase and the slave phase respectively; Ph. Error is the calculated phase error between the master phase and the slave phase; all of the three variables use digitalized and normalized value to MCU clock cycles)

Figure 7 is the experimental waveform with the closed-loop interleaving. The blue and the red waveforms are inductor current of each phase while the first waveform is the total input current after interleaving. Very similar to the simulation waveform, the measured total input current has an unstable ripple that randomly occurs as well. So with a 24 degree phase error, the first order component is becoming dominant and its magnitude is even higher than the second order component as indicated on Figure 2.

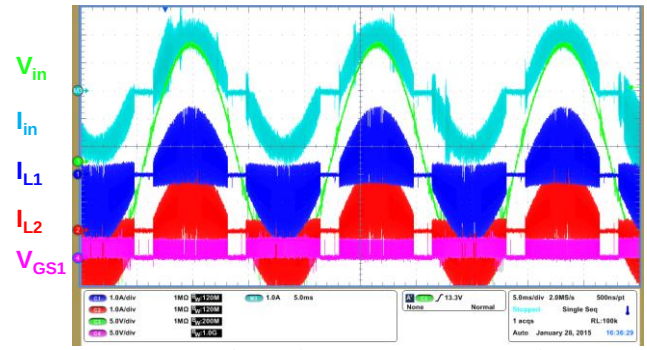


Fig. 7. Experimental waveforms of closed-loop interleaving of MHz CRM totem-pole PFC

On the contrary, the open loop interleaving has a small and non-amplified phase error. Although two limitations still exist, the phase error of the open-loop interleaving is able to stay smaller than one clock cycle. Detailed analysis of the phase error adjustment process of the open-loop interleaving with MCU implementation is shown on Figure 8. It clearly shows that the phase error is small and it has no oscillation. The maximum phase error is only one clock cycle.

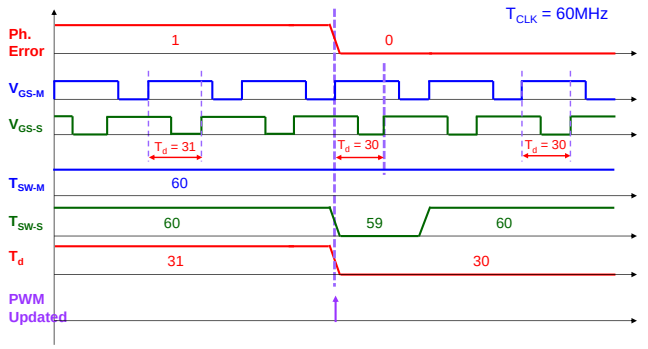
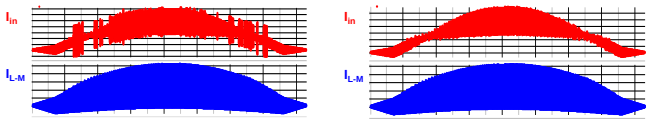


Fig. 8. Phase error adjustment with open-loop interleaving implemented by 60 MHz MCU (T_d is the delay time of the turn on instant of the slave phase compared to the turn on instant of the master phase)

Finally, Figure 9 offers a side by side comparison which demonstrates that open-loop interleaving outperforms the closed-loop interleaving with a small and stable phase error. The blue waveform is the inductor current of one phase. There is no difference between two interleaving methods. However, the total input currents shown in red color have significant difference. Both input currents have ripple cancellation effect as interleaving is implemented. For open-loop interleaving the ripple of the input current is minimized and its envelope is smooth which indicates well controlled and stable interleaving. In contrast, unstable ripple of the input current with closed-loop interleaving is shown in Figure 9(a) which is caused by the phase error oscillation analyzed. Through this comparison, the open-loop interleaving is the preferred method since it has better ripple cancellation effect.



(a) (b)

Fig. 9. Interleaving performance comparison of (a) closed-loop interleaving and (b) open-loop interleaving

IV. Optimization of Open-Loop Interleaving

Due to the discrete frequency, there is always a one clock cycle phase error existing in an open-loop interleaving. With 60 MHz, this is equivalent to a 6 degree phase error at 1MHz which is still larger than the critical value. Besides increasing the CPU speed of the MCU, a software improvement is possible.

Figure 10 shows the improvement method. The idea is that the total delay time is divided into two separate parts. The basic delay time is still an integer of the system clock. At the same time, it is also possible to give another extra delay time which positions the PWM single edge with one half clock cycle resolution. Then the edge is synchronized to the system clock when the master phase switching cycle is an even number; and the edge is placed in the middle of two adjacent system clocks to provide a one half clock cycle

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delay when the master phase switching cycle is an odd number. Ideally, when the two part delay times are combined, the total delay time is exactly equal to one half of the master phase switching period no matter if it is an even number or an odd number.

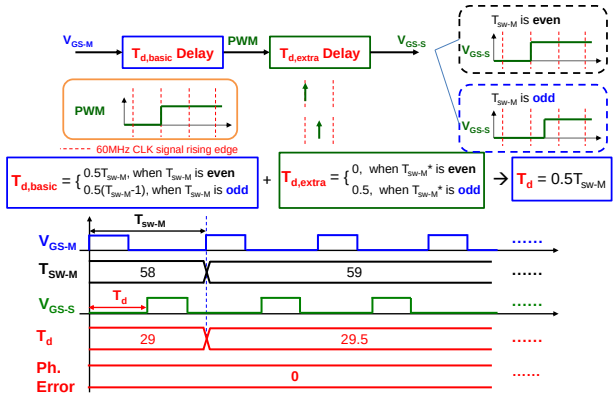

Fig. 10. Software optimization of open-loop interleaving ($T_{d,basic}$ is the basic delay time which must be an integer number of system clock; $T_{d,extra}$ is the extra delay time which can achieve zero or one-half system clock controlled by HALFCYCLE register in Dead-Band submodule)

Figure 11 further shows the phase error worst case of open-loop interleaving after the software optimization. It occurs in an abrupt change point of the switching frequency. Again, since the 4 μs control cycle is larger than the switching cycle, there is one half clock cycle phase error between the switching frequency change and next control cycle adjustment. It equals to a 3 degree phase error and it is smaller than the 5 degree critical phase error value if one stage DM filter is used.

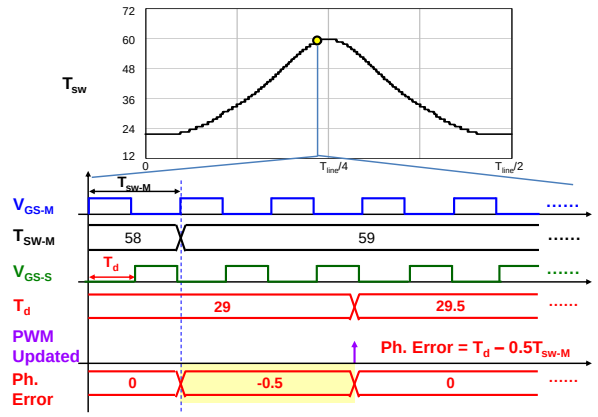

Fig. 11. Phase error worst case of open-loop interleaving after optimization

Figure 12 shows the measured DM noise spectrum comparison before and after optimization. So with optimization method, the 2 MHz noise component became the dominant factor for the 1-stage DM filter design in Figure 12(b). Figure 13 is the experimental waveform that shows good interleaving and ripple cancellation effect in different instant of a line cycle.

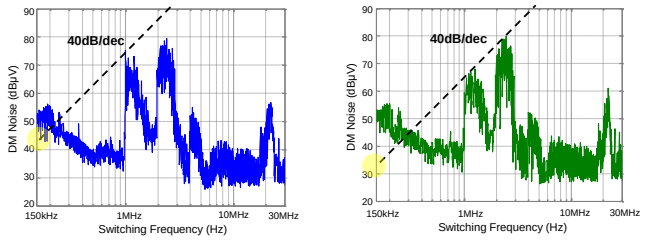

Fig. 12. Measured DM noise spectrum of open-loop interleaving (a) before optimization and (b) after optimization

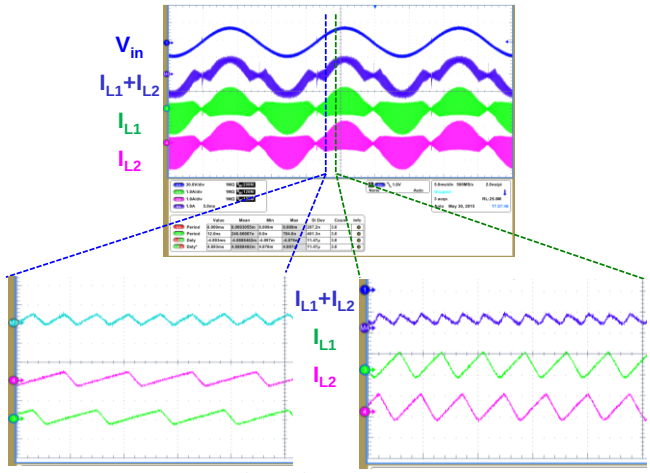

Fig. 13. Experimental waveform of open-loop interleaving

Even though the 60 MHz low cost MCU is used, the scope of the paper is not limited to one specific MCU. Several representative samples are selected for performance comparison and shown in Table I. As a simple function of CPU speed, the corresponding phase errors with closed-loop interleaving and open-loop interleaving are calculated respectively and the benefits offered by open-loop interleaving are clearly seen through this comparison.

Table I. Performance of interleaving with different MCU

	Series	CPU Speed	Closed-loop interleaving (4xT_{CLK})			Open-loop interleaving (0.5xT_{CLK})		
			Phase error	2-stage (1°)	1-stage (5°)	Phase error	2-stage (1°)	1-stage (5°)
Piccolo	F28027	**60 MHz**	24°	✗	✗	3°	✗	✓
	F28069	**90 MHz**	16°	✗	✗	2°	✗	✓
	F28075	**120 MHz**	12°	✗	✗	1.5°	✗	✓
Delfino	F28335	**150 MHz**	9.6°	✗	✗	1.2°	✗	✓
	F2837xS	**200 MHz**	7.2°	✗	✗	0.9°	✓	✓
	C28346	**300 MHz**	4.8°	✗	✓	0.6°	✓	✓

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V. Stability Analysis of Open-loop Interleaving at MHz Switching Frequency

According to [19], there are four scenarios of open-loop interleaving implementation, current mode with turn-on instant synchronization, current mode with turn-off instant synchronization, voltage mode with turn-on instant synchronization, and voltage mode with turn-off instant synchronization. Current mode with turn-on instant synchronization is the only stable case for both a duty cycle smaller or larger than 0.5 and for a positive and negative delay time perturbation. In the analysis of [19], there is an assumption that the resonant time is negligible compared to the switching period. This assumption is reasonable for the 70 kHZ CRM PFC. However, for the MHz CRM PFC the resonant time to achieve ZVS occupies up to 10% of the total switching period; or in other words, there is significant duty cycle loss so that the CRM mode at MHz is more like the discontinuous current mode (DCM) instead of the ideally boundary mode.

For this reason, the MHz totem-pole PFC with voltage mode control and turn-on instant synchronization open loop interleaving method is becoming more stable when compared to a 70 kHz case. Figure 14 shows the simulation waveform. Delay time perturbation, which in this case equals to a 10% switching period as an example, is applied to both 70 kHz CRM boost and 1MHz CRM boost with the same input and output condition (Vin=100 V and Vo=400 V). After the perturbation, in the 70 kHz case the inductor current of the slave phase immediately goes to a continuous current mode (CCM) with a very long settle down time (tens of switching period), while in the 1 MHz case CCM operation just happens in one or two switching cycles and the current settles down to steady state quickly. In Figure 14, both red dash lines show the inductor current of the slave phase without perturbation. They can be treated as a reference for the steady state operation. In addition, it is also verified that for both a duty cycle smaller or larger than 0.5, a similar conclusion can also be made.

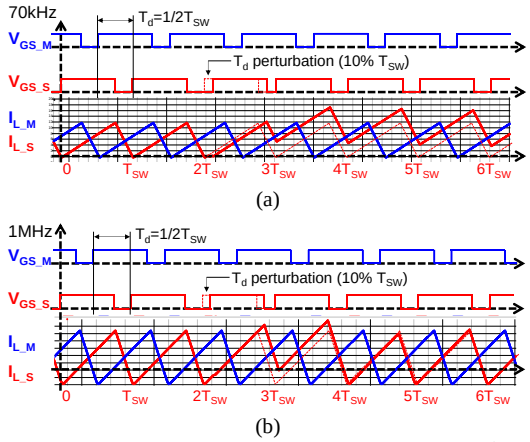

Fig. 14. Open-loop interleaving under delay time perturbation of (a) 70 kHz and (b) 1 MHz

The theory to explain this phenomenon is a volt-second unbalance. Figure 15 (a) shows the inductor current in critical mode operation and steady state with triangular shape approximation. Then Figure 15 (b) and (c) verifies that no matter how the circuit goes from CCM or quasi-square-waveform mode (QSW) after perturbation, the inductor current gradually settles down to the CRM steady state. For the CCM case, the original resonant time is becoming off time so that the average inductor current decreases each cycle. However, for the QSW case the original resonant time is becoming on time so that the average inductor current increases each cycle. Eventually, the unstable cases settle down very quickly due to a large duty cycle loss at MHz switching frequency.

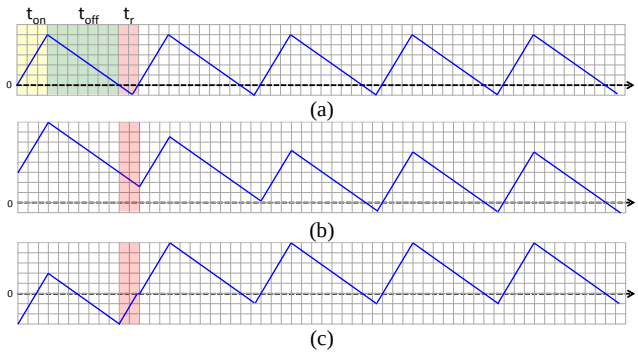

Fig. 15. Stability mechanism of (a) CRM, (b) CCM, and (c) QSW

For the other two control implementations: current mode with turn-off synchronization and voltage mode with turn-off synchronization, the unstable phenomenon is the sub-harmonic oscillation. They are still considered as unstable at MHz.

VI. Conclusions

Accurate interleaving control is very critical to effectively reducing input current ripple and to achieving the expected EMI filter size reduction for the MHz CRM totem-pole PFC. The superior characteristics of GaN devices offer the opportunity to dramatically increase the switching frequency of a PFC circuit with CRM simple soft switching implementation. However, MHz frequency operation bring new challenges to the traditional variable frequency interleaving control methods. This is because with a reasonable cost digital controller, cycle-by-cycle interleaving control cannot be realized at MHz.

Under this circumstances the previously preferred closed-loop interleaving, which is able to achieve good soft switching operation and minimal phase error at 70 kHz or 130 kHz, results in poor and unstable input current ripple cancellation effect at MHz. While on the other side, open-loop interleaving demonstrates significantly better performance especially after algorithm optimization in MCU. Implemented by a 60 MHz MCU, a less than 3

degree phase error is accomplished with open-loop interleaving, which is far better than 24 degree phase error achieved by closed-loop interleaving.

The dramatically increased switching frequency offer the opportunity to use 1-stage EMI filter. At the same time, 1-stage filter shows less sensitivity to the interleaving phase error.

Furthermore, when comparing the dynamic response under perturbation, 1 MHz operation shows significantly reduced settling time and thus better stability than conventional 70 kHz operation. The insight of this phenomenon is when switching frequency is increased, there is more negative current and duty cycle loss due to resonance to realized ZVS. The PFC essentially operates in deep DCM mode rather than at the boundary between CCM and DCM.

Based on the analysis and results, several system-level benefits can be projected including better efficiency, significantly improved power density due to size reduction of passive components and EMI filter, and better dynamic response under transient, which are all achieved by dramatically increased switching frequency enabled by GaN devices.

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DISCLAIMER

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