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# DSP-based current sharing of average current controlled two-cell interleaved boost power factor correction converter

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**Abstract:** Power factor correction (PFC) pre-regulators are used between the ac line and non-linear load to improve the line current in terms of power factor and total harmonic distortion (THD). In medium- and high-power applications, the interleaved boost PFC converter is the proper solution for this purpose to obtain a pre-regulator with lower size. The operation of the interleaved boost PFC converter provides a reduction of the inductor and electromagnetic interference filter volumes compared with those of the conventional single switch boost PFC converter. However, proper current sharing and current ripple minimisation must be ensured to achieve these benefits. The current sharing between cells of a two-cell interleaved boost PFC converter, which is an important problem in applications is analysed and discussed in this study and the problem is removed by using a digital signal processing (DSP)-based simple practical solution. The proposed technique provides the proper current sharing by sensing only the rectifier output current (total current of cells) without using any external control loop. The simulation and the experimental results are presented to show the validity.

## 1 Introduction

Several power factor correction (PFC) techniques have been developed to satisfy international standards such as EN-61000-3-2. The PFC technique reduces current harmonics in utility systems produced by non-linear loads. The boost PFC topology is the most popular configuration owing to the input current of boost inductor, which is easily programmed by current-mode control. The input current in this topology also has smooth waveform especially at continuous current mode (CCM) resulting in lower electromagnetic interference (EMI) filter requirements. Owing to the these advantages, the conventional boost-type PFC circuits have been proposed in the literature to meet the requirements and to improve power quality in terms of high-power factor and low total harmonic distortion (THD) with regulated output voltage [1, 2].

Generally, the implementation of a PFC converter has been accomplished by using analogue PFC integrated circuits (ICs). Analogue PFC control ICs that are commercially manufactured by different companies are available with several current control techniques [3, 4]. Analogue control provides continuous processing of signal allowing very high bandwidth. It also has the advantages of providing near infinite resolution of the signal measured. However, analogue control has several drawbacks such as, the number of components used in analogue controllers makes the converter complex and bulky, the design is inflexible and its performance cannot be optimised for various utility input conditions and disturbances [5]. Digital control method that is used in this study has several advantages, such as being less sensitive to environmental variation, lower size and more flexibility because of programmability.

Interleaved power conversion refers to the strategic interconnection of multiple switching cells for which the conversion frequency is identical, but for which the internal switching instants are sequentially phased over equal fractions of a switching period [6]. This arrangement lowers the net ripple amplitude and raises the effective ripple frequency of the overall converter without increasing switching losses or device voltage/current stresses. Therefore in high-power applications, interleaving or phase-shifted operation of two or more boost converters has been proposed to increase the output power and the converter's total efficiency and to reduce the current ripple [7–11]. The cancellation of low-frequency harmonics allows eventually the reduction of size and losses of the filtering stages [12]. The obvious benefit is an increase in the power density without the penalty of reduced power conversion efficiency. However, current sharing among the parallel cells in continuous inductor current mode and at average current control is a major design problem because of mismatching in duty cycles [8]. A desirable characteristic of an interleaved system is that each cell shares the load current equally and stably. Parallel cells are usually non-identical because of finite tolerances in the power stage and control parameters. If special provisions are not made to distribute the load current equally among paralleling cells, it is possible that one or

more cells may have an excessive load current. This causes higher thermal stress and reduces the system reliability.

In order to solve current sharing problem among the parallel cells of interleaved converters, various kinds of techniques have been proposed in the literature. The technique presented in [13] is a simple switching logic scheme, which ensures minimisation of the input current ripple and develops a Lyapunov–likelihood technique that is the combination of Lyapunov functions and likelihood method for the simultaneous design of the current sharing and output voltage controllers. Lyapunov functions that are important to the stability theory and control theory can be used to prove the stability of a certain fixed point in a dynamical system or autonomous differential equation. The likelihood method is a basic statistical technique for estimating parameters and variables, and is the starting point for many more sophisticated methods. The currents of both cells should be measured in the technique presented in [13] for proper operation. The sensing and measurement of more currents result in a complex control circuit and increases cost of converter. In [14], a predictive digital controller technique is proposed for equal current sharing among the parallel cells of the interleaved boost converter operating in CCM. In this technique, a phase-shift control circuit is used to generate the gate signals for the active power switches operating in parallel branches. The main problem of this technique is that the peaks of the triangular currents are not superimposed on each other, but are distributed evenly over the entire period. An analogue solution to correct the differences in the duty ratios of the boost switches is proposed in [2]. The main reason for the poor current sharing in analogue controllers is that the slopes of the phase-shifted ramps are not equal because of differences in the values of the timing capacitors and the charging currents. In order to remove this drawback an extra analogue circuit is used, which increases the complexity and cost of the converter. Kim and Enjeti [15] proposed a DSP-based control method for current sharing of multiple single-phase PFC modules. The controller used in this study senses the inductor current of each module and calculates the duty ratio for each module to provide proper current sharing. This technique has the same drawback of sensing and measurement of currents of both cells. Another disadvantage of this technique is that the DSP needs for much more time to determine the duty cycles of the switches separately. Another digital solution is proposed in [16]. In this technique, the current of all switches are sensed and an extra control loop is used to regulate the duty ratio of each cell. Inserting an extra control loop and sensing and measurement of more currents are disadvantages for the technique proposed in [16].

This paper proposes a DSP-based average current-controlled method, which ensures minimisation of the input current ripple and proper current sharing for two-cell interleaved boost PFC circuit. A 32-bit fixed-point, TMS320F2812 eZdsp is used as a controller to implement the interleaved boost PFC converter-based on CCM operation. The main contribution of this study is that the current sharing of two-cell interleaved boost PFC converter is ensured by sensing only one current without using any external control loop. The proposed control strategy is explained after analysing the circuit behaviour of the two-cell interleaved boost PFC converter.

## 2 Current relationship of two-cell interleaved boost PFC converter

In this section, the current relationship of the two-cell interleaved boost PFC converter is analysed. The state variables of the system are taken as inductor current and the capacitor voltage. Under normal operating conditions the supply can be modelled as a sinusoidal voltage source with peak value of $V_m$ and line frequency of $f$. The instantaneous input voltage of the converter is

$$V_g = |V_{in}(t)| = |V_m \sin\ \omega t| \tag{1}$$

where, $\omega = 2\pi f$ electrical radians/s and $t$ is the instantaneous time in seconds. In the analysis of the converter, the output filter capacitor is assumed as a constant voltage source $V_o$ during a switching period. In addition, the current of each inductor is assumed constant during a switching period because the inductors of two cells are large enough and the switching frequency, $f_s$ is very high compared with the line frequency, $f$. The relationship between the output voltage ($V_o$) and input voltage ($V_g$) determines the states of the switches. Since the input voltage applied to the PFC converter varies from 0 to $V_m$, there exist two different states. $V_o/2 < V_m$ and $V_o/2 > V_m$ states are investigated separately. The steady-state equation of two-cell interleaved converter can be given as follows [17]

$$X_{ss} = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ V_o \end{bmatrix} = \begin{bmatrix} \dfrac{V_g}{2 \cdot R_o(1-d)^2} \\ \dfrac{V_g}{2 \cdot R_o(1-d)^2} \\ \dfrac{V_g}{(1-d)} \end{bmatrix} \tag{2}$$

where, $d$ defines the duty ratio of the converter. The input current ripple and output capacitor ripple of two-cell interleaved boost converter related to the inductor currents are shown in Fig. 1. It is seen from Fig. 1 that the expression for input current ripple for an $N$-phase interleaved boost converter is dependent on the inductor value ($L$), input voltage ($V_g$), duty cycle of each cell ($d$), duty cycle of the input current ($q$) and period of input ripple current ($\tau$). This relationship can be expressed by equation (3) [18].

$$\Delta i_g = \frac{V_g \cdot (1-q)}{L \cdot (1-d)} \cdot q \cdot \tau \tag{3}$$

From Fig. 1, the relationship between the charge and the voltage of a capacitor in terms of the converter parameters are given by equations (4) and (5) [18].

$$\Delta Q_c = \frac{T_s}{2^2} \cdot \frac{V_o}{R_o} \cdot \frac{q \cdot (1-q)}{(1-d)} \tag{4}$$

$$\Delta V_o = \frac{\Delta Q_c}{C_o} = \frac{T_s}{2^2} \cdot \frac{V_o}{R_o \cdot C_o} \cdot \frac{q \cdot (1-q)}{(1-d)} \tag{5}$$

The variation of the 'ratio of the input current ripple to any inductor current ripple' against duty cycle for two and four phases interleaved boost converter is shown in Fig. 2*a*. It is seen that for duty cycles of zero and unity the 'ratio of the input current ripple to any inductor current ripple' is one. It is also seen that input current ripple decreases with increasing the number of interleaving phases. The output current of the converter ($i_o$) is the sum of capacitor current ($i_{Co}$) and load current ($I_o$). The output current has a periodical ac component and a dc component. For a converter with constant parameters




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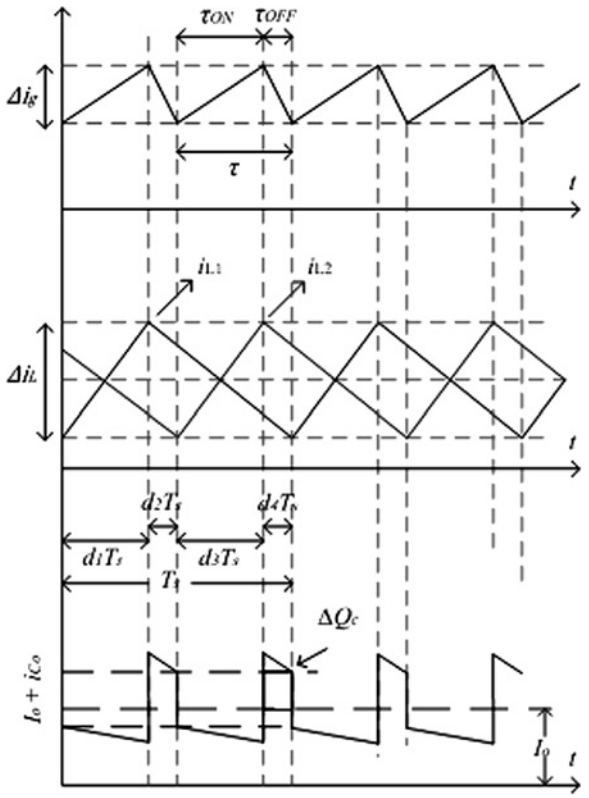


**Fig. 1** *Currents waveforms of two-cell interleaved boost converter*

as $R_o$, $C_o$ and switching period ($T_s$), the variation of the 'ratio of the output voltage ripple to the mean output voltage' against the duty cycle for two and four phases interleaved boost converter is shown in Fig. 2*b*. It is seen that the output voltage ripple is minimised at the points where the input current ripple is minimised. The output voltage ripple is decreased by increasing the number of interleaved phases.

## 3 Control strategy

The average current control method is introduced as the most popular strategy in the literature among the various control strategies, which can be implemented to PFC circuits. This control scheme ensures regulated dc output voltage with a high input power factor. The output voltage regulator generates a current signal, which is the amount of current required to regulate the output voltage to its reference value. The output of the voltage regulator is then multiplied with the sample of rectified input voltage and divided to output signal of the feed forward loop to generate a rectified input current reference. This current reference has the magnitude to maintain the output voltage close to its reference value and has the shape and phase of the rectified input voltage. The average value of the rectified input current is sampled to be compared with its reference value and produce an output via current regulator to drive pulse width modulation (PWM) modulator. In this way, the current regulator tends to minimise the error between the average input current $i_g$ and its reference. In this study, the average current control method is used as the controller. The scheme of the controller and the power stage is shown in Fig. 3. The proposed converter is designed to operate in CCM. A TMDSEZDF2812-0E controller from Texas Instrument is used to develop the shape and frequency of the input current.

The voltage control loop is a PI controller and makes the outer loop in the control system. This loop regulates the output voltage regardless of any variations in load current and the input voltage. The inputs of the voltage control loop are $V_o$ and $V_{o,ref}$. The output of the voltage control loop is a control signal, which determines the reference current ($i_{g,ref}$) for the current control loop. The current control loop is also a PI controller and makes the inner loop in the control system. This loop corrects the error between two currents, which are the rectified input current ($i_g$) and its reference signal ($i_{g,ref}$). The output of the current control loop is a control signal, which ensures that the input current follows the reference current. As seen from Fig. 3, except for voltage and current regulators, a feed forward loop is also used to compensate input voltage transients. In fact, when the input voltage increases, the input current should decrease in order to draw constant power. Therefore a feed forward action from the input voltage should be used to solve effects of the input voltage changes. Here, the root mean square (rms) input voltage is taken and this signal is squared and used in the multiplier to divide the current reference. Thus, the changes in the input voltage are compensated via feed forward loop [19].

For 600 W output power, 220 V_rms input voltage and 400 V_dc output voltage ranges, the voltage and current compensators are designed [20]. The bandwidth of the voltage control regulator that is given by equation (6) is selected 20 Hz, so that the effect of the input frequency ripple on the output dc voltage can be minimised at 100 Hz.

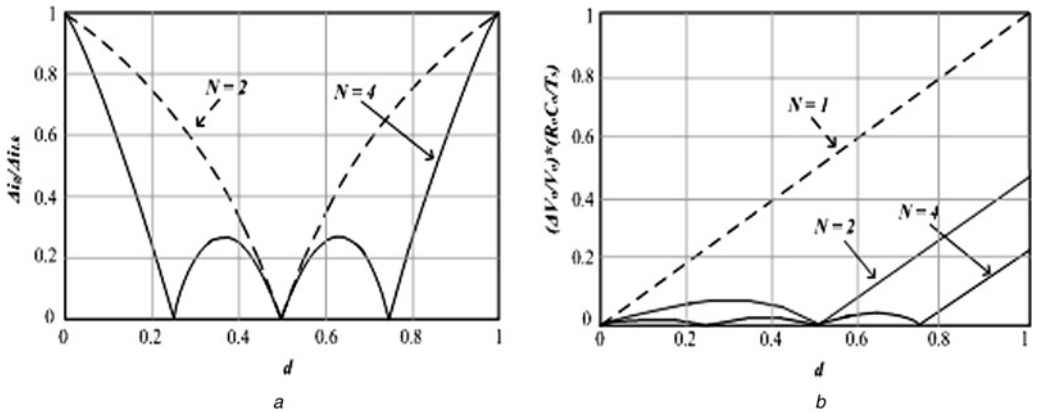


**Fig. 2** *Variation of*

*a* 'Ratio of the input current ripple to any inductor current ripple' against duty cycle
*b* 'Ratio of the output voltage ripple to the mean output voltage' against duty cycle

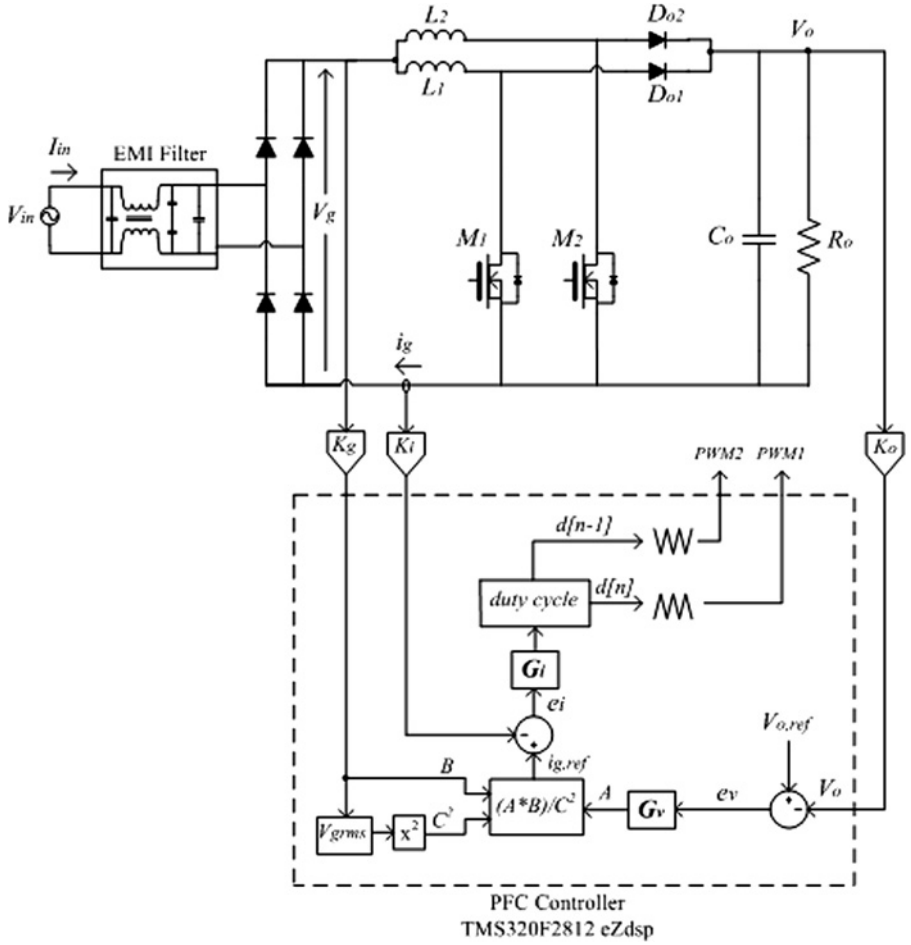


**Fig. 3** *Proposed controller scheme for two-cell interleaved boost PFC circuit*

The bandwidth current control regulator that is given by equation (7) is 3 kHz for a switching frequency of 50 kHz. The current controller should be much faster than that of the voltage controller because it has to track correctly the sinusoidal waveform. The output of the current control loop decides the required duty cycle ($d$) to switch the MOSFETs.

$$G_{v(s)} = G_v \cdot \frac{1 + T_v \cdot s}{s \cdot T_v} = K_{P1} + \frac{K_{I1}}{s} = 0.9 \cdot \frac{1 + 18 \times 10^{-3} \cdot s}{18 \times 10^{-3} \cdot s} \quad (6)$$

$$G_{i(s)} = G_i \cdot \frac{1 + T_i \cdot s}{s \cdot T_i} = K_{P2} + \frac{K_{I2}}{s} = 0.85 \cdot \frac{1 + 105.98 \times 10^{-6} \cdot s}{105.98 \times 10^{-6} \cdot s} \quad (7)$$

where, $G_{v(s)}$ and $G_{i(s)}$ define the voltage and current compensators, respectively. $K_{P1}$ and $K_{I1}$ define the proportional and integral coefficients of the voltage control compensator, respectively. $K_{P2}$ and $K_{I2}$ define the proportional and integral coefficients of the current control compensator, respectively. Bode plots of the designed voltage and current compensators are given in Fig. 4. From the figure, it is seen that the low-frequency gain of the current loop is 40 dB. The crossover frequency of the current controller loop is obtained at around 3 kHz and the phase margin is around 30°. The loop crossover frequency of the voltage regulator is around 15 Hz and the phase margin is 30°.

Since the proposed method is implemented using DSP, a digital implementation of the compensators is needed as given in equation (8)

$$u[n] = u[n-1] + K_P \cdot e[n] + K_I \cdot T \cdot e[n] \quad (8)$$

where, $e[n]$ is the discrete input value (difference between the current/voltage value and its reference value), $u[n]$ is the discrete output value of the compensators and $T$ is the sampling period.

In the proposed technique, parallel to measuring the output voltage and rectified input voltage, only one current (rectified input current) is sensed and measured. There is no need to measure and sense the currents of inductors or switches in the proposed method. All current and voltages of the power stage are sensed and used in the DSP via analogue digital converter (ADC) module. The output voltage compensator and the current compensator are implemented digitally based on the average control method. In the proposed technique, there is also no need for any extra controller loop such as load balance loop. As seen from Fig. 3, only one duty cycle ($d$) is computed at the output of the current compensator. In this technique, the duty cycle determined by the DSP is applied to the first switch and is also saved to be applied to the second switch, which operates with 180° phase shift with respect to the first one. The instant value of the duty cycle ($d[n]$) is used as a compare value in the first PWM signal which is a triangular wave with 50 kHz switching frequency. The former value of the duty cycle ($d[n-1]$) is used as a compare value in the second




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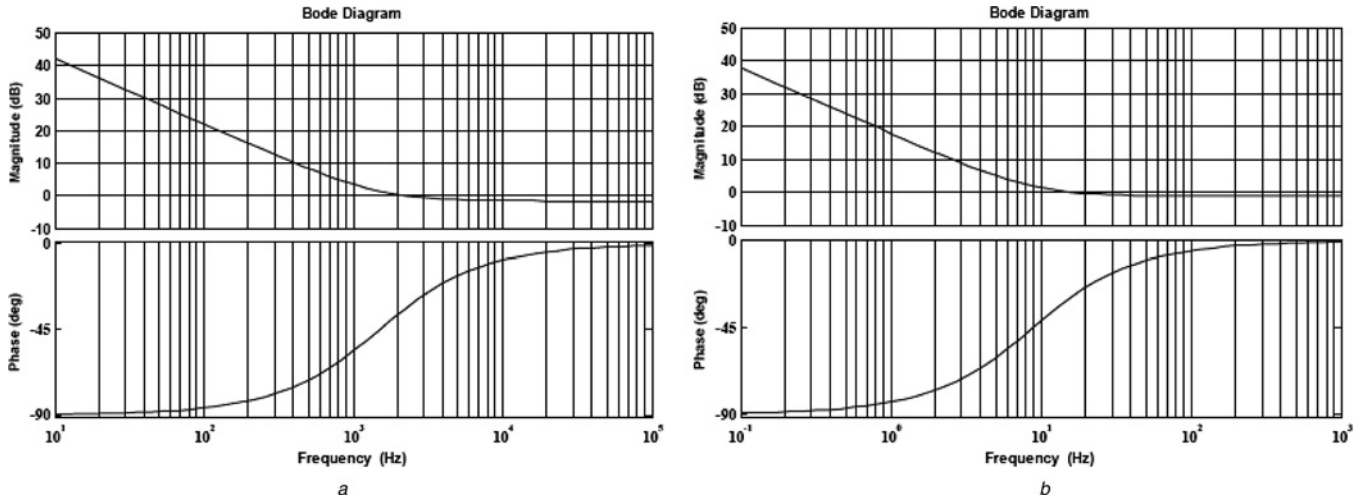


**Fig. 4** *Bode plots of the designed controllers*

*a* Current controller
*b* Voltage controller

PWM signal, which is a triangular wave with 50 kHz switching frequency and 180° phase shifted from the first PWM signal. The PWM signals of the proposed technique that are obtained from the duty cycle values and two different PWM modules of the DSP are given in Fig. 5. Two different PWM signals having the same period and 180° phase shift from each other are obtained by using two different COUNTERs of the DSP.

It is seen from Fig. 5, while the instant value of the duty cycle ($d[n]$) is used as a compare value in the first PWM signal, the former value of the duty cycle ($d[n-1]$) is used as a compare value in the second PWM signal, which is 180° phase shifted from the first PWM signal. By this way, the duty cycle duration (ON time) of the second switch ($M_2$) is fixed as the value of the first switch ($M_1$). Since the duty cycle of the first switch is applied to the second switch with a delay of 180° phase shift, the equal current sharing of the inductors are guaranteed both at steady state and at the dynamical changes. As it is stated before, the main advantage of this technique is that the current sharing of two-cell interleaved boost PFC converter is ensured by sensing only one current and without needing for any external control loop.

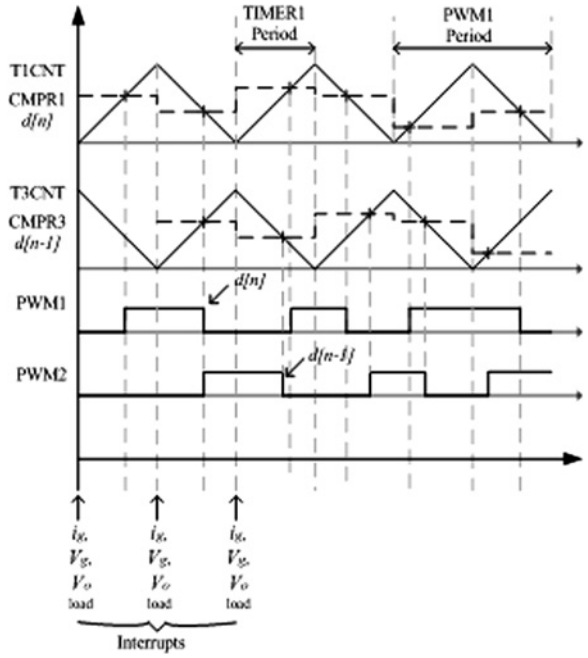


**Fig. 5** *PWM signals of the proposed technique obtained from TMS320F2812 eZdsp*

## 4 Simulation and experimental results

In this section, simulation and experimental studies are carried out to verify the proposed technique. A two-cell interleaved boost PFC converter is simulated via Ansoft/Simplorer 7.0 simulation program with and without proposed technique. Then, an experimental circuit is built up to verify the feasibility of the proposed technique. The simulated results of the proposed topology are shown in Figs. 6 and 7. The components and parameters used in the simulation and experimental studies are summarised in Table 1.

Fig. 6 shows the input voltage and current waveforms without electromagnetic interference (EMI) filter. This result shows that the power factor and THD of the input current obtained from analysing are suitable for international standards. The inductor currents and total rectified input current that are obtained with proposed

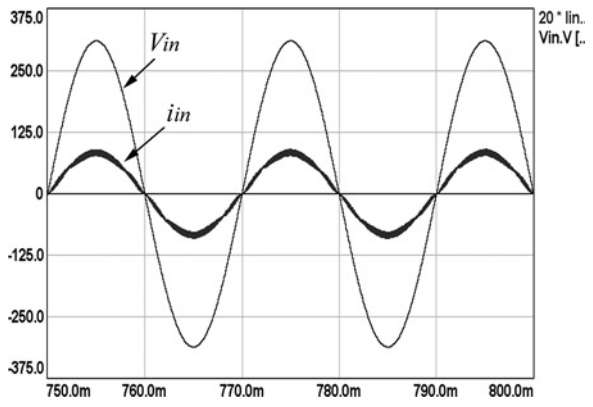


**Fig. 6** *Simulation results of input voltage ($V_{in} = 220\ V_{rms}$) and 20*input current ($i_{in} = 2.81\ A_{rms}$), waveforms ($THD_i = 8.6\%$, $pf = 0.998$)*

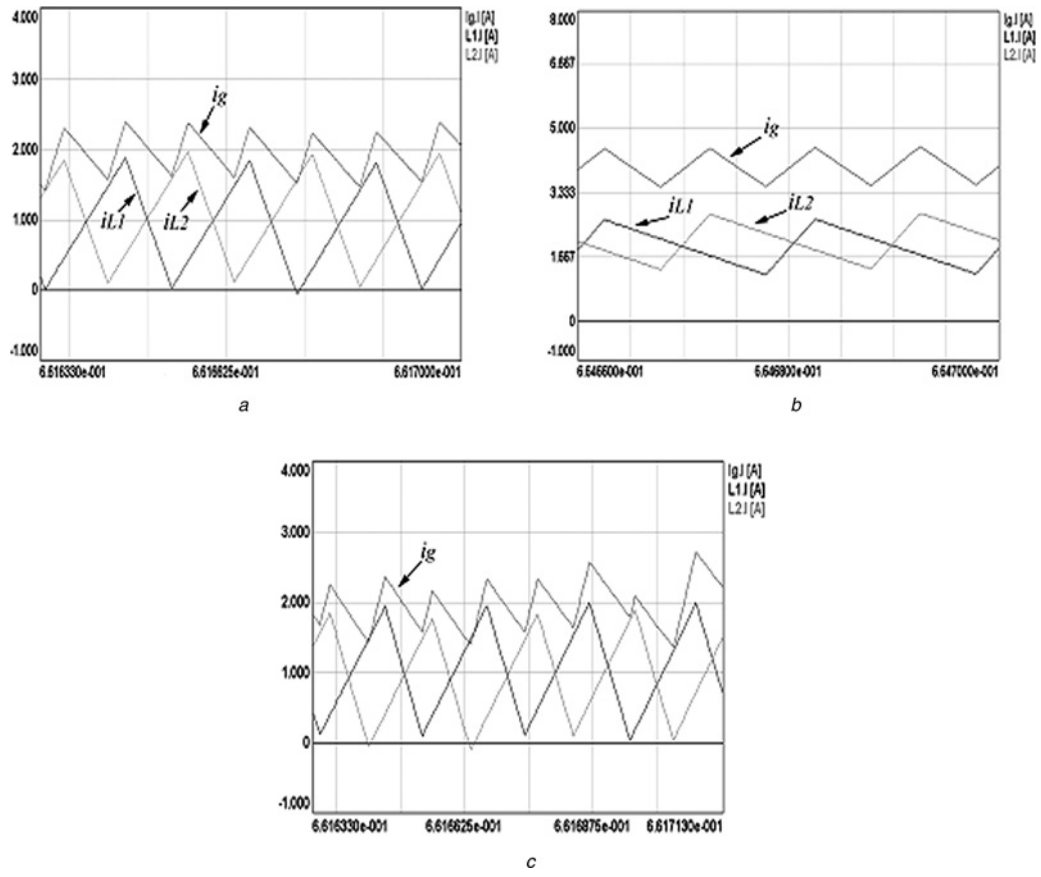


**Fig. 7** *Simulation results of $i_{L1}$, $i_{L2}$ and $i_g$*

*a* For $d > 0.5$ with proposed technique
*b* For $d < 0.5$ with proposed technique
*c* For $d > 0.5$ without proposed technique

**Table 1** Components used in the simulations and experiments studies

| Components | Parameters |
|---|---|
| $V_{in}$ (input voltage) | 220 $V_{rms}$ |
| $V_o$ (output voltage) | 400 $V_{dc}$ |
| $f_s$ (switching frequency) | 50 kHz/cell |
| $f$ (input voltage frequency) | 50 Hz |
| $L_1$ and $L_2$ (main inductances) | 700 μH |
| $C_o$ (output capacitance) | 470 μF |
| $M$ and $M_2$ | IRFP460 |
| $D_{o1}$ and $D_{o2}$ | DSEI30-12A |
| $P_o$ (output power) | 600 W |

technique are shown in Figs. 7*a* and *b*. The results obtained for $d > 0.5$ and $d < 0.5$ show that the input current ripple amplitude is smaller than that of the inductors currents. The input current ripple is greatly reduced for both cases of duty cycle by using interleaving technique. Since the two phases of the circuit work with the 180° phase shift, the input current ripple minimisation is best achieved at duty cycle of 0.5. As seen from the figure, using the proposed technique the equal current sharing of the inductors is obtained for both cases of $d > 0.5$ and $d < 0.5$. Fig. 7*c* shows the inductor currents and total rectified input current that are obtained without using the proposed technique and load balance loop. It is seen that the input current ripple amplitude is smaller than that of the inductors currents but there is no ensure of equally current sharing. The inequality between the current of inductors causes out of order in the total rectified input current.

The hardware realisation of the topology was carried out with proposed technique and experimental waveforms are presented in Figs. 8 and 9. It is shown from Fig. 8*a*, the experimental results of input voltage and current waveforms are in good agreement with the simulation ones. Nearly the same input power factor value is obtained from the experimental and simulation results. THD value is obtained as 10.4 and 8.6% from the experimental and simulation results, respectively. This difference is because of the shape of the input voltage. As it is known, the input voltage shape is pure sinusoidal in the simulation studies. However, the input ac voltage that is used in the laboratory is not purely sinusoidal but is distorted. In addition, 0.992 pf and 10.7% THD values are obtained by operating the topology with conventional method (without proposed technique). The dynamical behaviour of the topology is observed by changing the load. When the output power is increased from 300 to 600 W (changing load from 50 to 100%), the voltage controller controls the output voltage and keeps it constant at the reference value (Fig. 8*b*). During this period the current controller controls the input current considering the PFC requirements conditions. The recovery time value in the transient state is nearly 150 ms. In addition, Fig. 8*c* shows the level of the low-frequency ripple at the output. It is seen that the peak-to-peak output voltage ripple is 7.2 V. The voltage speed response can be increased by adjusting the voltage compensator parameters. However, increasing speed response results in higher value output voltage ripple.




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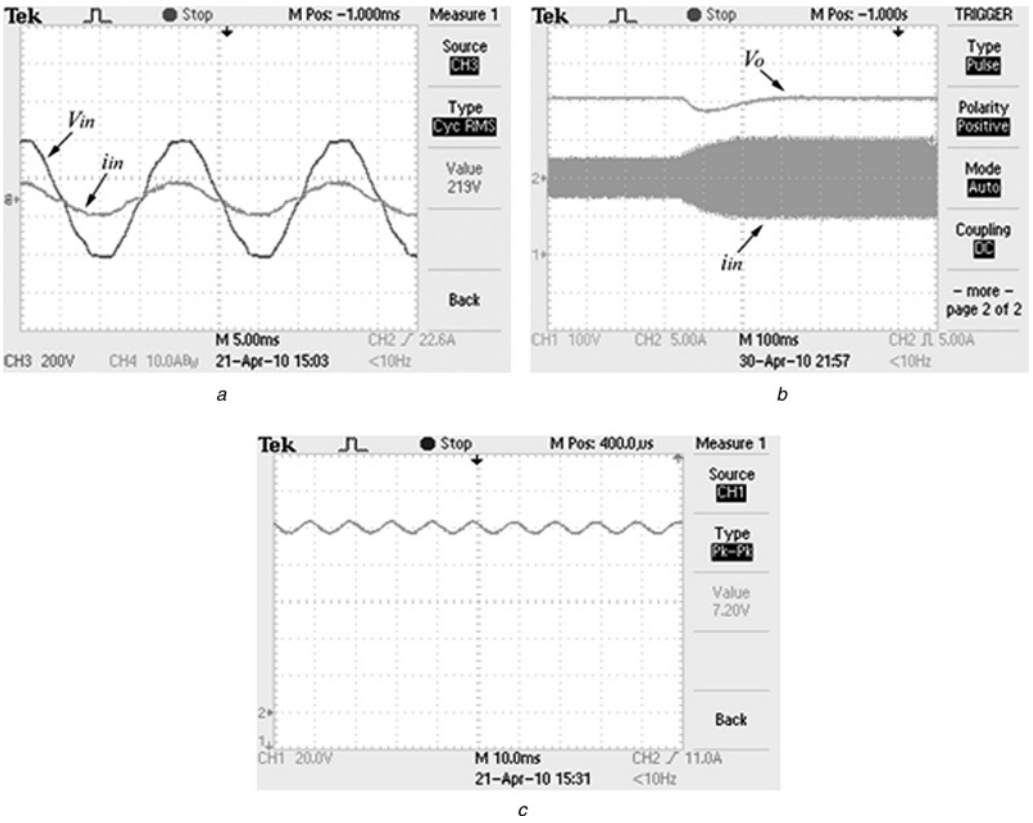


**Fig. 8** *Experimental results of*

*a* Input voltage-input current ($V_{in} = 220\ V_{rms}$, $i_{in} = 2.98\ A_{rms}$, pf = 0.994, THD = 10.4%)
*b* Output voltage and input current for different loads (changing load from 50 to 100%)
*c* Output voltage peak-to-peak ripple ($V_{o\_peak\text{-}to\text{-}peak} = 7.2$ V)

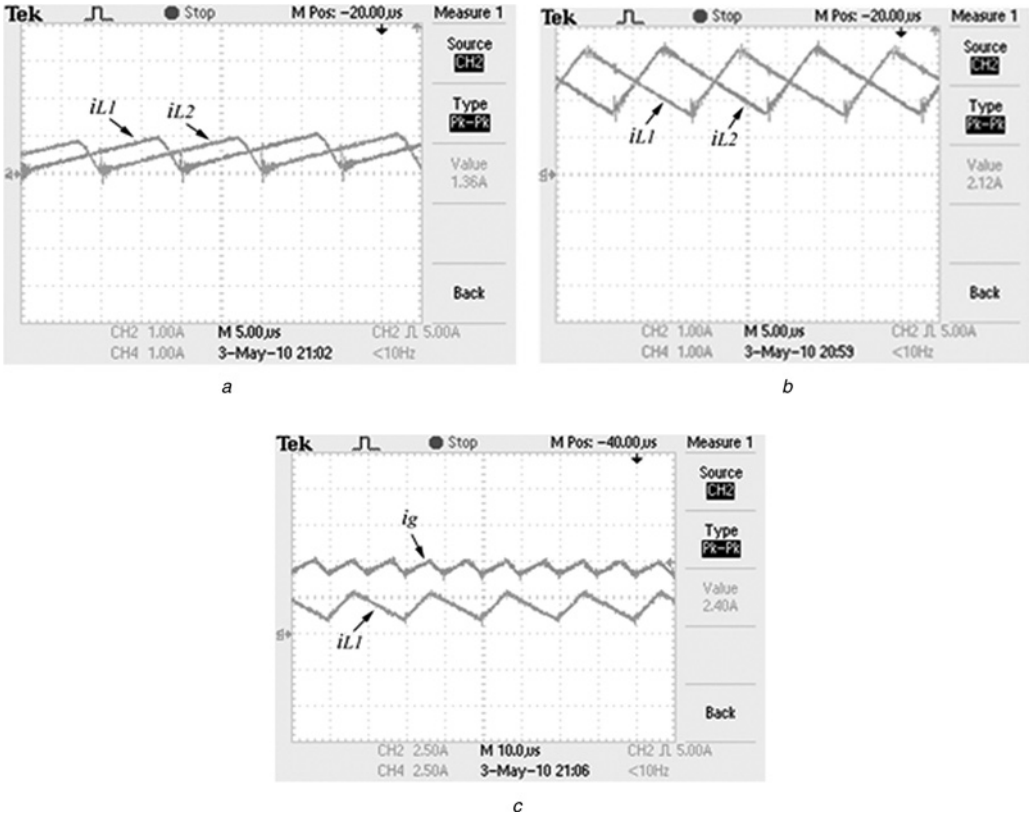


**Fig. 9** *Experimental results of proposed technique for*

*a* $i_{L1}$ and $i_{L2}$ for $d > 0.5$
*b* $i_{L1}$ and $i_{L2}$ for $d < 0.5$
*c* $i_{L1}$ and $i_g$

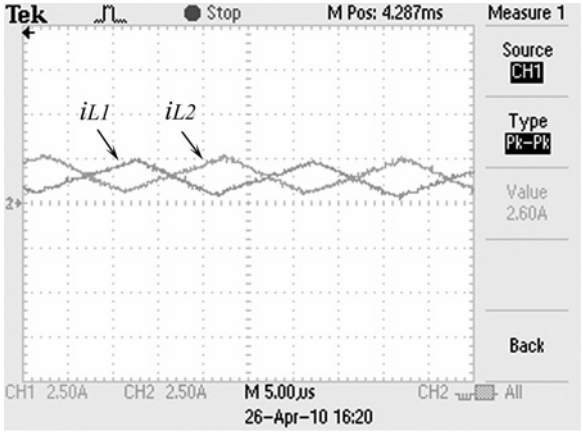


**Fig. 10** *Experimental results of $i_{L1}$ and $i_{L2}$ under load changing*

The experimental results of the inductor currents that are obtained with proposed technique are shown in Fig. 9. The results obtained for $d > 0.5$ and $d < 0.5$ show that for the case of using the proposed technique the two phases of the circuit work with the 180° phase shift and the equal current sharing of the inductors are obtained for both cases of the duty cycle. Fig. 9*c* shows the experimental results of first inductor current and total rectified input current waveforms. It is seen that the input current ripple amplitude is smaller than that of the inductor current. The experimental results of the inductor currents are also observed under load changing (Fig. 10) to show the share and the balance of currents between the cells. The changes in the input current cannot be seen clearly because of the larger value of the recovery time in the transient state of the output voltage (nearly 150 ms). Since the duty cycle of the first switch is applied to the second switch with a delay of 180° phase shift, the equal current sharing of the inductors are guaranteed both at steady state and at the dynamical changes.

## 5 Conclusion

In this paper, the problem of current sharing between the inductors of the interleaved boost PFC converter is pointed out and a DSP-based simple practical solution is recommended. In the proposed technique, the equal current sharing between two cells of an interleaved boost PFC is achieved by measuring or sensing only the total current of the converter without sensing the current of each cell separately. In the proposed technique there is also no need for an extra current balance loop. The proposed technique can be used for more than two interleaved stages theoretically. However, the implementation of the proposed technique for interleaved stages is limited because of the number of PWM module in DSP. A design example of a 600 W average current controlled two-cell interleaved boost PFC circuit, which ensures minimisation of the input current ripple and proper current sharing is implemented via TMS320F2812 eZdsp controller. The results obtained from simulation and experimental works are in a good agreement and verify the proposed technique. The input power factor and input current THD of the converter obtained from experiments are 0.99 and 10.4%, respectively. The input power qualities such as power factor and THD for simulation studies are more improved than the corresponding results for experimental works. This is because of conditions of simulation studies where the input voltage is a pure sinusoidal wave and the components are assumed to be ideal. The results of the proposed study are nearly the same as those of other studies available in the literature. However, sensing only one current and eliminating current balance loop for proper current sharing are the main advantages of the proposed technique.

## 6 References


1 Athab, H.S., Lu, D.D.-C.: 'Simple controller for single-phase power factor correction rectifier', *IET Power Electron.*, 2010, **3**, (4), pp. 590–600
2 Balogh, L., Redl, R.: 'Power-factor correction with interleaved boost converters in continuous inductor current mode'. Proc. IEEE APEC'93 Conf., San Diego, CA, March 1993, pp. 168–174
3 Yang, Z., Sen, P.C.: 'A dynamically robust current control technique for boost type power factor correction circuits'. Proc. IEEE-IAS Conf., 1998, pp. 1477–1485
4 Zhou, C., Jovanovic, M.M.: 'Design trade-offs in continuous current-mode controlled boost power-factor correction circuits'. Proc. HFPC'92 Conf., 1992, pp. 209–220
5 Fu, M., Chen, Q.: 'A DSP based controller for power factor correction (PFC) in a rectifier circuit'. Proc. IEEE-APEC Conf., 2001, pp. 144–149
6 Miwa, B.A.: 'Interleaved conversion techniques for high density power supplies'. PhD thesis, Massachusetts Institute of Technology, 1992
7 Lee, P.W., Lee, Y.S., Cheng, D.K.W., Liu, X.C.: 'Steady-state analysis of an interleaved boost converter with coupled inductors', *IEEE Trans. Ind. Electron.*, 2000, **47**, (4), pp. 787–795
8 Braga, H.A.C., Barbi, I.: 'A 3-kW unity-power-factor rectifier based on a two-cell boost converter using a new parallel-connection technique', *IEEE Trans. Power Electron.*, 1999, **14**, (1), pp. 209–217
9 Lin, B.-R., Huang, C.-L., Shih, K.-L.: 'Implementation of a ZVS interleaved converter with two transformer', *IET Power Electron.*, 2009, **2**, (5), pp. 614–623
10 Cadirci, I., Yafavi, A., Ermis, M.: 'Unity power factor boost converter with phase shifted parallel IGBT operation for medium power applications', *IEE Proc. Electr. Power Appl.*, 2002, **149**, (3), pp. 237–244
11 Genc, N., Iskender, I.: 'An improved soft switched PWM interleaved boost AC-DC converter', *Energy Convers. Manage.*, 2011, **55**, (1), pp. 403–413
12 Giral, R., Martinez-Salamero, L., Singer, S.: 'Interleaved converters operation based on CMC', *IEEE Trans. Power Electron.*, 1999, **14**, (4), pp. 643–652
13 Pinheiro, J.R., Vidor, D.L.R., Grundling, H.A., Baggio, J.E.: 'Control strategy of an interleaved boost power factor correction converter'. Proc. IEEE-PESC Conf., 1999, pp. 137–142
14 Sudhakar, B.C., Veerachary, M.: 'Predictive controller for interleaved boost converter'. Proc. IEEE-ISIE Conf., Dubrovnik, 2005, pp. 577–582
15 Kim, S., Enjeti, P.N.: 'Control of multiple single-phase PFC modules with a single low-cost DSP', *IEEE Trans. Ind. Appl.*, 2003, **39**, (5), pp. 1379–1385
16 Skanda, V., Nahar, A.: 'Interleaved power factor correction (IPFC) using the dsPICDSC' (DS01278A Microchip Technology Inc., 2009)
17 Senjyu, T., Veerachary, M., Uezato, K.: 'Steady-state analysis of PV supplied separately excited DC motor fed from IDB converter', *Sol. Energy Mater. Sol. Cells*, 2001, **71**, pp. 493–510
18 Kaya, M.C.: 'Design, implementation and control of a two-stage AC/DC isolated power supply with high input power factor and high efficiency'. PhD thesis, Middle East Technical University, 2008
19 Rossetto, L., Spiazzi, G., Tenti, P.: 'Control techniques for power factor correction converters'. Proc. PMEC Conf., USA, 1994, pp. 1310–1318
20 Genc, N.: 'Design and implementation of a new unity power factor interleaved boost converter with zero-voltage-transition'. PhD thesis, Gazi University, 2010





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