Control Strategy of an Interleaved Boost Power Factor Correction Converter

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Abstract – Power factor correction interleaved boost converters provide a reduction of the inductor volume and weight when compared with the conventional PFC boost converter. However, to achieve this benefits proper current sharing and current ripple minimization must be ensured. This paper proposes a controller based on Lyapunov-likelihood control technique for interleaved boost converters (IBC) that ensures output voltage regulation and proper current share for each boost cell. In addition, a switching logic scheme for the IBC is developed to guarantee the input current ripple minimization. Extensive simulations are presented to demonstrate the performance of the proposed control and switching logic scheme.

I. Introduction

The limit imposed by regulatory agency on harmonic current drawn by equipment connected to the utility grid led to the use of power factor pre-regulators converters.

Boost power factor pre-regulators have been widely used due to their simplicity (just one switch and a diode), voltage step-up characteristic, efficiency and performance. As the power rating increases, it is often required to associate converters in series or in parallel. This is mainly due to the lack of a single device that can withstand the voltage and/or current stresses of high power applications. For high voltage applications, the three level boost PFC is a strong candidate since the voltage stresses cross the switches are limited to half of the output voltage [4,5]. Similarly, for high current applications, the interleaved boost converter is preferable, since the currents through the switches are just a fraction of the input current [1-3]. In addition, the interleaved boost can also reduce the input current ripple, for a given switching frequency, when compared with a conventional parallel and sharing techniques [6].

The main attributes of the interleaved boost converter are: (i) the inductor volume can be reduced four times (two cells) when compared with the conventional boost converter [1-4]; (ii) the current rating of the semi-conductors are reduced to half (two cells); (iii) the input current ripple can be reduced. On the other hand, the main challenge found when implementing a interleaved boost converter are: (i) current unbalances resulted from intrinsic device parameters variations and differences, which is specially critical when operating in Continuous Conduction Mode (CCM); (ii) the circuitry complexity increases if compared with conventional boost converter.

This paper proposes a simple switching logic scheme which ensures minimization of the input current ripple and develops a Lyapunov-likelihood technique for the simultaneous design of the current sharing and output voltage controllers.

II. Interleaved Boost AC-DC Converter

Fig. 1 shows a typical two cells interleaved boost converter PFC. It is comprised of a uncontrolled diode rectifier followed by two boost cells. In continuous conduction mode of the currents i_{L1} and i_{L2}, the interleaved boost converter has four possible stages of operation.

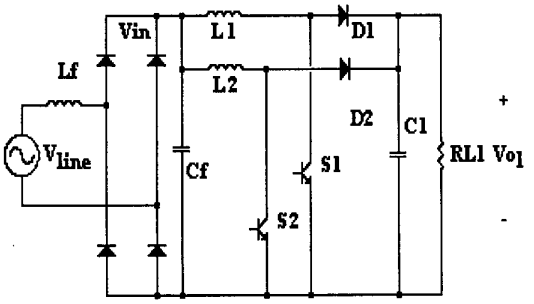

Fig. 1. Interleaved boost AC-DC converter.

First Stage: Switches S_1 and S_2 are on and the inductors currents increase. The output load current is supplied by the capacitor C_1. A diagram indicating the conduction path during this stage is shown in Fig. 2.

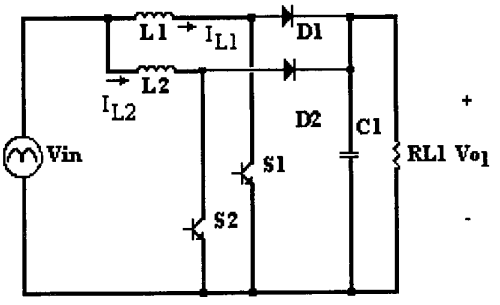

Fig. 2. First stage of operation.

Second Stage: In this stage, switch S_1 is off and switch S_2 is on. The inductor current i_{L1} has negative slope and the inductor current i_{L2} has a positive one. Fig. 3 presents the conduction path during this stage.

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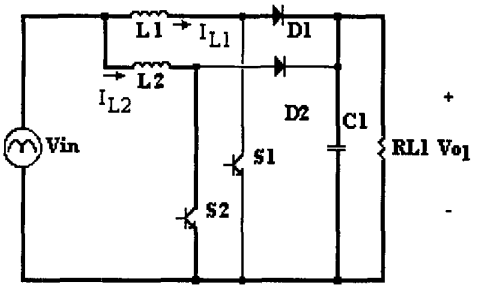

Fig. 3. Second stage of operation.

Third Stage: This stage occurs when switch S_1 is on and the switch S_2 is off. Therefore the inductors current slopes di_{L1}/dt and di_{L2}/dt are positive and negative respectively. Fig. 4 presents the conduction paths.

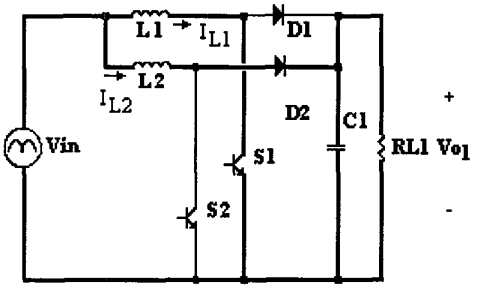

Fig. 4. Third stage of operation.

Fourth Stage: In this stage, the switches S_1 and S_2 are off. As a result, both inductors currents slopes are negative. The diagram of this stage is shown in Fig. 5.

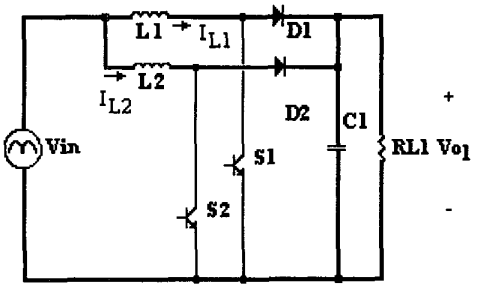

Fig. 5. Fourth stage of operation.

It is possible to see that during the second and third stages the slopes of the inductors currents are different. Therefore, this provide a degree of freedom that can be used to minimize the amplitude of the input current ripple.

III. Switching Logic Scheme

In this section, a switching logic scheme that ensures the minimization of the input current ripple is developed.

It is assumed that switches S_1 and S_2 operate with the same duty cycle, and that the variations of the input voltage $v_{in}(t)$ during one switching period is negligible.

In order to minimize the input current ripple, the PWM signals of each boost cell must be appropriately phase-shifted.

Fig. 6 shows the currents through the inductors L_1 and L_2, when $v_{in}(t)<V_O/2$. Here, it can be seen that just the stages 1, 2 and 3 occur.

When $v_{in}(t)>V_O/2$, just the stages 2, 3 and 4 occur, as can be seen in Fig. 7.

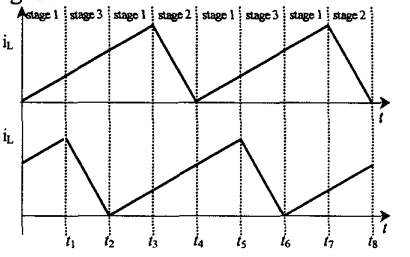

Fig. 6 – Inductor current ripple through L_1 and L_2 for $V_{in}(t)<Vo/2$

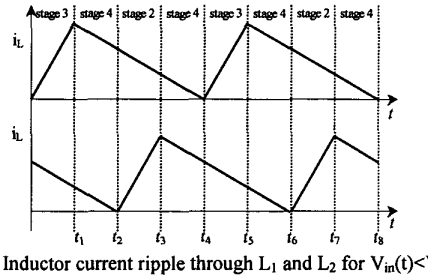

Fig. 7– Inductor current ripple through L_1 and L_2 for $V_{in}(t)<Vo/2$

Two modes of operation can be characterized depending on relative amplitude of $v_{in}(t)$ and V_0, as shown in Figures 6 and 7. Table I presents a switching logic for the boost interleaved converter which represents the above described modes.

TABLE I
SWITCHING LOGIC SCHEME

Mode 1 ($v_{in}(t)<V_O/2$)		
PWM Signal	Switches Status	Stage
High	S_1 on **and** S_2 on	1^{st}
Low	S_1 on **or** S_2 on	2^{nd} or 3^{rd}
Mode 2 ($v_{in}(t)> V_O/2$)		
PWM Signal	Switches Status	Stage
High	S_1 on **or** S_2 on	2^{nd} or 3^{rd}
Low	S_1 off **and** S_2 off	4^{th}

Once the switching logic that ensures the minimization of the input current ripple is defined, it is possible to investigate the impact of the input-output voltage ($V_O/V_{in_{max}}$) ratio and inductances ratio (L_1/L_2) on the input current ripple amplitude. In the Mode 1, the input current ripple is given by:

$$\Delta i_{in}(t) = \frac{v_{in}(t)D(t)T}{L_1} + \frac{v_{in}(t)(D(t)-1)T}{L_2}, \quad (1)$$

while in Mode 2:

$$\Delta i_{in}(t) = \frac{v_{in}(t)D(t)T}{L_1} + \frac{(v_{in}(t) - V_0)D(t)T}{L_2}, \quad (2)$$

where

$$D(t) = 1 - \frac{v_{in}(t)}{V_0}, \quad (3)$$

and V_O = output voltage, $v_{in}(t)$ = input voltage.

The high frequency input current ripple amplitude along a semi-cycle of the utility voltage for different input-output voltage ratio is presented in Fig. 8. It can be observed that the amplitude of the input current ripple depends of the input and output voltages. The ripple decreases as the ratio $V_0/V_{in_{max}}$ approaches one. In addition, the input ripple current amplitude of the boost interleaved converter is always smaller than the conventional boost for the same power and inductor trapped energy rating, even for large difference between interleaved boost inductances, as seen in Fig. 9.

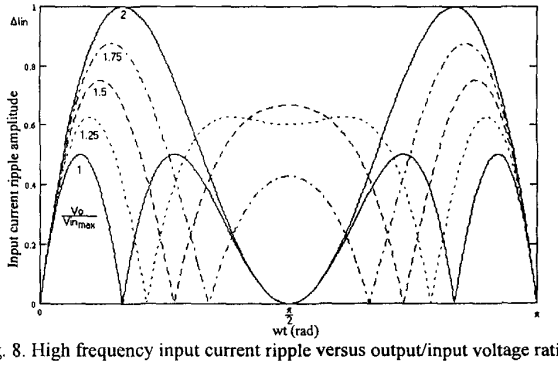

Fig. 8. High frequency input current ripple versus output/input voltage ratio.

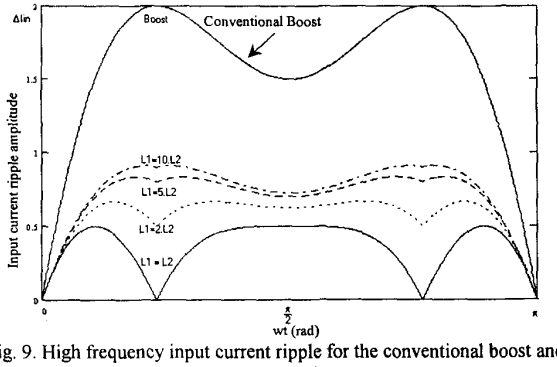

Fig. 9. High frequency input current ripple for the conventional boost and the interleaved boost.

IV. Plant and Control Objective

Based on the circuit of Fig. 1, it is possible to represent the interleaved boost converter as follows:

$$\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L1} \\ 0 & 0 & \frac{-1}{L2} \\ \frac{1}{C1} & \frac{1}{C1} & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \end{bmatrix} + \begin{bmatrix} \frac{V_{C1}}{L1} & 0 \\ 0 & \frac{V_{C1}}{L2} \\ \frac{-i_{L1}}{C1} & \frac{-i_{L2}}{C1} \end{bmatrix} \begin{bmatrix} \delta 1 \\ \delta 2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L1} \\ \frac{1}{L2} \\ 0 \end{bmatrix} (v_{in} + \Delta v_{in}) + \begin{bmatrix} 0 \\ 0 \\ \frac{-1}{C1} \end{bmatrix} io \quad (4)$$

$$[y] = [0 \quad 0 \quad 1] \cdot \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \end{bmatrix} = [v_{o1}] \quad (5)$$

where:

i_{L1} = boost inductor L_1 current,
i_{L2} = boost inductor L_2 current,
v_C = capacitor C_1 voltage,
δ_1 = switch S_1 excitation (S_1=on $\Rightarrow \delta_1$=1; S_1=off $\Rightarrow \delta_1$=0),
δ_2 = switch S_2 excitation (S_2=on $\Rightarrow \delta_2$=1; S_2=off $\Rightarrow \delta_2$=0),
v_{in} = rectified input voltage ,
Δv_{in} = additive perturbation of v_{in},
i_O = output current.

In order to simplify the control law, the following assumptions are established:

- Energy conservation principle,
- Boost inductor currents are $|I_L \sin(wt)|$,
- Input voltage is $|V_{in} \sin(wt)|$,
- Sup $|I_L \sin(wt)| = I_{LMAX}$,
- The power flux of the plant is unidirectional,
- V_{REF} is a uniformly bounded reference input signal.

The control objective can be stated as follows. Given the state space representation (4) and (5), under the above mentioned assumptions, design a controller that results a stable closed-loop system which tracks the references as close as possible, even when there is disturbances coming from the input voltage (Δv_{in}) and/or from the load.

The assumptions and control objectives are designed based on Lyapunov-likelihood techniques.

$$\dot{x}(t) = A \cdot x(t) + \beta(t) \cdot \delta + b \cdot v_{in} + D \cdot \zeta(t) \quad (6)$$

$$y(t) = C \cdot x(t) \quad (7)$$

where $x(t) = [i_{L1}(t) i_{L2}(t) v_{C1}(t)]^T$, $\delta = [\delta_1 \quad \delta_2]^T$ and $\zeta(t) = i_{01}$.

Let us consider a positive definite function V(t) given by:

$$V(t) = \frac{1}{2} x^T(t) \cdot P^{-1} \cdot x(t) \quad (8)$$

where P^{-1} is a positive definite symmetrical matrix. Therefore, the time derivative of V(t) is given as follows:

$$\dot{V}(t) = x^T(t) \cdot P^{-1} \cdot \dot{x}(t) \quad (9)$$

Then, by substituting (6) into (9) results:

$$\dot{V}(t) = x^T(t) \cdot P^{-1} \cdot (A \cdot x(t) + \beta(t) \cdot \delta + b \cdot v_{in} + D \cdot \zeta(t)) \quad (10)$$

In order to further simplify the function $\dot{V}(t)$, the matrix $\beta(t)$ can be written as:

$$\beta(t) = [\beta_1 x(t) \quad \beta_2 x(t)] \quad (11)$$

where

$$\beta_1 = \begin{bmatrix} 0 & 0 & 1/L1 \\ 0 & 0 & 0 \\ -1/C_1 & 0 & 0 \end{bmatrix} \text{ and } \beta_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 1/L2 \\ 0 & -1/C1 & 0 \end{bmatrix}.$$

In addition, defining a vector $u(t) = [v_{in}(t)\ \zeta(t)]^T$, the equation (10) can be rearranged as:

$$\dot{V}(t) = x^T P^{-1} A x + \delta_1 x^T P^{-1} \beta_1 x + \delta_2 x^T P^{-1} \beta_2 x + x^T P^{-1} B u(t) \quad (12)$$

where $B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} \end{bmatrix}$.

Therefore, in order to ensure that (8) does not increase indefinitely, it is necessary that $\dot{V}(t) \le 0$. If (12) is expressed as $\dot{V}(t) \le -x^T Q\, x$, then Q must be a positive definite matrix.

Using (12), it is possible to find a control law u(t) ($u(t) = K \cdot x(t)$), δ_1 and δ_2 such as $\dot{V}(t) \le -x^T Q\, x$. Moreover, the closed-loop control law must be able to absorb the disturbance and perturbation on $\zeta(t)$ (at load), on $v_{in}(t)$ (at input) and taking in account the conduction interval of the switches δ_1 and δ_2, such as the stored energy on L, C_1 and C_2 do not overlap the design specified limits.

Taking into account the assumptions and control objectives stated above, a controller for the interleaved boost is proposed, and it is shown in Fig. 10.

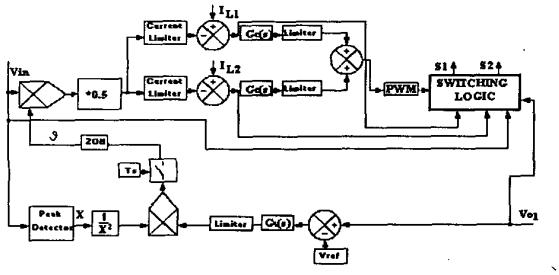

Fig. 10. The proposed control structure

To satisfy such specifications, the following control structure is proposed:

$$\dot{\omega} = \mathbf{b}^* \omega + \dot{\mathbf{e}} + \mathbf{a}^* \mathbf{e} \quad (13)$$

where: $\omega = [\omega_1\ \omega_2\ \omega_3]^T$, $\mathbf{e} = [e_1\ e_2\ e_3]^T$,

$$\mathbf{b}^* = \begin{bmatrix} -b_1 & 0 & 0 \\ 0 & -b_2 & 0 \\ 0 & 0 & -b_3 \end{bmatrix}, \quad \mathbf{a}^* = \begin{bmatrix} a_1 & 0 & 0 \\ 0 & a_2 & 0 \\ 0 & 0 & a_3 \end{bmatrix}$$

$e_1 = i_{ref1} - i_{L1}$, $e_2 = i_{ref2} - i_{L2}$, $e_3 = v_{ref} - v_{C1}$ and ($\mathbf{b}^*$, $\mathbf{a}^*$) is a controllable pair.

Control law u(t) is defined as: $\mathbf{u}(t) = \sigma \mathbf{G}\, \omega \quad (14)$

where σ is a limiter function and $\mathbf{G} = \begin{bmatrix} G_C & 0 & 0 \\ 0 & G_C & 0 \\ 0 & 0 & G_v \end{bmatrix}$.

The error equation and its time derivative are now defined by $\mathbf{e} = \mathbf{Y}_{Ref} - \mathbf{Y} \quad (15)$

and $\dot{\mathbf{e}} = \dot{\mathbf{Y}}_{Ref} - \dot{\mathbf{Y}} = \mathbf{C}\dot{\mathbf{x}} \quad (16)$

being $\mathbf{Y}_{Ref} = [i_{Ref1}\ i_{Ref2}\ v_{Ref}]^T$ and $\mathbf{Y} = [i_{L1}\ i_{L2}\ v_{C1}]^T$, or yet, if $\dot{\mathbf{e}} \to 0$ then $\mathbf{Y} \to \mathbf{Y}_{Ref}$ as $t \to \infty$.

Substituting (6) and (14) into (16), find

$$\dot{\mathbf{e}}(t) = \mathbf{C}(\mathbf{A} + \delta_1 \beta_1 + \delta_2 \beta_2)\mathbf{x}(t) + \sigma \mathbf{C}\mathbf{B}\mathbf{G}\, \omega(t) \quad (17)$$

Defining a new state vector $z = \omega - e$, and using the equation (14), then its time derivative can write

$$\dot{z} = \dot{\omega} - \dot{e} = -b^* \omega + a^* e \quad (18)$$

Rewriting the previous equation, it can be obtained

$$\dot{z} = -b^* z + (a^* - b^*)\, e \quad (19)$$

The feedback control system, (6) and (14), can be rewriting by

$$\dot{\mathbf{x}}(t) = (\mathbf{A} + \delta_1 \beta_1 + \delta_2 \beta_2)\mathbf{x}(t) + \sigma \mathbf{B}\mathbf{G}\, \mathbf{z}(t) + \sigma \mathbf{B}\mathbf{G}\mathbf{e}(t) \quad (20)$$

Defining a augmented state vector $\psi = [\mathbf{x}^T\ \ \mathbf{e}^T\ \ \mathbf{z}^T]^T$, and using the equations (17), (19), (20), and $z = \omega - e$, then it can write

$$\dot{\psi} = \begin{bmatrix} (\mathbf{A} + \delta_1 \beta_1 + \delta_2 \beta_2) & \sigma \mathbf{B}\mathbf{G} & \sigma \mathbf{B}\mathbf{G} \\ \mathbf{C}(\mathbf{A} + \delta_1 \beta_1 + \delta_2 \beta_2) & \sigma \mathbf{C}\mathbf{B}\mathbf{G} & \sigma \mathbf{C}\mathbf{B}\mathbf{G} \\ 0 & (\mathbf{a}^* - \mathbf{b}^*) & -\mathbf{b}^* \end{bmatrix} \psi = \Omega\, \psi \quad (21)$$

For the robustness analysis of the feedback system, it is considered the following positive definite function.

$$V_1 = \frac{1}{2} \sigma\, \psi^T\, \mathbf{P}^{-1} \psi. \quad (22)$$

Being its time derivative given by

$$\dot{V}_1 = \sigma\, \psi^T\, \mathbf{P}^{-1} \dot{\psi}\,. \quad (23)$$

where $\mathbf{P}^{-1}$ is a symmetrical positive definite matrix.

Substituting (22) into (24), it is obtained

$$\dot{V}_1 = \sigma z^T \mathbf{P}^{-1} \dot{z}\,. \quad (24)$$

Analyzing the equation (24) it is possible to find values to δ_1, δ_2 and $\mathbf{G}$ such as $\sigma \mathbf{P}^{-1} \Omega$ is a negative definite matrix and that $\dot{V}_1 \le 0$. Hence, it can be assured that the given system by (20) is globally stable and all feedback system signals are bounded. The gain matrixes $\mathbf{a}^*$, $\mathbf{b}^*$ and $\mathbf{G}$ can be obtained by using different techniques, such as Linear-Quadratic-Regulator.

To improve the system response it is introduced a feedforward voltage loop [7], as show Fig. 10. This loop is utilized to obtain an image of the input conductance and also the input voltage disturbance.

V. Simulation Results

In order to validate the proposed switching and control schemes for the interleaved Boost AC-DC Converter, several simulations were performed. Hereafter, some simulations results are presented, for an interleaved boost converter with the following parameters:

TABLE II
SIMULATION PARAMETERS

V_{in}=220 V_{rms}	f_{line}=50 Hz	V_o=400 V
P_o=2000 W	F_{sw}=50 kHz	$\Delta I_{in\max}$=0.5 A
L_1=1.9 mH	L2 = {1.9mH (case 1); 3.8mH (case 2)}	
C_1=4.7mF		

For the first case, it is assumed that the boost inductances are equals, that is, L_1=L_2. The obtained waveforms of the input voltage and input current (without input filter) are shown in Fig. 11. Fig. 12 shows the input rectified and inductor L_1 currents. It is important observe that the input current ripple amplitude is close to zero, when the input voltage is equal to half of the output voltage.

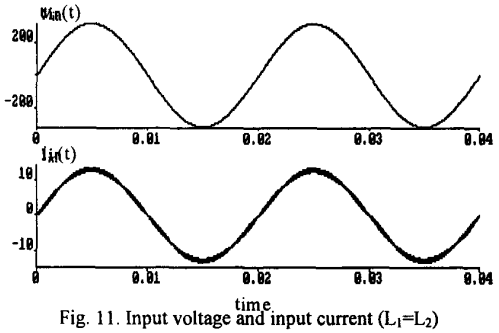

Fig. 11. Input voltage and input current (L_1=L_2)

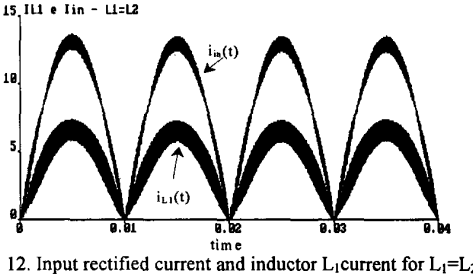

Fig. 12. Input rectified current and inductor L_1current for L_1=L_2.

Second case, it is assumed that one boost inductance is the double than the other, that is, L_2=2L_1. Fig. 13 presents the input current and L_1 inductor currents for this case. It can be observed that the input current ripple amplitude has increased. This is a result of the difference between the values of the boost inductances. Even in this case, the controller guarantees that the current through the two inductors have equals average values over one switching period.

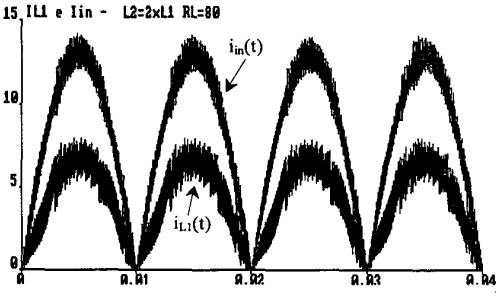

Fig. 13. Input rectified and inductor L_1 currents for L_1=2L_2.

In Figures 14 and 15 are presented the PWM signals of the power switches (S_1 and S_2) and the ripple of the currents (input and boost inductors currents), respectively, for the power factor correction interleaved boost converter operating in Mode 1 (v_{in}<V_o/2).

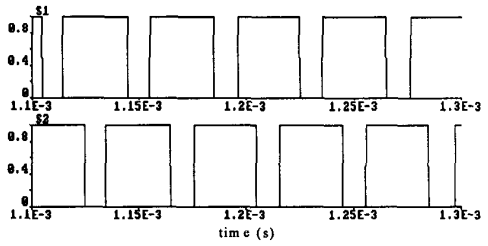

Fig. 14. PWM signals of the power switches - Mode 1.

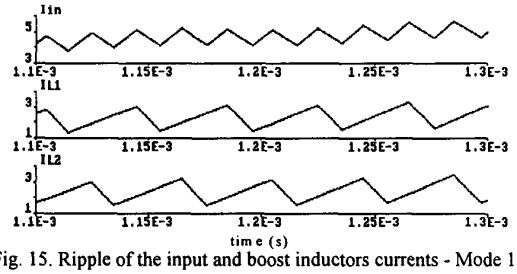

Fig. 15. Ripple of the input and boost inductors currents - Mode 1.

Figures 16 and 17 present the PWM signals of the power switches and input and inductors current, when operating in Mode 2 (v_{in}>V_o/2). It is observed from these figures, that the adequate displacement is obtained with the developed switching scheme.

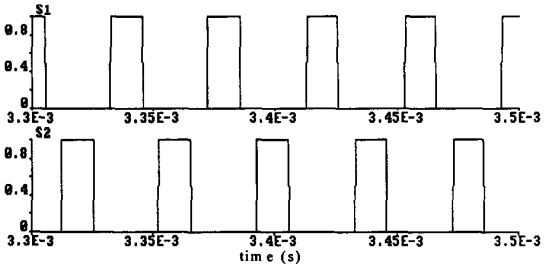

Fig. 16. PWM signals of the power switches – Mode 2.

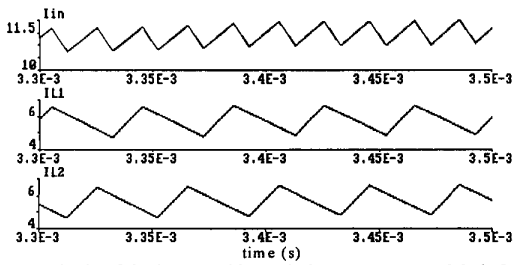

Fig. 17. Ripple of the input and boost inductors currents– Mode 2.

Figures 18 and 19 illustrate the transient of the output load due to load variation. For these load variations, the system presents similar performance of those published in [5].

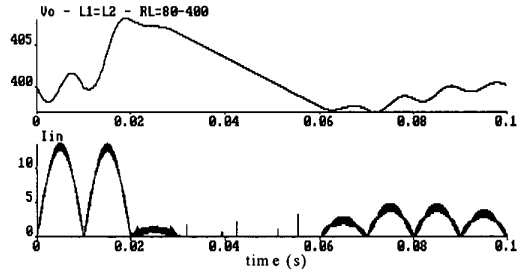

Fig. 18. Output voltage and input rectified current for load variation from 80Ω to 400Ω.

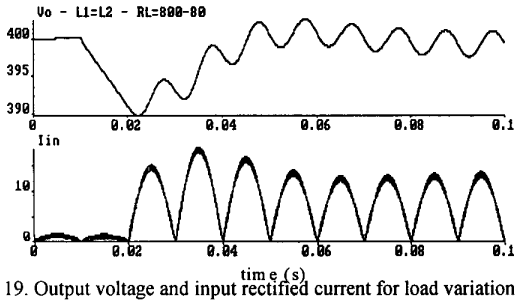

Fig. 19. Output voltage and input rectified current for load variation from 800Ω to 80Ω.

For a variation of the output power from 2000 Watts (rated power) to 200 Watts (10% of rated power), the output voltage under/overshoot is less than 5%. The time response is approximately equal to six line period. There is no distortion on the waveform of the input rectified current even during the transient.

V. Conclusions

This paper presents a new strategy of command and control for the Power Factor Correction Interleaved Boost Converter. This technique permits to share appropriately the input rectified current through the boost inductors and power switches, even in the presence of intrinsic device parametric differences and command variations, as well as in the designs with different values of boost inductances.

The analytical study and the obtained simulation results show that the input current ripple amplitude is minimized when the boost inductance are of equal values.

The interleaved boost AC-DC Pre-Regulator is an interesting alternative and choice for high current applications. This is because beyond to share the input current through the components, it reduces by four times the boost inductor volume, in comparison with the conventional boost converter.

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