Control of Multiple Single Phase PFC Modules with a Single Low-Cost DSP

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***Abstract*- In this paper, a new control scheme is proposed for controlling multiple single-phase power factor correction (PFC) modules with a single low-cost digital signal processor (DSP). The proposed scheme allows for multiple PFC modules of different current ratings to be operated in parallel and controlled via a single DSP. DSP based control handles simple current sharing and provides size reduction. The paper describes a current sense technique for each PFC module and a closed loop control algorithm for output voltage and input current control for operating multiple modules. In the example design, switching frequency is set at 120 kHz and two continuous conduction mode (CCM) PFC stages are operated in parallel and controlled via a single TMS320LF2407 DSP. Experimental results show that the proposed scheme is capable to be used for modern switching power supplies.**

I. INTRODUCTION

Parallel connection and operation of switchmode rectifiers are gaining popularity due to the following advantages: overall higher efficiency, reduced development cost due to modular design, redundancy, ease in maintenance, and high reliability [1, 2]. Further, the I^2R conduction power loss associated with power components of each module is tremendously reduced. Parallel modules have to share currents equally. Current imbalance can occur due to the component tolerances and/or parameter variations. Present industry standard for the control of switch mode rectifier systems is analog control. However, with the advent of high speed, lower cost digital signal processors (DSP), interest on digital control methods is increasing [3].

Up to now, the demands for digital processor have been on the raise due to its low cost, high speed operation, and flexibility. Most of single chip DSP provides several integrated peripherals such as PWM channels, A/D converters, etc. Therefore, DSP enables multiple functional implementations to provide efficient use of DSP [4].

This paper describes a new control scheme of multiple single-phase power factor correction (PFC) modules with a single low-cost digital signal processor (DSP). DSP based control of multiple single phase PFC modules for SMPS is mainly to obtain distributed power and efficiently to use a single DSP. Multiple PFC stages require to be controlled via a single DSP chip for current sharing since analog control IC is not able to obtain good performance. Control design is based on several techniques such as feed-forward control and the 2nd harmonic ripple rejection control on the dc output capacitor.

The advantages of the proposed digital PFC control are:

- Ability to operate multiple PFC modules of different ratings.
- Efficient and full use of the DSP capabilities
- Distributed power supply with current sharing
- Unity power factor over a wide range of input voltage.
- Digital implementation of the control strategy on a low cost DSP (TMS320LF2407).
- Smaller EMI filter due to interleaved switching pattern
- Simplified and easy to implement control algorithm.

A 16-bit fixed point DSP, TMS320LF2407, is used to evaluate for implementing PFC function based on the continuous conduction mode (CCM) operation for higher power level. Experimental results with two PFC stages in parallel are shown to demonstrate PFC control of SMPS.

II. ANALOG VS DIGITAL CONTROL

Traditionally, the implementation of the switching power supply has been accomplished by using analog power factor correction. Analog PFC control ICs which are commercially manufactured by TI/Unitrode, Fairchild, and STmicroelectronics are available and have been able to provide improved power factor employing several current control techniques [5-7]. Analog control can provide continuous processing of signal, thus allowing very high bandwidth. It also has the advantages of providing near infinite resolution of the signal measured. Analog control, however, possesses several drawbacks such as: a number of components and their susceptibility to aging and environmental variations which lead to degraded performance; the design is inflexible and its performance cannot be optimized for various utility input conditions and disturbances [8, 9]. In the view of this, this paper explores digital control strategy for multiple single phase power factor correction (PFC) stage of SMPS. Digital control method has several advantages such as: less susceptibility to environmental variation; lower part count (size reduction); and increased flexibility due to programmability and ability to implement advance control algorithm. DSP based digital control provides simple current sharing for the proposed multiple PFC structure as well. With the above advantages a smaller size SMPS could be realized with software controllability with built in serial communication.

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III. DESCRIPTION OF THE PROPOSED SCHEME

Fig. 1 shows the proposed multiple single phase PFC stage and control system. N modules are paralleled with a shared dc-link. The proposed PFC boost converter is designed to operate in continuous conduction mode (CCM) with interleaved switching pattern and is suitable for higher power levels [10]. The PFC controller senses the common input/output voltages for all modules and an inductor current per module. The controller forces the input inductor current to track the line voltage to achieve the unity input power factor. For a general single module DSP control, current sense resistor can be placed on the return path. However, the proposed multiple PFC modules do not allow such a simple sense resistor because the return path is common for all the modules. The proposed current sense technique is shown in Fig. 2. A sense resistor is placed in series with a boost switch to obtain the boost inductor current and to use it for switch protection. Analog switch acts as an analog buffer and samples a signal right before the switch is turned off and holds the current during switch turn-off time. A small low pass filter (LPF) maintains the average value of input inductor current to be

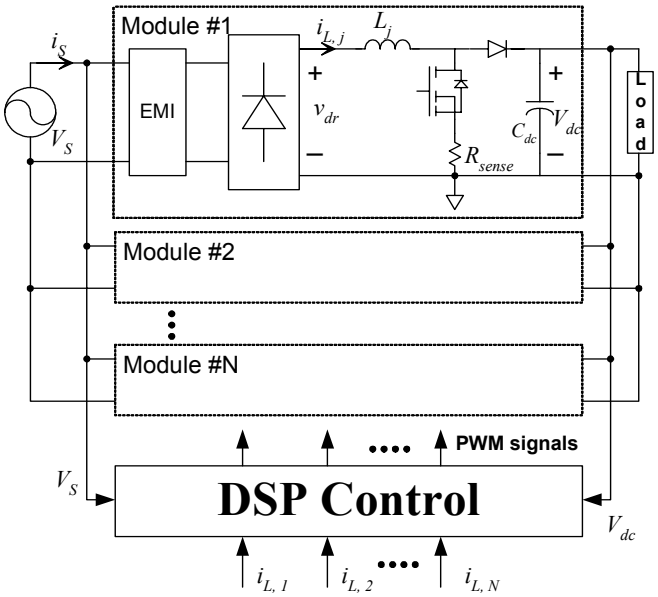


Fig. 1 Distributed power system with N paralleled PFC modules.

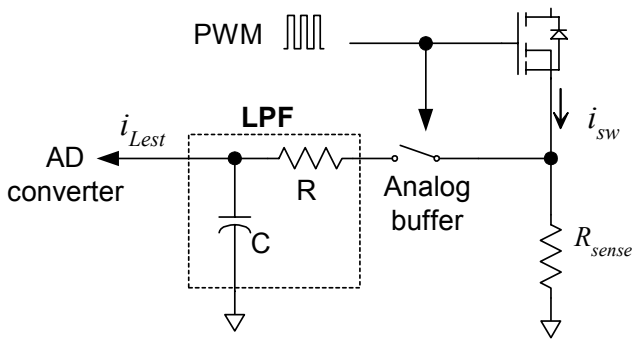
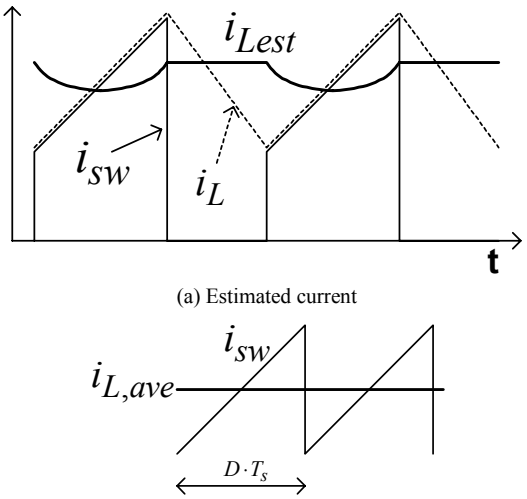


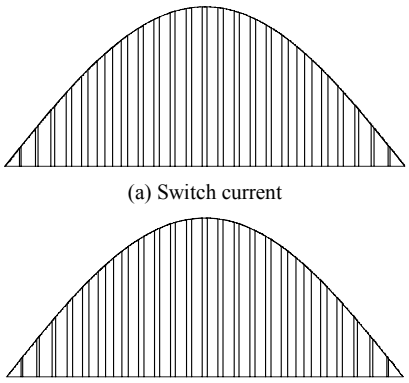
Fig. 2 Inductor current estimation with analog buffer.



(a) Estimated current

(b) Equivalent switch current by an analog buffer

Fig. 3 Inductor current waveform from estimation circuit shown in Fig. 2.



(a) Switch current

(b) Diode current

Fig. 4 Switch and diode current waveforms in PFC stage.

sensed through an AD converter in DSP. Fig. 3 shows the detail sensed waveforms using an analog buffer. The exact average current i_{Lest} can be obtained by low pass filtering of the equivalent switch current as shown in Fig. 3 (b). The sense resistor can be replaced by a high frequency current transformer. The open loop duty ratio D_{open} of boost stage is defined as,

$$D_{open} = \frac{V_{dc}^* - v_{dr}}{V_{dc}^*}, \tag{1}$$

where V_{dc}^* is the reference output voltage and the input voltage is $v_{dr} = \sqrt{2} V_s \left| \sin \omega t \right|$. The average switch ($i_{sw}$) and diode ($i_{diode}$) currents from Fig. 4 can be expressed as,

$$\begin{aligned} i_{diode,ave} &= i_L (1 - D_{open}) \\ &= \frac{V_s I_s}{V_{dc}^*} (1 - \cos 2\omega t) \end{aligned} \tag{2}$$

$$\begin{aligned} i_{sw,ave} &= i_L D_{open} \\ &= i_L - i_{diode,ave} \end{aligned} \tag{3}$$

where the input current $i_L = \sqrt{2} I_s |sin\,\omega t|$. Further, RMS currents are,

$$i_{sw} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L^2(\omega t) D(\omega t) d(\omega t)} = \sqrt{1 - \frac{8\sqrt{2}}{3\pi M}}, \quad (4)$$

$$i_{diode} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L^2(\omega t)[1 - D(\omega t)] d(\omega t)} = \sqrt{\frac{8\sqrt{2}}{3\pi M}}, \quad (5)$$

$$i_{L,rms} = \sqrt{i_{sw}^2 + i_{diode}^2}, \quad (6)$$

where, $D(\omega t) = 1 - \frac{\sqrt{2}|sin\,\omega t|}{M} = D_{open}$, and $M = \frac{V_{dc}}{V_{dr}}$ is the transfer function. Two average and RMS currents according to the conversion ratio M of the dc output voltage to the input voltage are potted in Fig. 5. From (2), the voltage ripple of the dc-link capacitor is calculated as,

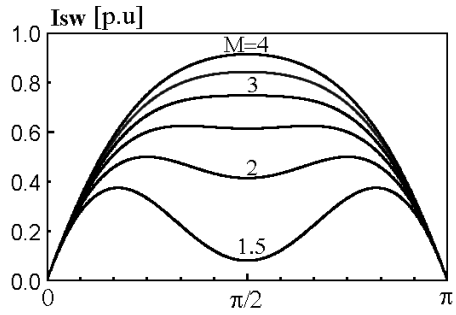
$$V_{dc,ripple} = \frac{1}{C_{dc}}\int i_c dt = -\frac{i_{diode,ave}}{2\omega C_{dc}} sin\,2\omega t, \quad (7)$$

where C_{dc} is the dc-link capacitance and i_c is the output capacitor current. Based on the calculation of RMS switch current, the power loss through a sense resistor is obtained as shown in Fig. 6. The loss can be 40% of general PFC scheme assuming M=2. Fig. 7 shows the input current waveforms with interleaved switching pattern of multiple circuits. The switching frequency appears N times as high to the input utility side [11]. Therefore, EMI filter can be minimized in the proposed multiple PFC scheme.

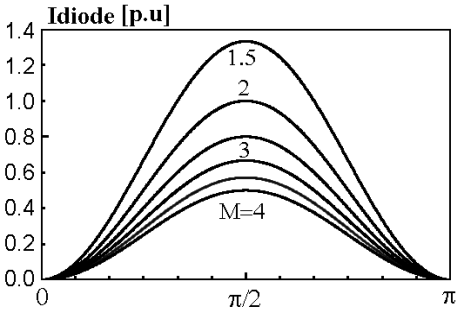
IV. CONTROLLER DESIGN

As shown in Fig. 8 (a), conventional boost PFC stage consists of two control loops: an inner current control loop and an outer voltage loop. This type of control has several disadvantages such as: input current distortion near zero crossing and slow responses for line disturbances and load changes. To address these issues, a new digital control strategy is proposed in this paper. Three feed-forward control is added into the conventional PFC control to achieve higher control performance. The rectified voltage v_{dr} can be considered as a disturbance since the input voltage of the boost converter is basically a dc quantity. Based on (1), the feed-forward open loop duty ratio, according to conversion ratio M, is calculated as shown in Fig. 8 (b) and the closed loop duty ratio D_{pi}, which contains a small amount of variations depending on load conditions, is obtained from current control. The switch gate input, or final duty ratio D_{total} is obtained by adding two duty cycles,

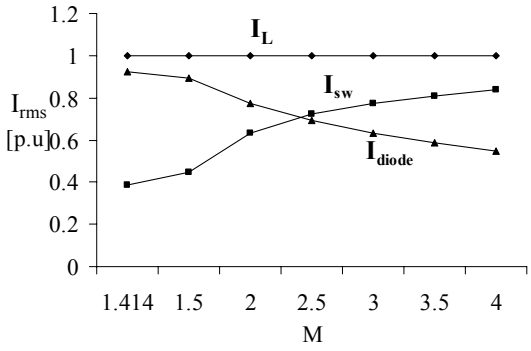
$$D_{total} = D_{open} + D_{pi}. \quad (8)$$



(a) Average switch current



(b) Average diode current



(c) RMS current

Fig. 5 Average and RMS currents

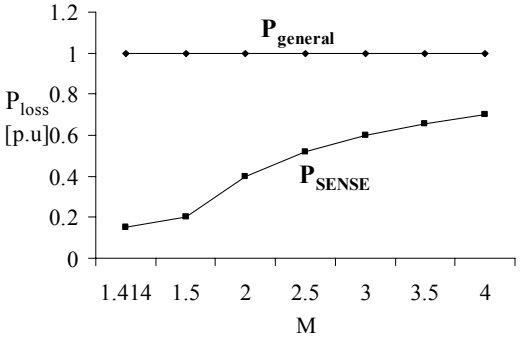
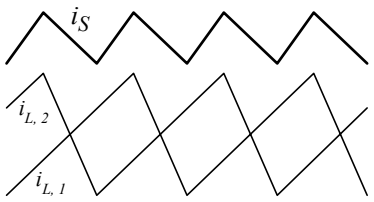
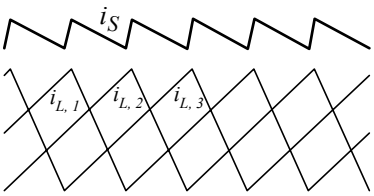


Fig. 6 Power loss in sense resistor.

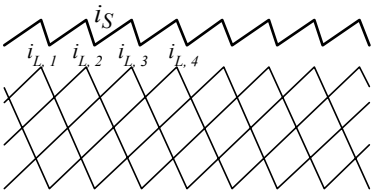
($P_{general}$: Power loss in PFC stage)



(a) N=2



(b) N=3



(c) N=4

Fig. 7 Input current waveform due to multiphase converter operation.

The average of final duty cycle D_{total} is the same as D_{open} since the average of D_{pi} is zero. Fig. 9 illustrates the control responses for open loop feed-forward control. It is shown that the output average dc voltage can be regulated with 2nd harmonic ripple but the input current is distorted. Therefore, this method requires the digital PI current regulator to be more effective around zero crossover point of the input current. The control for multiple PFC stage consists of a total current control (Fig. 8 a) and a feed-forward control (Fig. 8 b), and a current control of each module (Fig. 8 c). The total input current is obtained from the proposed current sense technique,

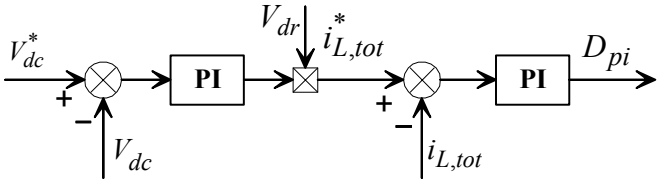
$$i_{L,tot} = i_{L,1} + i_{L,2} + \cdots + i_{L,N} . \quad (9)$$

Since the final duty cycle for each module is updated with the correction due to tolerances and parameter variations, the each current control can be implemented by a simple proportional controller (Fig. 8 c). The gate input for each module is,

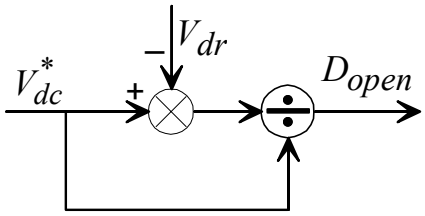
$$D_j = D_{total} + (i^*_{L,tot} - N \cdot i_{L,j}) \cdot K , \quad (10)$$

where j=1,2,…,N and K is a gain factor. Fig. 10 shows an example for load sharing using two modules with different VA ratings. Basically, all power ratings must be the same until one reaches rated power. And then the rest of power is obtained from the other module.

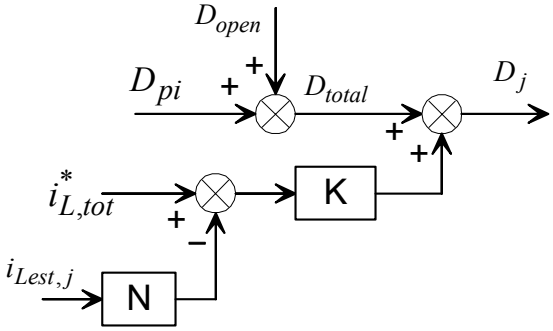
A dc output voltage across the capacitor in the PFC front-end converter contains a 2nd harmonic ripple at twice the line frequency. This ripple cannot be eliminated with a realistically sized bulk capacitor and results in the input current distortion since the output of the voltage controller contains harmonics instead of a near dc component [12-14]. The bandwidth of the voltage control is generally below 30Hz for a 60Hz utility system. In this case, the dynamic response of an output voltage for sudden load changes cannot be improved. Therefore, the



(a) General control block



(b) Feed-forward control



(c) Duty ratio calculation for each module

Fig . 8 PFC control in paralleled N modules.

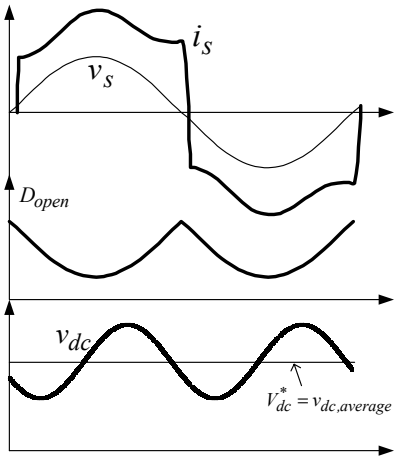


Fig. 9. Input current and output voltage responses by open loop duty ratio.

control signal of the 2nd harmonic ripple needs to be eliminated. It can be assumed that the output of the voltage control is,

$$C_{pi} = \alpha_o + \alpha \sin 2\omega t , \quad (11)$$

where α_o is a dc quantity in ideal case and α is a scale factor given by dc voltage ripple and voltage PI controller. The rectified current i_L is calculated by,

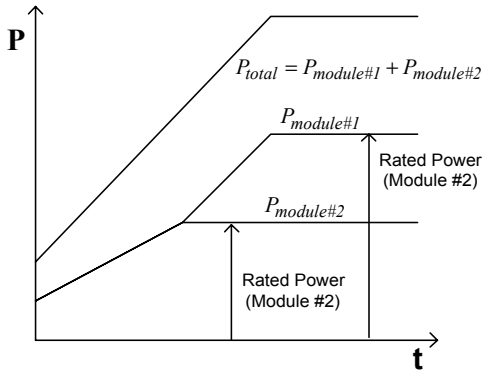


Fig. 10 Load sharing for different power modules.

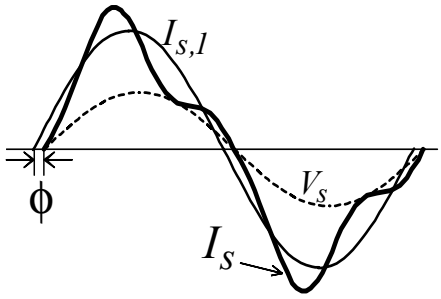


Fig. 11 Effects on 2nd harmonic voltage ripple.

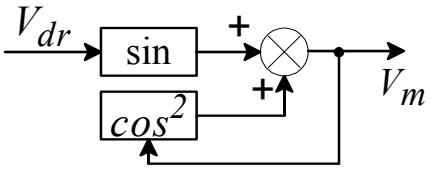


Fig. 12 Instantaneous voltage magnitude calculation.

$$i_L = \alpha_o \left| sin\,\omega t \right| + \alpha\, sin\, 2\omega t \left| sin\,\omega t \right| . \quad (12)$$

Based on this current, the input current i_s has a leading displacement power angle ϕ and contains a fundamental component and other harmonics such as 3rd, 5th, 7th, etc. due to 2nd harmonic ripple. Fig. 11 shows the input current and its fundamental waveforms. Therefore, the magnitude of the 2nd harmonic component which can be estimated and feed-forwarded needs to be cancelled. The dc voltage rejecting the 2nd harmonic ripple is obtained by adding the reversed ac component as,

$$\hat{V}_{dc} = V_{dc,sense} + \frac{V_s I_s}{2\omega C_{dc} V_{dc}^*} sin\, 2\omega t , \quad (13)$$

$$V_s I_s = \frac{V_m I_m}{2} , \quad (14)$$

where $\hat{V}_{dc}$ is a ripple free dc voltage and V_m and I_m are the magnitudes of input voltage and current. To detect the line voltage disturbances, the magnitude of the input voltage is calculated on the synchronous reference frame. The dc magnitude V_m of the utility voltage shown in Fig. 12 is instantaneously updated by,

$$V_m = V_{dr}\, sin\,\theta + V_m\, cos^2\,\theta . \quad (15)$$

Similarly input current magnitude is calculated. Therefore, the fast response of voltage control can be achieved by adding 2nd harmonic ripple on dc voltage sensing.

V. Digital Implementation

The proposed PFC approach is implemented on TMS320LF2407 DSP which provides a function of 16 bit fixed-point arithmetic with unique one-chip peripherals and is designed to meet a wide range of digital motor control and other control applications [4]. The DSP comes from the 24x family, which is optimized for control applications. It has a 30Mhz CPU clock and several peripherals such as Event Manager, CAN Interface, SPI, SCI, and ADC modules. The DSP communicates with a personal computer through a serial port. The TMS320LF2407 DSP also has a flash ROM, allowing it to be reprogrammed for software updates. The '240x series of TI DSP controllers combines this real-time processing capability with controller peripherals to create an ideal solution for control system applications.

As shown in Fig. 1, the rectified voltage v_{dr}, output dc voltage V_{dc}, and inductor current $i_{L,j}$ are sensed through A/D converters. Maximum 10 gate signals for 10 multiple modules are obtained from PWM channels. An inner current control loop is always faster than an outer control for dc voltage. Therefore, the control loop sampling frequency, which is synchronized with current control, is set to 60 [kHz], voltage loop frequency is 10[kHz], and the switching frequency is 120[kHz]. Due to the slow sampling frequency, the proposed current sense technique is required. For safety issue, the duty ratio has limitations as a function of input voltage [15],

$$D_{\lim it}(\omega t) = \frac{T_{on}}{T_s} = \frac{\Delta I \cdot L_{boost}}{v_{dr}(\omega t) \cdot T_s} . \quad (16)$$

where T_s is a sampling period and ΔI is allowable peak to peak current. To provide a monitoring function, the DSP can be interfaced with a computer so that average voltage, current, and power are displayed on a monitor. Average power is obtained as,

$$P_{ave} = \frac{1}{\pi}\int_0^{\pi} v_{dr}(t) i_L(t) d\omega t . \quad (17)$$

Flow chart is shown in Fig. 13 for real implementation. Outer control loop with 10kHz loop frequency includes 2nd harmonic rejection algorithm and dc output voltage control. And inner loop consists of analog to digital conversion, reference current calculation, current control, feed-forward control, etc.

VI. Experimental Results

Real implementation circuit is shown in Fig. 14. Two laboratory prototype 250W PFC modules are connected in parallel. High frequency current transformer is used for current sensing instead of sense resistor. The modules are controlled

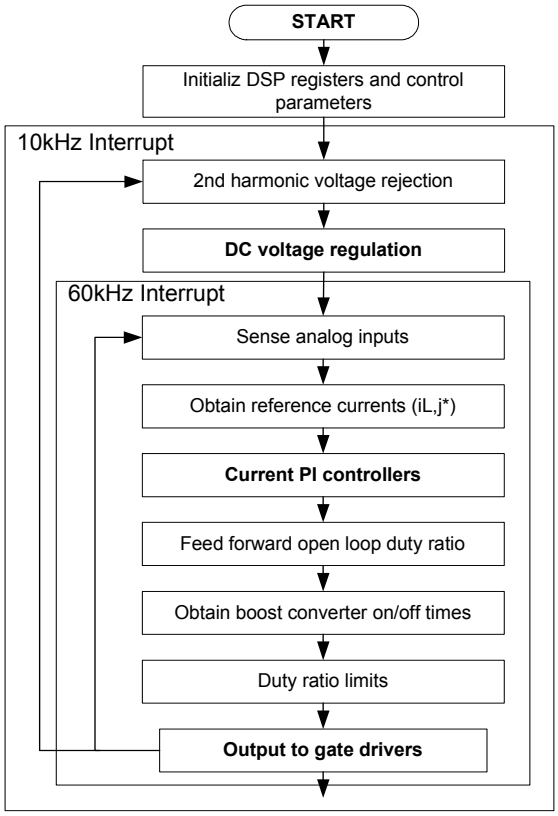


Fig. 13 Flow chart for real implementation.

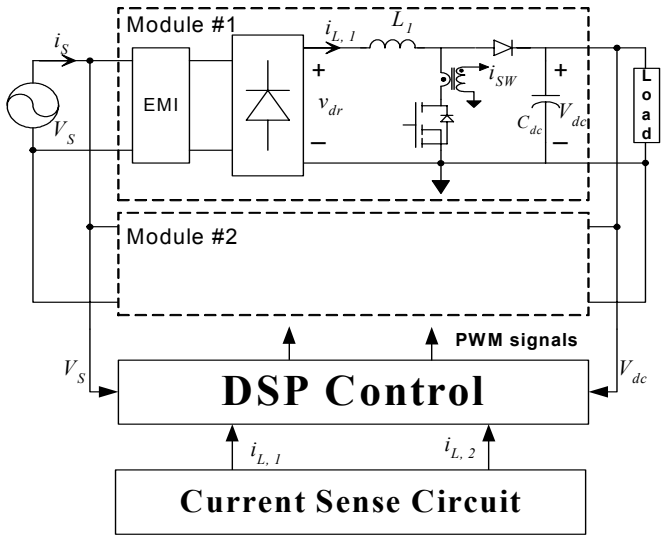


Fig. 14 Detail implementation circuit.

by a single DSP chip. Experimental results are shown in Fig. 15 and Fig. 16. The output voltage contains 2nd harmonic ripple on the output capacitor as shown in Fig. 15. By employing the proposed control scheme such as separate current sensing method, feed-forward control, and the 2nd harmonic ripple rejection control on the dc output capacitor, the input power factor is near unity and DC output voltage is 240V with high 2nd ripple due to small electrolytic capacitor.

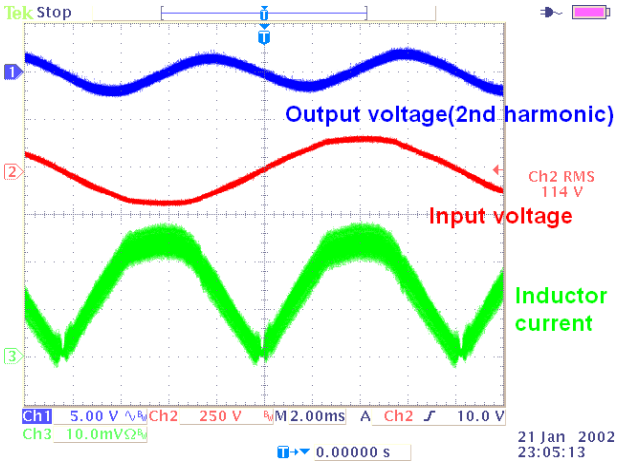
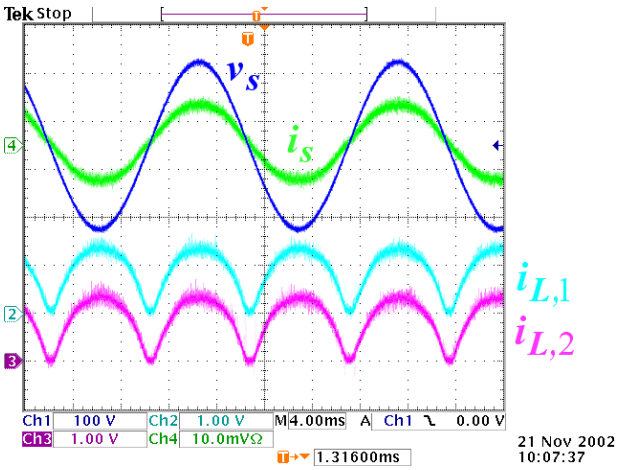
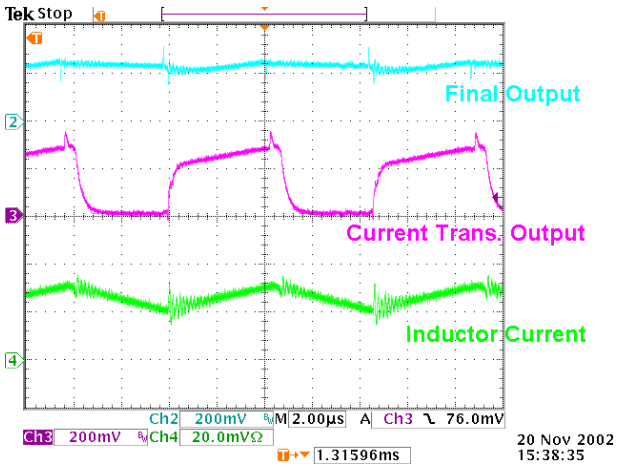


Fig. 15 Experimental results (Single module control).



(a) Input current waveforms



(b) Waveforms from current sense circuit

Fig. 16 Experimental results with two PFC modules.

Experimental results with two PFC modules are shown in Fig. 16. Current sharing in two different modules is achieved as shown in Fig. 16 (a). Using a current transformer in series with the boost switch, the input inductor current can be estimated for DSP control (Fig. 16 b).

VII. CONCLUSIONS

In this paper, a new control scheme has been proposed for controlling multiple single-phase power factor correction (PFC) modules with a single low-cost digital signal processor (DSP). A single DSP has been employed to achieve the current sharing and reduce the size of power supply with multiple PFC structures. A current sense technique has been proposed to sense each current in a separate PFC module. Further, feed-forward and 2nd harmonic ripple rejection controls have been presented to improve the control performance. Experimental results demonstrate the capability of the proposed control scheme for multiple PFC stage.

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