Boost Interleaved PFC versus Bridgeless Boost Interleaved PFC Converter Performance/Efficiency Analysis

Mihaela-Codruta ANCUTI*, Marcus SVOBODA*,
Sorin MUSUROI*, Alexandru HEDES*,
Department of Electrical Engineering,
University *Politehnica* of Timisoara,
Timisoara, Romania
codruta-m.ancuti@upt.ro, marcus.svoboda@upt.ro,
sorin.musuroi@upt.ro, alexandru.hedes@upt.ro

Nicola-Valeriu OLARESCU**, Martin Wienmann**
AKO-DIEHL Controls,
Munchen, Germany,
nicola.olarescu@diehl-controls.com,
martin.wienmann@diehl-controls.com

***Abstract*— In the last two decades, a great part of research in the power electronics area has been involved in finding methods of improving the input current waveform while simultaneously avoiding phase displacement. The aim of the paper consists of selecting two of the most relevant single phase power factor correction (PFC) topologies currently existing for the power range of 1.5 kW up to 4 kW and to analyse and evaluate them. The investigated topologies are the boost interleaved PFC converter and the bridgeless boost interleaved PFC converter. Performances of the two studied topologies are simulated in Matlab/Simulink. Loss analysis and efficiency evaluation are also provided. The simulation results verify that the bridgeless boost interleaved PFC converter demonstrates a slightly higher efficiency than the interleaved boost PFC converter topology.**

Keywords — boost interleaved converter, bridgeless boost interleaved converter, power factor correction (PFC)

I. INTRODUCTION

For single-phase low power applications, Power Factor Correction (PFC) converters are designed in order to ensure a high power factor at the mains side, and to emulate a purely resistive operation of the diode bridge-based front-end rectifier. One major drawback, related to the PFC circuits, is that they involve additional losses, thus reducing the overall efficiency.

The PFC solutions can be categorized as *passive* or *active*, [1]-[2]. For passive PFC, only passive elements are used in addition to the diode bridge rectifier, to improve the shape of the line current. Obviously, the output voltage is not controllable. Even though the passive PFC converters are simple, , their disadvantages make them not being suitable for industrial applications because they demonstrate poor dynamic response, lack of voltage regulation, the shape of input current depend on the load, thus the power factor is reduced.

For active PFC, active switches are used in conjunction with reactive elements in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage. The switching frequency further differentiates the active PFC solutions into two classes: *In low-frequency* active PFC, switching takes place at low-order harmonics of the line-frequency and it is synchronized with the line voltage. *In high-frequency* active PFC, the switching frequency is much higher than the line frequency.

An active PFC is using active switches in conjunction with reactive elements in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage. Because active PFC uses a circuit to correct power factor, active PFC is able to generate a theoretical power factor of over 95%, up to 99%, but they are expensive [5].

The boost PFC topology is an active PFC converter topology, suitable for a low to medium power range up to approximately 1kW due to the diode bridge losses which significantly degrade the efficiency by dissipating heat in a limited area.

The boost interleaved converter has the advantage of paralleled semiconductors. It also reduces output capacitor high frequency ripple, but it still has the problem of heat management for the input diode bridge rectifiers [3].

The inductor ripple current cancellation allows the a reduction in boost inductor magnetic volume. This is due to the energy storage requirement of the two interleaved inductors being half that of single stage designed for the same power level, switching frequency and inductance. But, the reduction in energy storage does not directly translate into magnetic volume reduction [4].

The family of bridgeless boost converters has been widely used since it allows considerable reduction in conduction losses providing increased global efficiency of the converter structure [5].

Compared to the boost interleaved PFC converter, the bridgeless boost interleaved PFC converter introduces two more FETs and two more fast diodes in place of four slow diodes used in input bridge for the former converter. In this

978-1-4799-4161-2/14/$31.00 ©2014 IEEE

case the application of the interleaving of multiple converters cells technique is interesting because allows the division of the current stresses in the semiconductors [6].

Based on literature studies, efficiency improvement is expected for the bridgeless interleaved PFC topology compared with the interleaved boost PFC topology.

The general aim of this paper is to investigate the performances/efficiency of the two PFC topologies: the boost interleaved PFC converter and the bridgeless boost interleaved PFC converter. Losses analysis and efficiency evaluation of the two above mentioned converters is also provided.

II. BOOST INTERLEAVED PFC CONVERTER TOPOLOGY

The boost interleaved PFC converter topology is presented in Fig. 1. It uses a dedicated diode bridge to rectify the AC input voltage to DC, which is then followed by two boost PFC converters in parallel, operating 180o out of phase.

The boost interleaved PFC converter has the advantage of paralleled semiconductors. The input current is the sum of two inductor currents, therefore it reduces output capacitor high frequency ripple, but it still has the problem of heat management for the input diode bridge rectifiers.

The hardware implementation for the boost interleaved PFC converter topology as well as its controller implementation is done in Matlab/Simulink environment as depicted in Fig. 2. Its functionality is described below.

The measured DC bus voltage is compared with a reference voltage. The resulting voltage error is then fed into a PI voltage controller for zero error DC bus voltage regulation. The output of the controller is taken as amplitude of the reference supply current and is fed to the inner controller.

In addition, in order to emulate a pure resistor behavior, the current reference must have the same shape as the rectified source voltage V_{DC}, with an adjustable magnitude. An analog multiplier is used for this purpose.

The sensed inductance current is then subtracted from the reference current and limited. By its comparison with two triangular carriers of 48 kHz (180° phase-shifted from each other), gate commands for Q_1, respectively for Q_2 MOSFET devices are generated.

To ensure high stability of the control system, the outer loop is designed to be enough slower than the inner one.

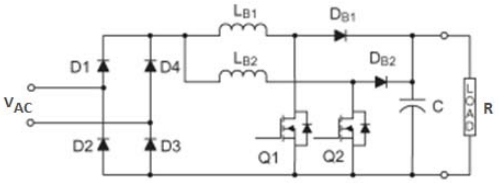

Fig. 1. BOOST INTERLEAVED PFC converter topology

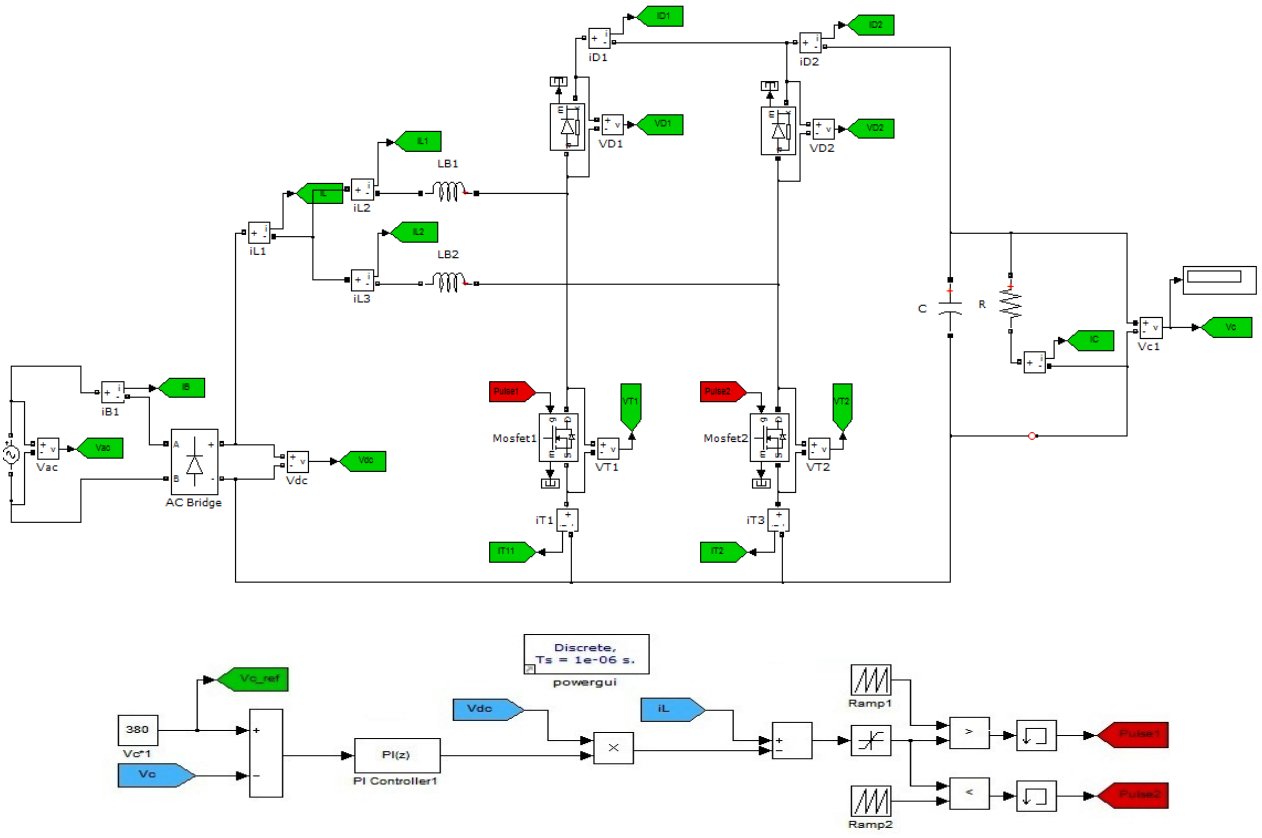

Fig. 2. Boost Interleaved PFC converter model implementation in Matlab/Simulink

III. BRIDGELESS BOOST INTERLEAVED PFC CONVERTER TOPOLOGY

In the bridgeless boost interleaved configuration topology shown in Fig. 3, the need for the rectifier input bridge is avoided by making use of the intrinsic body diode connected between drain and source of MOSFET switches. Two more MOSFETs and two more fast diodes are introduced in place of four slow diodes used in the input bridge of the interleaved boost PFC converter. It retains the same semiconductor device count as the boost interleaved PFC converter presented in the precedent paragraph.

It control consists in two loops. A slow outer control loop is used to regulate the output voltage V_o to a constant reference voltage and to generate a reference current signal for the fast inner current control loop with similar waveform shape of the rectified input voltage, as it is shown by its implementation in Matlab/Simulink in Fig. 4.

Further, the current error signal is compared with a triangular carrier of 48 kHz and the resulted signal is then compared with the AC voltage signal, providing the gate commands for Q_1 and Q_3 MOSFET devices.

The gate commands for the other two switches Q_2, respectively for Q_4 are generated by comparing the current error signal with a second triangular carrier of 48 kHz, which is 180° phase-shift from the first one.

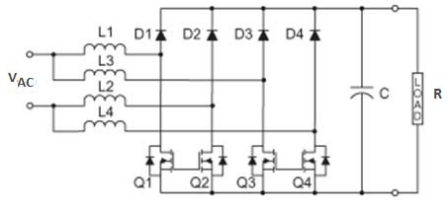

Fig. 3. BRIDGELESS BOOST INTERLEAVED PFC converter topology

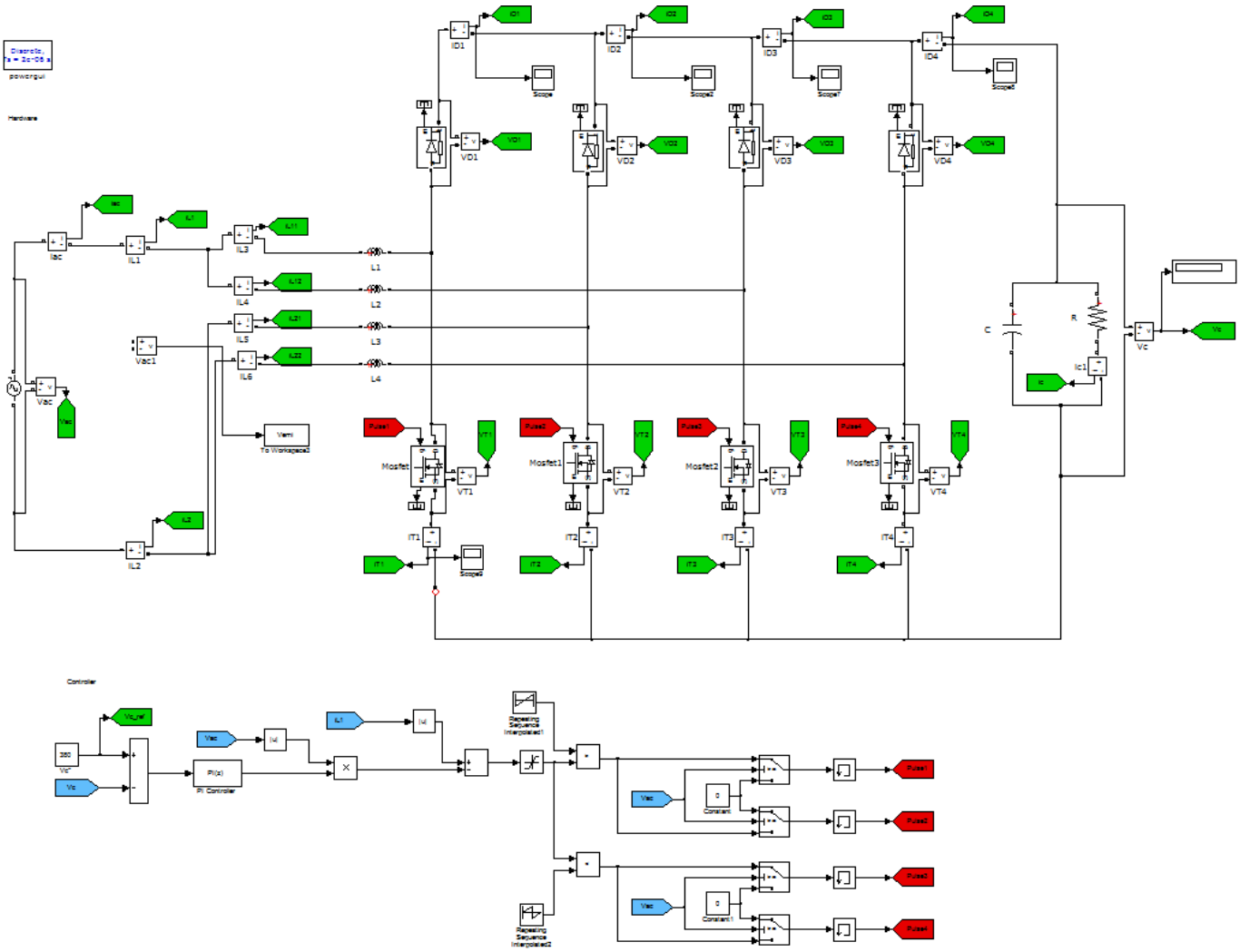

Fig. 4. Bridgeless Boost Interleaved PFC converter model implementation in Matlab/Simulink

IV. Simulation Results

1) Simulation results for the Interleaved Boost Power Factor Correction Converter

The following assumptions were made before proceeding with the performances analysis of the two converters topologies:

- Continuous conduction mode (CCM) operation is assumed;
- Unity power factor achievement, i.e. the line current is in phase with the input line voltage, and has a sinusoidal waveform;
- The PFC output voltage regulation, with minimum ripple.

The simulation results presented in this paragraph were obtained in the next operation conditions and parameters: input AC voltage set to 230 [V] (RMS), a 48 [kHz] switching frequency, the DC-link capacitor voltage controlled to around 380 [V] by a PI type controller, the dc capacitance C around at 780 [μF], the two inductances in case of boost interleaved topology $L_{B1} = L_{B2} = 150$ [μH], respectively the four inductances in case of bridgeless boost interleaved topology $L_1 = L_2 = L_3 = L_4 = 300$ [μH] and the resistive load set to 57.76 [Ω].

The parameters of PI controller are: kp = 0.05e-3, ki = 0.01 and the hysteresis band is ± 0.8.

The simulation results showing the two PFC converter topologies performances (waveforms of the input voltage, input current, current through one inductor, current per one diode, sensed current per one MOSFET device) are next presented (see Fig. 5 – Fig. 9). The reference and the regulated DC voltage is shown in Fig. 10. They were all obtained for operation at P = 2.5 kW.

The simulations were carried out for different loading conditions at 48 [kHz] switching frequency, in order for the efficiency curves to be drawn, as shown in Fig.11.

Table I presents the RMS and average values for one MOSFET (I_{mosfet}), one diode (I_{diode}) and one inductance (I_{ac}). The losses for the two PFC converter topologies, as per Table II, were computed based on the catalogue parameters for the MOSFET, diode and inductance devices, as follows: R_{mosfet} = 0.38 [Ω], R_{diode} =0.118 [Ω] and R_{copper}=0.075 [Ω]. $P_{mosfet\ COND}$ and $P_{mosfet\ SW}$ stand for the conducting losses, respectively for the switching losses. P_{diode} and P_{copper} stand for the diode losses, respectively for the copper losses in inductor.

The employed equations for power losses computation are:

$$P_{diode} = R_{diode} * I_{diode(RMS)}^2 \quad (1)$$

$$P_{mosfet\ COND} = R_{mosfet} * I_{mosfet(RMS)}^2 \quad (2)$$

$$P_{mosfet\ SW} = (E_{on} + E_{off})*f_{sw} \quad (3)$$

$$P_{copper} = R_{copper} * I_{ac(RMS)}^2 \quad (4)$$

Where E_{on} and E_{off} represent the turn-on energy (the mosfet is on), respectively the turn-off energy (the mosfet is off) and they can be read from Fig. 5, respectively Fig. 6.

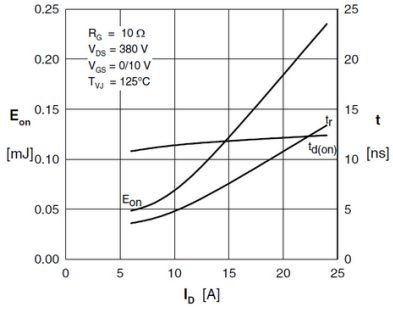

Fig. 5. Typ. Turn-on energy and switching times versus drain current, inductive switching.

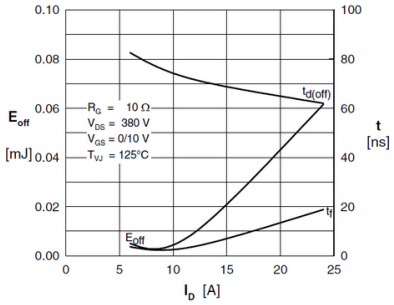

Fig. 6. Typ. Turn-off energy and switching times versus drain current, inductive switching.

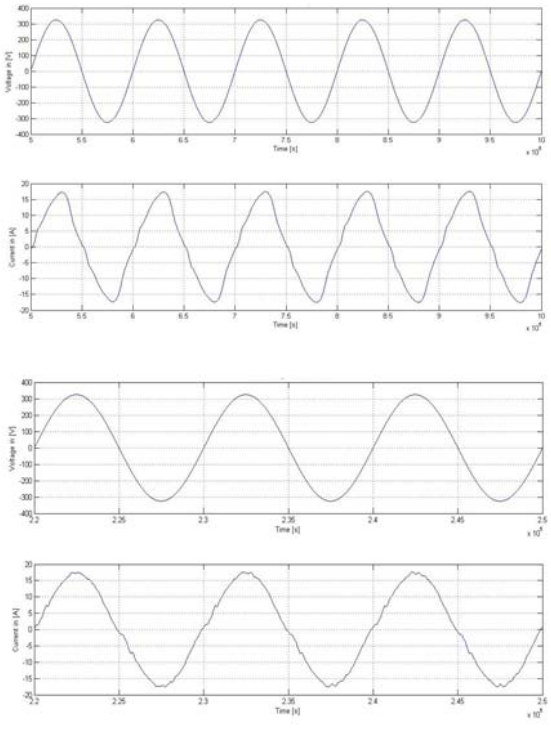

Fig. 7. Zoom on input voltage & input current for the BOOST IL topology (a), respectively for the BRIDGELESS BOOST IL (b).

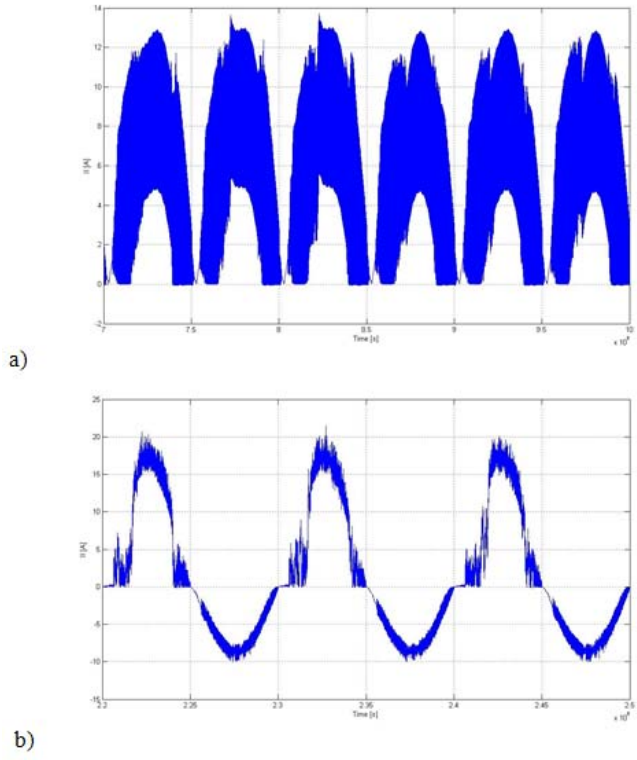

Fig. 8. Zoom on inductance current for the BOOST IL topology (a), respectively for the BRIDGELESS BOOST IL (b).

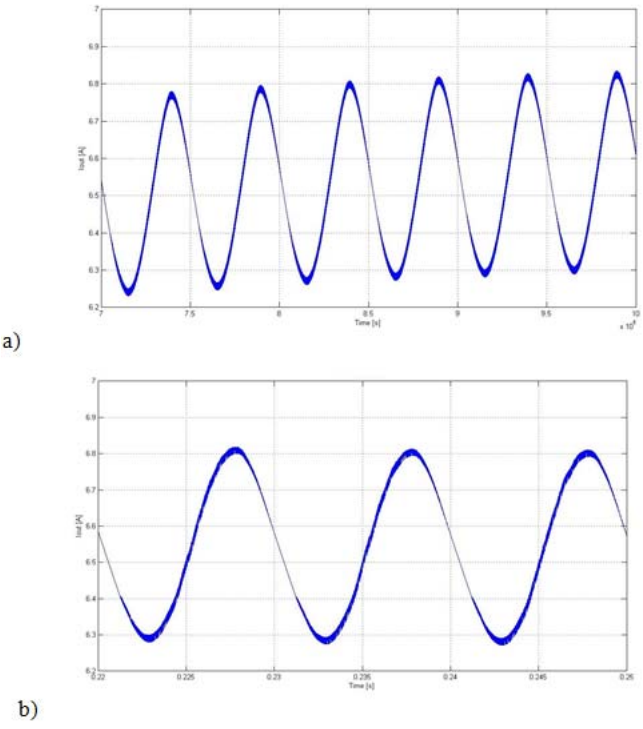

Fig. 9. Zoom on capacitor current for the BOOST IL topology (a), respectively for the BRIDGELESS BOOST IL (b).

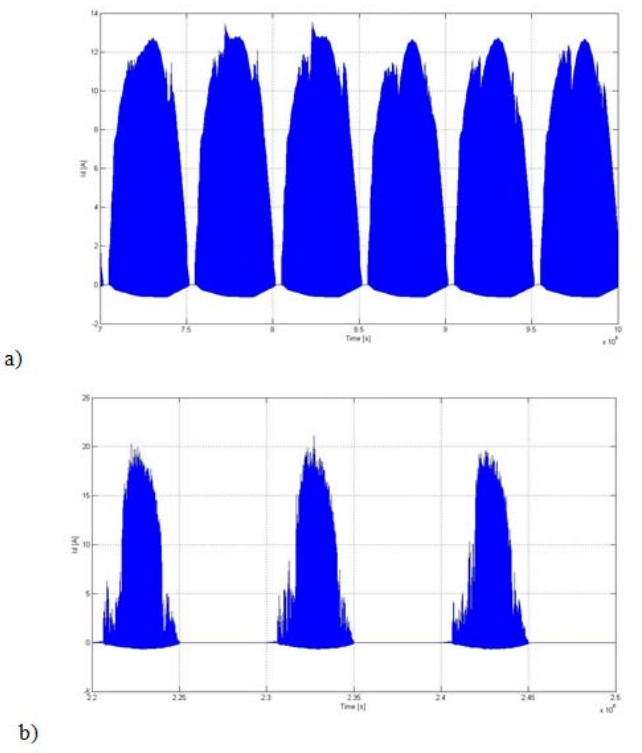

Fig. 10. Zoom on diode current for the BOOST IL topology (a), respectively for the BRIDGELESS BOOST IL (b).

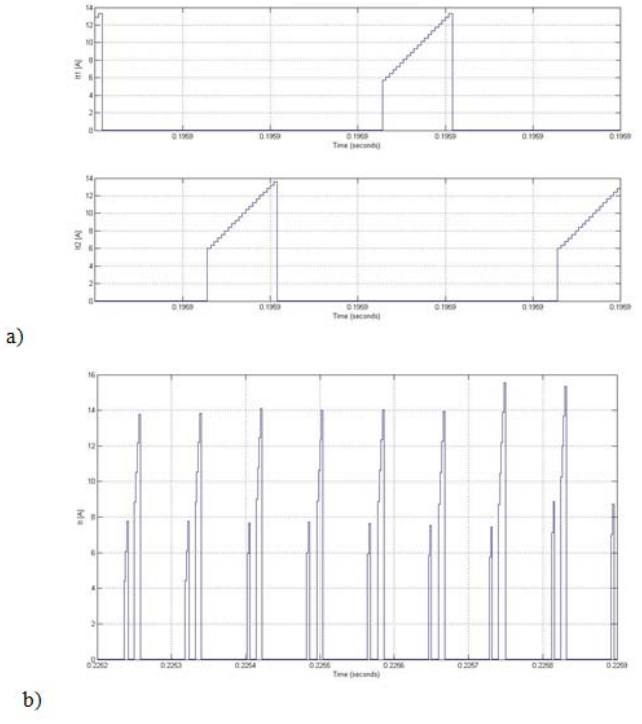

Fig. 11. Zoom on Mosfet currents for the BOOST IL topology (a), respectively for the BRIDGELESS BOOST IL (b).

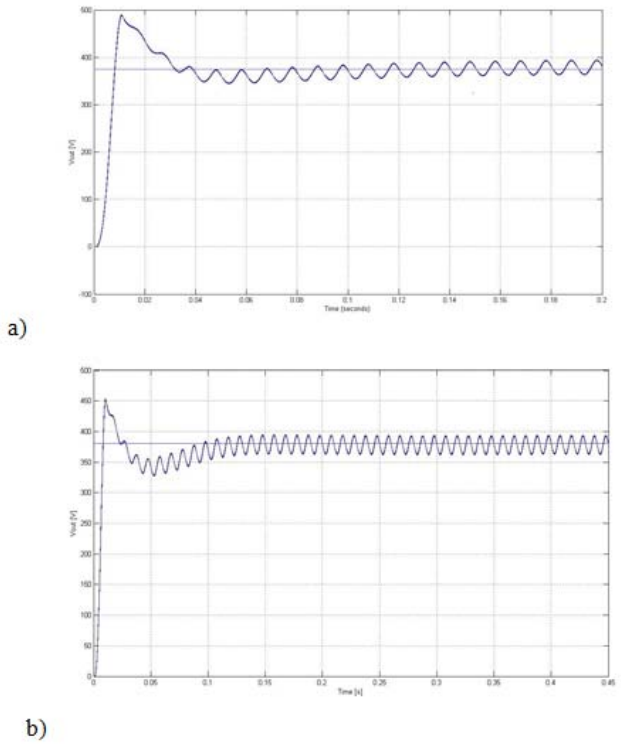

Fig. 12. Voltage output for the BOOST IL topology (a), respectively for the BRIDGELESS BOOST IL (b).

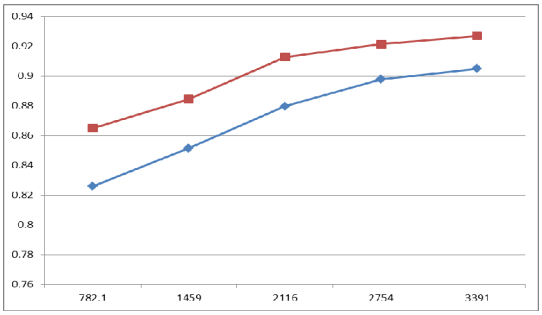

Fig. 13. Efficiency versus power curve for the BOOST INTERLEAVED (blue line) and BRIDGELESS BOOST INTERLEAVED (red line) topology.

TABLE I. RMS & AVG VALUES [A]

Topology		*RMS*	*AVG*
BOOST INTERLEAVED	**Imosfet [A]**	4.088	9.226
	Idiode [A]	0.4393	0.3881
	Iac [A]	11.68	0.007998
BRIDGELESS BOOST INTERLEAVED	**Imosfet [A]**	5.535	1.482
	Idiode [A]	6.229	2.539
	Iac [A]	11.88	0.0202

TABLE II. BREAKDOWN OF LOSSES AT NOMINAL LOAD [W]

Topology	*Pdiode/1device [W]*	*Pmosfet COND/1device [W]*	*Pmosfet SW/ 1device [W]*	*Pcopper/ 1 inductor [W]*	*Pout [W]*	*Pin [W]*
BOOST IL	0.02277	6.35	2.07	10.23	2474	2705
BRIDGELESS BOOST IL	4.578	11.64	2.412	10.58	2538	2730

V. CONCLUSION

In this paper, the topologies which are chosen to be investigated are: the boost interleaved PFC and the bridgeless boost interleaved PFC converters. In the last two decades, both topologies have been chosen for power application ranges up to 4 kW.

The paper deals with their design implementation of both hardware and control parts in Matlab/Simulink simulation environment and finally with their performances evaluation by comparison.

Simulation results, run for the same operation mode, show that the input current is in phase with the input voltage, and its shape is nearly perfectly sinusoidal, as expected, for both topologies, as shown in Fig. 5.

In the interleaved boost PFC topology, the input current is the sum of the two inductor currents. It can be noted from Fig. 9a, that for interleaved topology, the currents flowing through the two inductors are 180^{o} phase-shifted. Thus, the total input current has smaller ripple than in each individual inductor.

Comparing the two efficiency curves versus power for both topologies, depicted in Fig. 11, it results that for the bridgeless interleaved topology there is a slightly gain in efficiency.

So, in conclusion, interleaving and paralleling power converters can increase the efficiency of the power converter; as long as, the inductor ripple currents are kept within reason. The semiconductor switching losses will remain roughly the same, as it can be seen in Table II.

Further experimental results from the two prototypes studied in here will be presented in a next-future paper.

REFERENCES

[1] H.Z.Azazi, E. E. EL-Kholy, S.A.Mahmoud, S.S.Shokralla, "Review of Passive and Active Circuits for Power Factor Correction in Single Phase, Low Power AC-DC Converters", Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10), Cairo University, Egypt, December 19-21, 2010, Paper ID 154.

[2] H. Y. Kanaan, Al-Haddad, "A Comparative Study of Single-Phase Power Factor Correctors: Modeling, Steady-State Analysis, Tracking Ability and Design Criteria," International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2012, ISBN 978-1-4673-1301-8/12.

[3] C. Marxgut, J. Biela, J.W. Kolar, "Interleaved Triangular Current Mode (TCM) Resonant Transition, Single Phase PFC Rectifiers with High Efficiency and High Power Density," Proceedings of the 2010 IEEE International Power Electronics Conference, pp. 1725-1732.

[4] M. Bhuvaneswari, R.Suresh Kumar, "A High Efficiency Power Factor Correction Using Interleaved Boost Converter With Fuzzy Logic Control," International Journal of Engineering Science and Technology, vol. 5, no. 06S, Jun 2013.

[5] Fariborz Musavi, Wilson Eberle, William G. Dunford, "A High-Performance Single- Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers," IEEE Trans. On Industry Applications, vol. 47, no. 4, July/August 2011.

[6] A.P. Vyshakh., M.R. Unni, "BLIL PFC Boost Converter for Plug in Hybrid Electric Vehicle Battery Charger," International Journal of Scientific Engineering and Research (IJSER), Volume 2 Issue 1, January 2014.