AN FPGA-BASED SINGLE-PHASE INTERLEAVED BOOST-TYPE PFC CONVERTER EMPLOYING GAN HEMT DEVICES

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***Abstract* - The recent development of higher blocking voltage gallium nitride (GaN) power FETs has the potential to enhance the power density of future power electronic converters. In this work, GaN devices are used to assemble a 100 W single-phase two-channel interleaved boost-type power factor correction (PFC) converter. The constructed hardware is able to operate with a switching frequency up to 1 MHz per channel, and hence a 2 MHz effective ripple frequency at the input and output terminals of the interleaved system. Furthermore, in order to cope with the high frequency requirements an average current mode control strategy is implemented in an FPGA device. Finally, the experimental results shown attest the feasibility of the developed digital feedback control scheme and laboratory prototype.**

***Keywords* – Gallium nitride FETs, single-phase interleaved PFC rectifier, digital control, FPGA.**

I. INTRODUCTION

The progress of Power Electronics technology and the prospect of realizing very compact power converters lead to the use of new materials into power switching devices. In this context, gallium nitride (GaN) power FETs can provide significant power density benefits over their silicon counterparts. GaN based converters with efficiency over 99% have been reported [1] and comparison of devices have demonstrated that first generation GaN devices are better than the silicon (Si) state-of-the-art devices [2].

The use in Power Electronics of wide bandgap materials impacts not only the electrical performance of power converters but also changes the way converters are designed. This is clear from the switched currents and voltages slopes, which increase and allow for higher switching frequencies to be used. In short, the switching losses are dramatically reduced and the switching frequency can be higher than what is typical today. Increasing the switching frequency leads to important challenges in fields such as circuit layout, magnetic components design, electromagnetic compatibility (EMC), gate drivers and, very important, the control and modulation devices.

Today there is a wide field of applications that profit from digital processing devices to implement the supervision, control, protection, communication and pulse width modulation (PWM). Some of the most used devices being the digital signal processors (DSP) and controllers (DSC). However, such devices are dimensioned to typical power converter switching frequencies, which today range from 1 kHz up to 150 kHz. The most used DSPs and DSCs for Power Electronics would have a very difficult time when employed in very high switching frequency ($f_s \geq 200$ kHz) applications. Therefore, DSP based solutions will probably evolve to cope with higher switching frequency requirements. In the mean time programmable logic devices (CPLDs and FPGAs) appear as an alternative to the digital control of very high frequency PWM converters. Unfortunately, these typically present higher cost than DSPs/DSCs. Nevertheless, today these are perhaps the most fitted devices to implement all digital functions required by a power converter. This work discusses the use of an FPGA to implement the control, protection and modulation tasks of a GaN based power factor correction (PFC) rectifier in addition to a vision of the status of GaN technology in PFC applications.

The first part of this work presents a panorama of GaN devices and reviews their capabilities and main characteristics. A PFC rectifier topology featuring modular interleaved half-bridge converters (cf. Fig1) is chosen and discussed in Section III. The main challenges of implementing a current control strategy are discussed in Section IV along with the proposal for the implementation of an average current mode PFC control strategy for the chosen topology. Finally, experimental results illustrate the performance of the GaN based rectifier and conclusions are presented.

II. GALLIUM NITRIDE POWER FETS

Semiconductor devices based on silicon are quickly approaching their physical limitations. Wide bandgap semiconductor devices are being researched to allow further improvements in the field of Power Electronics with the new materials.

Gallium nitride is a wide bandgap semiconductor of the III-V nitride group. Wide bandgap semiconductors, such as GaN and silicon carbide (SiC), present many interesting properties

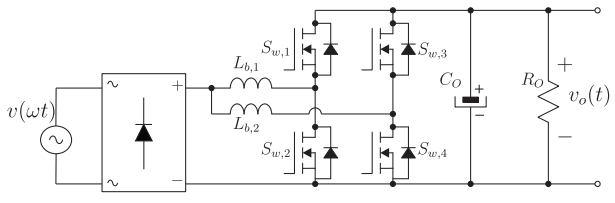

Fig. 1. : Single-phase two-channel interleaved PFC boost-type rectifier.

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that make them more attractive over the industry-established silicon. High breakdown voltages of 1.6 kV have been reported in AlGaN/GaN HEMTs in 2006 [3]. Operating temperatures in excess of 300 °C have been demonstrated since 1999 [4]. Very high switching frequencies and low on-state resistance can be obtained in GaN devices due to its high electron mobility.

With GaN it is possible to build High Electron Mobility Transistors (HEMT), which is used today by different GaN devices manufacturers as the basis for their transistors design. GaN HEMTs work by forming a two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction interface, which leads to very high conductivity between source and drain. The operation of GaN HEMTs is somewhat similar to MOSFETs, in that the conductivity is controllable by the gate-source voltage. AlGaN/GaN HEMTs on silicon substrates also incorporate an intrinsic internal body diode which presents no reverse recovery. On the other hand, it has a much higher forward conduction voltage drop compared to normal silicon FETs.

Initially, the research on GaN devices focused on depletion mode HEMTs. Enhanced mode devices were later developed due to the need for safer switches. Table I shows the results of some recent researches focused on PFC assembled with GaN devices. These reports have used research stage GaN devices of up to 600 V.

TABLE I: Research with GaN devices in PFC systems

Research Group	η	P_o	f_s	V_o	Mode	Year
Semicond. Co. [5]	94,2%	122 W	1 MHz	350 V	Depl.	2008
Transphorm Inc. [6]	97,8%	300 W	1 MHz	350 V	Depl.	2008
K.U. Leuven (ESAT-ELECTA) [7]	96%	106 W	512 kHz	142 V	Enhan.	2010
HRL Laboratories [8]	95%	425 W	1 MHz	351 V	Enhan.	2011
HRL Laboratories [9]	94%	1.2k W	1 MHz	300 V	Enhan.	2012

In fact, GaN devices are still in an early stage of large-scale production. Companies currently offering commercial GaN solutions include Efficient Power Conversion (EPC), Transphorm, HRL Laboratories, International Rectifier, and GaN Systems, among others. The commercially available devices are today limited to blocking voltages up to 200 V.

In the construction of static power switches, the widespread use of GaN substrates have been prohibitively high-priced. However, epitaxial process allows for volume deposition of GaN based material on low cost silicon wafers, costing about 100 times less than SiC. This makes GaN power devices a very attractive solution for the future of Power Electronics.

III. POWER CONVERTER

A PFC rectifier prototype was designed and built in order to evaluate the performance of commercially available GaN devices. The chosen topology is a single-phase two-channel interleaved boost converter [10–12]. As known from literature, [10], the channels should be preferably operated with 180^o (in general $\Delta\varphi = 360^o/n$) phase shift. The main power circuit is seen in Fig. 1, in which $S_{w,1-4}$ are HEMT GaN power FETs. The chosen topology allows one to investigate the synchronous rectification [13] features of the GaN devices. This is very important to reduce losses as the forward conduction voltage drop of the body diode in these devices is high. Therefore, a power converter can profit from the nonexistent reverse recovery of the body diode and still have low conduction losses by activating the device channel whenever the body diode should be conducting.

Another reason to choose this topology to evaluate the GaN devices is that the losses can be distributed through four devices instead of two in a single channel topology. According to losses and thermal computation based on the loss data presented in [14], this structure is able to deliver an output power of $P_o \cong 100$ W with a fully surface mount devices (SMD) assembly. The losses are computed considering the inductors high frequency ripple. The calculated current stress across the GaN devices are

$$I_{Sb,\text{rms}} \cong 0.763\,\text{A} \tag{1}$$
$$I_{Db,\text{rms}} \cong 0.492\,\text{A} \tag{2}$$
$$I_{Db,\text{avg}} \cong 0.625\,\text{A}. \tag{3}$$

This leads to the following conduction losses

$$P_{cond,\text{diode}} \cong 4.542\,\text{W} \tag{4}$$
$$P_{cond,\text{sync-rect}} \cong 59.77\,\text{mW}, \tag{5}$$

where $P_{cond,\text{diode}}$ is the total GaN devices conduction loss without synchronous rectification and $P_{cond,\text{sync-rect}}$ is the loss considering ideal synchronous rectification. From these results it becomes clear that the backward conduction in GaN HEMT devices is advantageous for a high efficiency design. The loss characteristic fitting parameters extracted from the device EPC2010 datasheet are: GaN HEMT conduction resistance at 100°C $R_{on} = 1.45 \cdot 25$ mΩ and the forward voltage drop of the body diode $V_f = 1.8$ V.

The switching losses are computed with the integration of a loss energy function w_{sw},

$$P_{sw} = \frac{1}{2\pi}\int_0^{2\pi} w_{sw}\, d\omega t, \tag{6}$$

where

$$w_{sw} = K_0 + K_1\, i_{sw} + K_2\, i_{sw}^2, \tag{7}$$

and i_{sw} is the value of the switched current, i.e. the local average value of the boost inductor current added with the high frequency ripple. The polynomial coefficients are computed from [14]: $K_0 = 1.8319\,\mu$J; $K_1 = 1.9227\,\mu$J/A; and, $K_2 = 24.5990$ nJ/A^2. The total switching losses P_{sw} for the GaN devices with the converter switching at $f_s = 250$ kHz is,

$$P_{sw} \cong 1.462\,\text{W}, \tag{8}$$

where the switching losses is mainly generated by the parallel capacitance of the devices.

Finally, the computed efficiency considering only the power semiconductors losses is

$$\eta_{GaN} \cong 98.1\% \text{ for } f_s = 250\text{ kHz}. \tag{9}$$

This is reduced to $\eta_{GaN} \cong 96.7\%$ for $f_s = 500$ kHz and $\eta_{GaN} \cong 94.1\%$ for $f_s = 1$ MHz. In case a four-channel interleaved PFC were used the new converter efficiency would

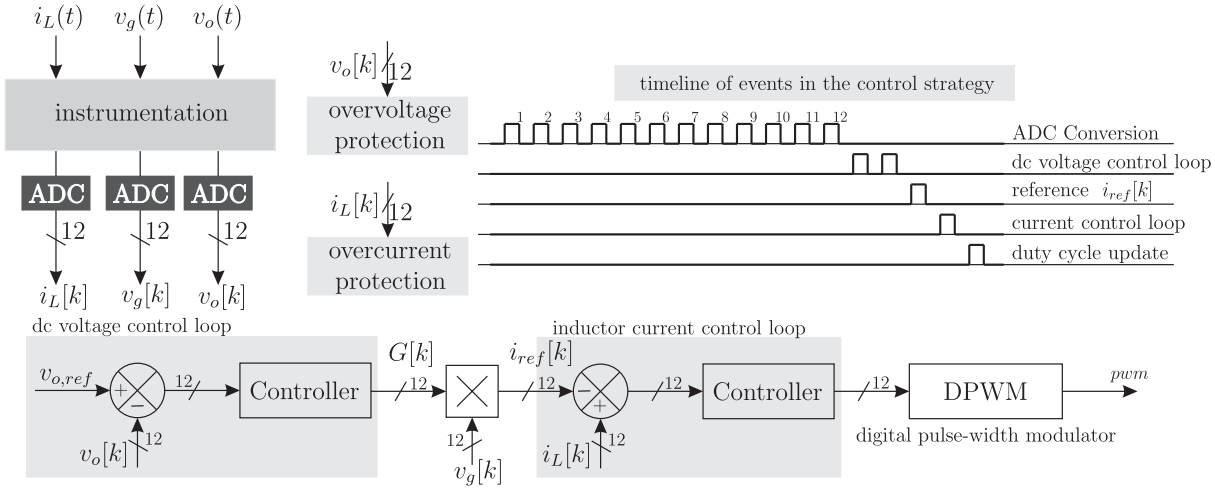


Fig. 2. : Feedback control strategy implemented in an FPGA.

be $\eta_{GaN} \cong 99.5\%$ for $f_s = 250$ kHz, $\eta_{GaN} \cong 98.9\%$ for $f_s = 500$ kHz, and $\eta_{GaN} \cong 97.9\%$ for $f_s = 1$ MHz.

In order to make a brief comparison, state-of-the-art Si MOSFET model FDP18N20F that presents approximate voltage and current ratings as the used GaN device would lead to a 5 to 10 times larger PCB area. The efficiency for a two-channel converter with Si MOSFETs technology is close to $\eta_{GaN} \cong 91,9\%$ for $f_s = 500$ kHz.

IV. CONTROL STRATEGY

As seen in Table I, the reported switching frequencies for PFC rectifier employing GaN devices are higher than 500 kHz. This illustrates the potential for such devices as it does show the need for high frequency control/modulation/protection auxiliary circuitry. The control circuits of choice today being analog integrated circuits (ICs) and DSPs, both of which do not have many options for switching frequencies above 500 kHz. Analog ICs are only recently being developed for use with GaN devices [15]. Thus, this work employs an FPGA based solution for the control and modulation functions of a GaN-based single-phase PFC rectifier.

The control strategy is the average current mode control, largely employed in PFC converters operating in continuous conduction mode (CCM) [16]. It is implemented in an FPGA device employing hardware description language (VHDL) with the development environment Quartus II Web Edition [17]. As shown in Figure 2, three sensed variables are needed to the control system, namely: the inductor current $i_L(t)$, the ac voltage $v_g(t)$ and the output dc voltage $v_o(t)$. The analog-to-digital conversion of these measured variables is performed with three Analog-to-Digital Converter (ADC) devices, IC AD 7276 – Analog Device, operating in parallel and independently. The interface employed between each ADC and FPGA was an SPI – *Serial Peripheral Interface* with a sampling frequency of 1 MHz and a 16 MHz clock signal.

Figure 2 shows the time diagram with the main events within the proposed control strategy. The state machine begins a counter which implements a sawtooth carrier of a digital pulse width modulator (DPWM). At the same instant a signal initializes the analog to digital conversion at each ADC. After one clock cycle, the ADC processed data is sent to the FPGA. After 12 clock cycles the measured input voltage, inductor current and output dc voltage are available to the PFC control processing. These data are transferred by the SPI interface. In the output dc voltage a Proportional-Integral (PI) controller is employed to guarantee good voltage regulation. On other hand, in the inductor current loop a Proportional (P) controller is implemented. The duty cycle is updated to the PWM modulator after all control laws are computed. As previously discussed, the inductor current $i_L(t)$ and the dc voltage $v_o(t)$ are sampled at every 1μs. Therefore, a moving average filter with 16 samples of these variables is used in the protection tripping logic in order to avoid untimely activation of the software system protection.

V. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed digital control strategy, which is well suited for high frequency Power Electronics converters, a laboratory prototype of the single-phase PFC system depicted in Fig. 3 has been built. The hardware implementation is shown in Fig. 4. The power stage of the prototype comprises an EMC input filter, a diode bridge, a two-channel interleaved GaN boost-type converter and a dc-link SMD capacitor bank. As commercial 600 V GaN turn-off devices are not readily available at the moment, the converter was assembled with reduced voltage specifications in order to be able to use the 200 V GaN devices from EPC.

The prototype specifications are listed in Table II. Even though, the ac voltage is reduced when compared to typical PFC applications, all control and supervision functionality of a PFC rectifier were implemented within an FPGA kit in a DE0-Nano Board. This FPGA development platform includes: an Altera Cyclone IV EP4CE22F17C6N FPGA; 153 FPGA pins to be used as digital logical input or output; an on-board USB-Blaster circuit for programming; a memory device with 32 MB SDRAM; and an on-board clock system with a 50 MHz clock oscillator.

The switching behavior of the GaN devices is shown in

TABLE II: Prototype specifications.

Specification	*Value*
Input voltage RMS value	40 V
Input voltage frequency	50 Hz
Output voltage dc value	80 V
Switching frequency range	250 and 500 kHz
Gan devices	EPC2010
GaN devices gate drivers	LM5113
GaN devices gate resistance	0 Ω
Inductance value (dc and no current)	100 μH
Dc capacitance value	1100 μF

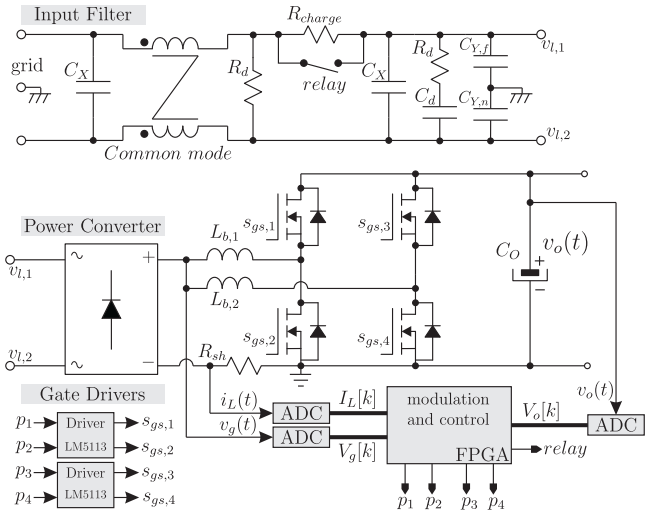


Fig. 3. : Schematics and feedback control scheme of a single-phase two-channel interleaved boost-type PFC rectifier.

Fig. 4. : Hardware implementation of fully digital high switching frequency single-phase interleaved boost-type PFC rectifier.

Fig. 5 when these devices are switched at 1000 kHz. Switching transitions of approximately 80 V occur in less than 5 ns leading to a dv/dt of more than 18 kV/μs during the turn on or turn off processes. Such times make it clear that the devices can be operated at very high switching frequency. The experimental results are performed with the prototype operating as a dc-dc boost interleaved converter with an output dc voltage V_{dc}=80 V; dead-time t_d= 10 ns, switching frequency f_s= 1 MHz, and an output power of P_o= 50 W.

The prototype was supplied from a programmable ac power supply of Agilent Technologies model 6813B *AC Power Source – Analyzer*, and the main external waveforms are shown in Fig. 6. The control effectiveness is observed as the input ac current closely follows the sinusoidal input voltage even with a relatively low modulation index.

The switching frequency of the converter was varied in order to verify the influence of this parameter on the temperature of the GaN devices. Two switching frequencies were tested: 250 kHz and 500 kHz. The thermal results are presented in Fig. 7, where the infrared image shows the temperature at the main power components for the 250 kHz operation. There, the output power was set to $P_o = 75$ W and the maximum measured temperature at the GaN devices surface was 90.3°C. At $f_s = 500$ kHz the output power was also set to $P_o = 75$ W

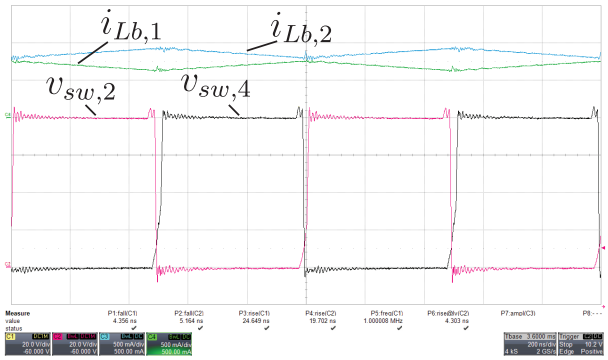


Fig. 5. : Experimental results showing the switching transitions of the EPC2010 GaN HEMTs with a switching frequency per leg of f_s= 1000 kHz.

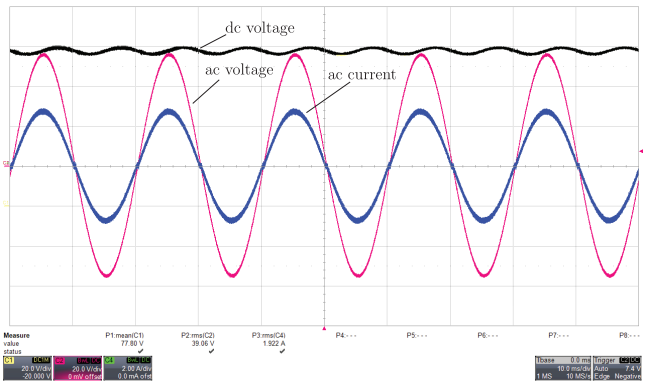
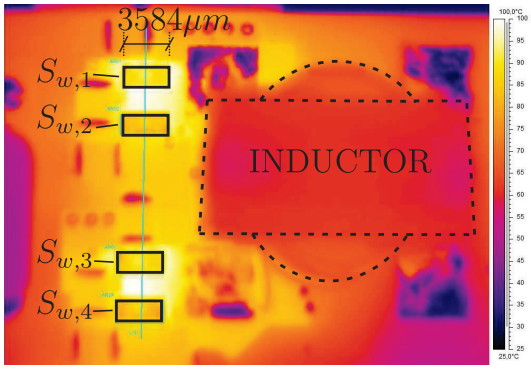


Fig. 6. : Experimental results of the assembled PFC rectifier at $P_o = 75$ W. Ac voltage [20 V/div.], input current [2 A/div.] and dc voltage [20 V/div.].



	$250k\ Hz$	$500k\ Hz$
$S_{w,1}$	90.3^o	92.6^o
$S_{w,2}$	85.1^o	86.6^o
$S_{w,3}$	88.6^o	90.6^o
$S_{w,4}$	84.2^o	85.0^o

Fig. 7. : Experimental thermal measurements regarding the GaN HEMT devices and the boost inductor for the PFC rectifier operation with two switching frequencies of a partial interleaved subcircuit of 250 kHz and 500 kHz (and hence a 500 kHz and 1 MHz effective switching frequency, respectively). It is important to notice that no external cooling mechanism was used.

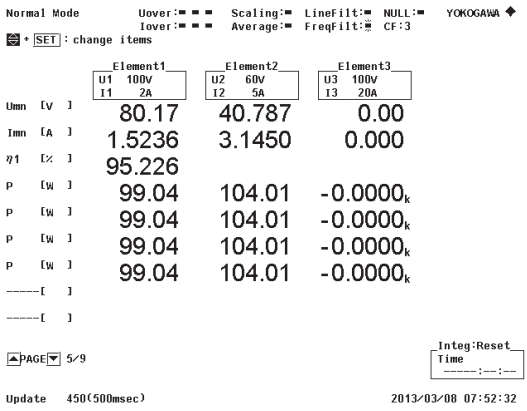


Fig. 8. : Measured efficiency of the prototype operating with partial interleaved subcircuit switching frequency of f_s = 250 kHz.

and the maximum measured temperature was 92.6°C. In Fig. 8 the efficiency of the prototype operating at $P_o \cong 75$ W with $f_s = 250$ kHz was measured with a Yokogawa power analyzer leading to $\eta \cong 95.23\%$. This measurement includes the losses of the semiconductor and passive devices including the EMI filter components and the dc-link capacitors.

The harmonic spectrum of the filtered phase ac current measured at the input of the built prototype operating with f_s=250 kHz (per device) and consequently f_s=500 kHz effective ripple frequency is shown in Fig. 9.

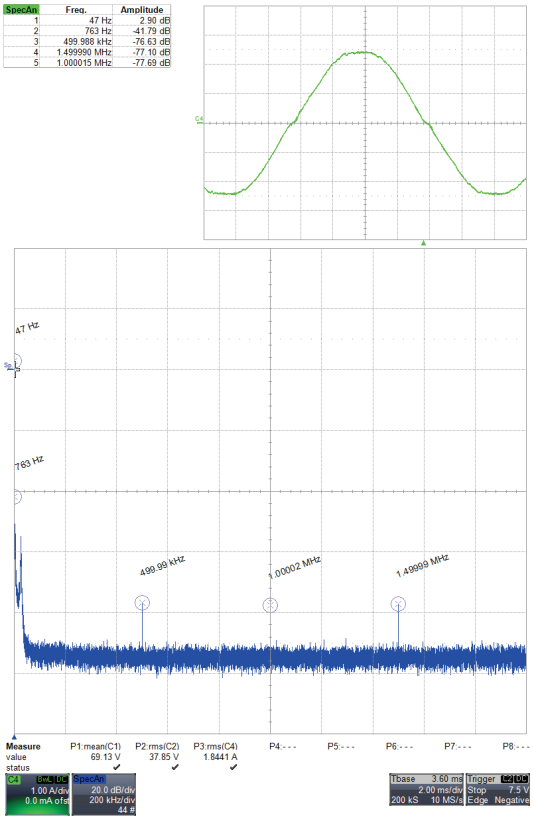


Fig. 9. : Measured spectrum harmonics of the current in an interleaved bridge-leg for operation with effective switching frequency of 500 kHz (250 kHz per power device). In this test the PFC rectifier was fed by an auto-transformer connected to a 220 V/60 Hz power mains to avoid the switching noise of the ac power supply.

VI. CONCLUSIONS

Wide bandgap semiconductor materials impacts Power Electronics converters due to improved electrical performance regarding voltage drops and switching transition times. In addition, such materials are changing the way power converters are designed. In this work, a discussion on the status of GaN power devices for PFC rectification applications was presented to introduce the requirements regarding the switching frequency. A brief comparison was carried out at 500 kHz switching frequency showing that PCB area, losses and cooling can be highly improved with GaN devices. The feasibility of very high switching frequencies was identified and the challenges faced by today's most deployed control/modulation solutions, i.e. analog ICs and DSPs, were highlighted. In this context, a very high switching frequency digital control/modulation platform was developed to allow the implementation of a 1 MHz GaN HEMTs-based single-phase two-channel interleaved boost-type PFC rectifier. This was done based on an FPGA. The choice of an FPGA device was made based on the very high switching frequency and the advantages of a digital control implementation. However, as analog ICs and DSPs become appropriate for such frequencies the use of an FPGA will depend on how prices evolve. Because of the use of two converter channels, the turn-off one of them at light load oper-

ation is possible, reducing gate driver and magnetic core losses or a very high efficiency can be attained even at light loads. Experimental results have attested the feasibility of this solution and shown the potential for high efficiency designs even at relatively low converter rated power.

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REFERENCES

[1] T. Morita, S. Tamura, Y. Anda, M. Ishida, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "99.3% efficiency of three-phase inverter for motor drive using gan-based gate injection transistors," in *Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 481–484, 2011.

[2] D. Costinett, H. Nguyen, R. Zane, and D. Maksimovic, "Gan-fet based dual active bridge dc-dc converter," in *Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition, APEC*, pp. 1425–1432, 2011.

[3] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. Khan, "The 1.6-kv algan/gan hfets," *IEEE Electron Device Letters*, vol. 27, no. 9, pp. 716–718, 2006.

[4] S. Pearton, J. Zolper, R. Shul, and F. Ren, "Gan: Processing, defects, and devices," *Journal of Applied Physics*, vol. 86, no. 1, pp. 1–78, 1999.

[5] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "A 120-w boost converter operation using a high-voltage gan-hemt," *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 8–10, 2008.

[6] Y. Wu, M. Jacob-Mitos, M. Moore, and S. Heikman, "A 97.8% efficient gan hemt boost converter with 300-w output power at 1 mhz," *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 824–826, 2008.

[7] J. Everts, J. Das, J. Van dan Keybus, M. Germain, and J. Driesen, "Gan-based power transistors for future power electronic converters," in *Proceedings Young Researchers Symposium on Smart Sustainable Power Delivery*, 2010.

[8] B. Hughes, Y. Yoon, D. Zehnder, and K. Boutros, "A 95% efficient normally-off gan-on-si hemt hybridic boost-converter with 425-w output power at 1 mhz," in *Compound Semiconductor Integrated Circuit Symposium, CSICS*, pp. 1–3, IEEE, 2011.

[9] B. Hughes, J. Lazar, S. Hulsey, D. Zehnder, D. Matic, and K. Boutros, "Gan hfet switching characteristics at 350v/20a and synchronous boost converter performance at 1mhz," in *Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition, APEC*, pp. 2506–2508, IEEE, 2012.

[10] B. A. Miwa, D. Otten, and M. Schlecht, "High efficiency power factor correction using interleaving techniques," in *Conference Proceedings Seventh Annual Applied Power Electronics Conference and Exposition APEC '92*, pp. 557–568, 1992.

[11] L. Balogh and R. Redl, "Power-factor correction with interleaved boost converters in continuous-inductor-current mode," in *Conference Proceedings of Eighth Annual Applied Power Electronics Conference and Exposition, APEC '93.*, pp. 168–174, 1993.

[12] P.-W. Lee, Y. S. Lee, D.-W. Cheng, and X.-C. Liu, "Steady-state analysis of an interleaved boost converter with coupled inductors," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 4, pp. 787–795, 2000.

[13] M. Scott, K. Zou, and J. Wang, "A gallium-nitride switched-capacitor circuit using synchronous rectification," *IEEE Transactions on Industry Applications*, vol. PP, no. 99, pp. 1–1, 2013.

[14] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," in *Energy Conversion Congress and Exposition, ECCE*, pp. 2681–2688, 2011.

[15] S. Bandyopadhyay, B. Neidorff, D. Freeman, and A. Chandrakasan, "90.6% efficient 11mhz 22w led driver using gan fets and burst-mode controller with 0.96 power factor," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers, ISSCC*, pp. 368–369, 2013.

[16] P. C. Todd, "UC3854 controlled power factor correction circuit design," in *Unitrode Product and Applications Handbook*, pp. 10.303–10.322, 1995–1996.

[17] T. Jappe, S. Mussa, and R. Rosendo, "Synchronous state machine inner FPGA controlling PFC boost converter," in *IEEE International Symposium on Industrial Electronics (ISIE)*, pp. 1097–1102, 2010.

[18] Terasic Technologies, http://www.terasic.com.tw, *DE0-Nano User Manual*, v1.7 ed., 2012.

[19] M. Kasper, D. Bortis, T. Friedli, and J. Kolar, "Classification and comparative evaluation of PV panel integrated DC-DC converter concepts," in *15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, pp. 4–8, 2012.

[20] J. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics," in *7th International Conference on Integrated Power Electronics Systems (CIPS)*, pp. 1–22, 2012.

[21] F. Musavi, W. Eberle, and W. Dunford, "A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers," *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1833–1843, 2011.