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An improved soft switched PWM interleaved boost AC–DC converter

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ABSTRACT

In this paper, an improved soft switched two cell interleaved boost AC/DC converter with high power factor is proposed and investigated. A new auxiliary circuit is designed and added to two cell interleaved boost converter to reduce the switching losses. The proposed auxiliary circuit is implemented using only one auxiliary switch and a minimum number of passive components without an important increase in the cost and complexity of the converter. The main advantage of this auxiliary circuit is that it not only provides zero-voltage-transition (ZVT) for the main switches but also provides soft switching for the auxiliary switch and diodes. Though all semiconductor devices operate under soft switching, they do not have any additional voltage and current stresses. The proposed converter operates successfully in soft switching operation mode for a wide range of input voltage level and the load. In addition, it has advantages such as fewer structure complications, lower cost and ease of control. In the study, the transition modes for describing the behavior of the proposed converter in one switching period are described. A prototype with 600 W output power, 50 kHz/cell switching frequency, input line voltage of 110–220 V_{rms} and an output voltage of 400 V_{dc} has been implemented. Analysis, design and the control circuitry are also presented in the paper.

1. Introduction

The conventional method of reducing input current harmonics using passive filters is no longer practically sufficient to meet the requirements in many applications. Several active power factor correction (PFC) techniques have been developed to satisfy international standards such as EN-61000-3-2. The PFC technique reduces current harmonics in utility systems produced by nonlinear loads. Among the different alternatives, the boost converter operating in continuous conduction mode (CCM) has been widely adopted as a front-end PFC preregulator [1,2]. The favorable features of boost converter are: simple topology, high power density, fast transient response and continuous input current. Therefore, boost converters are usually used in different power electronics applications such as active PFC, photovoltaic power systems and fuel cells [3–6].

In high power applications, interleaved operation (the parallel connection of switching converters) of two or more boost converters has been proposed to increase the output power and to reduce the output ripple [7–9]. This technique consists of a phase shifting of the control signals of several cells in parallel operating at the same switching frequency. As a result, the input and output current waveforms exhibit lower ripple amplitude and smaller harmonics content than in synchronous operation modes. The resulting cancellation of low-frequency harmonics allows the reduction of size and losses of the filtering stages. Moreover, a converter employing the interleaving strategy can feature a great power density without the penalty of reduced power-conversion efficiency. However, current sharing among the parallel paths in continuous inductor current and at average current control is a major design problem because of the mismatch in duty cycle [9].

Higher power density and faster transient response can be achieved by increasing switching frequency. Higher switching frequency causes increase in switching losses and a serious electromagnetic interference (EMI) problem in hard switched PWM converters. The switching losses of the boost switches make a significant amount of power dissipation. Therefore, the switching losses of the converter should be minimized to increase the efficiency and power density by using soft switching techniques. These techniques are implemented by passive or active snubber circuits.

Various kinds of soft switching techniques have been proposed in the literature to minimize switching losses of the boost converters. Converters operating at soft switching with passive snubbers are attractive, since there is no need for extra active switches and also the control scheme is simpler. The main problem with these kinds of converters is that the voltage stresses on the power switches are too high and the converter is bulky. The study presented in [10] is an example for this type application in which the active power switches of the converter are turned on at zero voltage switching by which the switching losses are reduced. The

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auxiliary inductor used in this circuit is very big (nearly half of the main inductors) and this results in a bulky circuit. Active auxiliary snubbers are also developed to reduce switching losses of boost and interleaved boost converters without having the disadvantages of passive auxiliary circuits. These active snubbers have additional gate circuits for the auxiliary switches to generate their gate pulses and to synchronize them with the main switch. In the soft switching boost converter proposed in [11], the main switch operates in zero voltage switching (ZVS) but the auxiliary diodes are under hard switching condition and the reverse recovery of the auxiliary diodes causes parasitic oscillations and increases the voltage stresses. The most preferred scheme used for boost converters is given in [12]. This scheme provides zero voltage switching condition for the main switch without increasing the voltage stress of the main and auxiliary switches. However, the disadvantage of this converter is that the auxiliary switch operates under hard switching condition and this increases the EMI noise level and decreases the efficiency of the converter.

Though, there are many studies in which active auxiliary cells are implemented for conventional boost DC–DC converters [13,14], the number of papers applying active auxiliary circuit to the interleaved boost topology is very low in the literature. Recently, there have been published some studies about interleaved boost converter including active auxiliary circuit [15,16]. In [15], the main switches operate under zero current switching (ZCS) and the auxiliary switches operate under ZVS during the whole switching transition. However, since the converter given in [15] operates at critical conduction mode, higher current rating switches should be selected to be used in the circuit. The soft switching operation in the two cell interleaved boost converter presented in [16] is achieved based on using auxiliary circuit including two switches. In this circuit, the main switches operate under ZCS at turn on transition and under ZVS at turn off transition. The added auxiliary switches also operate at ZVT during the whole switching transition. However, the main disadvantage of this converter is using two auxiliary switches that increase the cost and the complication of the control circuit.

The review of literature shows that the ZVT technique provides basically a perfect turn on process for the main switches of a converter by using a quasi resonant active circuit. No overlap between the voltage and the current of the main switches and so no switching losses take place at turn on process. Unfortunately, the turn off process of a ZVT converter is not perfect. Since the turn off loss of MOSFETs is very low compared to the turn on loss, using MOSFETs in a converter with ZVT auxiliary circuit is more suitable. In addition, the cost and losses of an active auxiliary circuit are important subjects that must be taken into account during designing of the converter. The auxiliary circuits which are used for soft switching should not increase the size or cost of the converter considerably.

In this study, an improved ZVT interleaved boost PFC topology (Fig. 1) is introduced. The proposed ZVT interleaved boost converter is composed of two cell boost conversion units and an active auxiliary circuit.

The proposed auxiliary circuit is implemented using only one auxiliary switch and a minimum number of passive components without an important increase in the cost and complexity of the converter. The main advantage of the proposed converter with respect to previously published soft switching interleaved boost converters is that it not only provides ZVT in the main switches but also provides soft switching in the auxiliary switch and diodes. The semiconductor devices used in the converter (main and auxiliary) do not have any additional voltage and current stresses. In addition, using only one switch in the auxiliary circuit is another advantage of this topology compared to the previously published soft switching interleaved boost converters. The operating modes of the proposed converter are analyzed in detail and the results of which are verified with the simulation and experimental studies carried out on a prototype rated at 600 W and 50 kHz/cell interleaved boost converter. The simulation and experimental results are in a satisfactory agreement and verify the theoretical analysis results.

2. Analysis of operation

In the analysis of the proposed converter; the output filter capacitor is assumed as a constant voltage source V_o during a switching period. In addition, since the inductor of each cell is large enough and the switching frequency, f_s is very high compared to the line frequency, f, the current of each inductor can be taken constant during a switching period. The voltage, V_g is the rectified input voltage and is defined with Eq. (1). Since the input voltage is sinusoidal, the duty cycle ratio, d is not constant. The variation of the duty cycle for PFC circuits is expressed with Eq. (2) and can be represented as given in Fig. 2 for an input line voltage of 220 V_{rms}, 50 Hz line frequency and an output voltage 400 V_{dc}.

$$V_g(t) = |V_m \cdot \sin(2 \cdot \pi \cdot f)| \tag{1}$$

$$d = 1 - \frac{V_g}{V_o} = 1 - \frac{|V_m \cdot \sin(2 \cdot \pi \cdot f)|}{V_o} \tag{2}$$

where, V_m is maximum value of the input voltage.

It is shown from Eq. (2) and Fig. 2 that the duty ratio is not constant and varies in time for PFC circuits. For duty cycle value less and greater than 0.5 there are two different conditions for the proposed topology. To simplify the analysis, L_1 and L_2 are replaced with current source and the capacitor C_o is replaced by voltage source as shown in Fig. 3.

In this section, the operating modes of the proposed circuit are analyzed. The main switches of the converter, M_1 and M_2 are gated with 180° phase shift with identical frequencies and duty ratios. The auxiliary switch, M_a is gated with constant duty ratio just be-

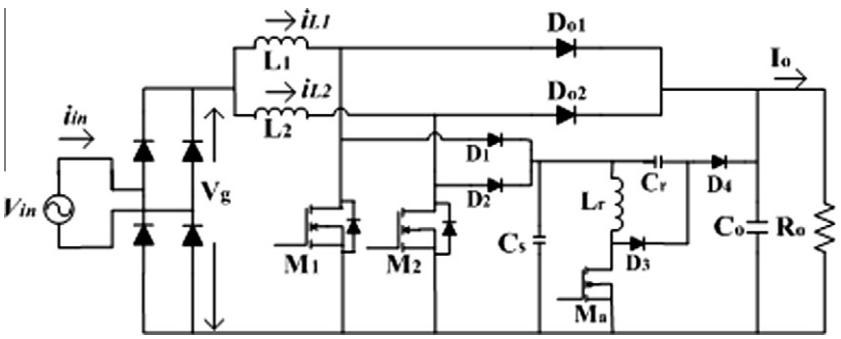

Fig. 1. The proposed ZVT two cell interleaved boost PFC converter.

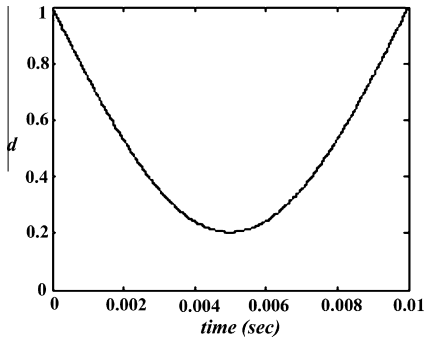

Fig. 2. Variation of the duty cycle (d) for PFC circuits.

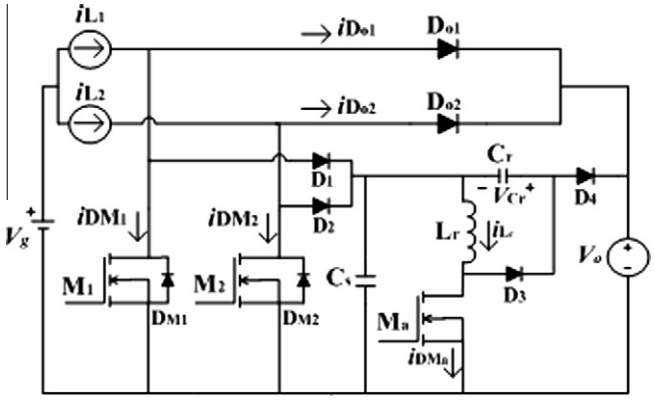

Fig. 3. Simplified circuit diagram of the proposed topology.

fore the main switches. Analyzing the operation of the converter shows that there are 16 modes during one period of operation for $d > 0.5$ and for $d < 0.5$. Since the cells of the proposed converter are identical with the same operating frequency and duty ratios and their main switches are operating with phase shift of 180°, the 16 operating modes of the converter can be divided into two similar groups. The first eight operating modes are similar to the next eight operating modes of the converter. The differences between these two groups of operating modes are in the main switches and output diodes. The second eight modes are obtained by replacing M_2 with M_1 and D_{o2} with D_{o1} in the first eight modes. Therefore, to simplify the analysis of the converter operation the equivalent circuits of the first eight modes of the proposed converter are given. The theoretical waveforms of the proposed topology for $d > 0.5$ and $d < 0.5$ are illustrated in Fig. 4. The equivalent circuits of the topology for $d > 0.5$ are also discussed and given in Fig. 5.

Mode-1; ($t_0 < t < t_1$) (Fig. 5a). Initially, the main switch, M_1 and the auxiliary switch, M_a are in off state and the output diode of the first stage is in on state. The switch M_a is turned on at t_0. The resonant inductor (L_r) current starts to rise through the path of V_g–L_1–L_r–M_a–V_g. Since the rise rate of this current is limited by the auxiliary inductor, L_r, the auxiliary switch, M_a is turned on under soft switching. During this mode, the current of M_a rises and the current of D_{o1} falls simultaneously and linearly. Therefore, the reverse recovery loss of D_{o1} is greatly reduced. Since the voltage across the C_s is equal to the output voltage, V_o in this mode, the time interval and the current of L_r can be expressed as;

$$i_{L_r}(t) = \frac{V_{C_s}}{L_r} \cdot (t_1 - t_0) = \frac{V_o}{L_r} \cdot (t - t_0) \tag{3}$$

$$V_{C_r}(t) = 0 \tag{4}$$

$$(t_1 - t_0) = \Delta t_1 = \frac{i_{L_1} \cdot L_r}{V_o} \tag{5}$$

$$i_{D_{o1}}(t) = i_{L_1} - i_{L_r} \tag{6}$$

Mode-2; ($t_1 < t < t_2$) (Fig. 5b). At $t = t_1$, the current of D_{o1} falls to zero. The snubber capacitor, C_s begins to discharge and current of auxiliary inductor, L_r increases because of the resonance between L_r and C_s. C_s discharges until its voltage reaches zero at t_2. The time intervals corresponding to this operation mode, the current of L_r and the voltage across C_s can be written as;

$$i_{L_r}(t) = i_{L_1} + \frac{V_o}{Z_1} \cdot \sin w_1(t - t_1) \tag{7}$$

$$V_{C_s}(t) = V_o \cdot \cos w_1(t - t_1) \tag{8}$$

$$(t_2 - t_1) = \Delta t_2 = \frac{\pi}{2} \cdot \sqrt{L_r \cdot C_s} \tag{9}$$

where $\omega_1 = 1/\sqrt{L_r \cdot C_s}$ and $Z_1 = \sqrt{L_r/C_s}$.

Mode-3; ($t_2 < t < t_3$) (Fig. 5c). Prior to $t = t_2$, M_1 and D_{o1} are in off state, M_2 and the auxiliary switch, M_a are in on state. M_a conducts the current i_{Lr} through the body diodes of the main switches. At t_2 snubber capacitor C_s is fully discharged and the current of L_r reaches its maximum value. It should be noted that the capacitor, C_s includes the parasitic capacitors of the main switches, the parasitic capacitors of the output diodes and the auxiliary diodes. So, the C_s can be assumed to be equal to sum of snubber capacitor and the parasitic capacitors. In this interval, i_{Lr} flows in L_r–M_a and body diodes of the main switches. Maximum i_{Lr} can be expressed as;

$$i_{L_r}(t) = i_{L_{r\max}} = i_{L_1} + V_o/Z_1 \tag{10}$$

$$V_{C_r}(t) = 0 \tag{11}$$

In this interval, the main switch should be turned onto satisfy the ZVT condition. It can be assumed that the average inductor current of L_1 is the half of the input current at steady state. The time delay for M_1, t_d can be expressed as;

$$t_d = \Delta t_1 + \Delta t_2 = \frac{i_{L_1} \cdot L_r}{V_o} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot C_s} = \frac{i_{in} \cdot L_r}{2 \cdot V_o} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot C_s} \tag{12}$$

It is shown from Eq. (12) the worst case occurs at maximum input current. Since the input and output voltages of converters are known or defined initially, the auxiliary circuit parameters values must be chosen according to the input current value. In other words, the worst case is determined according to the converter power rating.

Mode-4; ($t_3 < t < t_4$) (Fig. 5d). Prior to t_3, the auxiliary switch, M_a conducts the i_{Lr} and the main switch, M_1 conducts a small current value on its body diode, D_{M1}. At t_3, the auxiliary switch is turned off and M_1 is turned on at the same time. In this interval, the main switches, M_1 and M_2 conduct the input current together. Auxiliary capacitor, C_r begins to charge up and the current of L_r begins to fall until the end of this mode. The capacitor, C_r limits the rate of rise of voltage across M_a in this operation mode. Thus, the turning off of M_a occurs at ZVS condition. A resonance operation starts through L_r–D_3–C_r and the energy stored in the auxiliary inductor, L_r begins to transfer to the auxiliary capacitor, C_r. The auxiliary diode, D_3 begins to conduct in ZVS condition at t_3. For this period of operation, the following equations are derived;

$$i_{L_r}(t) = i_{D_3} = i_{L_{r\max}} \cdot \cos \omega_2(t - t_3) \tag{13}$$

$$V_{C_r}(t) = i_{L_{r\max}} \cdot Z_2 \cdot \sin w_2(t - t_3) \tag{14}$$

where $\omega_2 = 1/\sqrt{L_r \cdot C_r}$ and $Z_2 = \sqrt{L_r/C_r}$

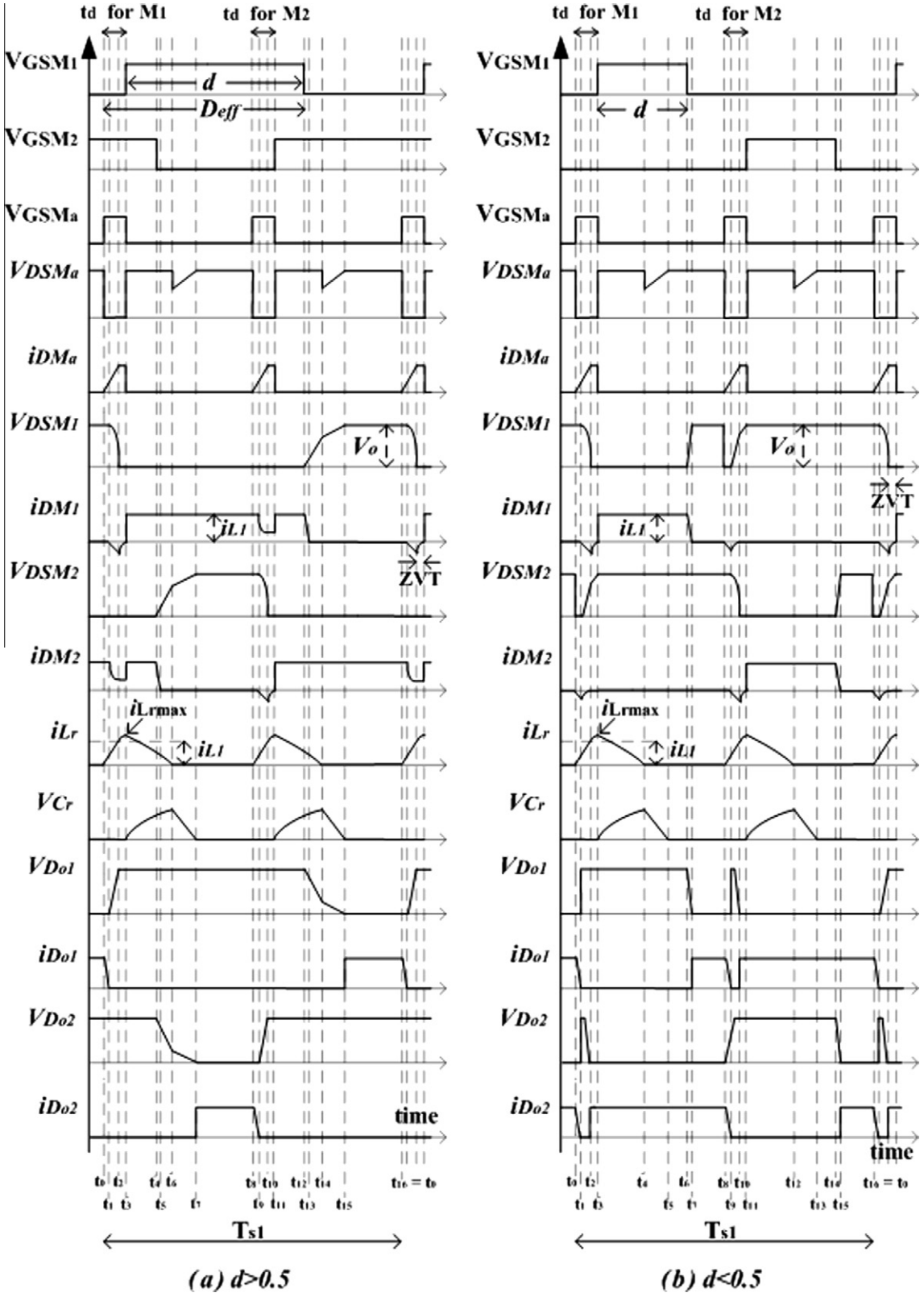

Fig. 4. Theoretical waveforms of the proposed topology (for $d > 0.5$ and $d < 0.5$).

Mode-5; ($t_4 < t < t_5$) (Fig. 5e). This mode starts with turning off of the main switch, M_2. The snubber capacitor, C_s starts to charge. The energy transfer from L_r to C_r continues in this operation mode and the voltage across the M_a reaches the output voltage at the end of this mode. Since the C_r restricts the rate of rise of the voltage across the switch, M_2, M_2 is turned off under near ZVS operation.

Mode-6; ($t_5 < t < t_6$) (Fig. 5f). At t_5, the current of M_2 falls to zero and voltage across the auxiliary switch, M_a reaches output voltage,

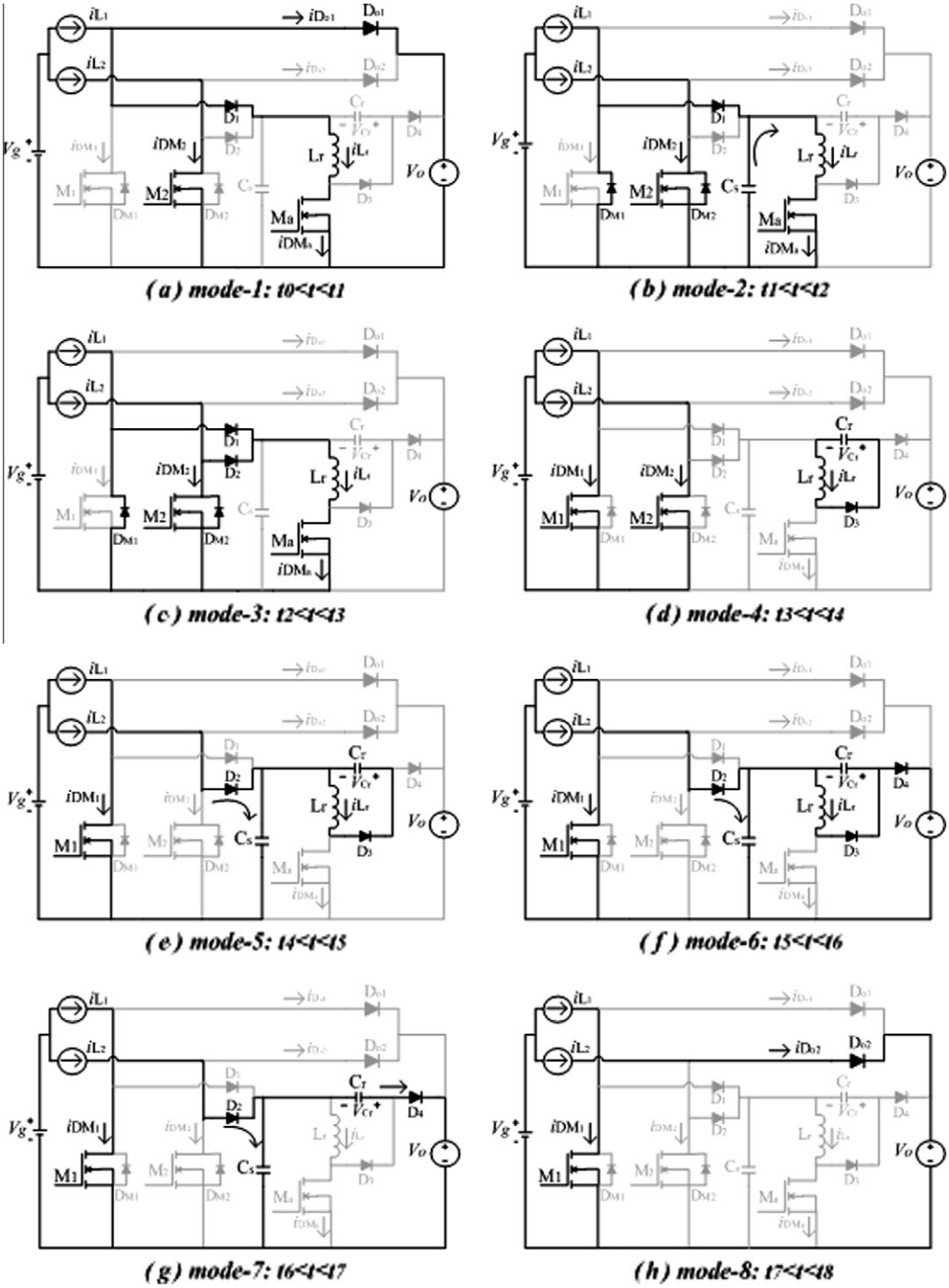

Fig. 5. Equivalent circuits corresponding to different operating modes (for $d > 0.5$).

V_o. The auxiliary capacitor begins to discharge through auxiliary diode, D_4 and the current of L_r starts to flow to the output. At the end of this operation mode, i_{Lr} falls to zero. Since the voltage on the auxiliary capacitor, C_r is not fully discharged, the snubber capacitor, C_s continues to charging.

Mode-7; ($t_6 < t < t_7$) (Fig. 5g). At t_6, the current of L_r is zero. In this operating mode, only the main switch, M_1 is conducting. While the auxiliary capacitor, C_r is discharging, the snubber capacitor, C_s continues to charging up to output voltage. At the end of this mode, the voltage across the C_r falls to zero and the voltage across C_s reaches the output voltage level, V_o. The auxiliary diode, D_4 turns off without reverse recovery loss. The voltage across the snubber capacitor, V_{Cs} during the operating modes of 5, 6 and 7 can be expressed as;

$$V_{C_s}(t) = V_o - V_{C_r} \tag{15}$$

Mode-8; ($t_7 < t < t_8$) (Fig. 5h). When the voltage across the C_r capacitor falls to zero at t_7, the output diode, D_{o2} starts to conduct. During this mode of operation, while the output diode, D_{o2} is conducting the current of second cell of the converter (i_{L2}), the current of first cell (i_{L1}) flows through the main switch, M_1. This mode ends by applying a gate signal to turn on the auxiliary switch, M_a for the

second cell. During this mode of operation the input current which is shared between the main switch, M_1 and the output diode, D_{o2} can be written as;

$$i_{in} = i_{L_1} + i_{L_2} = i_{D_{M1}} + i_{D_{o2}} \tag{16}$$

Mode-9–16; since two cells of the converter are identical and operating with the same frequency and duty cycles and there is only 180° phase shift between these two cells, the circuit behavior during operation modes of 9–16 is similar to that of during modes of 1–8. The circuit analysis of the converter during the last eight modes is similar to that of the first eight modes and can be achieved by replacing M_2, D_{o2}, and D_{M2} with M_1, D_{o1}, and D_{M1}, respectively.

3. Design procedure

The design procedure for the proposed ZVT interleaved boost AC/DC converter operating in continuous conduction mode (CCM) is presented in this section. The design specifications are as:

Output power P_o = 600 W
Output voltage V_o = 400 V
Input voltage V_{in} = 110–220 V_{rms}
Input frequency f = 50 Hz
Switching frequency f_s = 50 kHz/cell

The design procedure is explained in the following steps.

3.1. Considerations on relationship of duty cycle with output/input

The relationship between the duty cycle and the output/input ratio for conventional interleaved boost converter are derived in [17]. In the proposed ZVT interleaved boost converter, the duration of the gate signal applied to the gate of the main switches is less than that for conventional converter. This is due to a delay exists only at the starting of this signal. The signal duration applied to the gate of the auxiliary switch is equal to this delay. Therefore, as shown in Fig. 4 the effective duty cycle, D_{eff} is equal to the duty cycle of the conventional converter. The voltage across L_1 is $(V_g - V_o)$ for $(1 - D_{eff})Ts$ by ignoring the tiny period of modes 1 and 2. Applying the voltage–second balance principle on inductor L_1, we can obtain Eq. (17) as;

$$V_o = \frac{1}{1 - D_{eff}} \cdot V_g = \frac{1}{1 - D_{eff}} \cdot |V_m \cdot \sin(2 \cdot \pi \cdot f)| \tag{17}$$

The relationship between the input and output current of the converter in terms of efficiency (η) and duty cycle is given as follows;

$$I_o = \eta(1 - D_{eff}) i_{in} \tag{18}$$

3.2. Considerations on relationship of delay time and components of the auxiliary circuit

The key point of this study is to determine the delay time and passive components values of the auxiliary circuit to operate the proposed converter with soft switching successfully at very wide load ranges and at considerably high frequencies. The mathematical analysis of the circuit determines the necessary conditions to obtain the delay time and the passive components values. As seen from Eq. (12), the passive components of the auxiliary circuit are related to delay time t_d, output voltage V_o and input current i_{in}. The delay time required for proper ZVT operation can be determined from Eq. (19) derived from rearranging of Eq. (12).

$$t_d \geqslant \frac{i_{in} \cdot L_r}{2 \cdot V_o} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot C_s} \tag{19}$$

It is seen form Eq. (19) that t_d depends on V_o, i_{in}, L_r and C_s. Since the output/input parameters of the converter affect the delay time and passive components values, firstly the value of output voltage and output maximum power of the converter should be specified to determine the worst case condition. From Eq. (19), the worst case occurs at the lowest output voltage and maximum input current. For the same output power, the converter draws the maximum input current when the input voltage is at the lowest value. Therefore, for the proposed converter, the worst case occurs at 110 V_{rms} input voltage. The second important consideration is based on choosing the passive components values of the auxiliary circuit. These components should be chosen according to the desired delay time which is suitable as 5–10% of the switching period. Since the inductor value affects the converter volume more than that of the capacitors, selecting small value inductor for L_r is more suitable to obtain small volume converter. Eq. (19) shows that the capacitance value of C_r does not affect the delay time. The value of C_r determines the time period of energy transferring from the auxiliary circuit to the output and it should be determined using Eqs. (13) and (14). For the same load, the time interval required to transfer energy increases with increasing the value of C_r.

3.3. Considerations on input current ripple

Under CCM operation, the values of L_1 and L_2 affect the input current ripple amplitude. Since an active type of auxiliary circuit is used in the proposed converter, the values of the main inductors do not dominate the ZVT operation of the converter. The current ripples, ΔI_L of the inductor of each boost cell can be denoted as;

$$\Delta I_L = \frac{D_{eff} \cdot T_s}{L} \cdot V_g = \frac{D_{eff} \cdot T_s}{L} \cdot |V_m \cdot \sin(2 \cdot \pi \cdot f)| \tag{20}$$

The input current of the interleaved converter is sum of the currents of the inductors. Since the inductor currents are shifted with a 180° phase shift, the magnitude of the input current ripple is less than the sum of current ripples of main inductors.

$$\Delta I_{in} = \frac{|2D_{eff} - 1| \cdot T_s}{L} \cdot V_g = \frac{|2D_{eff} - 1| \cdot T_s}{L} \cdot |V_m \cdot \sin(2 \cdot \pi \cdot f)| \tag{21}$$

Using Eqs. (20) and (21), the values of main inductors (L_1 and L_2) can be obtained for the certain requirement of input current ripple.

3.4. Considerations on output voltage ripple

Since the load and output capacitor are supplied through two diodes D_{o1} and D_{o2}, the frequency of the output ripple current is twice the switching frequency. This decreases the output ripple voltage ΔV_o. For ideal output capacitor the output voltage ripple can be determined as;

$$\Delta V_o = \frac{V_o \cdot D_{eff}^2 \cdot T_s}{2 \cdot R_o \cdot C_o} \tag{22}$$

3.5. Control strategy

In this paper, the average current mode is used as the control reference. The scheme of the controller and the power stage is shown in Fig. 6. The proposed converter is designed to operate in CCM. A TMDSEZDF2812-0E controller from Texas Instrument is used to develop the shape and frequency of the input current. An extra logic circuit is also used to obtain command of the auxiliary switch. In order to regulate the output voltage, a sample signal is sensed from the output and compared to the reference value in a PI regulator. Another sample is also taken from the rectified input voltage to obtain unity power factor. A Hall-effect sensor for detecting the rectified input current is installed for the average

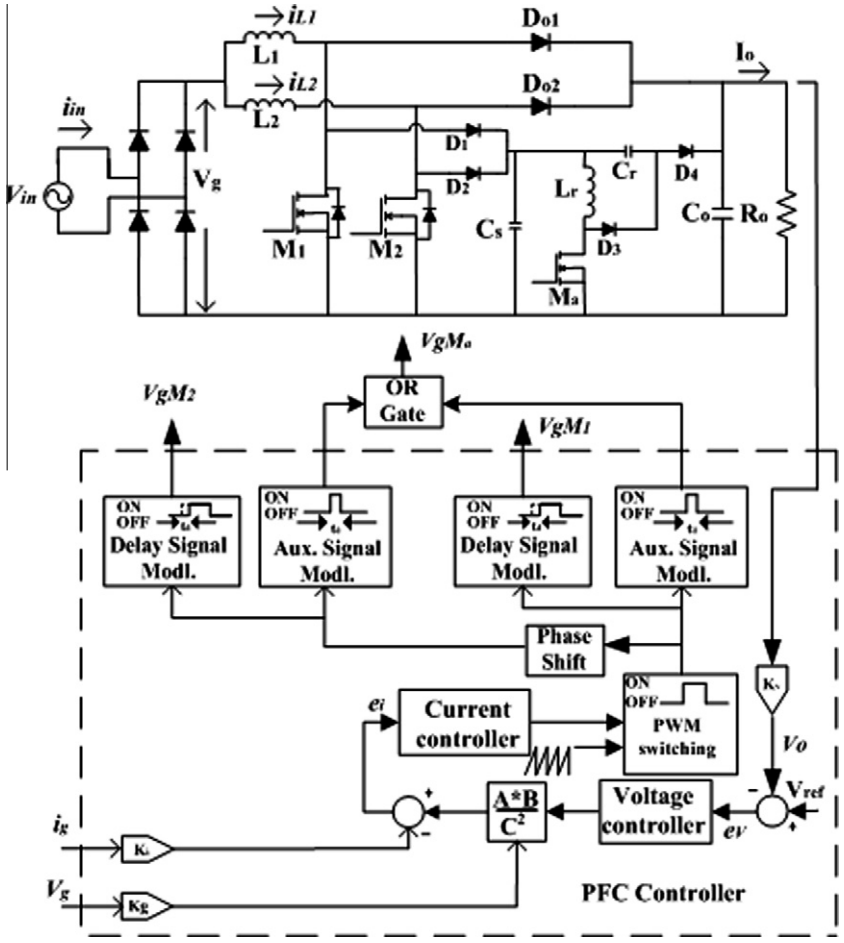

Fig. 6. The scheme of controller and power stage of the proposed topology.

current mode control. The reference current is then generated by the multiplier/divider combination of the synchronous feedback loop, and input voltage feed forward loop. The command signal for the auxiliary switch is produced from the DSP by using dead time modulator. An extra logic circuit is used to obtain the command signal of the auxiliary circuit at beginning of the command signals applied to the main switches. The command signal of the auxiliary switch is constant and calculated according to the delay time for ZVT operation.

4. Simulation and experimental results

In this section, simulations and experiments are carried out to verify the theoretical analysis given in the previous sections. The

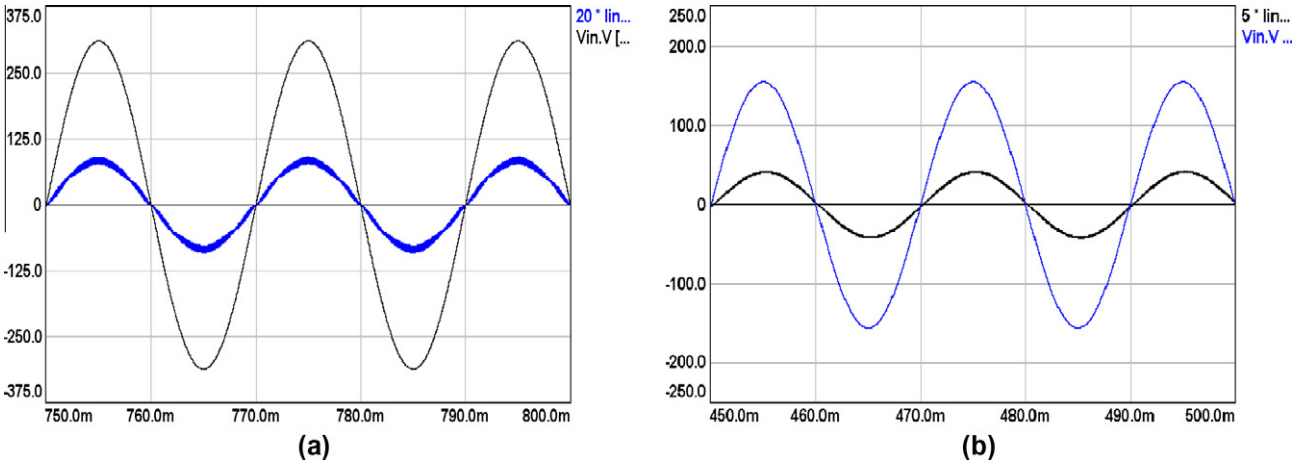

Fig. 7. Simulation results of (a) input voltage (V_{in} = 220 V_{rms}) and 20 $*$ input current (i_{in} = 2.77 A_{rms}) and (b) input voltage (V_{in} = 110 V_{rms}) and 5 $*$ input current (i_{in} = 5.59 A_{rms}) waveforms.

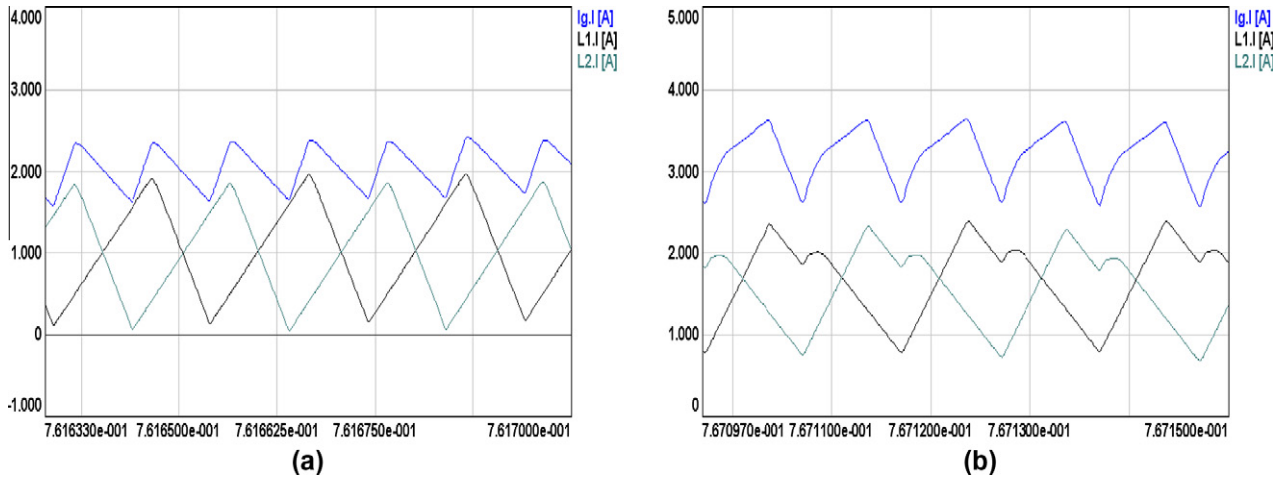

Fig. 8. Simulation results of (a) i_{L1}–i_{L2}–i_g (for $d > 0.5$) and (b) i_{L1}–i_{L2}–i_g (for $d < 0.5$).

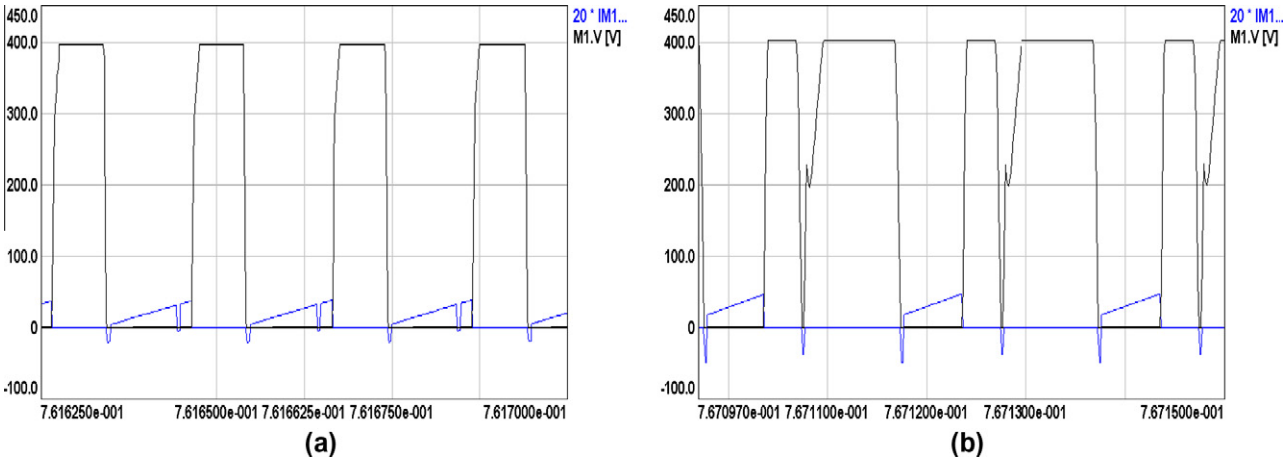

Fig. 9. Simulation results of (a) V_{DSM1}, $20 * i_{DM1}$ (for $d > 0.5$) and (b) V_{DSM2}, $20 * i_{DM2}$ (for $d < 0.5$).

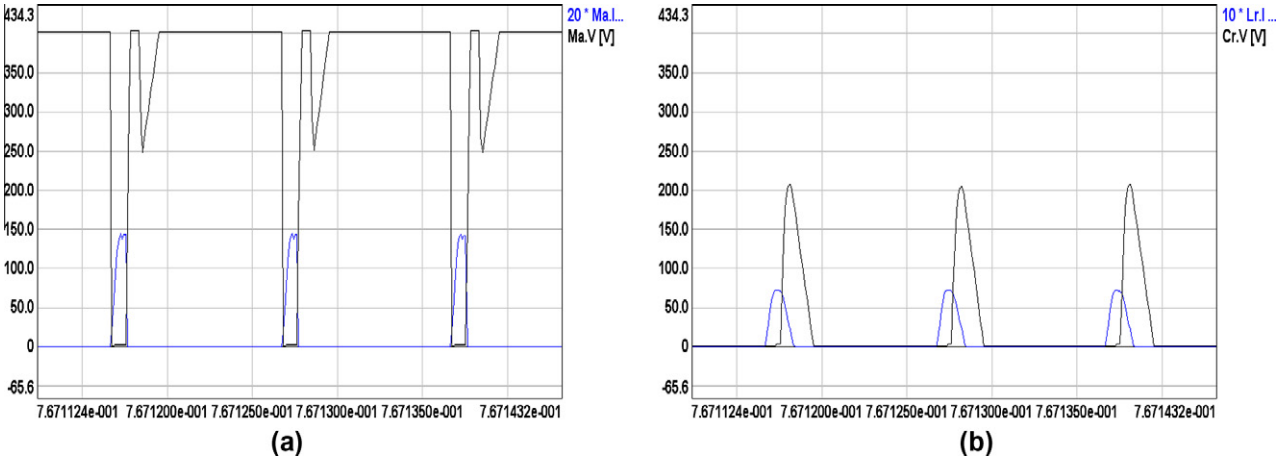

Fig. 10. Simulation results of (a) V_{DSMa}, $20 * i_{DMa}$ and (b) VC_r, $10 * iL_r$.

proposed topology is firstly simulated via Ansoft/Simplorer 7.0 simulation program and an experimental circuit is built up to verify the feasibility of the proposed topology. The simulated results of the proposed topology are shown in Figs. 7–10. The components and parameters used in the simulation and experimental studies are summarized in Table 1.

The hardware realization of the proposed topology was competed and experimental results were recorded. The results are shown in Figs. 11–16. As seen from Figs. 7, 11 and 12, the experi-

Table 1
Components used in the simulations and experiments studies.

Components	Parameters
V_{in} (input voltage)	110–220 V_{rms}
V_o (output voltage)	400 V_{dc}
f_s (switching frequency)	50 kHz/cell
f (input voltage frequency)	50 Hz
L_1 and L_2 (main inductances)	700 μH
L_r (auxiliary inductance)	15 μH
C_s (snubber capacitance)	1.1 nF
C_r (auxiliary capacitance)	10 nF
C_o (output capacitance)	470 μF
M_1, M_2 and M_a	IRFP460
D_{o1} and D_{o2}	DSEI30-12A
D_1, D_2, D_3 and D_4	UF5408
t_d (time delay)	0.85 μs
P_o (output power)	600 W

mental results are in a good agreement with the simulation ones. The controller used in the proposed topology regulates both the output voltage and input current for different values of input voltage.

The inductor currents and total rectified input current are shown in Figs. 8, 13 and 14 from the simulations and experimental studies respectively. The results obtained for $d > 0.5$ and $d < 0.5$ show that the input current ripple amplitude is smaller than that of the main inductors currents. The input current ripple is greatly reduced by interleaving technique for both cases of duty cycle by using interleaving technique. The simulation and experimental results of voltage and current of the main switches (M_1 and M_2) are shown in Figs. 9 and 15, respectively. These results which are obtained for $d > 0.5$ and $d < 0.5$ illustrate that the main switches of the proposed topology are turned on under ZVT condition and turned off under near ZVS condition. The switching conditions of the auxiliary switch, M_a are illustrated in Figs. 10a and 16a corresponding to simulation and experimental studies, respectively. According to these results, the auxiliary switch is turned on and off under soft switching conditions. Figs. 10b and 6b show the simulation and experimental results of the voltage of resonant capacitor used in the auxiliary circuit.

The switching operations of the output and auxiliary circuit diodes are also observed via simulation and experimental studies. It is observed that the output diodes and auxiliary circuit diodes turn on and turn off under soft switching and there is no voltage stress on the diodes. The simulation and experimental results are in very close agreement and verify the theoretical studies given in Section 2.

An experimental circuit for conventional hard switched interleaved boost converter is also built up to compare with the pro-

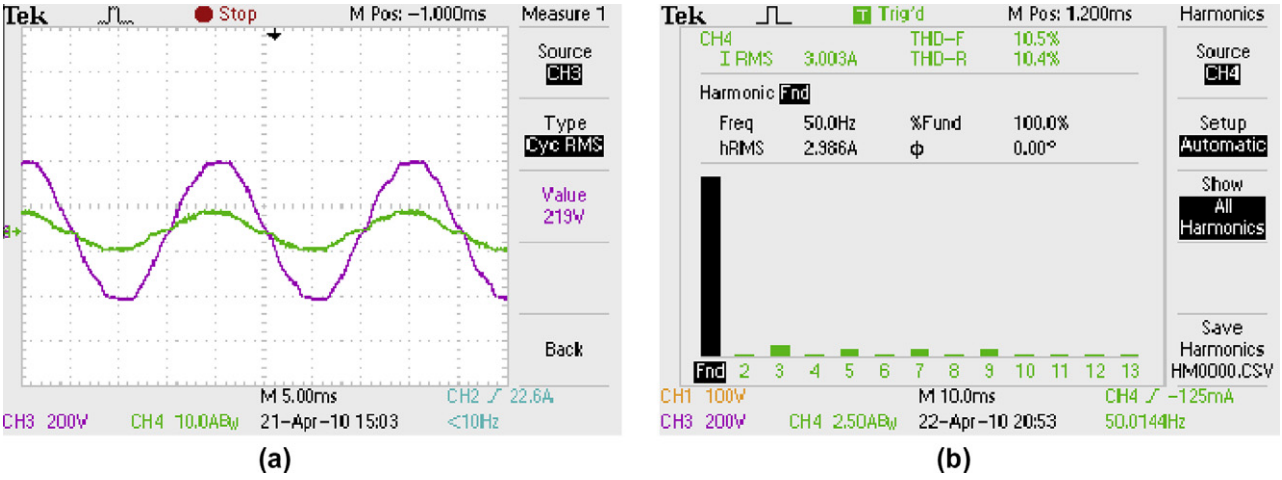

Fig. 11. Experimental results of (a) input voltage (V_{in} = 220 V_{rms}) and input current (i_{in} = 2.98 A_{rms}) and (b) harmonic analysis of input current (THD = 10.4%, pf = 0.994).

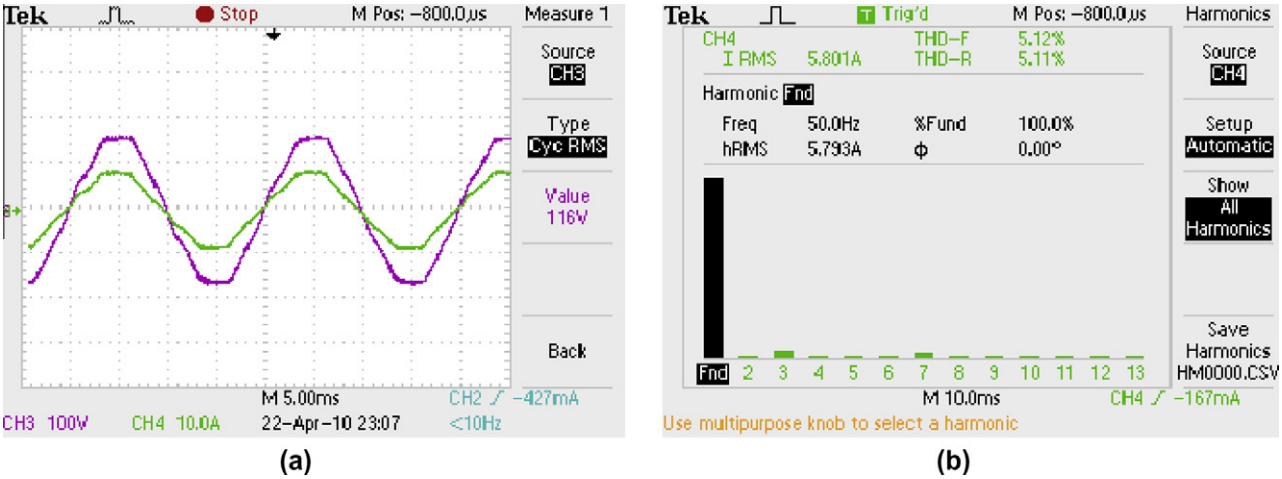

Fig. 12. Experimental results of (a) input voltage (V_{in} = 110 V_{rms}) and input current (i_{in} = 5.80 A_{rms}) and (b) harmonic analysis of input current (THD = 5.1%, pf = 0.998).

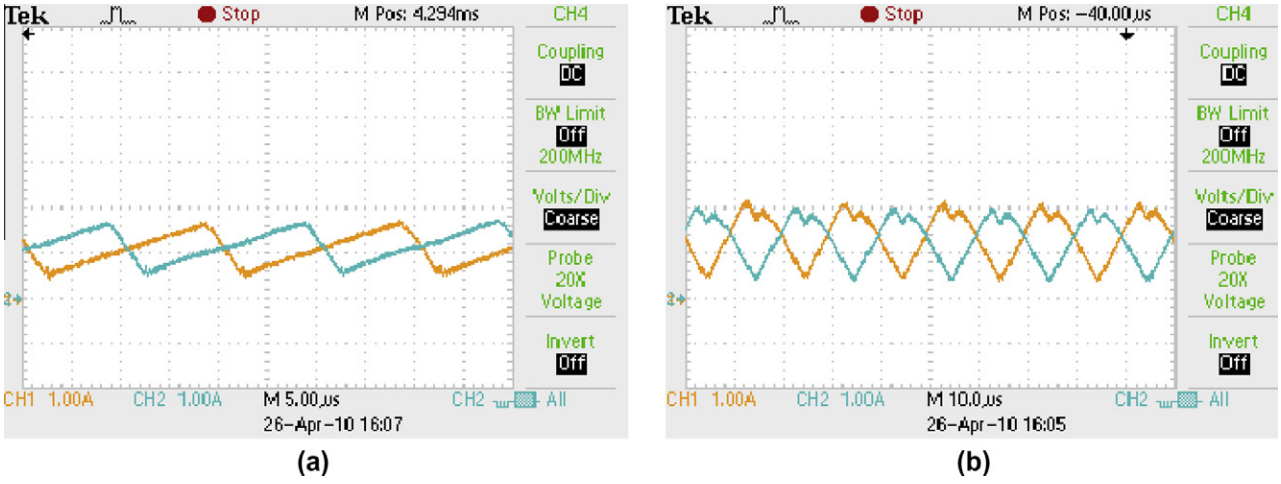

Fig. 13. Experimental results of (a) i_{L1}–i_{L2} (for $d > 0.5$) and (b) i_{L1}–i_{L2} (for $d < 0.5$).

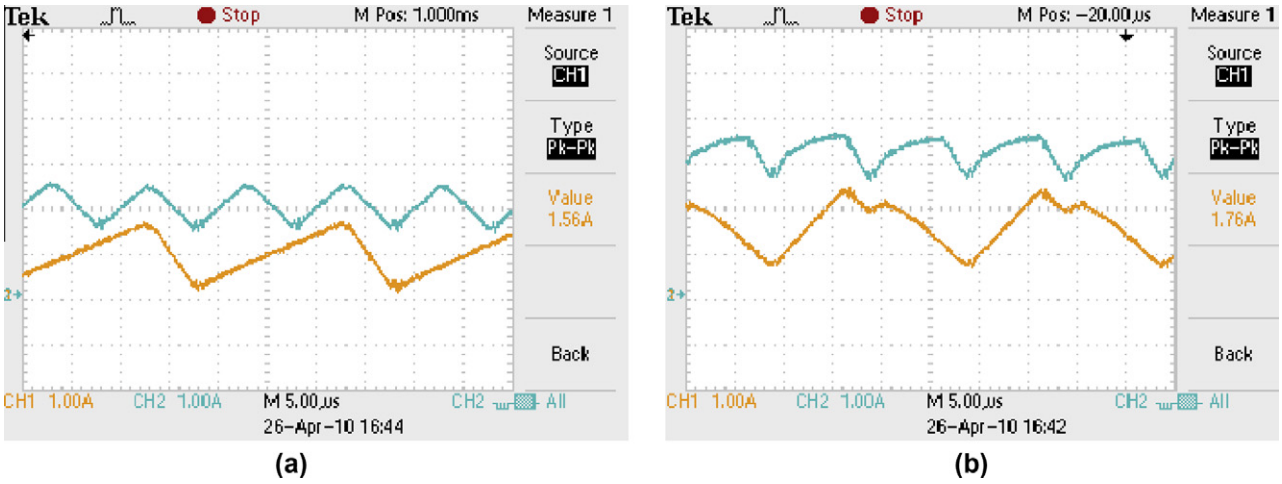

Fig. 14. Experimental results of (a) i_{L1}–i_g (for $d > 0.5$) and (b) i_{L1}–i_g (for $d < 0.5$).

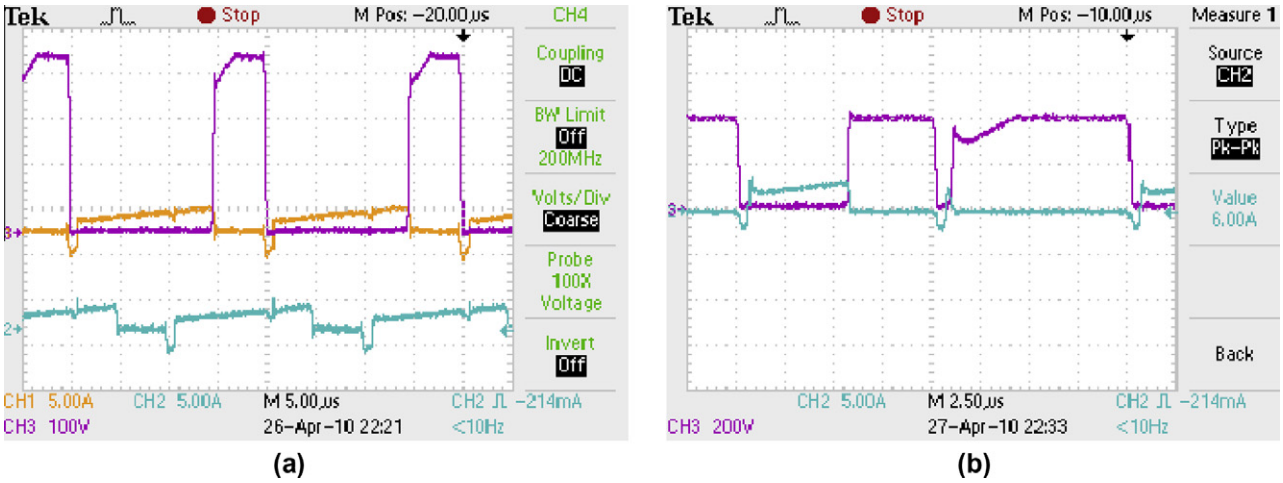

Fig. 15. Experimental results of (a) V_{DSM1}, i_{DM1}, i_{DM2} (for $d > 0.5$) and (b) V_{DSM1}, i_{DM1} (for $d < 0.5$).

posed soft switched topology. Fig. 17 shows the efficiency of the proposed ZVT interleaved boost PFC converter compared with the conventional hard switched topology. The results obtained from experiments show that for an output power of 600 W the effi-

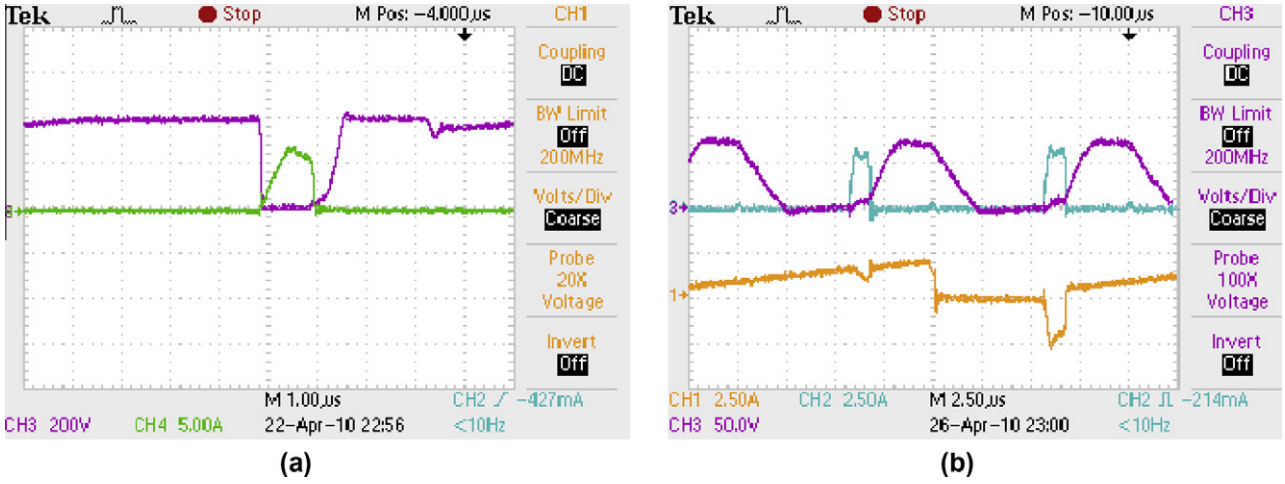

Fig. 16. Experimental results of (a) V_{DSMa}, i_{DMa} and (b) VC_r, i_{DM1}, i_{DMa}.

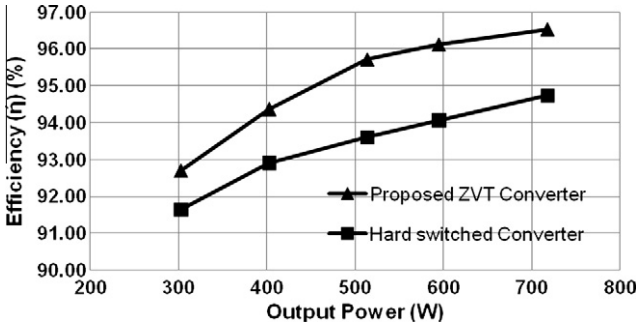

Fig. 17. Experimental efficiency comparison of the proposed ZVT interleaved boost PFC converter and conventional hard switched interleaved boost PFC converter.

ciencies of the proposed ZVT interleaved boost PFC converter and the hard switched converter are equal to 96.12% and 94.06%, respectively.

5. Conclusion

In this paper, an improved ZVT interleaved boost PFC topology is introduced. The proposed ZVT interleaved boost converter is composed of two cell boost conversion units and an active auxiliary circuit. The proposed converter has two important advantages over the similar soft switching converters. The first one is that parallel to the main switches of the converter the auxiliary switch also operates under soft switching condition. Providing soft switching conditions for interleaved boost converters with more than one cells using only one auxiliary switch is another advantage of this topology. The detail theoretical analysis of the converter and turning on and off behavior of the semiconductor switching existing in the circuit are given. In the proposed topology the main switches turn on under ZVT and turn off under near ZVS conditions. Auxiliary switch, M_a is turned on and off under ZVS. In addition, the main and auxiliary diodes turn on and off under soft switching mode. Since there are no voltage and current stresses on the switches, there is no need to use switches with higher current and voltage ratings. Due to the soft switching operation of the switches and diodes used in the converter the passive components of the auxiliary unit are very small. This results the proposed topology not to be a bulky converter. A design example of a 600 W proposed ZVT converter was implemented to verify the system performance. A high power efficiency of 96.12% and a power factor over 0.99% were achieved. The results obtained from simulation and experimental works are in a good agreement and verify the theoretical analysis.

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