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A Dc-Dc Converter with High Voltage Gain and Two Input Boost Stages

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***Abstract* - A family of non-isolated high-voltage-gain dc-dc power electronic converters is proposed. The suggested topologies can be used as multiport converters and draw continuous current from two input sources. They can also draw continuous current from a single source in an interleaved manner. This versatility makes them appealing in renewable applications such as solar farms. The proposed converters can easily achieve a gain of 20 while benefiting from a continuous input current. Such a converter can individually link a PV panel to a 400-Vdc bus. The design and component selection procedures are presented. A 400-W prototype of the proposed converter with V_{in}=20 V and V_{out}=400 V has been developed to validate analytical results.**

I. INTRODUCTION

With increased penetration of renewable energy sources and energy storage, high voltage gain dc-dc power electronic converters find increased applications in green energy systems. They can be used to interface low voltage sources like fuel cells, photovoltaic (PV) panels, batteries, etc., to the 400-V bus in a dc microgrid system (shown in Fig. 1) [1-3]. They also find applications in different types of electronic equipment such as high-intensity-discharge (HID) lamps for automobile headlamps, servo-motor drives, X-ray power generators, computer periphery power supplies, and uninterruptible power supplies (UPS) [4].

To achieve high voltage gains, classical boost and buck-boost converters require large switch duty ratios. Large duty cycles result in high current stress in the boost switch. The maximum voltage gain that can be achieved is constrained by the parasitic resistive components in the circuit and the efficiency is drastically reduced for large duty ratios. There are diode reverse recovery problems because the diode conducts for a short period of time. Also, larger ripples on the high input current and output voltage would further degrade the efficiency of the converter [5]. Typically high frequency transformers or coupled inductors are used to achieve high voltage conversion ratios [6-15]. The transformer design is complicated and the leakage inductances increase for achieving larger gains, as it requires higher number of winding turns. This leads to voltage spikes across the switches and voltage clamping techniques are required to limit voltage stresses on the switches. Consequently, it makes the design more complicated.

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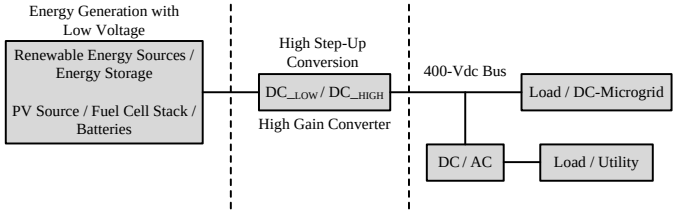

Fig. 1. High voltage gain dc-dc converter in dc-microgrid system.

To achieve high voltage conversion ratios, a new family of high voltage gain dc-dc power electronic converters has been introduced. The proposed converter can be used to draw power from two independent dc sources as a multiport converter [16, 17] or one source in an interleaved manner. They draw continuous input current from both the input sources with low current ripple which is required in many applications, e.g., solar. Several diode-capacitor stages are cascaded together to boost up the voltage which limits the voltage stresses on the switches, diodes and capacitors. Due to the advantages listed above, these converters are good solutions to integrate solar panels into a dc microgrid. In conventional approaches as the output voltage of PV panel is low, several panels are connected in series when connecting the PV array to the 400-Vdc bus through conventional step-up converters. This results in reduced system reliability which can be addressed by connecting high voltage gain converter to each individual PV panel. Moreover, since it is a multi-port converter with a high voltage gain, independent sources can be connected and power sharing, MPPT algorithms etc. can be implemented independently at each input port.

Similar converters with interleaved boost input have been proposed earlier using the Cockcroft-Walton (CW) voltage multiplier [18, 19]. Current fed converters are superior in comparison to the voltage fed counterparts as they have lower input current ripple [19]. The limitation with the CW based converters is that the output impedance increases rapidly with the number of multiplying stages [20]. The efficiency and the output voltage regulation of these converters depend on the output impedance, thus for high gains the converter efficiency would be affected.

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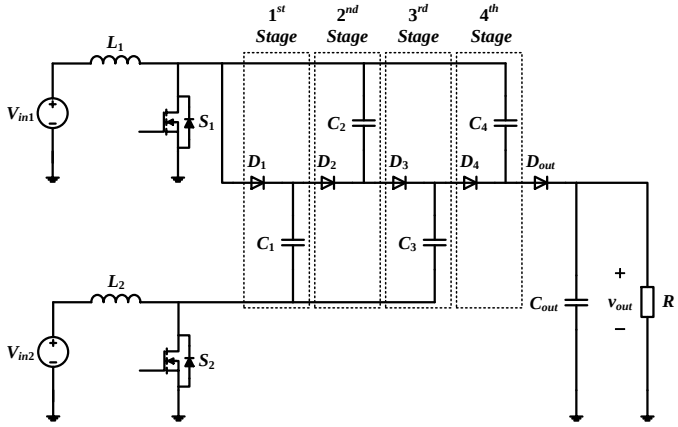

Fig. 2. Proposed high voltage gain dc-dc converter with four VM stages.

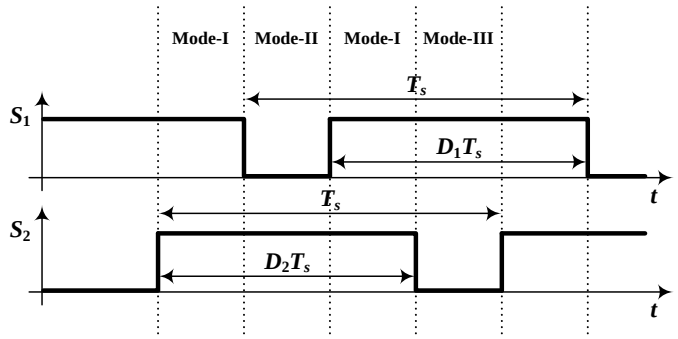

Fig. 3. Switching signals for the input boost stage for the proposed converter.

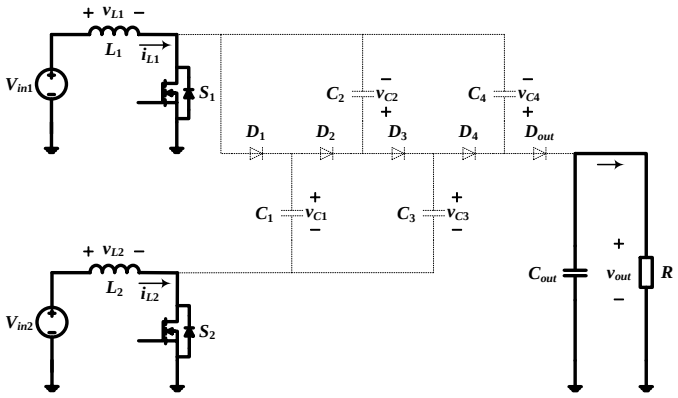

Fig. 4. Mode-I of operation for the proposed converter with four VM stages.

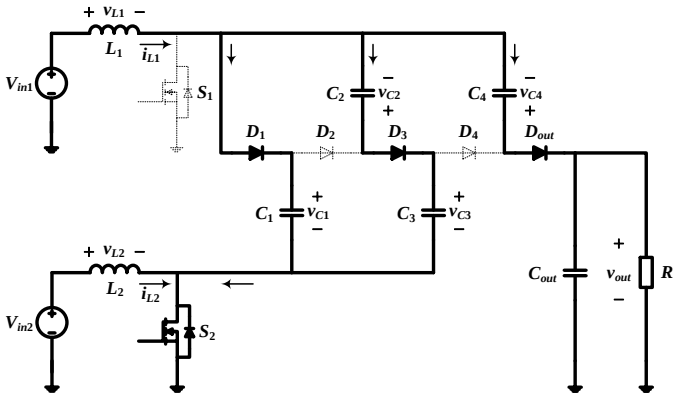

Fig. 5. Mode-II of operation for the proposed converter with four VM stages.

In this paper, a topology is proposed which can easily achieve a gain of 20 while benefiting from a continuous input current. Such a converter can individually link a PV panel to a 400-Vdc bus. In Section II, the proposed converter topology is introduced and different modes of operation are explained. In Section III, the voltage gain of the converter is derived and an alternative topology is also explained. In Section IV, current and voltage stresses required for component selection and loss calculations along with simulation results are provided. In Section V, experimental results for the prototype converter are provided and Section VI concludes the paper.

II. Topology Introduction and Modes of Operation

The proposed converter is inspired from a Dickson charge pump [20]. Diode-capacitor voltage multiplier (VM) stages are integrated with two boost stages at the input. The VM stages are used to help the boost stage achieve a higher overall voltage gain. The voltage conversion ratio depends on the number of VM stages and the switch duty ratios of the input boost stages. Fig. 2 shows the proposed converter with four VM stages. For simplicity and better understanding, the operation of the converter with four multiplier stages has been explained here. Similar analysis can be expanded for a converter with N stages.

For normal operation of the proposed converter, there should be some overlapping time when both the switches are ON and also one of the switches should be ON at any given time (as shown in Fig. 3). Therefore, the converter has three modes of operation. The proposed converter can operate when the switch duty ratios are small and there is no overlap time between the conduction of the switches. However, this mode of operation is not of interest as it leads to smaller voltage gains.

A. *Mode-I*:

In this mode both switches S_1 and S_2 are ON. Both the inductors are charged from their input sources V_{in1} and V_{in2}. The current in both the inductors rise linearly. The diodes in different VM stages are reverse biased and do not conduct. The VM capacitor voltages remain unchanged and the output diode D_{out} is reverse biased (as shown in Fig. 4), thus the load is supplied by the output capacitor C_{out}.

B. *Mode-II*:

In this mode switch S_1 is OFF and S_2 is ON (shown in Fig. 5). All the odd numbered diodes are forward biased and the inductor current I_{L1} flows through the VM capacitors charging the odd numbered capacitors (C_1, C_3, …) and discharging the even numbered capacitors (C_2, C_4, …). If the number of VM stages is odd, then the output diode D_{out} is reverse biased and the load is supplied by the output capacitor. However, if the number of VM stages is even, then the output diode is forward biased charging the output capacitor and supplying the load. In the particular case considered here, since there

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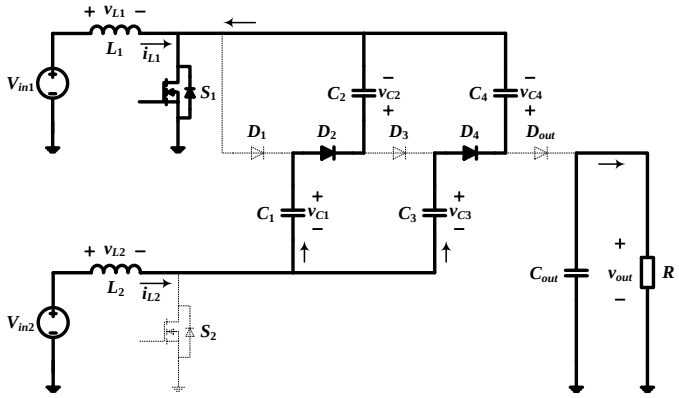

Fig. 6. Mode-III of operation for the proposed converter with four VM stages.

are four VM stages, the output diode is forward biased.

C. *Mode-III*:

In this mode switch S_1 is ON and S_2 is OFF (shown in Fig. 6). Now the even numbered diodes are forward biased and the inductor current I_{L2} flows through the VM capacitors charging the even numbered capacitors and discharging the odd numbered capacitors. If the number of VM stages is odd, then the output diode D_{out} is forward biased charging the output capacitor and supplying the load. However, if the number of VM stages is even, then the output diode is reverse biased and the load is supplied by the output capacitor.

III. Voltage Gain of the Converter

The charge is transferred progressively from input to the output by charging the VM stage capacitors. For a converter with four stages of VM (shown in Fig. 2), the voltage gain can be derived from the volt-sec balance of the boost inductors. For L_1 one can write

$$\langle v_{L1} \rangle = 0 \tag{1}$$

Therefore from Fig. 5, it can be observed that the capacitor voltages can be written in terms of upper boost switching node voltage as

$$V_{C1} = V_{C3} - V_{C2} = V_{out} - V_{C4} = \frac{V_{in1}}{(1-d_1)} \tag{2}$$

where d_1 is the switching duty cycle for S_1.

Similarly, from the volt-sec balance of the lower leg boost inductor L_2, one can write the capacitor voltages (shown in Fig. 6) in terms of lower boost switching node voltage as

$$V_{C2} - V_{C1} = V_{C4} - V_{C3} = \frac{V_{in2}}{(1-d_2)} \tag{3}$$

where d_2 is the switching duty cycle for S_2.

From (2) and (3), the capacitor voltages for the proposed converter with four VM stages can be derived as

$$\begin{aligned} V_{C1} &= \frac{V_{in1}}{(1-d_1)} \\ V_{C2} &= \frac{V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)} \\ V_{C3} &= \frac{2V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)} \\ V_{C4} &= \frac{2V_{in1}}{(1-d_1)} + \frac{2V_{in2}}{(1-d_2)} \end{aligned} \tag{4}$$

The output voltage is derived from (2), which is given by

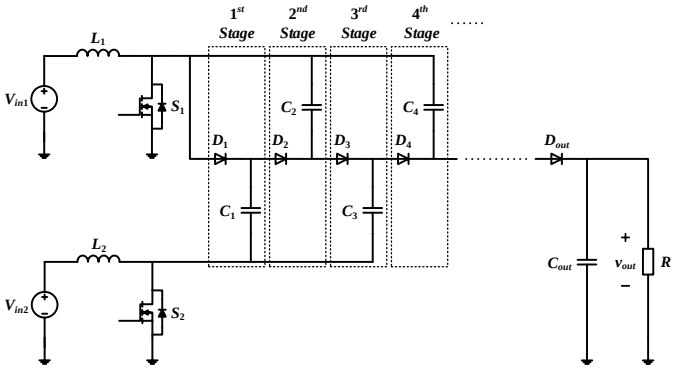

Fig. 7. Proposed converter with N number of VM stages.

$$\begin{aligned} V_{out} &= V_{C4} + \frac{V_{in1}}{(1-d_1)} \\ &= \frac{3V_{in1}}{(1-d_1)} + \frac{2V_{in2}}{(1-d_2)} \end{aligned} \tag{5}$$

Similar analysis can be extended to a converter with N number of VM stages (shown in Fig. 7). Thus the VM stage capacitor voltages are given by

$$\begin{aligned} V_{Cn} &= \left(\frac{n+1}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{n-1}{2}\right)\frac{V_{in2}}{(1-d_2)} \quad \text{if } n \text{ is odd } \& \, n \le N \\ V_{Cn} &= \left(\frac{n}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{n}{2}\right)\frac{V_{in2}}{(1-d_2)} \quad \text{if } n \text{ is even } \& \, n \le N \end{aligned} \tag{6}$$

The output voltage equation of the converter with N number of VM stages depends on whether N is odd or even and is given by

$$\begin{aligned} V_{out} &= V_{CN} + \frac{V_{in2}}{(1-d_2)} \\ &= \left(\frac{N+1}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N+1}{2}\right)\frac{V_{in2}}{(1-d_2)} \end{aligned} \quad \text{if } N \text{ is odd} \tag{7}$$

$$\begin{aligned} V_{out} &= V_{CN} + \frac{V_{in1}}{(1-d_1)} \\ &= \left(\frac{N+2}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N}{2}\right)\frac{V_{in2}}{(1-d_2)} \end{aligned} \quad \text{if } N \text{ is even} \tag{8}$$

When the converter operates in an interleaved manner with single input source, if d_1 and d_2 are also chosen to be identical, i.e., $d_1 = d_2 = d$, then the output voltage is given by

$$V_{out} = (N+1)\frac{V_{in}}{(1-d)} \tag{9}$$

In [21], an interleaved boost power factor corrected converter with voltage-doubler characteristics is introduced. It

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can be observed that it is a special case of the proposed converter with a single VM stage (N = 1).

It is worth noting that there is an alternative to the proposed converter (shown in Fig. 8) where diode D_1 of the first VM stage is connected to the lower boost switching node and capacitor C_1 is connected to the upper boost switching node (compare with Fig. 7).

The output voltage equation for this alternative topology is given by

$$V_{out}=\left(\frac{N+1}{2}\right)\frac{V_{in1}}{(1-d_1)}+\left(\frac{N+1}{2}\right)\frac{V_{in2}}{(1-d_2)} \quad \text{if } N \text{ is odd} \tag{10}$$

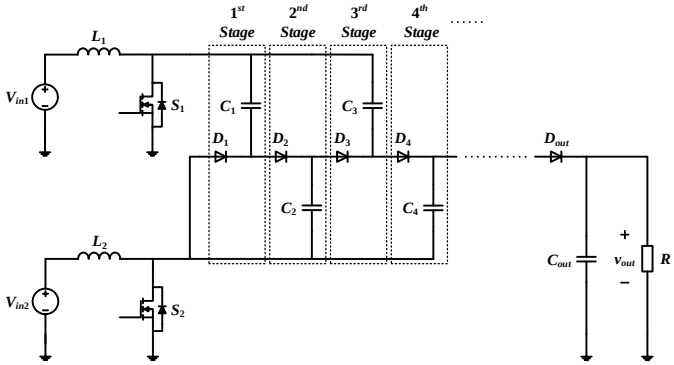

Fig. 8. Alternative to the proposed converter with N number of VM stages.

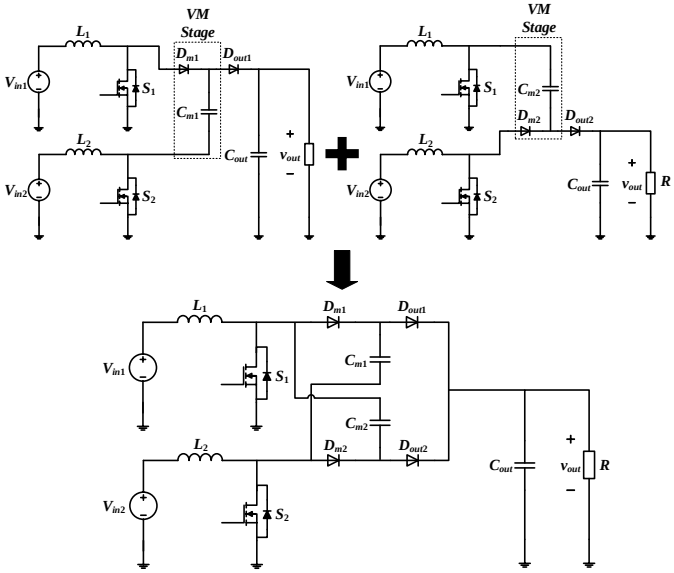

Fig. 9. Combined topology with single VM stage.

$$V_{out}=\left(\frac{N}{2}\right)\frac{V_{in1}}{(1-d_1)}+\left(\frac{N+2}{2}\right)\frac{V_{in2}}{(1-d_2)} \quad \text{if } N \text{ is even} \tag{11}$$

For N = 1, if one combines the topology depicted in Fig. 7 with its alternative (see Fig. 8), then the resulting converter in Fig. 9 is similar to the multiphase converter introduced in [22].

In general, when both topologies with N number of VM stages are combined, then the resulting converter is shown in Fig. 10. When N is odd, then from (7) and (10), the voltage gain of the combined topology is given by

$$V_{out}=\left(\frac{N+1}{2}\right)\frac{V_{in1}}{(1-d_1)}+\left(\frac{N+1}{2}\right)\frac{V_{in2}}{(1-d_2)} \quad \text{if } N \text{ is odd} \tag{12}$$

In this case, the original topology and its alternative each process half of the output power. In other words, the average currents of D_{out1} and D_{out2} are equal.

When N is even, the output voltage of the combined topology would be either (8) or (11) and will be dictated by the topology that provides a higher output voltage. Both legs (shown in Fig. 10) would compete with each other and only one of the output diodes (D_{out1} and D_{out2}) would process the entire power while the other will be reverse biased. When N is

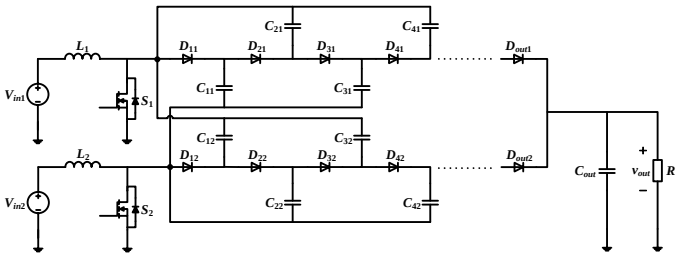

Fig. 10. Combined topology with N number of VM stages.

even, putting the converters in parallel only makes sense if there is only one source used and $d_1 = d_2$. In that case both (8) and (11) determine the output voltage to be

$$V_{out}=(N+1)\frac{V_{in}}{(1-d)} \quad \text{if } N \text{ is even} \tag{13}$$

For the combined topology with a single input source and identical duty ratios d_1 and d_2, i.e., $d_1 = d_2 = d$, both the boost stages will always have symmetrical inductor and switch currents irrespective of the number of VM stages.

IV. Component Selection and Simulation Results

A. Inductor Selection

The inductor currents in both the boost stages depend on the number of VM stages connected to each leg. The average inductor current in each boost stage (shown in Fig. 2) is given by

$$\begin{aligned} I_{L1,avg}&=\left(\frac{N+1}{2}\right)\frac{I_{out}}{(1-d_1)} \quad \text{if } N \text{ is odd}\\ I_{L2,avg}&=\left(\frac{N+1}{2}\right)\frac{I_{out}}{(1-d_2)} \end{aligned} \tag{14}$$

$$\begin{aligned} I_{L1,avg}&=\left(\frac{N+2}{2}\right)\frac{I_{out}}{(1-d_1)} \quad \text{if } N \text{ is even}\\ I_{L2,avg}&=\left(\frac{N}{2}\right)\frac{I_{out}}{(1-d_2)} \end{aligned} \tag{15}$$

It can be observed from (14) and (15) that for a converter with single input source and identical duty ratios d_1 and d_2, when N is odd, then both boost stages have equal average inductor currents (shown in Fig. 11(a)). Whereas when N is even, then $I_{L1,avg}$ is larger than $I_{L2,avg}$ as observed in Fig. 11(b).

The inductor design is similar to that of the normal boost converter. The inductor value is selected such that both the

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boost stages operate in continuous conduction mode (CCM). The minimum inductor value for the CCM operation of both the boost stages is given by

$$L_{1,crit} = \frac{V_{in1} d_1 (1-d_1)}{(N+1) I_{out} f_{sw}} \quad \text{if } N \text{ is odd}$$
$$L_{2,crit} = \frac{V_{in2} d_2 (1-d_2)}{(N+1) I_{out} f_{sw}} \quad (16)$$

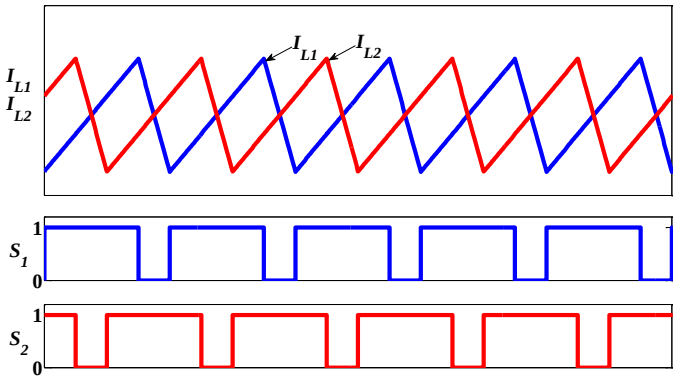

Fig. 11(a). Inductors currents for odd number of VM stages.

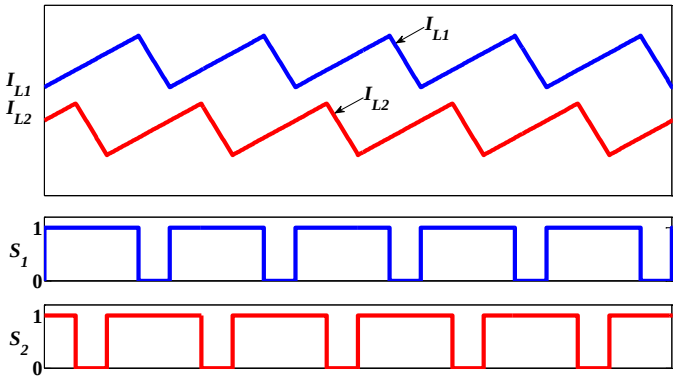

Fig. 11(b). Inductors currents for even number of VM stages.

$$L_{1,crit} = \frac{V_{in1} d_1 (1-d_1)}{(N+2) I_{out} f_{sw}} \quad \text{if } N \text{ is even}$$
$$L_{2,crit} = \frac{V_{in2} d_2 (1-d_2)}{N I_{out} f_{sw}} \quad (17)$$

The inductor values selected for the assumed ripple current is

$$L_1 = \frac{V_{in1} d_1}{\Delta I_{L1} f_{sw}} \quad (18)$$

$$L_2 = \frac{V_{in2} d_2}{\Delta I_{L2} f_{sw}} \quad (19)$$

The peak value of the inductor currents is given by

$$I_{L1,pk} = \frac{(N+1) I_{out}}{2(1-d_1)} + \frac{V_{in1} d_1}{2 L_1 f_{sw}} \quad \text{if } N \text{ is odd}$$
$$I_{L2,pk} = \frac{(N+1) I_{out}}{2(1-d_2)} + \frac{V_{in2} d_2}{2 L_2 f_{sw}} \quad (20)$$

$$I_{L1,pk} = \frac{(N+2) I_{out}}{2(1-d_1)} + \frac{V_{in1} d_1}{2 L_1 f_{sw}} \quad \text{if } N \text{ is even}$$
$$I_{L2,pk} = \frac{N I_{out}}{2(1-d_2)} + \frac{V_{in2} d_2}{2 L_2 f_{sw}} \quad (21)$$

For inductor copper loss calculation, it is important to know the rms value of the inductor currents, which can be calculated as

$$I_{L1,rms} = \sqrt{\left(\frac{(N+1) I_{out}}{2(1-d_1)}\right)^2 + \left(\frac{V_{in1} d_1}{2\sqrt{3} L_1 f_{sw}}\right)^2} \quad \text{if } N \text{ is odd}$$
$$I_{L2,rms} = \sqrt{\left(\frac{(N+1) I_{out}}{2(1-d_2)}\right)^2 + \left(\frac{V_{in2} d_2}{2\sqrt{3} L_2 f_{sw}}\right)^2} \quad (22)$$

$$I_{L1,rms} = \sqrt{\left(\frac{(N+2) I_{out}}{2(1-d_1)}\right)^2 + \left(\frac{V_{in1} d_1}{2\sqrt{3} L_1 f_{sw}}\right)^2} \quad \text{if } N \text{ is even}$$
$$I_{L2,rms} = \sqrt{\left(\frac{N I_{out}}{2(1-d_2)}\right)^2 + \left(\frac{V_{in2} d_2}{2\sqrt{3} L_2 f_{sw}}\right)^2} \quad (23)$$

B. *MOSFET Selection*

The peak blocking voltage of both switches is similar to that of the normal boost converter (shown in Fig. 2) which is given by

$$V_{S1} = \frac{V_{in1}}{(1-d_1)} \quad (24)$$

$$V_{S2} = \frac{V_{in2}}{(1-d_2)} \quad (25)$$

The current stresses on both the switches depend on the number of VM stages. The average current through the switches is given by

$$I_{S1,avg} = \left(\frac{(N+1) d_1}{2(1-d_1)} + \frac{(N-1)}{2}\right) I_{out} \quad \text{if } N \text{ is odd}$$
$$I_{S2,avg} = \left(\frac{(N+1) d_2}{2(1-d_2)} + \frac{(N+1)}{2}\right) I_{out} \quad (26)$$

$$I_{S1,avg} = \left(\frac{(N+2) d_1}{2(1-d_1)} + \frac{N}{2}\right) I_{out} \quad \text{if } N \text{ is even}$$
$$I_{S2,avg} = \left(\frac{N d_2}{2(1-d_2)} + \frac{N}{2}\right) I_{out} \quad (27)$$

From (26) and (27), for a converter with single input source and identical duty ratios d_1 and d_2, it can be observed that when N is odd, the average current through S_2 is greater than S_1 (seen in Fig. 12(a)). When N is even, the average current through S_1 is greater than S_2 (as can be seen in Fig. 12(b)). Also, the rms values of switch currents required for loss calculations are given by

$$I_{S1,rms} = \left(\sqrt{\left(\frac{(N+1)}{2(1-d_1)}\right)^2 (d_1 + d_2 - 1) + \left\{\frac{(N-1)}{2(1-d_2)} + \frac{(N+1)}{2(1-d_1)}\right\}^2 (1-d_2)}\right) I_{out}$$
$$I_{S2,rms} = \left(\sqrt{\left(\frac{(N+1)}{2(1-d_2)}\right)^2 (d_2 + d_1 - 1) + \left\{\frac{(N+1)}{2(1-d_1)} + \frac{(N+1)}{2(1-d_2)}\right\}^2 (1-d_1)}\right) I_{out} \quad (28)$$

if N is odd

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$$I_{S1,rms}=\left(\sqrt{\left(\frac{(N+2)}{2(1-d_1)}\right)^2(d_1+d_2-1)+\left\{\frac{N}{2(1-d_2)}+\frac{(N+2)}{2(1-d_1)}\right\}^2(1-d_2)}\right)I_{out}$$

$$I_{S2,rms}=\left(\sqrt{\left(\frac{N}{2(1-d_2)}\right)^2(d_2+d_1-1)+\left\{\frac{N}{2(1-d_1)}+\frac{N}{2(1-d_2)}\right\}^2(1-d_1)}\right)I_{out} \quad (29)$$

if N is even

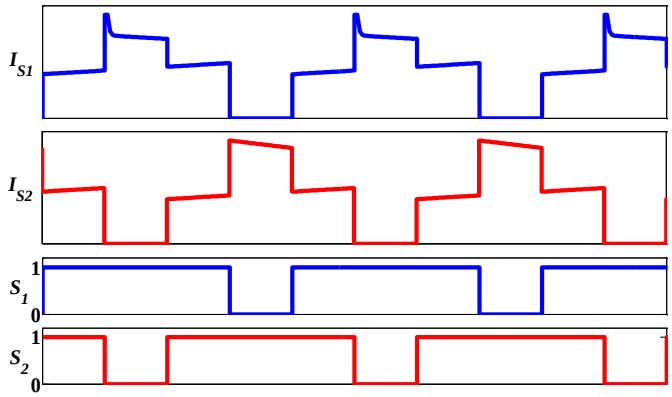

Fig. 12(a). Switch current for odd number of VM stages.

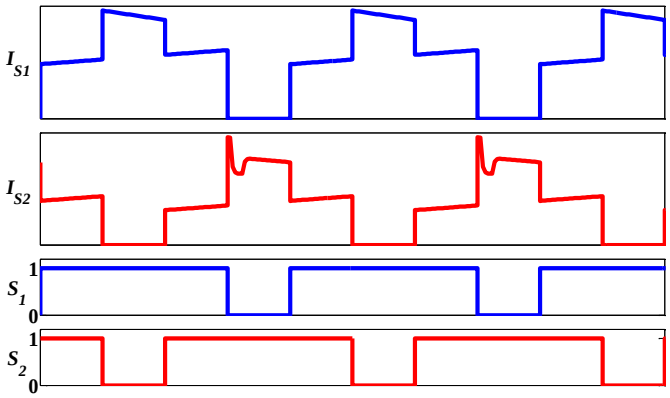

Fig. 12(b). Switch current for even number of VM stages.

It is observed that there is a distortion and spike in the switch current waveforms (as seen in Figs. 12(a), 12(b), and 13). The spike is observed in I_{S1} when the number of VM stages are odd. However, when the number of VM stages are even, the spike is observed in I_{S2}. The spike in switch currents is due to the voltage imbalance between VM stage capacitors. Fig. 13 shows the switch and diode currents for the converter with four VM stages (shown in Fig. 2). The spike in I_{S2} appears during mode-II of operation of the converter (see Fig. 5). Initially diode D_3 conducts the total inductor current I_{L1}, since v_{C3}-v_{C2} is less than v_{C1} and v_{out}-v_{C4}. When v_{C3}-v_{C2} and v_{out}-v_{C4} are both balanced, then diodes D_3 and D_{out} start conducting and share almost equal inductor current $I_{L1}/2$. Diode D_1 starts conducting when v_{C1}, v_{C3}-v_{C2}, and v_{out}-v_{C4} are all balanced. During this period diode current I_{D1} is greater than I_{D3} and I_{Dout} since the impedance seen by the current path is lower. The ratio between the currents is dependent on the values chosen for the VM stage capacitors. Switch current I_{S2} during this period is the sum of I_{L2}, I_{D1}, and I_{D3} and hence there is spike and distortion of the switch current. The magnitude of spike is equal to the sum of both the inductor currents I_{L1} and I_{L2}. It can be observed that the currents exhibit characteristics similar to charging/discharging of an RC circuit which is mainly due to the circuit parasitic resistances such as switch $R_{DS(on)}$, inductor *DCR* and VM stage capacitor *ESR*.

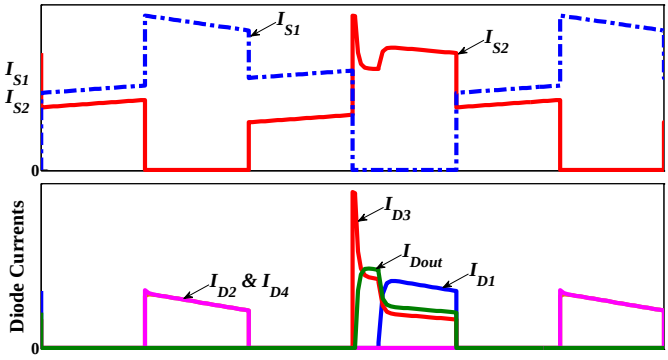

Fig. 13. Switch and diode currents for the proposed converter with four VM stages.

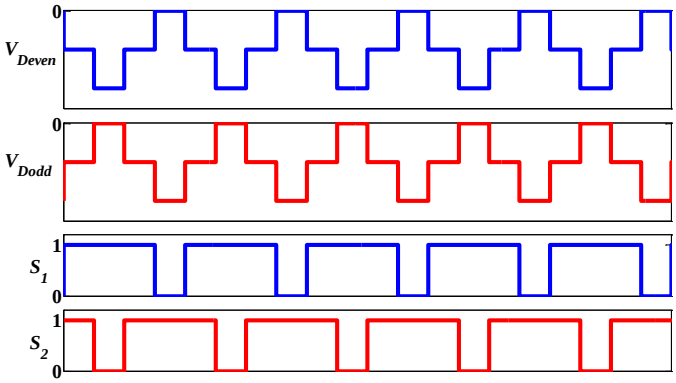

Fig. 14. Diode voltages for odd and even number of VM stages.

C. Diode Selection

The voltage stresses across the diodes depend on the capacitor voltages as it is connected between two VM stage capacitors (shown in Fig. 2). It can be observed that in mode-II of operation, when S_1 is OFF and S_2 is ON, the odd numbered diodes are forward biased and even numbered diodes are in blocking mode.

Similarly, the odd numbered diodes are in blocking mode in the mode-III of operation, when S_1 is ON and S_2 is OFF (shown in Fig. 14). The maximum blocking voltage of the VM stage diodes is given by

$$V_{Dn}=\frac{V_{in1}}{(1-d_1)}+\frac{V_{in2}}{(1-d_2)} \quad (30)$$

However, the output diode conducts during mode-III of operation when there is odd number of VM stages as shown in Fig. 15(a) and conducts during mode-II of operation when there is even number of VM stages as shown in Fig. 15(b). The peak blocking voltage of the output diode is given by

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$$V_{Dout} = \frac{V_{in2}}{(1-d_2)} \quad \text{if } N \text{ is odd} \tag{31}$$

$$V_{Dout} = \frac{V_{in1}}{(1-d_1)} \quad \text{if } N \text{ is even} \tag{32}$$

As explained earlier, the odd numbered diodes conduct during mode-II of operation and the even numbered diodes conduct during mode-III of operation. The average and rms

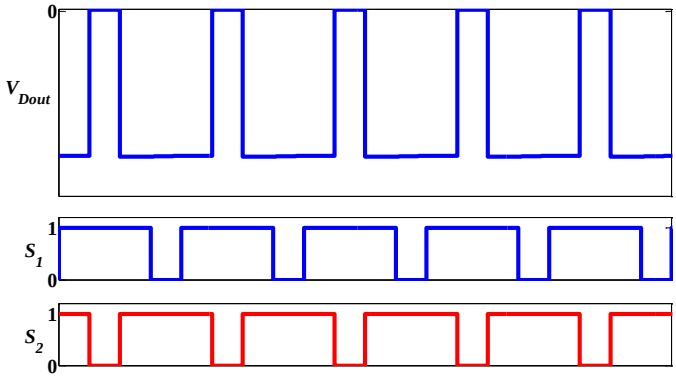

Fig. 15(a). Output diode voltage for odd number of VM stages.

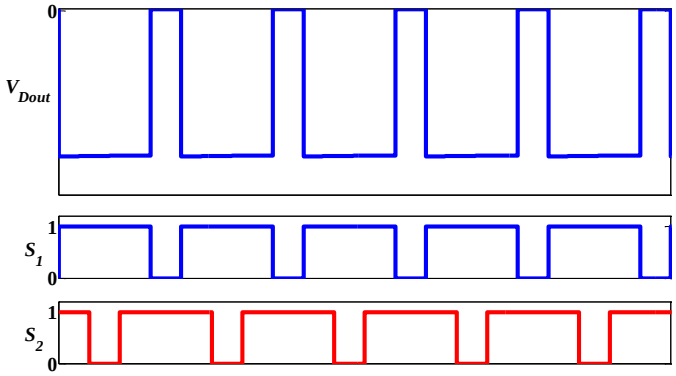

Fig. 15(b). Output diode voltage for even number of VM stages.

diode currents required for diode selection and loss calculation is given by

$$I_{Dodd,avg} = I_{Deven,avg} = I_{Dout,avg} = I_{out} \tag{33}$$

$$I_{Dodd,rms} = \sqrt{\frac{1}{1-d_1}} I_{out} \tag{34}$$

$$I_{Deven,rms} = \sqrt{\frac{1}{1-d_2}} I_{out} \tag{35}$$

$$I_{Dout,rms} = \sqrt{\frac{1}{1-d_2}} I_{out} \quad \text{if } N \text{ is odd} \tag{36}$$

$$I_{Dout,rms} = \sqrt{\frac{1}{1-d_1}} I_{out} \quad \text{if } N \text{ is even} \tag{37}$$

V. Experimental Results

The laboratory prototype with four VM stages and with interleaved boost input stage with a single source was built to test and validate the proposed converter operation. The components used for building the prototype are listed in Table I. The converter is rated at 400 W with input voltage of 20 V and output voltage of 400 V. The switching frequency of the converter is 100 kHz.

The component selection is critical as it determines the output voltage regulation and the efficiency of the converter. The output capacitor is selected based on the amount of

TABLE I

Component List for the Experimental Prototype

Item	Reference	Rating	Part No
Inductor	L_1, L_2	100µH DCR = 11mΩ	CTX100-10-52LP
MOSFET	S_1, S_2	150V, 43A $R_{DS(on)}$ = 7.5mΩ	IPA075N15N3G
Diode	D_1, D_2, D_3, D_4, D_{out}	250V, 40A V_D = 0.97V	MBR40250T
Capacitor	C_1, C_2, C_3, C_4	20µF, 450V ESR = 2.2mΩ	C4ATGBW5200A3MJ
Capacitor	C_{out}	22µF, 450V	B32774D4226

charge that is transferred to the output for a desired output voltage ripple which is given by

$$q_{out} = C_{out}\Delta V_{out} = \frac{I_{out}}{f_{sw}}(1-d) \tag{38}$$

where d is either d_1 or d_2 based on whether the number of VM stages are even or odd. The same amount of charge q_{out} is transferred progressively by the VM stage capacitors. The VM stage capacitors for a desired ripple voltage is given by

$$C_n\Delta V_{Cn} = \frac{I_{out}}{f_{sw}}(1-d) \tag{39}$$

The VM stage capacitors are selected such that the equivalent series resistance due to charging/discharging of the capacitors is low keeping the total capacitance to reasonable levels, thus improving the efficiency and output voltage regulation. It is important to select VM stage capacitors with low *ESR* to minimize the losses, for that purpose thin film capacitors are selected as they have low *ESR* values. Furthermore, the VM stage capacitors and the output capacitor are selected based on the ripple current ratings of the capacitors. For the VM stage capacitors, the ripple current will be higher, therefore capacitor C4ATGBW5200A3MJ (20 µF, 450 V) is selected which has a ripple current rating of 29 A. Since the output capacitor has lower ripple currents, capacitor B32774D4226 (22 µF, 450 V) is selected which has a ripple current rating of 9 A. The output voltage gain and efficiency also depends on the inductor *DCR*, forward voltage drop of the diode, and the MOSFET $R_{DS(on)}$.

The losses in the proposed converter can be easily calculated based on the average and rms currents calculated in the previous section. Fig. 16 shows the loss distribution of the proposed converter at 400 W output power. The switching

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losses in both the MOSFETs are calculated by a commonly used formula given by

$$P_{SW} = \frac{1}{2} \times I_{L,avg} \times V_S \times (t_{off} + t_{on}) + \frac{1}{2} \times f_{sw} \times C_{oss} \times V_S^2 \qquad (40)$$

where $I_{L,avg}$, V_S, and f_{sw} are the inductor current, switch voltage and switching frequency respectively. While t_{on} and t_{off} are the MOSFET turn-on and turn-off switching times [23].

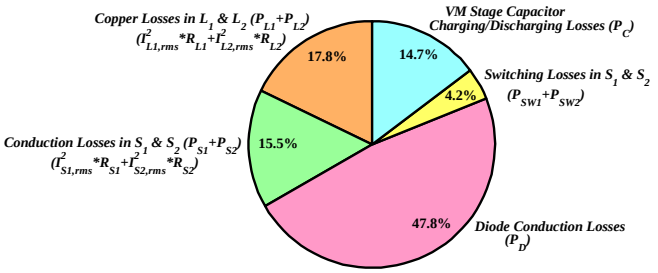

Fig. 16. Loss distribution of the proposed converter at 400 W output power.

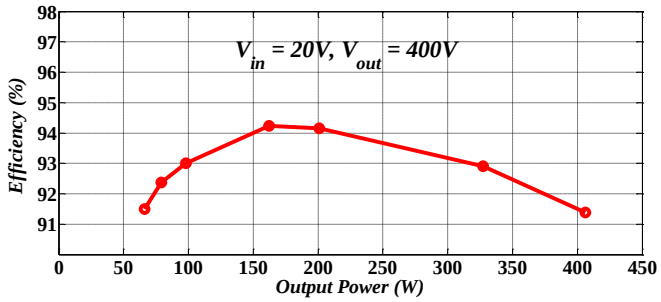

Fig. 17. Efficiency of the proposed converter with interleaved input and four VM stages.

The power loss associated with the charging/discharging of the VM stage capacitors can be calculated by calculating the series equivalent resistance [20]. When all the VM stage capacitors are assumed to be the same, then the power loss is given by

$$P_C = I_{out}^2 \times \frac{N}{C \times f_{sw}} \qquad (41)$$

where C is the value of the VM stage capacitors. The total power loss in the proposed converter is given by

$$P_{Loss} = P_{L1} + P_{L2} + P_{S1} + P_{S2} + P_{SW1} + P_{SW2} + P_D + P_C \qquad (42)$$

Based on the loss breakdown, the efficiency of the proposed converter comes out to be 96.6% at 400 W with total power loss being 13.61 W. Compared to this, the efficiency of the prototype was measured to be 91.4% at 400 W. Fig. 17 shows the efficiency of the converter at different load levels. Maximum efficiency of 94.24% is observed at the output power of 162 W. From (15), the average inductor currents $I_{L1,avg}$ and $I_{L2,avg}$ are calculated as 6.125 A and 4.083 A respectively. Fig. 18 shows the inductor current waveforms and the average values measured for I_{L1} and I_{L2} are 6.461 A and 4.210 A respectively. Fig. 18 shows the voltage stresses across the switches which can be calculated from (24) and (25). The measured peak blocking voltage of the switches is 83.5 V. Figs. 20 and 21 show the voltages across diodes D_4 and D_{out} respectively. The peak blocking voltage of VM stage diodes is given by (30) and is measured as 165 V. Similarly the peak blocking voltage of the output diode for even number of VM stages is given by (32) and is measured as 83.5 V. The measured waveforms shown in Figs. 18 to 21 match the simulated waveforms and thus validate the operation of the converter.

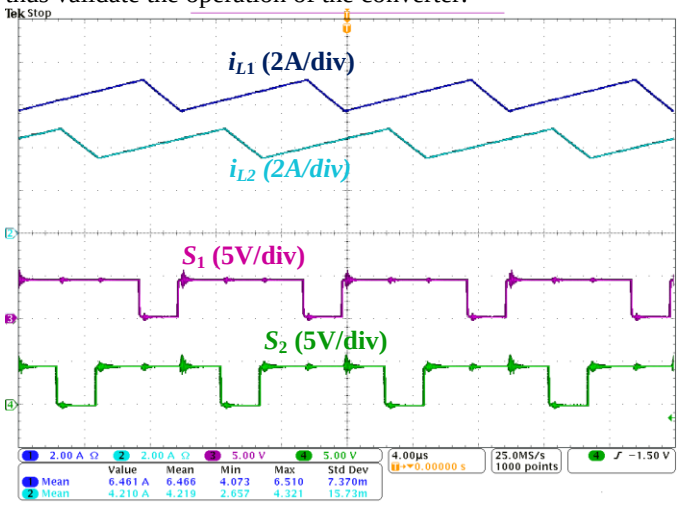

Fig. 18. Inductor current waveforms at 200 W output power.

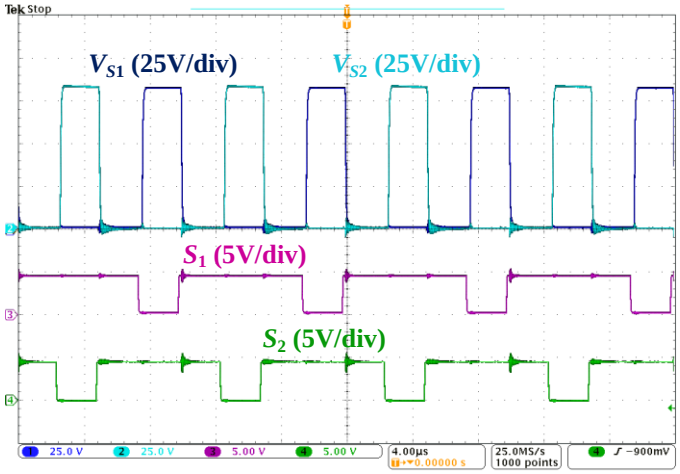

Fig. 19. Voltage stresses on the boost switches.

VI. CONCLUSION

In this paper, a family of novel high voltage gain dc-dc converters with two boost stages at the input has been proposed. The proposed converter is based on diode-capacitor VM stages and the voltage gain is increased by increasing the number of VM stages. It can draw power from two input sources like a multiport converter or operate in an interleaved manner when connected to a single source. One of the advantages of the proposed converter is that since it is a multi-port converter with high voltage gain, it has the flexibility to be connected to independent sources while allowing power sharing, MPPT algorithms etc. to be implemented independently at each input port. Furthermore, an alternative topology of the proposed converter has been

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presented and combining them both would result in a new converter topology. The proposed converter can be used for solar applications where each panel can be individually linked to the 400-Vdc bus. The experimental prototype is built to validate the operation of the converter.

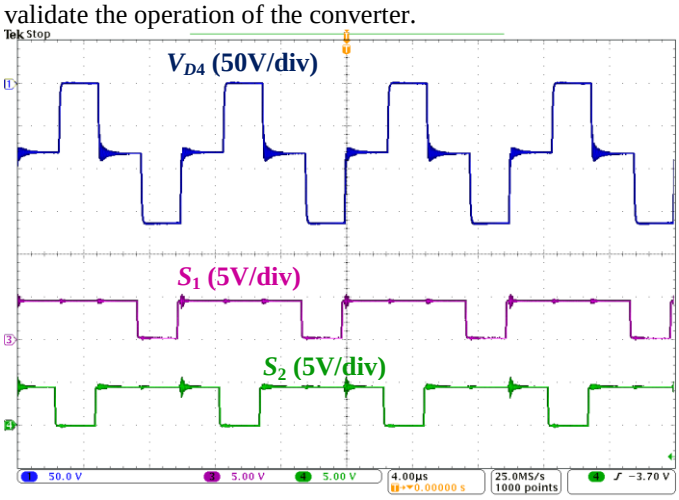

Fig. 20. Voltage waveform across diode D_4.

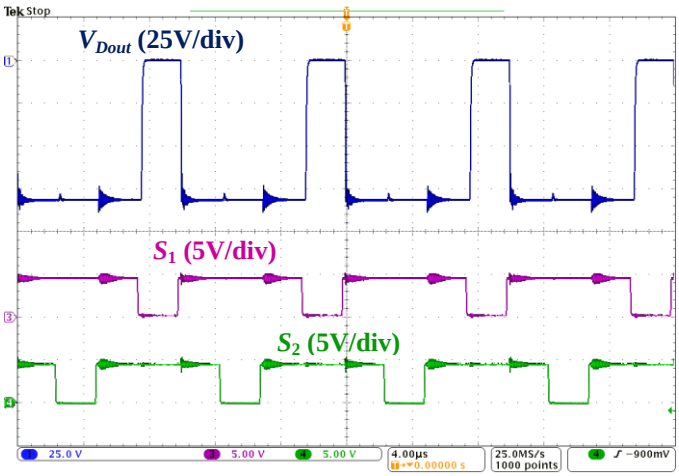

Fig. 21. Voltage waveform across output diode D_{out}.

REFERENCES

[1] S. Jain and V. Agarwal, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking," *IEEE Trans. on Power Electronics*, vol. 22, no. 5, pp. 1928–1940, Sep. 2007.

[2] X. Kong and A. M. Khambadkone, "Analysis and implementation of a high efficiency, interleaved current-fed full bridge converter for fuel cell system," *IEEE Trans. on Power Electronics*, vol. 22, no. 2, pp. 543–550, Mar. 2007.

[3] C. Liu and J. S. Lai, "Low frequency current ripple reduction technique with active control in a fuel cell power system with inverter load," *IEEE Trans. on Power Electronics*, vol. 22, no. 4, pp. 1429–1436, Jul. 2007.

[4] Esam H. Ismail, Mustafa A. Al-Saffar, Ahmad J. Sabzali, and Abbas A. Fardoun, "A Family of Single-Switch PWM Converters With High Step-Up Conversion Ratio," *IEEE Trans. on Circuits and Systems-I: Regular Papers*, vol. 55, no. 4, pp. 1159–1171, May 2008.

[5] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA: Kluwer Academic Publishers, 2001.

[6] W. Li, and, and X. He, "A family of interleaved DC-DC converters deduced from a basic cell with winding-cross-coupled inductors (WCCIs) for high step-up or step-down conversions," *IEEE Trans. on Power Electronics*, vol. 23, no. 4, pp. 1791-1801, Jul. 2008.

[7] W. Li, and X. He, "An interleaved winding-coupled boost converter with passive lossless clamp circuits," *IEEE Trans. on Power Electronics*, vol. 22, no. 4, pp. 1499-1507, Jul. 2007.

[8] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion," *IEEE Trans. on Power Electronics*, vol. 25, no. 9, pp. 2397-2408, Sep. 2010.

[9] Yi-Ping Hsieh, Jiann-Fuh Chen, Tsorng-Juu Liang, and Lung-Sheng Yang, "A novel high step-up DC–DC Converter for a microgrid system," *IEEE Trans. on Power Electronics*, vol. 26, no. 4, pp. 1127-1136, Apr. 2011.

[10] R. Xie, W. Li, Y. Zhao, J. Zhao, X. He, and F. Cao, "Performance analysis of isolated ZVT interleaved converter with winding-cross-coupled inductors and switched-capacitors," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Atlanta, USA, 2010, pp. 2025-2029.

[11] Wuhua Li, Weichen Li, Xiangning He, David Xu, and Bin Wu, "General derivation law of nonisolated high-step-up interleaved converters with built-in transformer," *IEEE Trans. on Industrial Electronics*, vol. 59, no. 3, pp. 1650-1661, Mar. 2012.

[12] Kuo-Ching Tseng, Chi-Chih Huang, and Wei-Yuan Shih, "A high step-up converter with a voltage multiplier module for a photovoltaic system," *IEEE Trans. on Power Electronics*, vol. 28, no. 6, pp. 3047-3057, Jun. 2013.

[13] Wuhua Li, Yi Zhao, Jiande Wu, and Xiangning He, "Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells," *IEEE Trans. on Power Electronics*, vol. 27, no. 1, pp. 133-143, Jan. 2012.

[14] Kuo-Ching Tseng, and Chi-Chih Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Trans. on Industrial Electronics*, vol. 61, no. 3, pp. 1311-1319, Mar. 2014.

[15] Kuo-Ching Tseng, and Chi-Chih Huang, "A high step-up passive absorption circuit used in non-isolated high step-up converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, USA, 2013, pp. 1966-1971.

[16] K. Gummi and M. Ferdowsi, "Synthesis of double-input dc-dc converters using single pole triple throw switch as a building block," in *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, Rhodes, Greece, 2008, pp. 2819-2823.

[17] V. A. K. Prabhala, D. Somayajula and M. Ferdowsi, "Power sharing in a double-input buck converter using dead-time control", in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, San Jose, USA, 2009, pp. 2621-2626.

[18] Sanghyuk Lee, Pyosoo Kim,and Sewan Choi, "High step-up soft-switched converters using voltage multiplier cells," *IEEE Trans. on Power Electronics*, vol. 28, no. 7, pp. 3379-3387, Jul. 2013.

[19] Chung-Ming Young, Ming-Hui Chen, Tsun-An Chang, Chun-Cho Ko, and Kuo-Kuang Jen, "Cascade Cockcroft–Walton Voltage Multiplier Applied to Transformerless High Step-Up DC–DC Converter," *IEEE Trans. on Industrial Electronics*, vol. 60, no. 2, pp. 523-537, Feb. 2013.

[20] John F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, Issue: 3, pp. 374-378, Jun. 1976.

[21] Yungtaek Jang and Milan M. Jovanovic, "Interleaved Boost Converter With Intrinsic Voltage-Doubler Characteristic for Universal-Line PFC Front End," *IEEE Trans. on Power Electronics*, vol. 22, no. 4, pp. 1394–1401, Jul. 2007.

[22] Marcos Prudente, Luciano L. Pfitscher, Gustavo Emmendoerfer, Eduardo F. Romaneli, and Roger Gules, "Voltage Multiplier Cells Applied to Non-Isolated DC–DC Converters," *IEEE Trans. on Power Electronics*, vol. 23, no. 2, pp. 871–887, Mar. 2008.

[23] Z. J. Shen, Yali Xiong, Xu Cheng, Yue Fu, and P. Kumar, "Power MOSFET Switching Loss Analysis: A New Insight," in *Proc. IEEE Industry Applications Conference*, Tampa, USA, 2006, pp. 1438-1442.