Novel High-Conversion-Ratio High-Efficiency Isolated Bidirectional DC–DC Converter

Tsorng-Juu Liang, *Member*, *IEEE*, and Jian-Hsieng Lee

Abstract **–This paper proposes a novel high-conversion-ratio high-efficiency isolated bidirectional DC–DC converter. The proposed converter is operated in the step-down stage. The DC-blocking capacitor in the high-voltage side is used to reduce the voltage on the transformer, and the current-doubler circuits are used in the low-voltage side to reduce the output current ripple. The energy stored in the leakage inductance is recycled to the DC-blocking capacitor. When the proposed converter is operated with a step-up function, dual current-fed circuits on the low-voltage side are used to reduce the current ripples and conduction losses of the switches in the low-voltage side. The voltage-doubler circuit in the high-voltage side increases the conversion ratio. The proposed converter can achieve high conversion with high efficiency. Experimental results based on a prototype implemented in the laboratory with a high voltage of 200 V, low voltage of 24 V, and output power of 200 W verify the performance of the proposed converter. The peak efficiency of the proposed converter in the high-step-down and high-step-up stages is 96.3% and 95.6%, respectively.**

Index Terms **– High conversion ratio, current-fed converter, voltage-doubler circuit, current-doubler rectifier, synchronous rectifier.**

I. Introduction

The extensive use of fossil fuels and nuclear energy has caused major pollution and safety problems, such as the nuclear accident in a power plant in Fukushima, Japan. Therefore, to reduce environmental damage, many countries have committed to developing green energy, such as solar and wind energy [1]–[8]. In addition to improvements in the conversion efficiency of green energy, the storage and reuse of excess energy have become important research topics. Thus, high-step-up/step-down converters have become important research subjects. Converters with high conversion ratios can be used in energy storage systems, high-intensity discharge lamps, high power applications, communication power, solar power, and uninterruptible power supplies. These converters are designed by combining switched-capacitor cells, coupled-inductor techniques, and Z source techniques [9]–[21].

Manuscript received January 20, 2014; revised May 29, 2014, August 15, 2014 and November 08, 2014; accepted November 26, 2014.

T.-J. Liang and J.-H. Lee are with the Department of Electrical Engineering / Advanced Optoelectronic Technology Center (AOTC) / Green Energy Electronics Research Center (GREERC) National Cheng-Kung University, Tainan, Taiwan, R.O.C. (Corresponding author e-mail: tjliang@mail.ncku.edu.tw)

Compared with high-step-up and high-step-down converters, bidirectional high-conversion-ratio converters can significantly reduce the overall system volume, cost, and number of components. Non-isolated bidirectional topologies with high conversion ratios have been presented in lectures [18]–[27]. These non-isolated bidirectional converters can be constructed by using coupled inductors [18]–[21], switched-capacitor techniques [22]–[25], and cascade techniques [26], [27] to obtain a high conversion ratio with an appropriate duty ratio. However, non-isolated converters fail to meet the safety standards of galvanic isolation in many applications. Numerous isolated bidirectional converters with high-conversion-ratio applications have been presented in many papers [28]–[39]. Bidirectional isolated DC–DC converters derived from push–pull topologies [28], full-bridge topologies [29]-[31], [42], and series-resonant full-bridge [32] converters can increase the conversion ratio by adjusting the turns ratio of the transformer. However, a high turns ratio increases the transformer size. The conversion ratio of bidirectional DC–DC converters can be improved with current-doubler techniques [33], [34], voltage-doubler techniques [35], [36], Z source [37], and cascade techniques [38], [39] to increase the conversion ratio.

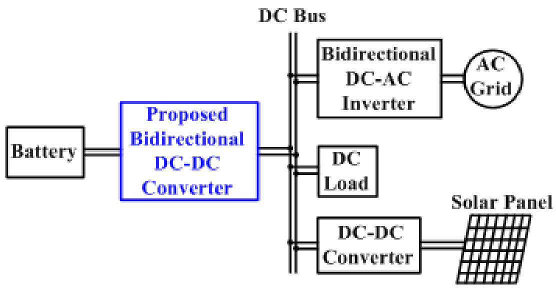


Fig. 1 Configuration of a distributed generation system.

The distributed generation system shown in Fig. 1 indicates that bidirectional dc-dc converter plays a very important role between energy storage device (Battery) and voltage bus. The function of the bidirectional converter is to transfer energy between the battery and the DC bus. The energy generated from the renewable source(s) will be transferred to the dc voltage bus. Load(s) may be connected with dc voltage bus and ac utility grid. Battery is used to provide energy to dc voltage bus when the grid voltage outage and renewable energy sources can't provide enough energy to the load connected with dc voltage bus. This paper proposes a high-conversion-ratio isolated bidirectional DC–DC converter for distributed generation applications, the topology configuration of which is shown in Fig. 2. The circuit includes high voltage V_{HV}; high-voltage capacitor C_1 and DC-blocking capacitor C_2; four active switches S_1, S_2, S_3, and S_4; a transformer T_1; two inductors L_1 and L_2; a low-voltage capacitor C_3; and low voltage V_{LV}. The gate signals of S_1 and S_2 in the high-step-down stage are interlaced by a phase shift of 180 degrees, and S_3 and S_4 are synchronous rectifiers. In the high-step-up mode, the gate signals of S_3 and S_4 are greater than 50% and are controlled by a phase shift of 180 degrees. The gate signals of S_1 and S_2 are smaller than 50% and are controlled by a phase shift of 180 degrees with synchronous rectifiers [40],[41]. The function of the proposed bidirectional converter is like the "double voltage step-down" instead of LLC mode. (When S_1 is turned on, the voltage on the primary winding is reduced by half because of the capacitor C_2. Thus the voltage gain can be reduced by half by adding C_2 in series with the half bridge converter.) This converter is controlled with duty control on frequency control so that the effect of leakage inductance can be neglected. The proposed cannot achieve ZVS on the high voltage side power switches but the low voltage side synchronous rectifier can achieve ZVS. Thus, the turn ratio can be reduced as compared with the traditional half bridge converter. The size of the transformer can be decreased by using a voltage-doubler circuit with low turns ratio, so that a lower turns ratio is needed on the secondary side. The features of the proposed converter are as follows: 1) It meets the safety standards of galvanic isolation; 2) The size of the transformer can be reduced; 3) The energy in the leakage inductance of the transformer can be recycled; 4) It has a high conversion ratio; 5) The low-voltage side has low ripple current; 6) Synchronous rectifiers improve system efficiency.

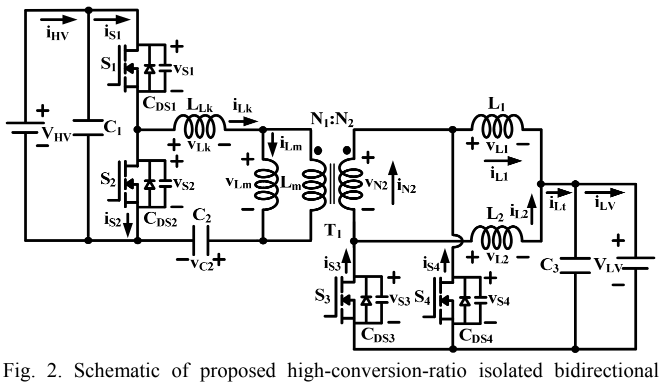


Fig. 2. Schematic of proposed high-conversion-ratio isolated bidirectional DC–DC converter.

II. Operating Principles of Proposed Converter

To simplify the analysis of the proposed converter, the following are assumed over one switching period:

1) C_1, C_2, and C_3 are large enough; thus, V_{LV}, V_{C2}, and V_{HV} are regarded as constant.
2) All active switches are regarded as ideal.
3) L_1 is equal to L_2.
4) The turns ratio of transformer T_1 is $n = N_1/N_2$, and the leakage inductance L_{Lk} is considered in the analysis, where N_1 and N_2 are the winding turns in high-voltage and low-voltage sides, respectively.
5) The parasitic inductors, capacitors, and resistors of circuit traces are ignored.

(A) Step-Down Stage

The key waveforms of the proposed converter in the high-step-down stage in continuous-conduction mode (CCM) operation are illustrated in Fig. 3. The main switches are S_1 and S_2; S_3 and S_4 are the synchronous rectifiers. The operating mode of the proposed converter can be divided into ten operating modes over one switching period:

1) Mode I [t_0, t_1]: During this interval, S_1 and S_3 are on, while S_2 and S_4 are off. The equivalent circuit is shown in Fig. 4(a). The current i_{Lk} increases linearly. V_{HV} and C_1 provide energy to L_1, C_3, and V_{LV} via T_1. C_2 is charged by V_{HV} and C_1. The energy stored in L_2 is transferred to C_3 and V_{LV}. Switch current i_{S1} is equal to i_{Lk}, and switch current i_{S3} is equal to $i_{L1}+i_{L2}$. The voltage across S_2 is equal to V_{HV}, and that across S_4 is equal to $(V_{HV}-v_{C1})/n$. This operating mode ends when S_1 is turned off at $t = t_1$.

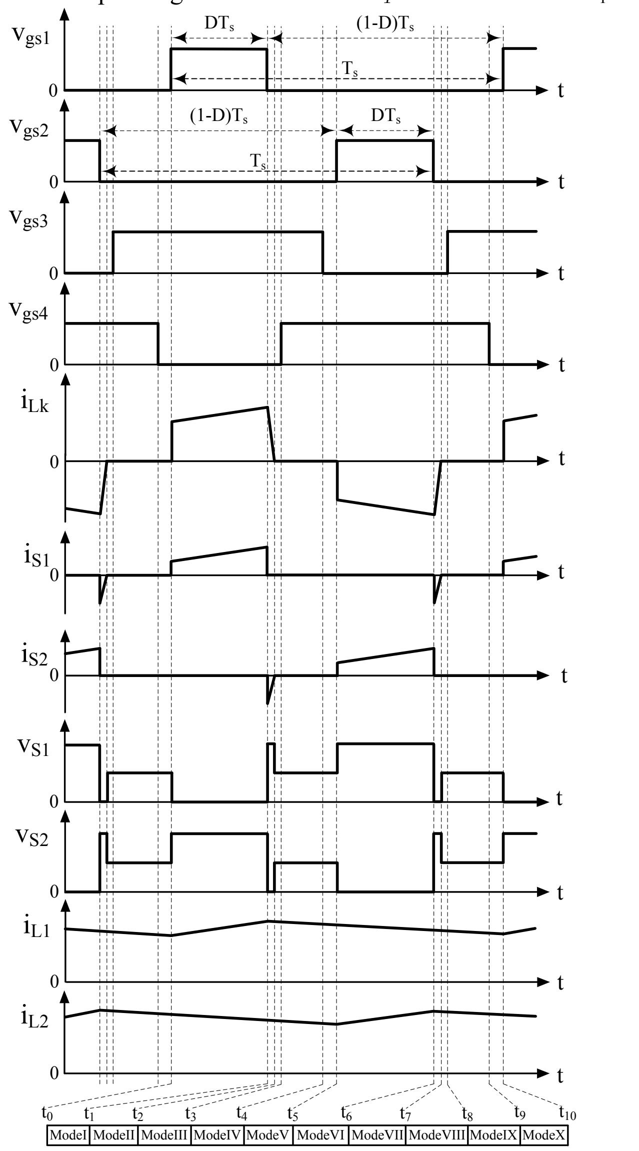
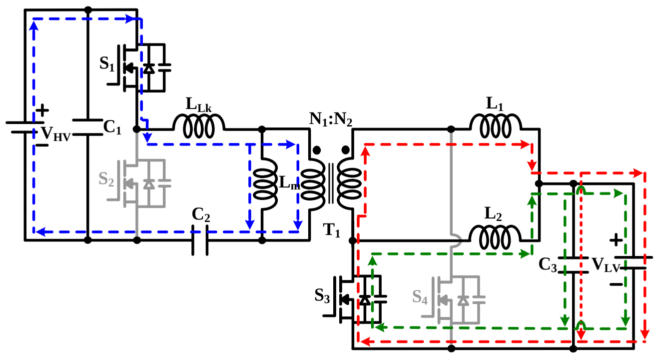


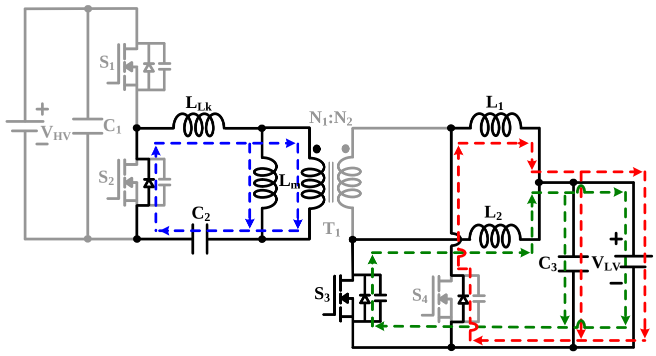
Fig. 3. Key waveforms of proposed isolated bidirectional converter in high-step-down stage during CCM operation.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2386284, IEEE Transactions on Industrial Electronics

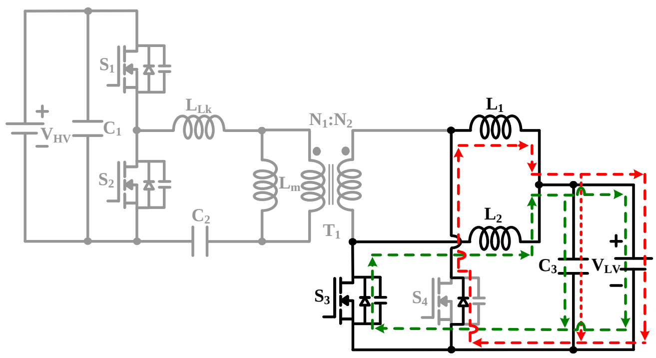
2) Mode II [t_1, t_2]: During this interval, S_3 is on while S_1, S_2, and S_4 are off. The equivalent circuit is illustrated in Fig. 4(b). The leakage current i_{Lk} flows into the anti-parallel diode of S_2 to charge C_2 and to clamp the maximum voltage spike of S_1 such that the energy stored in L_{lk} can be recycled. The energy stored in L_2 continues to release energy to C_3 and V_{LV}. The energy stored in L_1 is released through the anti-parallel diode of S_4 to C_3 and V_{LV}. This operating mode ends when i_{Lk} is equal to zero at $t = t_2$.
3) Mode III [t_2, t_3]: During this interval, S_3 is on, while S_1, S_2, and S_4 are off. The equivalent circuit is illustrated in Fig. 4(c). The voltages across S_1 and S_2 are $V_{HV}/2$. The voltage across winding N_2 is equal to zero. The anti-parallel diode of S_4 conducts to achieve zero-voltage switching (ZVS) condition. Through this diode flows inductor current i_{L1} to release energy to C_3 and V_{LV}, which continuously receive the energy stored in L_2. This operating mode ends when S_4 is turned on at $t = t_3$.
4) Mode IV [t_3, t_4]: During this interval, S_1 and S_2 are off, while S_3 and S_4 are on. The equivalent circuit is illustrated in Fig. 4(d). S_4 achieves ZVS when it is turned on with the synchronous rectifier and thus improves system efficiency. The energy stored in L_1 and L_2 is simultaneously delivered to C_3 and V_{LV}. Switch currents i_{S3} and i_{S4} are equal to i_{L1} and i_{L2}. Current i_{Lt} equals i_{L1}+i_{L2}; thus, its ripple current can be reduced. This operating mode ends when S_3 is turned off at $t = t_4$.
5) Mode V [t_4, t_5]: During this interval, S_4 is on, while S_1, S_2, and S_3 are off. The equivalent circuit is illustrated in Fig. 4(e). The energy stored in L_1 and L_2 is simultaneously released to C_3 and V_{LV}. This operating mode ends when S_2 is turned on at $t = t_5$.
6) Mode VI [t_5, t_6]: During this interval, S_2 and S_4 are on, while S_1 and S_3 are off. The equivalent circuit is illustrated in Fig. 4(f). C_2 provides energy to N_2 through T_1 to release energy to L_2, C_3, and V_{LV}. Switch current i_{S2} is equal to $-i_{Lk}$, and i_{S4} is equal to i_{L1}+i_{L2}. The voltage across S_1 is equal to V_{HV}, and that across S_3 is equal to $(V_{HV}-v_{C1})/n$. The energy stored in L_1 is transferred to C_3 and V_{LV}. This operating mode ends when S_2 is turned off at $t = t_6$.
7) Mode VII [t_6, t_7]: During this interval, S_1, S_2, and S_3 are off while S_4 is on. The equivalent circuit is illustrated in Fig. 4(g). The leakage current i_{Lk} flows into the anti-parallel diode of S_1 to charge V_{HV} and C_1 and to clamp the maximum voltage spike of S_2 such that the leakage energy can be recycled. The energy stored in L_1 continues to release energy to C_3 and V_{LV}. The energy stored in L_2 is released through the anti-parallel diode of S_3 to C_3 and V_{LV}. This operating mode ends when i_{Lk} is equal to zero at $t = t_7$.
8) Mode VIII [t_7, t_8]: During this interval, S_1, S_2, and S_3 are off, while S_4 is on. The equivalent circuit is illustrated in Fig. 4(e). The anti-parallel diode of S_3 conducts to achieve ZVS condition. Through this diode flows inductor current i_{L2} to release energy to C_3 and V_{LV}, which continuously receive the energy stored in L_1. This operating mode ends when S_3 is turned on at $t = t_8$.
9) Mode IX [t_8, t_9]: During this interval, S_1 and S_2 are off, while S_3 and S_4 are on. The equivalent circuit is illustrated in Fig. 4(d). S_3 achieves ZVS when it is turned on with the synchronous rectifier. The energy stored in L_1 and L_2 is simultaneously delivered to C_3 and V_{LV}. This operating mode ends when S_4 is turned off at $t = t_9$.
10) Mode X [t_9, t_{10}]: During this interval, S_1, S_2, and S_4 are off, while S_3 is on. The equivalent circuit is illustrated in Fig. 4(c). The energy stored in L_1 and L_2 is released via S_3 and the anti-parallel diode of S_4, respectively, to release energy to C_3 and V_{LV}. This operating mode ends when S_1 is turned on at $t = t_{10}$.



(a) Mode I

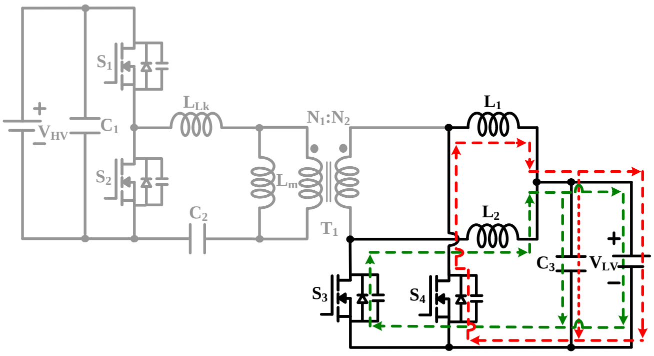


(b) Mode II

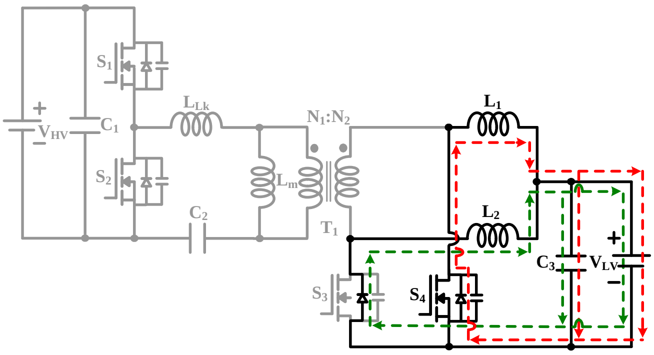


(c) Modes III and X

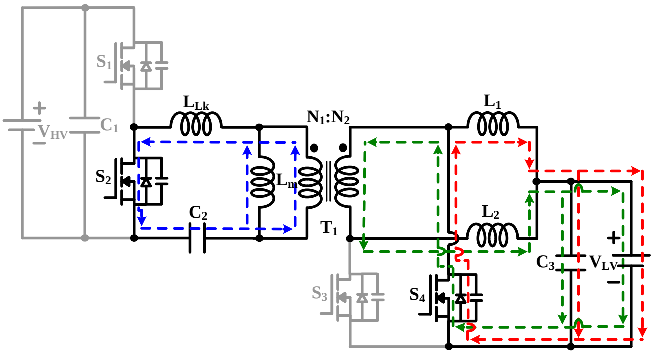
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2386284, IEEE Transactions on Industrial Electronics



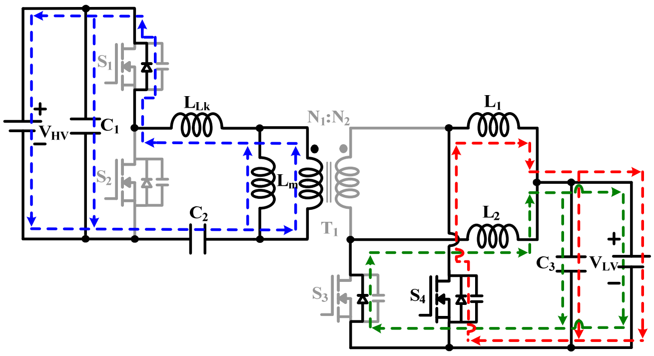
(d) Modes IV and IX



(e) Modes V and VIII



(f) Mode VI



(g) Mode VII

Fig. 4. Equivalent circuits of isolated bidirectional DC–DC converter in high-step-down stage over one switching period during CCM operation: (a) mode I, (b) mode II, (c) modes III and X, (d) modes IV and IX, (e) modes V and VIII, (f) mode VI, and (g) mode VII.

(B) Step-Up Stage

The key waveforms of the proposed converter in the high-step-up stage in CCM operation are shown in Fig. 5. The main switches are S_3 and S_4; S_1 and S_2 are the synchronous rectifiers. The operating mode of the proposed converter can be divided into ten operating modes over one switching period:

1) Mode I [t_0, t_1]: During this interval, S_3 and S_4 are on while S_1 and S_2 are off. The equivalent circuit is shown in Fig. 6(a). The energy stored in L_{Lk} is released via the anti-parallel diode of S_1 to V_{HV} and C_1. Therefore, the leakage energy can be recycled, and the voltage of S_2 is clamped at V_{HV}. V_{LV} and C_3 simultaneously provide energy to L_1 and L_2. This operating mode ends when i_{Lk} is equal to zero at $t = t_1$.

2) Mode II [t_1, t_2]: During this interval, S_3 and S_4 are on, while S_1 and S_2 are off. The equivalent circuit is shown in Fig. 6(b). V_{LV} and C_3 continue to provide energy to L_1 and L_2. i_{L1} and i_{L2} are equal to $i_{Lt}/2$. Thus, the conduction losses of L_1 and L_2 and S_3 and S_4 are reduced, and system efficiency improves. The voltage across T_1 is equal to zero, and that across S_1 and S_2 is equal to $V_{HV}/2$. i_{L1} is equal to i_{S4}, and i_{L2} is equal to i_{S3}. C_1 releases energy to V_{HV}. This operating mode ends when S_3 is turned off at $t = t_2$.

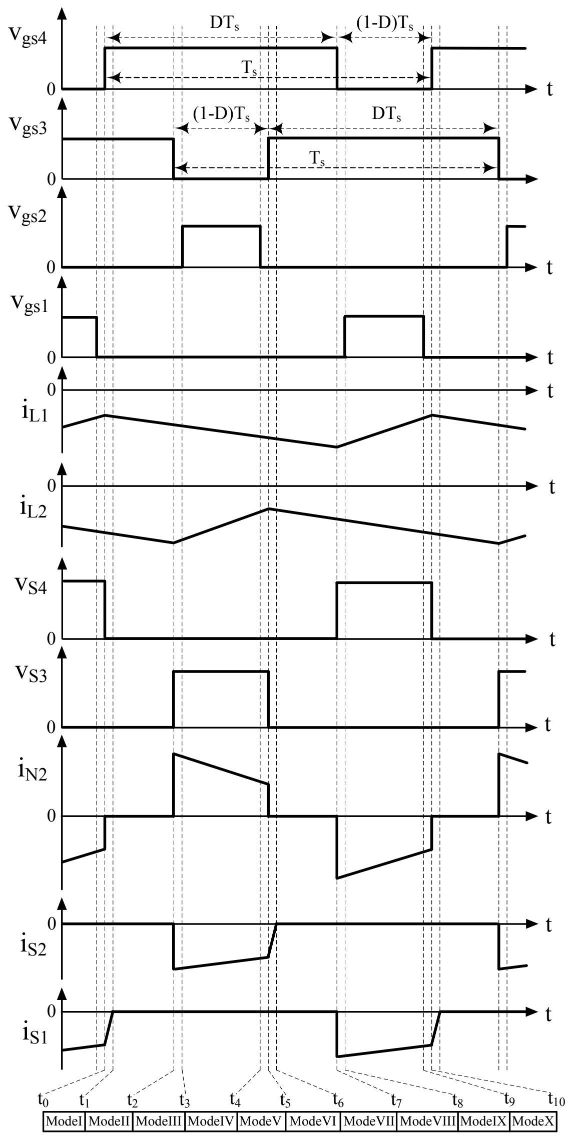
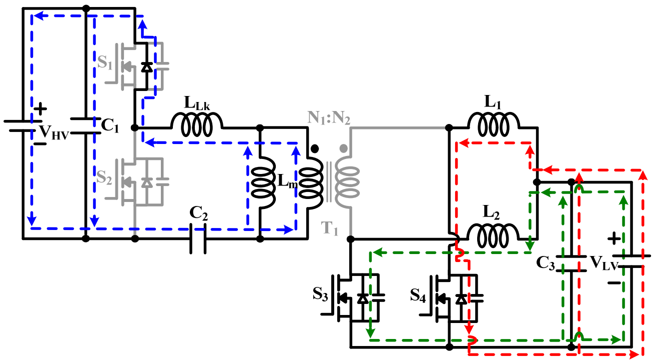


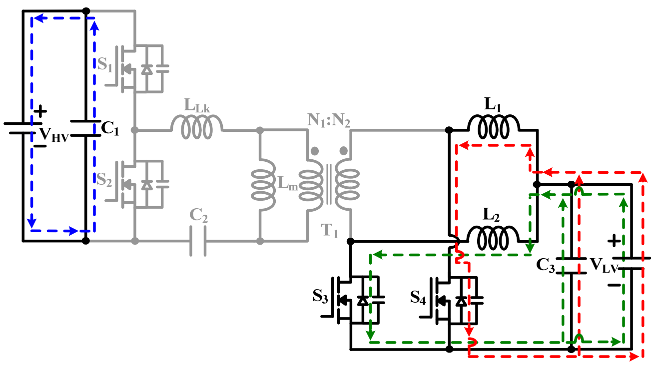
Fig. 5. Key waveforms of proposed isolated bidirectional converter in high-step-up stage in CCM operation.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2386284, IEEE Transactions on Industrial Electronics

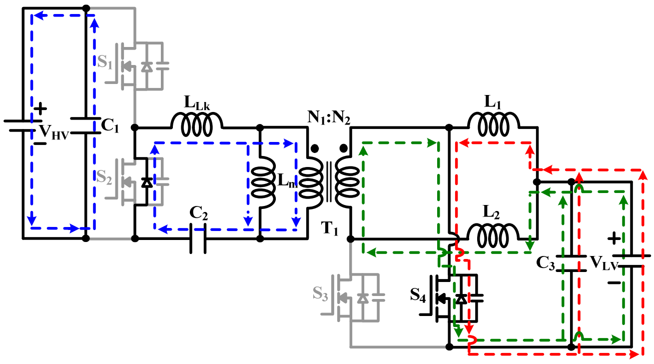
3) Mode III [t_2, t_3]: During this interval, S_4 is on, while S_1, S_2, and S_3 are off. The equivalent circuit is shown in Fig. 6(c). L_1 stores energy from V_{LV} and C_1. The anti-parallel diode of S_2 conducts to achieve ZVS conduction. The energy stored in L_2 is released to C_2 through T_1. i_{S4} is equal to $i_{L1}+i_{L2}$. The voltage across S_3 is equal to $V_{LV}+v_{L2}$, that across the magnetizing inductance L_m is equal to $n(V_{LV}+v_{L2})$, that across C_2 is equal to $n(V_{LV}+v_{L2})$, and that across S_1 is equal to V_{HV}. C_1 continues to release energy to V_{HV}. This operating mode ends when S_2 is turned on at $t = t_3$.
4) Mode IV [t_3, t_4]: During this interval, S_2 and S_4 are on, while S_1 and S_3 are off. The equivalent circuit is shown in Fig. 6(d). S_2 achieves ZVS when it is turned on with the synchronous rectifier, and thus improves system efficiency. L_1 continues to store energy from V_{LV} and C_3. The energy stored in L_2 continues to be released to C_2 through T_1. C_1 continues to release energy to V_{HV}. This operating mode ends when S_2 is turned off at $t = t_4$.
5) Mode V [t_4, t_5]: During this interval, S_4 is on, while S_1, S_2, and S_3 are off. S_2 achieves ZVS when it is turned off. The equivalent circuit is shown in Fig. 6(c). L_1 continues to store energy from V_{LV} and C_3. The energy stored in L_2 continues to be released to C_2 via T_1 and the anti-parallel diode of S_2. C_1 continues to release energy to V_{HV}. This operating mode ends when S_3 is turned on at $t = t_5$.
6) Mode VI [t_5, t_6]: During this interval, S_3 and S_4 are on while S_1 and S_2 are off. The equivalent circuit is shown in Fig. 6(e). The energy stored in L_{Lk} is released via the anti-parallel diode of S_2 to C_2. Therefore, the leakage energy can be recycled, and the voltage of S_1 is clamped at V_{HV}. V_{LV} and C_3 provide energy to L_1 and L_2. This operating mode ends when i_{Lk} is equal to zero at $t = t_6$.
7) Mode VII [t_6, t_7]: During this interval, S_3 and S_4 are on, while S_1 and S_2 are off. The equivalent circuit is shown in Fig. 6(b). L_1 and L_2 simultaneously store energy from V_{LV} and C_3. This operating mode ends when S_4 is turned off at $t = t_7$.
8) Mode VIII [t_7, t_8]: During this interval, S_3 is on, while S_1, S_2, and S_4 are off. The equivalent circuit is shown in Fig. 6(f). The anti-parallel diode of S_1 conducts to achieve ZVS condition. The voltage across S_2 is equal to V_{HV}, and that across S_4 is equal to $v_{L1}+V_{LV}$. Energy from V_{LV} and C_3 is stored by L_2. The energy stored in L_1 is released to N_2. C_2 and winding N_1 are linked in series to release energy to C_1 and V_{HV}. This operating mode ends when S_1 is turned on at $t = t_8$.
9) Mode IX [t_8, t_9]: During this interval, S_1 and S_3 are on, while S_2 and S_4 are off. The equivalent circuit is shown in Fig. 6(g). S_1 achieves ZVS when it is turned on with the synchronous rectifier. The voltage across S_4 is $V_{LV}+v_{L1}$, and that across S_2 is V_{HV}. L_2 continues to store energy from V_{LV} and C_3. The energy stored in L_1 continues to be released to N_2. C_2 and N_1 are linked in series to release energy to C_1 and V_{HV}. This operating mode ends when S_1 is turned off at $t = t_9$.
10) Mode X [t_9, t_{10}]: During this interval, S_3 is on, while S_1, S_2, and S_4 are off. The equivalent circuit is shown in Fig. 6(f). S_1 achieves ZVS when it is turned off. L_2 continues to store energy from V_{LV} and C_3. C_2 and N_1 are linked in series to release energy to C_1 and V_{HV}. This operating mode ends when S_4 is turned on at $t = t_{10}$.



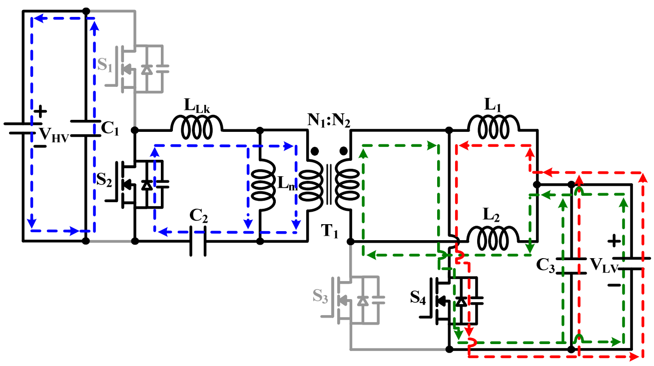
(a) Mode I



(b) Modes II and VII

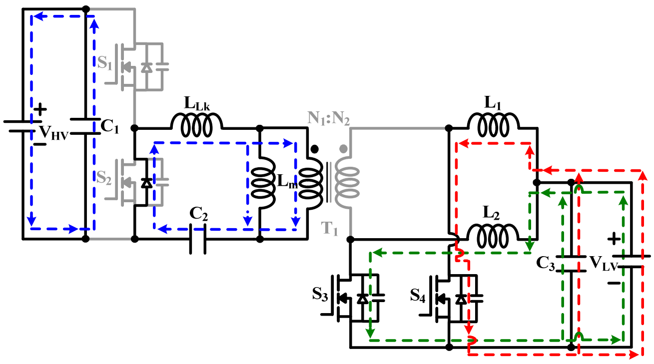


(c) Modes III and V

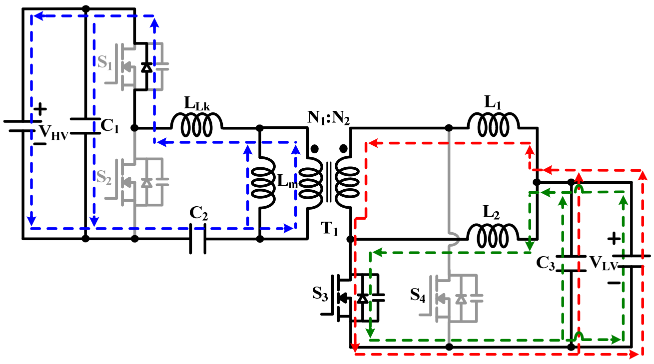


(d) Mode IV

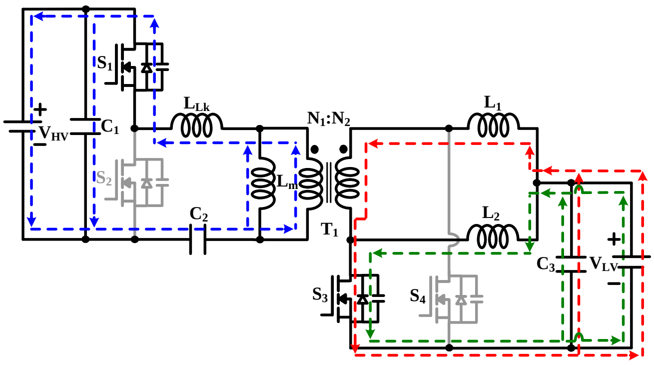
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2386284, IEEE Transactions on Industrial Electronics



(e) Mode VI



(f) Modes VIII and X



(g) Mode IX

Fig. 6. Equivalent circuits of isolated bidirectional converter in high-step-up stage over one switching period during CCM operation: (a) mode I, (b) modes II and VII, (c) modes III and V, (d) mode IV, (e) mode VI, (f) modes VIII and X, and (g) mode IX.

III. Steady-State Analysis of Proposed Converter

To simplify the steady-state condition analysis of the high-step-down and high-step-up stages in CCM, the leakage inductance L_{Lk} of the transformer is neglected because the magnetizing inductance L_m of the transformer is much larger than its leakage inductance.

(A) Step-Down Stage

The turned-on period (DT_s) and turned-off period ($(1-D)T_s$) of S_1 and S_2 in one switching period are defined as shown in Fig. 3.

When S_1 and S_2 are the switches used in the turned-on period (DT_s), inductor voltages v_{L1} and v_{L2} and high-capacitor voltage v_{C2} are given by

$$v_{L1} = v_{L2} = \frac{V_{HV}}{2n} - V_{LV}, \qquad (1)$$

$$v_{C2} = \frac{V_{HV}}{2}. \qquad (2)$$

When S_1 and S_2 are the switches not used in the turned-off period ($(1-D)T_s$), v_{L1} and v_{L2} for this interval are

$$v_{L1} = v_{L2} - V_{LV}. \qquad (3)$$

The application of the principle of volt-second balance to L_1 and L_2 yields

$$\int_0^{DT_S} \left(\frac{V_{HV}}{2n} - V_{LV}\right)dt + \int_{DT_S}^{T_S} -V_{LV}\,dt = 0. \qquad (4)$$

Based on (4), the voltage gain is

$$M_{Step-down} = \frac{V_{LV}}{V_{HV}} = \frac{1}{2n}D. \qquad (5)$$

From (5), the voltage gain of the isolated bidirectional full-bridge converters [30], [31] are compared with that of the proposed bidirectional converter in the high-step-down stage in CCM operation with a turns ratio of n=1.5 (Fig. 7). The voltage gain of the proposed converter is smaller than that of other converters [30], [31] when the duty cycle D is lower than 0.5.

The voltage stresses of all four switches are given by

$$v_{S1} = v_{S2} = V_{HV}, \qquad (6)$$

$$v_{Q3} = v_{S4} = \frac{V_{HV}}{2n}. \qquad (7)$$

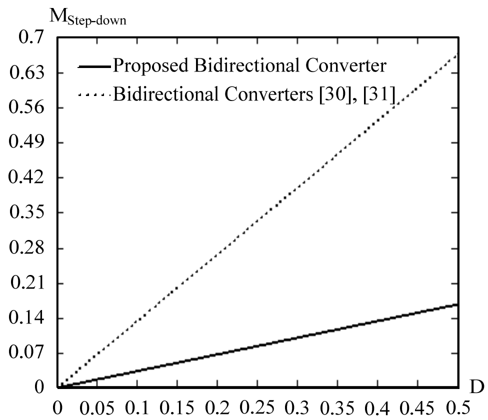


Fig. 7. Comparison of voltage gains of the isolated bidirectional full-bridge converters [30], [31] and of proposed bidirectional converter in high-step-down stage in CCM operation.

When the proposed converter is operated in boundary-conduction mode, the peak currents of i_{L1} and i_{L2} and the average currents of I_{L1}, I_{L2}, and I_{LV} can be expressed as

$$i_{L1} = i_{L2} = \frac{V_{LV}}{L_1}(1-D)T_s = \frac{V_{LV}}{L_2}(1-D)T_s, \tag{8}$$

$$I_{L1} = I_{L2} = \frac{V_{LV}}{2L_1}(1-D)T_s = \frac{V_{LV}}{2L_2}(1-D)T_s = \frac{I_{LV}}{2}, \tag{9}$$

$$I_{LV} = \frac{V_{LV}}{R} = \frac{V_{LV}}{L_1}(1-D)T_s = \frac{V_{LV}}{L_2}(1-D)T_s \cdot \tag{10}$$

The boundary normalized magnetizing-inductance time constant in high-step-down stage is defined as

$$\tau_{Step-down} \equiv \frac{L_1}{RT_s} \equiv \frac{L_2}{RT_s} \cdot \tag{11}$$

The solution of (11) yields the following expression of $\tau_{Step-down}$:

$$\tau_{Step-down} = 1 - D \cdot \tag{12}$$

Fig. 8 illustrates the relationship of $\tau_{Step-down}$ and D at n=1.5. If the normalized magnetizing-inductance time constant τ_L is higher than $\tau_{Step-down}$ in the high-step-down stage, the converter is operated in CCM; otherwise, it is operated in discontinuous-conduction mode (DCM).

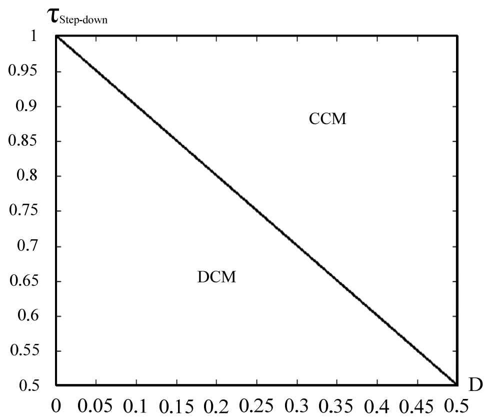


Fig. 8. Boundary-conduction mode of proposed isolated bidirectional converter in high-step-down stage with *n*=1.5.

(B) Step-Up Stage

The turned-on period (DT_s) and turned-off period ($(1-D)T_s$) of S_3 and S_4 in one switching period are defined as shown in Fig. 5.

When S_3 and S_4 are the switches used in the turned-on period (DT_s), v_{L1}, v_{L2}, and v_{C2} are given by

$$v_{L1} = v_{L2} = -V_{LV}, \tag{13}$$

$$v_{C2} = \frac{n}{1-D}V_{LV} \cdot \tag{14}$$

When S_4 (S_3) is the switch not used in the turned-off period ($(1-D)T_s$) and S_3 (S_4) is the switch used in the turned-on period (DT_s), v_{L1}, v_{L2}, N_2, and v_{Lm} for this interval are

$$v_{L1} = v_{L2} = v_{N2} - V_{LV}, \tag{15}$$

$$v_{N2} = \frac{v_{Lm}}{n}, \tag{16}$$

$$v_{Lm} = V_{HV} - v_{C2} \cdot \tag{17}$$

The application of the principle of volt-second balance to L_1 and L_2 yields

$$\int_0^{DT_S} -V_{LV}\,dt + \int_{DT_S}^{T_S} (v_{N2} - V_{LV})\,dt = 0 \cdot \tag{18}$$

The solution of (18) explains the voltage gain as follows:

$$\frac{v_{N2}}{V_{LV}} = \frac{1}{1-D} \cdot \tag{19}$$

Equation (18) can be rewritten as

$$\int_0^{DT_S} -V_{LV}\,dt + \int_{DT_S}^{T_S} \left(\frac{V_{HV} - \frac{nV_{LV}}{1-D}}{n} - V_{LV}\right)dt = 0 \cdot \tag{20}$$

From (20), the high-step-up voltage gain can be explained as

$$M_{CCM} = \frac{V_{HV}}{V_{LV}} = \frac{2n}{1-D} \cdot \tag{21}$$

By (21), the voltage gains of the isolated bidirectional full-bridge converters [30], [31] and of the proposed isolated bidirectional converter in CCM operation with a turns ratio of n=1.5 are compared in Fig. 9. The voltage gain of the proposed converter is greater than that of the isolated bidirectional full-bridge converter [30], [31] in the high-step-up stage.

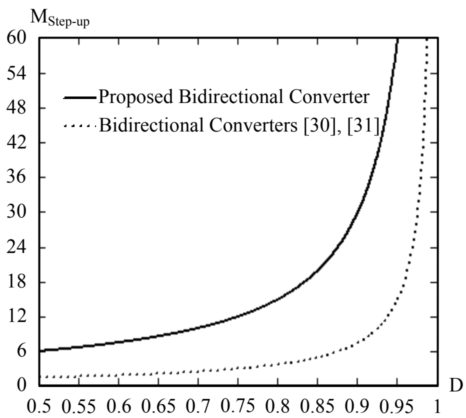


Fig. 9. Comparison of voltage gains of bidirectional converters [30], [31] and proposed bidirectional converter in high-step-up stage in CCM operation.

The voltage stresses of all four switches are given by

$$v_{S1} = v_{S2} = \frac{2n}{1-D} V_{LV}, \quad (22)$$

$$v_{S3} = v_{S4} = \frac{V_{LV}}{1-D}. \quad (23)$$

When the proposed converter is operated in boundary-conduction mode, the peak currents of i_{L1} and i_{L2} and the average currents of I_{L1}, I_{L2}, I_{LV}, and I_{HV} can be expressed as

$$i_{L1} = i_{L2} = \frac{V_{LV}}{L_1} DT_s = \frac{V_{LV}}{L_2} DT_s, \quad (24)$$

$$I_{L1} = I_{L2} = \frac{V_{LV}}{2L_1} DT_s = \frac{V_{LV}}{2L_1} = \frac{I_{LV}}{2}, \quad (25)$$

$$I_{LV} = \frac{2n}{1-D} I_{HV}, \quad (26)$$

$$I_{HV} = \frac{V_{HV}}{R} = \frac{1-D}{2nL_1} V_{LV} DT_s = \frac{1-D}{2nL_2} V_{LV} DT_s. \quad (27)$$

Equation (27) can be rewritten as

$$I_{HV} = \frac{V_{HV}}{R} = \frac{(1-D)^2 DT_s}{4n^2 L_1} V_{HV} = \frac{(1-D)^2 DT_s}{4n^2 L_2} V_{HV}. \quad (28)$$

The boundary normalized magnetizing-inductance time constant in the high-step-up stage is defined as

$$\tau_{Step-up} \equiv \frac{L_1}{RT_s} \equiv \frac{L_2}{RT_s}. \quad (29)$$

The solution of (29) yields the following expression of $\tau_{Step\text{-}up}$:

$$\tau_{Step-up} = \frac{D(1-D)^2}{4n^2}. \quad (30)$$

Fig. 10 illustrates the relationship between $\tau_{Step\text{-}up}$ and D at n=1.5. If the normalized magnetizing-inductance time constant τ_H is higher than $\tau_{Step\text{-}up}$ in the high-step-up stage, the converter is operated in CCM; otherwise, it is operated in DCM.

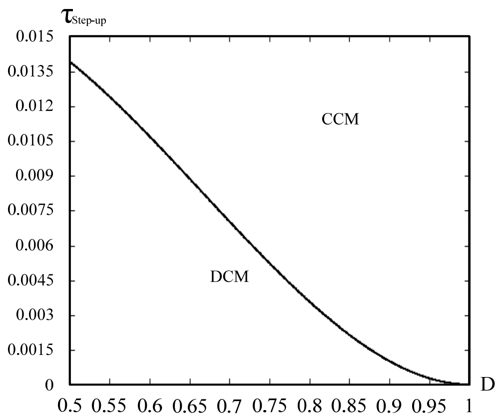


Fig. 10. Boundary-conduction mode of proposed bidirectional converter in high-step-up stage at *n*=1.5.

IV. Design and Experiment of Proposed Converter

The laboratory prototype sample is implemented to demonstrate the practicability of the proposed converter. The system specifications and components are as follows:

1) V_{LV}: 24 V
2) V_{HV}: 200 V
3) operating frequency: 50 kHz
4) maximum output power P_o: 200 W
5) C_1 and C_2: 22 μF/450 V, metallized polypropylene film capacitors
6) S_1 and S_2: IXFH120N25T
7) transformer: PQ3535, core PC-40, N_1:N_2=1.5:1, L_m=2 mH, leakage inductance=0.38 μH
8) S_3 and S_4: FDP075N15A
9) L_1 and L_2: 780 μH
10) C_3: 2200 μF/63 V, aluminum capacitor

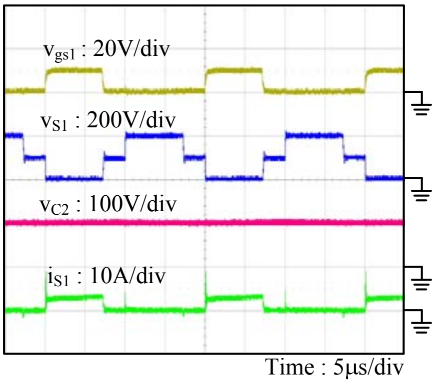
The experimental results in high-step-down stage at full load P_o = 200 W and V_{HV} = 200 V are shown in Fig. 11. Figs. 11(a) and 11(b) show the waveforms of v_{gs1}, v_{S1}, v_{C2}, i_{S1}, v_{gs2}, v_{S2}, and i_{S1}. v_{gs1} and v_{gs2} indicate that the gate signals of S_1 and S_2 are interlaced by a phase shift of 180 degrees. The voltage across C_2 is about 100 V. The voltage spike in S_1 and S_2 is about 225 V. Thus, low voltage stresses and low on-resistance R_{on} switches can be selected. i_{S1} is similar to i_{S2}. Figs. 11(c) and 11(d) show the waveforms of v_{gs3}, v_{S3}, i_{S3}, v_{gs4}, v_{S4}, and i_{S4}. v_{gs3} and v_{gs4} are gate signals with synchronous rectifiers. v_{gs3}, v_{S3}, v_{gs4}, and v_{S4} indicate that S_3 and S_4 achieve ZVS when they are turned on. The voltage spike on S_3 and S_4 is a little bit high -- about 120 V. S_3, S_4 utilize MOSFETs with voltage ratings of 150 V. The current in S_3 and S_4 is increased by the anti-parallel diode reverse-recovery effect. Fig. 11(e) shows the waveforms of V_{LV}, i_{N2}, and i_{Lt}. The low-side voltage V_{LV} is 24 V. The current frequency of i_{Lt} is double the operating frequency of the system. i_{Lt} indicates that the current is reduced.

The measured results in high-step-up stage at full load P_o = 200 W and V_{LV} = 24 V are shown in Fig. 12. Figs. 12(a) and 12(b) show the waveforms of v_{gs4}, v_{S4}, i_{S4}, i_{Lt}, v_{gs3}, v_{S3}, and i_{S3}. v_{gs4} and v_{gs3} are phase shifts of 180 degrees with an overlap, which ensure that the inductor energy can be delivered to N_1. The voltage increase in S_3 and S_4 is about 75 V. The current frequency of i_{Lt} is 100 kHz. Fig. 12(c) shows the waveforms of i_{L1} and i_{L2}. The interleaved inductor currents i_{L1} and i_{L2} reduce the ripple current of i_{Lt}. Furthermore, C_3 enables the selection of a low capacitor value. Fig. 12(d) shows the waveforms of v_{gs2}, v_{S2}, and i_{S2}. v_{gs2} is a gate signal with a synchronous rectifier. v_{gs2} and v_{S2} indicate that S_2 achieves ZVS when it is turned on and turned off. Fig. 12(e) shows the waveforms of V_{HV}, v_{C2}, and i_{Lk}. V_{HV} is 200 V, and the capacitor voltage v_{C2} is about 100 V.

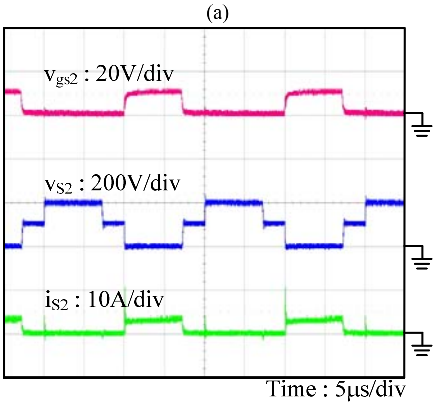
Figure 13 shows the measured conversion efficiency of the proposed converter in the high-step-down stage. The maximum efficiency is 96.3% with a synchronous rectifier. Compared with the conversion efficiency, the efficiency with the synchronous rectifier is higher than that with the anti-parallel diode. Thus, the synchronous rectifier can significantly improve efficiency. Figure 14 shows the measured conversion efficiency of the proposed converter in the high-step-up stage. Fig. 14 shows that the synchronous rectifier efficiency is

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2386284, IEEE Transactions on Industrial Electronics

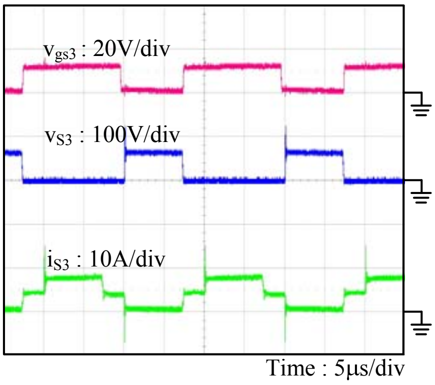
higher than the anti-parallel diode efficiency, and that the peak efficiency is 95.6% in the high-step-up stage. S_1~S_4 will suffer from high current spikes, which occur due to the recovery problem of the switches' anti-parallel diodes, so the switch-current waveforms presented in the experiments are slightly different with the operating waveforms in Figures 3 and 5. The proposed bidirectional converter can be applied in photovoltaic stand alone system, energy storage system and emergency power systems. The output voltage of a single PV module is 24~40 V. A dc-dc converter will be used to converter the PV output voltage to dc bus voltage and also achieving maximum power tracking. The dc bus voltage is usually designed as 200V for the 110 Vac power system. This is why we selected the dc bus voltage (V_{HV}) is 200V and battery voltage (V_{LV}) is 24 V. In this system, the battery needs to be charged or discharged depending on the PV power generation and the load requirement. The low voltage (battery voltage) with 24 V can prove the high efficiency of the proposed converter. If the battery voltage is selected at 36 V or higher voltage level, the system efficiency will be higher because the conduction losses will be reduced. The proposed converter is suitable for portable energy storage systems, emergency power systems and micro DC grid systems. The power-loss analysis of the proposed converter in step-down mode at 200 W is shown in Table 1. The measured efficiency is 96.3 % and the calculated result is 98.1 %, because the calculated results ignore the reverse-recovery effect of the anti-parallel diode, iron, and resistance of circuit traces.



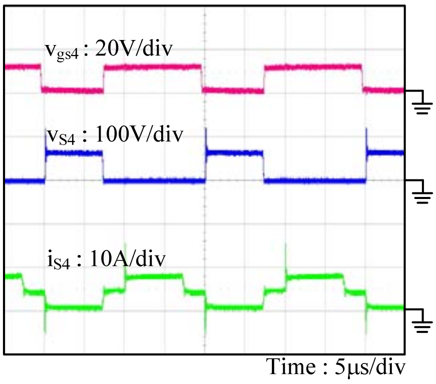
(a)



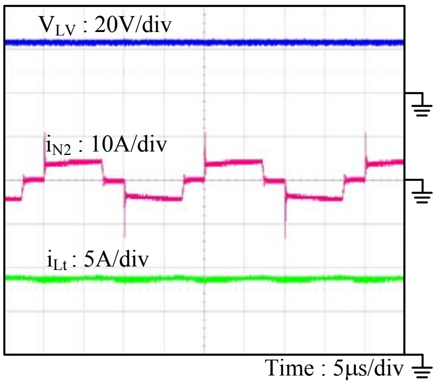
(b)



(c)

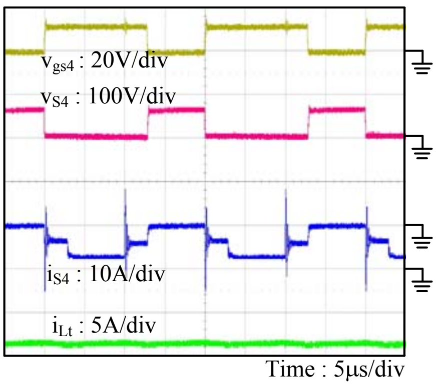


(d)



(e)

Fig. 11. Experimental waveforms of high-step-down stage at P_o=200 W.



(a)

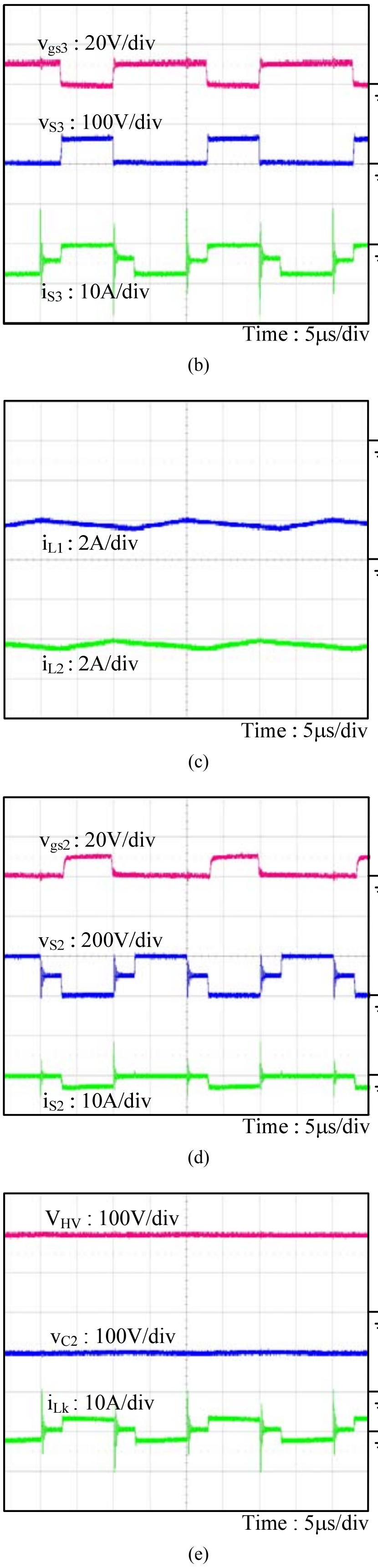


Fig. 12. Experimental waveforms of high-step-up stage at P_o=200 W.

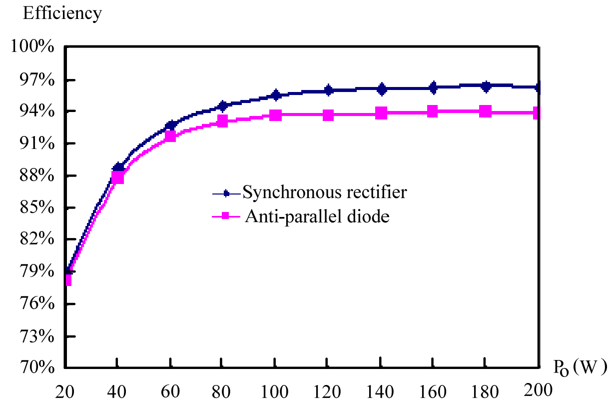


Fig. 13. Experimental conversion efficiency of proposed isolated bidirectional converter in high-step-down stage.

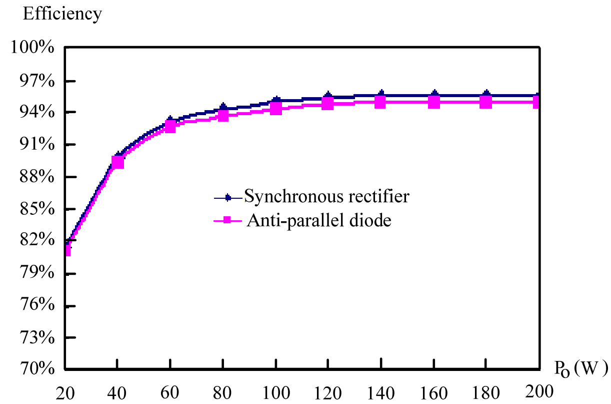


Fig. 14. Experimental conversion efficiency of proposed isolated bidirectional converter in high-step-up stage.

TABLE 1. POWER-LOSS ANALYSIS OF THE PROPOSED CONVERTER IN STEP-DOWN MODE AT FULL LOAD (200 W).

Components	Parameters	Loss (W)		%
Switches S_1 and S_2	22 mΩ	Conduction	Switching	0.86
		0.13	1.58	
Resistance of Transformer T_1	25 mΩ	0.13		0.07
Resistances of Inductors L_1 and L_2	35 mΩ	1.3		0.65
Switches S_3 and S_4	7.5 mΩ	Conduction	Switching	0.31
		0.43	0.19	
Total Loss		3.76		1.9

V. CONCLUSIONS

In this paper, a high-efficiency and high-conversion-ratio isolated bidirectional DC–DC converter with a low transformer turns ratio is presented. The size of the capacitor on the voltage side can be decreased by using current-doubler circuits with low current ripples. The synchronous-rectifier circuit can achieve zero voltage switching and improve system efficiency. The operating principles, steady-state analysis, and experimental results are discussed in detail. The efficiencies of the proposed converter with synchronous rectifiers and anti-parallel diodes are compared in the experimental results. The full-load efficiency in the step-down and step-up stages is near 96.3% and 95.6%, respectively.

REFERENCES

[1] Z. Dong, "Nonlinear adaptive power-level control for modular high temperature gas cooled reactors," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 2, pp. 1332-1345, April 2013.

[2] T. J. Liang, J. H. Lee, S. M. Chen, and L. S. Yang, "Novel isolated high-step-up DC–DC converter with voltage lift," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1483-1491, April 2013.

[3] A. Koran, T. Labella, and J. S. Lai, "High efficiency photovoltaic source simulator with fast response time for solar power conditioning systems evaluation," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1285–1297, March 2014.

[4] M. Trifkovic, M. Sheikhzadeh, K. Nigim, and P. Daoutidis, "Modeling and control of a renewable hybrid energy system with hydrogen storage," *IEEE Trans. Control Syst. Technol.*, vol. 22, no. 1, pp. 169–179, Jan. 2014.

[5] Y. K. Lo, H. J. Chiu, T. P. Lee, I. Purnama, and J. M. Wang, "Analysis and design of a photovoltaic system DC connected to the utility with a power factor corrector," *IEEE Trans. Power Electron.*, vol. 56, no. 11, pp. 4354–4362, Nov. 2009.

[6] I. Laird and D. D. C. Lu, "High step-up DC/DC topology and MPPT algorithm for use with a thermoelectric generator," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3147–3157, July 2013.

[7] S. K. Chattopadhyay, C. Chakraborty, and B. C. Pal, "Cascaded H-bridge & neutral point clamped hybrid asymmetric multilevel inverter topology for grid interactive transformerless photovoltaic power plant," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 5074-5079, Oct. 2012.

[8] W. L. Chen and J. S. Lin, "One-dimensional optimization for proportional-resonant controller design against the change in source impedance and solar irradiation in PV systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1845-1854, April 2014.

[9] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor / switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687-696, March 2008.

[10] A. Ioinovici, C. K. Tse, and H. C. –H. Chung "Common on" Design and analysis of switched-capacitor-based step-up resonant converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 6, pp. 1403, June 2006.

[11] C. K. Cheung, S. C. Tan, C. K. Tse, and A. Ioinovici, "On energy of switched-capacitor converter," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 862–876, Feb. 2013.

[12] D. Gu, D. Czarkowski, and A. Ioinovici, "A large dc-gain highly efficient hybrid switched-capacitor-boost converter for renewable energy systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, pp. 2495–2500, Sept 2011..

[13] S. M. Chen, T. J. Liang, L. S. Yang, and J. F. Chen, "A boost converter with capacitor multiplier and coupled inductor for AC module application," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1503-1511, April 2013.

[14] T. J. Liang, S. M. Chen, L. S. Yang, J. F. Chen, and A. Ioinovici, "Ultra large gain step-up switched-capacitor DC-DC converter with coupled inductor for alternative sources of energy," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 864-874, April 2012.

[15] S. M. Chen, T. J. Liang, L. S. Yang, and J. F. Chen, "A safety enhanced, high step-up DC-DC converter for AC photovoltaic module application," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1809 – 1817, April2012.

[16] Y. P. Hsieh, J. F. Chen, T. J. Liang, L. S. Yang, "Novel high step-up DC-DC converter with coupled-inductor and switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol.59,no.2, pp.998 – 1007, Feb. 2012.

[17] S. M. Chen, T. J. Liang, K. R. Hu, "Design, Analysis, and implementation of solar power optimizer for DC distribution system", *IEEE Trans. Power Electron.*, vol.28, no.4, pp. 1764 –1772, April 2013.

[18] Y. P. Hsieh, J. F. Chen, L. S. Yang, C.Y. W, and W. S. Liu, "High-conversion-ratio bidirectional DC-DC converter with high coupled inductor," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 210-222, Jan. 2014.

[19] E. Sanchis, E. Maset, A. Ferreres, J. B. Ejea, V. Esteve, J. Jordan, J. Calvente, A. Garrigos, and J. M. Blanes, "Bidirectional high-efficiency nonisolated step-up battery regulator," *IEEE Trans. Aerospace and Electronic Systems.*, vol. 47, no. 3, pp. 2230-2239, July 2011

[20] R. J. Wai, R. Y. Duan, and K. H. Jheng, "High-efficiency bidirectional dc–dc converter with high-voltage gain," *IET Power Electron.*, vol. 5, no. 2, pp. 173–184, Feb. 2012.

[21] L. S. Yang and T. J. Liang, "Analysis and implementation of a novel bidirectional dc–dc converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 422–434, Jan. 2012.

[22] Y. S. Lee and Y. Y. Chiu, "Zero-current-switching switched-capacitor bidirectional dc–dc converter," *in Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 152, no. 6, pp. 1525–1530, Nov. 2005.

[23] M. Kwon, S. Oh, and S. Choi, "High gain soft-switched bidirectional DC-DC converter for eco-friendly vehicles," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1659–1666, April 2014.

[24] R. L. Andersen, T. B. Lazzarin, and I. Barbi, "A 1-kW step-up/step-down switch capacitor AC-AC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3329–3340, July 2013.

[25] O. C. Onar, J. Kobayashi, D. C. Erb, and A. Khaligh, "A bidirectional high-power-quality grid interface with a novel bidirectional noninverted buck-boost converter for PHEVs," *IEEE Trans. Veh. Technol.*, vol. 61, no. 5, pp. 2018–2032, June 2012.

[26] H. W. Seong, H. S. Kim, K.B. Park, G. W. Moon, and M. J. Youn, "High step-up dc-dc converters using zero-voltage switching boost integration technique and light-load frequency modulation control," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1383–1400, March 2012.

[27] C. M. Hong, L. S. Yang, T. J. Liang, and J. F. Chen, "Novel bidirectional DC-DC converter with high step-up/down voltage gain," *in Proc. IEEE Energy Convers. Congr. Expo.*, pp. 60–66, Sept 2009.

[28] K. Yamamoto, E. Hiraki, T. Tanaka, M. Nakaoka, and T. Mishima, "Bidirectional DC-DC converter with full-bridge / push-pull circuit for automobile electric power systems," *in Proc. 37th IEEE Annu. Power Electron. Spec. Conf.*, pp. 1-5, June 2006.

[29] B. Zhao, Q. Song, and W. Liu, "Experimental comparison of isolated bidirectional DC–DC converters based on all-si and all-sic power devices for next-generation power conversion application," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1389-1393, March 2014.

[30] T. F. Wu, J. G. Yang, C. L. Kuo, and Y. C. Wu, "Soft-switching bidirectional isolated full-bridge converter with active and passive snubbers," *IEEE Trans. Ind. Electron.*, vol. 16, no. 3, pp. 1368-1376, March 2014.

[31] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307-2315, May 2014.

[32] F. Ibanze, J. M. Echeverria, and L. Fontan, "Novel technique for bidirectional series-resonant DC/DC converter in discontinuous mode," *IET Power Electron.*, vol. 6,no. 5, pp. 1019–1028, May 2013.

[33] A. K. Rathore and U. R. Prasanna, "Analysis, design, and experimental results of novel snubberless bidirectional naturally clamped ZCS/ZVS current-fed half-bridge DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4482-4491, Oct. 2013.

[34] U. R. Prasanna, A. K. Rathore, and S. K. Mazumder "Novel zero-current-switching current-fed half-bridge isolated DC/DC converter for fuel-cell-based applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 1658-1668, Aug. 2013.

[35] Z. Zhang, Z. Ouyang, O. C. Thomsen, and M. Xu, "Analysis and design of a bidirectional isolated DC–DC converter for fuel Cells and supercapacitors hybrid system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 848–859, Feb. 2012.

[36] L. Wang, Z. Wang, and H. Li, "Asymmetrical duty cycle control and decoupled power flow design of a three-port Bidirectional DC-DC converter for fuel cell vehicle application," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 891–904, Feb. 2012.

[37] B. Zhao, Q. Yu, Z. Leng, and X. Chen, "Switched Z-source isolated bidirectional DC–DC converter and its phase-shifting shoot-through bivariate coordinated control strategy," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4657-4670, Dec. 2012.

[38] D. Yu, A. Q. Hung, M. Wang, and S. M. Lukic, "A novel high step-up ratio bi-directional DC-DC converter," *in Proc. IEEE Appl. Power Electron. Conf.*, 2012, pp. 524-513.

[39] S. M. Chen, T. J. Liang, and Y. H. Huang, "A isolated bidirectional interleaved flyback converter for battery backup system application," *in Proc. IEEE Int. Symp. on Circuits & Syst.*, 2013, pp. 1328-1331.

[40] D. Wang and Y. F. Liu, "A zero-crossing noise filter for driving synchronous rectifiers of *LLC* resonant converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1953–1965, April 2014.

[41] J. Zhang, J. Wang, G. Zhang, and Z. Qian, "A hybrid driving scheme for full-bridge synchronous rectifier in *LLC* resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4549–4561, Nov. 2012.

[42] H. Wen, W. Xiao, B. Su, "Nonactive Power Loss Minimization in a Bidirectional Isolated DC–DC Converter for Distributed Power Systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6822-6831, Dec. 2014.

Tsorng-Juu (Peter) Liang (M'93–SM'10) was born in Kaohsiung, Taiwan. He received the B.S. degree in electrophysics from National Chiao Tung University, Hsinchu, Taiwan, in 1985 and the M.S. and Ph.D. degrees in electrical engineering from the University of Missouri, Columbia, MO, USA, in 1990 and 1993, respectively.

He is currently the Director of the Green Energy Electronics Research Center, National Cheng Kung University, Tainan, Taiwan, where he is also a Professor of electrical engineering. His research interests include high-efficiency power converters, high-efficiency lighting systems, renewable energy conversion, and power IC design.

Dr. Liang is currently an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I, and the Technical Committee Chair of the IEEE Circuits and Systems Society Systems Power and Energy Circuits and Systems Technical Committee.

Jian-Hsieng Lee was born in Miaoli, Taiwan, in 1980. He received the B.S. and M.S. degrees in electrical engineering from I-Shou University, Taiwan, in 2003 and 2005, respectively. He is currently pursuing the Ph.D. degree at National Cheng-Kung University, Taiwan. His research interests include high efficiency power converters, renewable energy conversion, electronic ballasts, and high efficiency lighting systems.